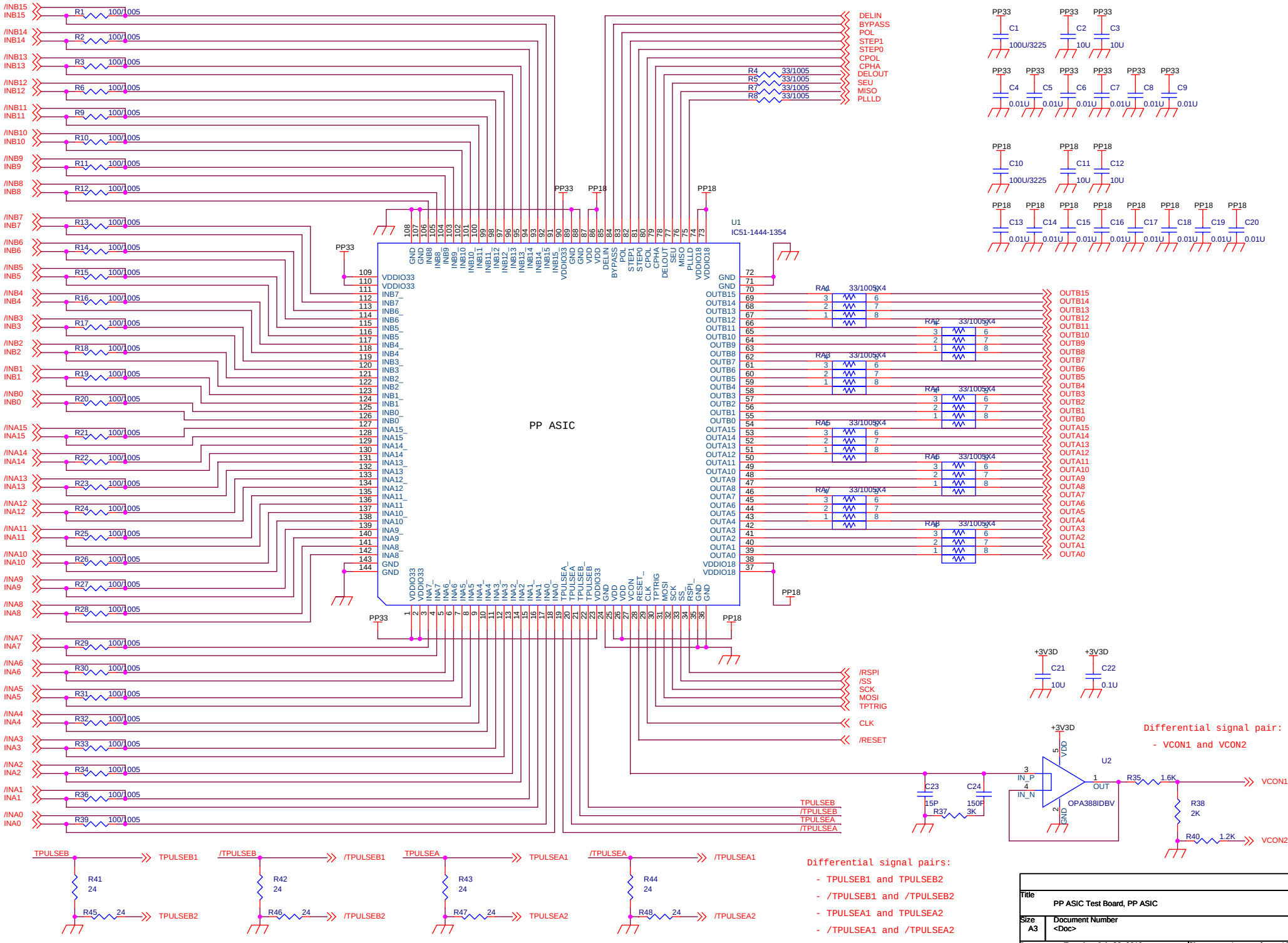
PP ASIC
U1
IC51-1444-1354
/INB15
/INB14
/INB13
/INB12
/INB11
/INB10
/INB9
/INB8
/INB7
/INB6
/INB5
/INB4
/INB3
/INB2
/INB1
/INB0
/INA15
/INA14
/INA13
/INA12
/INA11
/INA10
/INA9
/INA8
/INA7
/INA6
/INA5
/INA4
/INA3
/INA2
/INA1
/INA0
100/1005
DELIN
BYPASS
POL
STEP1
STEP0
CPOL
CPHA
DELOUT
SEU
MISO
PLLLD
33/1005
OUTB15
OUTB14
OUTB13
OUTB12
OUTB11
OUTB10
OUTB9
OUTB8
OUTB7
OUTB6
OUTB5
OUTB4
OUTB3
OUTB2
OUTB1
OUTB0
OUTA15
OUTA14
OUTA13
OUTA12
OUTA11
OUTA10
OUTA9
OUTA8
OUTA7
OUTA6
OUTA5
OUTA4
OUTA3
OUTA2
OUTA1
OUTA0
/RSPI
/SS
SCK
MOSI
TPTRIG
CLK
/RESET
TPULSEB
/TPULSEB
TPULSEA
/TPULSEA
PP33
PP18
100U/3225
10U
0.01U
+3V3D
0.1U
OPA388IDBV
Differential signal pair:
- VCON1 and VCON2
VCON1
VCON2
1.6K
1.2K
Differential signal pairs:
- TPULSEB1 and TPULSEB2
- /TPULSEB1 and /TPULSEB2
- TPULSEA1 and TPULSEA2
- /TPULSEA1 and /TPULSEA2
TPULSEB1
/TPULSEB1
TPULSEA1
/TPULSEA1
TPULSEB2
/TPULSEB2
TPULSEA2
/TPULSEA2
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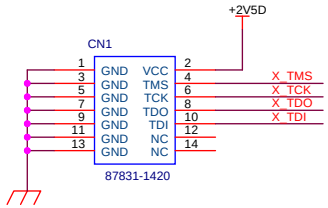
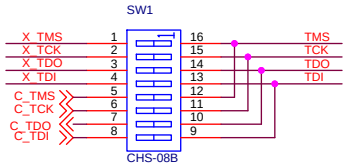
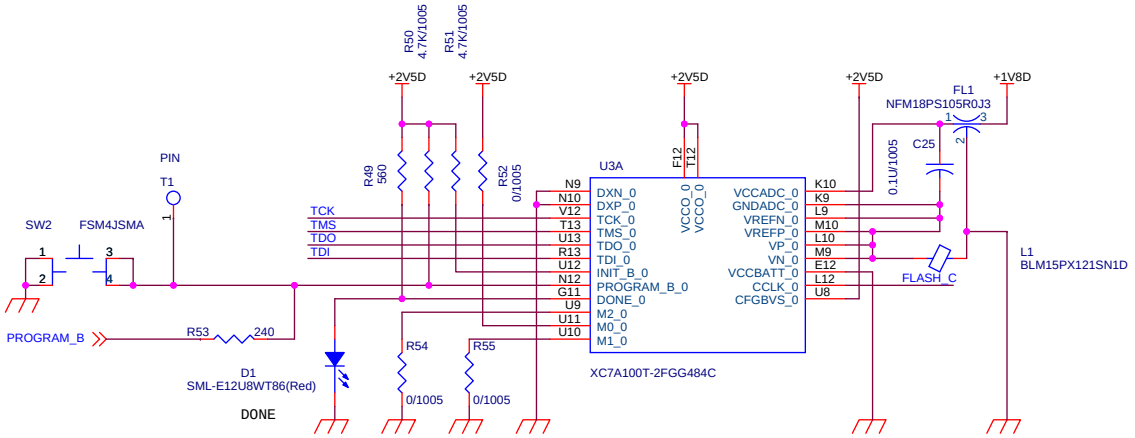
Xilinx JTAG



JTAG Selector

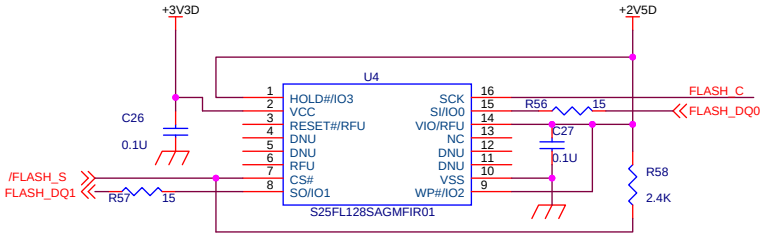


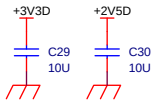
FPGA Bank 0

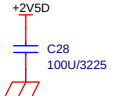


Blue: pin change prohibited

SPI Flash







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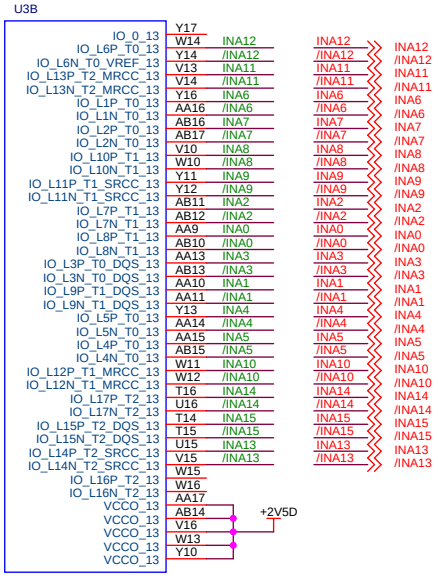
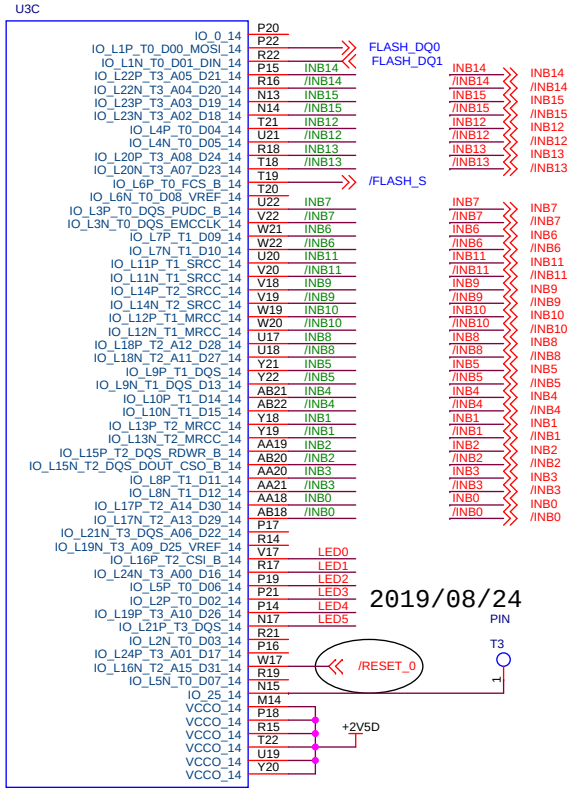
FPGA Bank 13



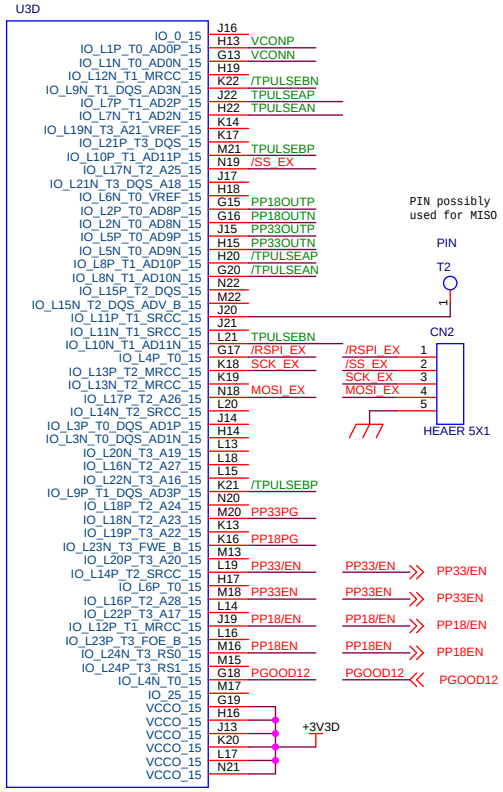
Green: LVDS pin change possible
but P/N pair should be kept.

FPGA Bank 14

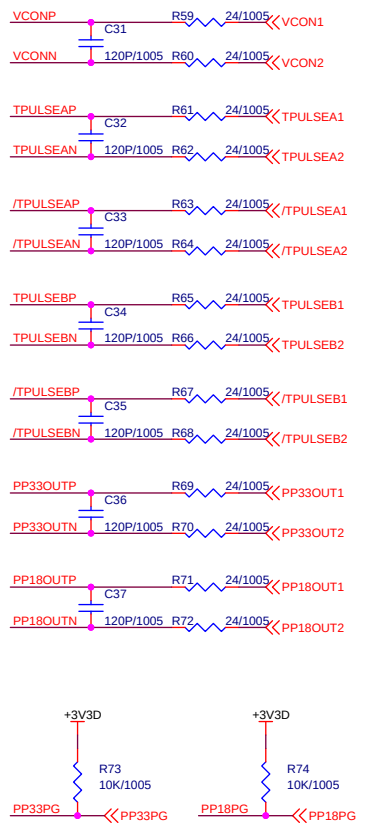


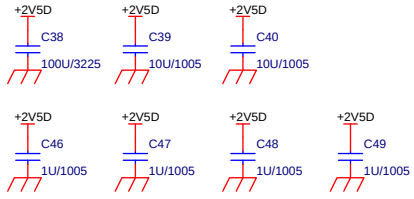
Blue: pin change prohibited.
Green: LVDS pin change possible
but P/N pair should be kept.

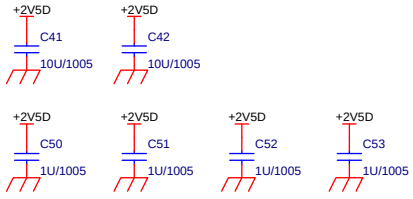
FPGA Bank 15

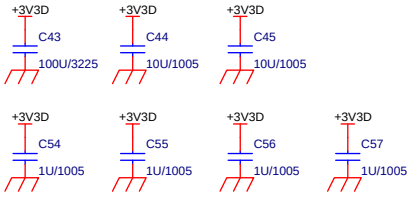


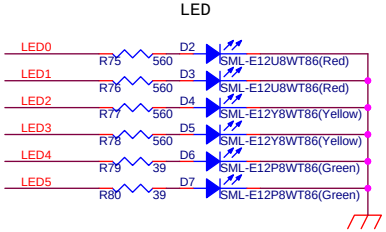
Green: AD pin change possible
but P/N pair should be kept.











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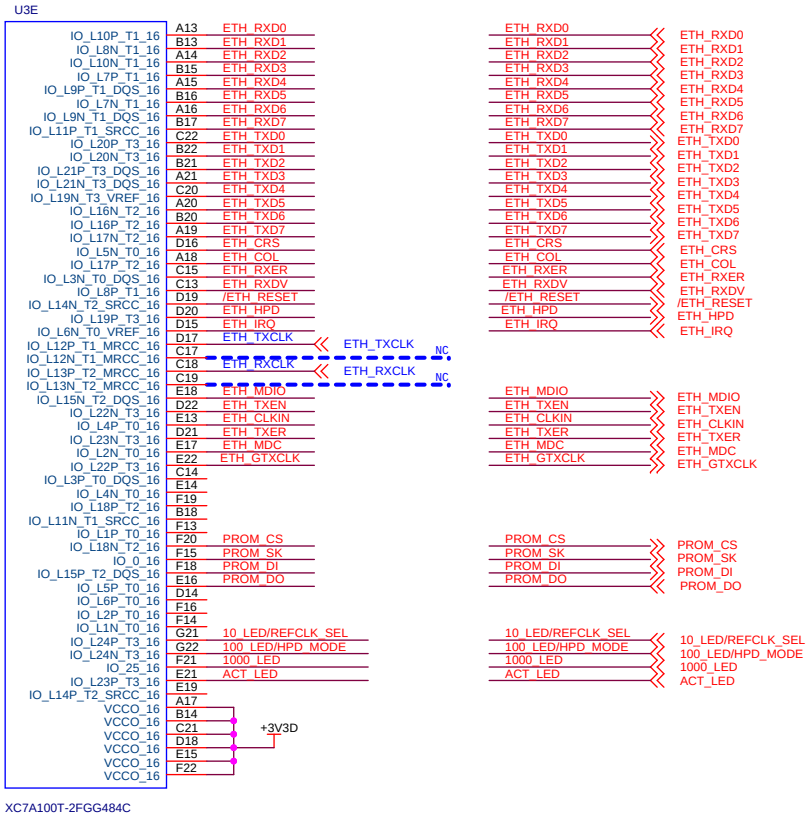
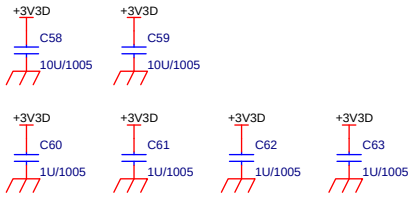
FPGA Bank 16



ETH_TXCLK,ETH_RXCLK はMRCC のPピ ン に

ETH_TXCLK , ETH_RXCLK 以外はスワップ 可

LAN8810-AKZEにつながる信号はシングル50Ω



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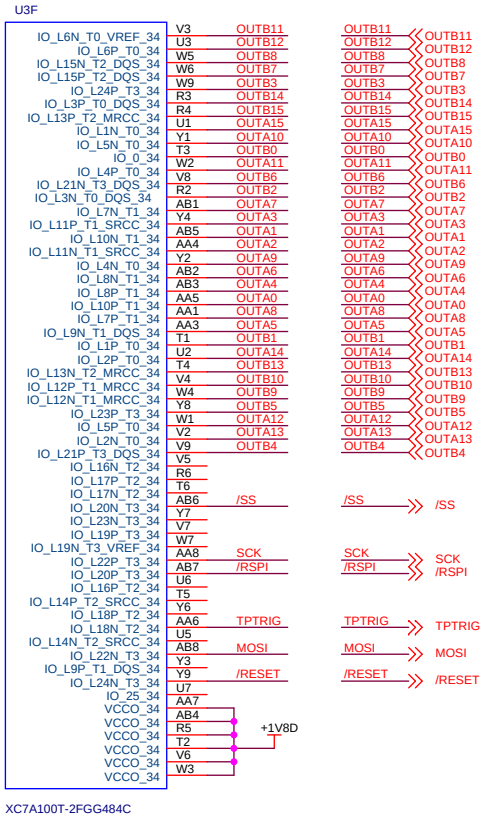
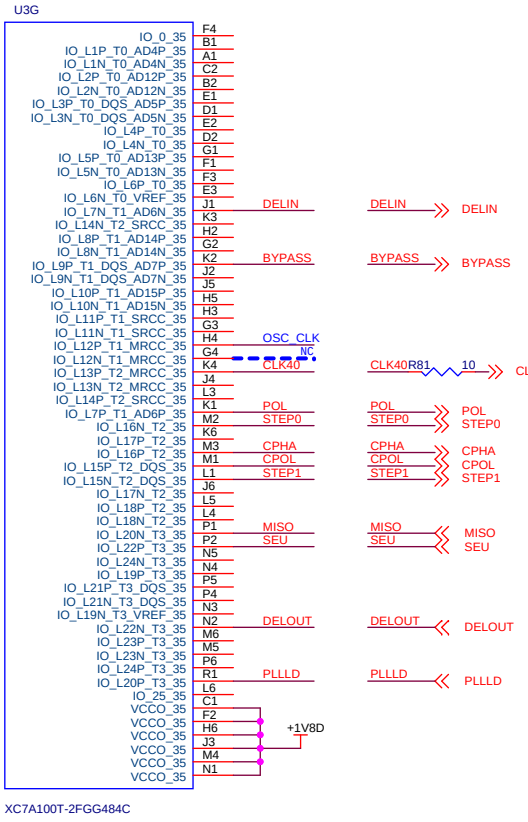
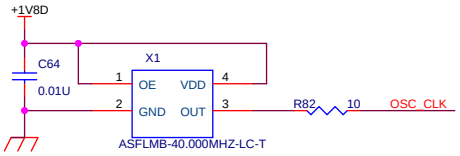
FPGA Bank 34

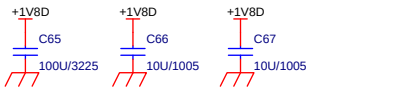


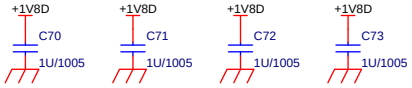
FPGA Bank 35

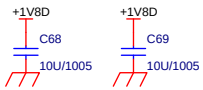


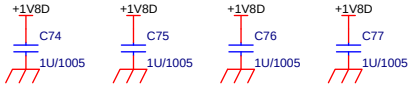


Blue: clock (pin change prohibited)









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Title	PP ASIC Test Board, FPGA Others	
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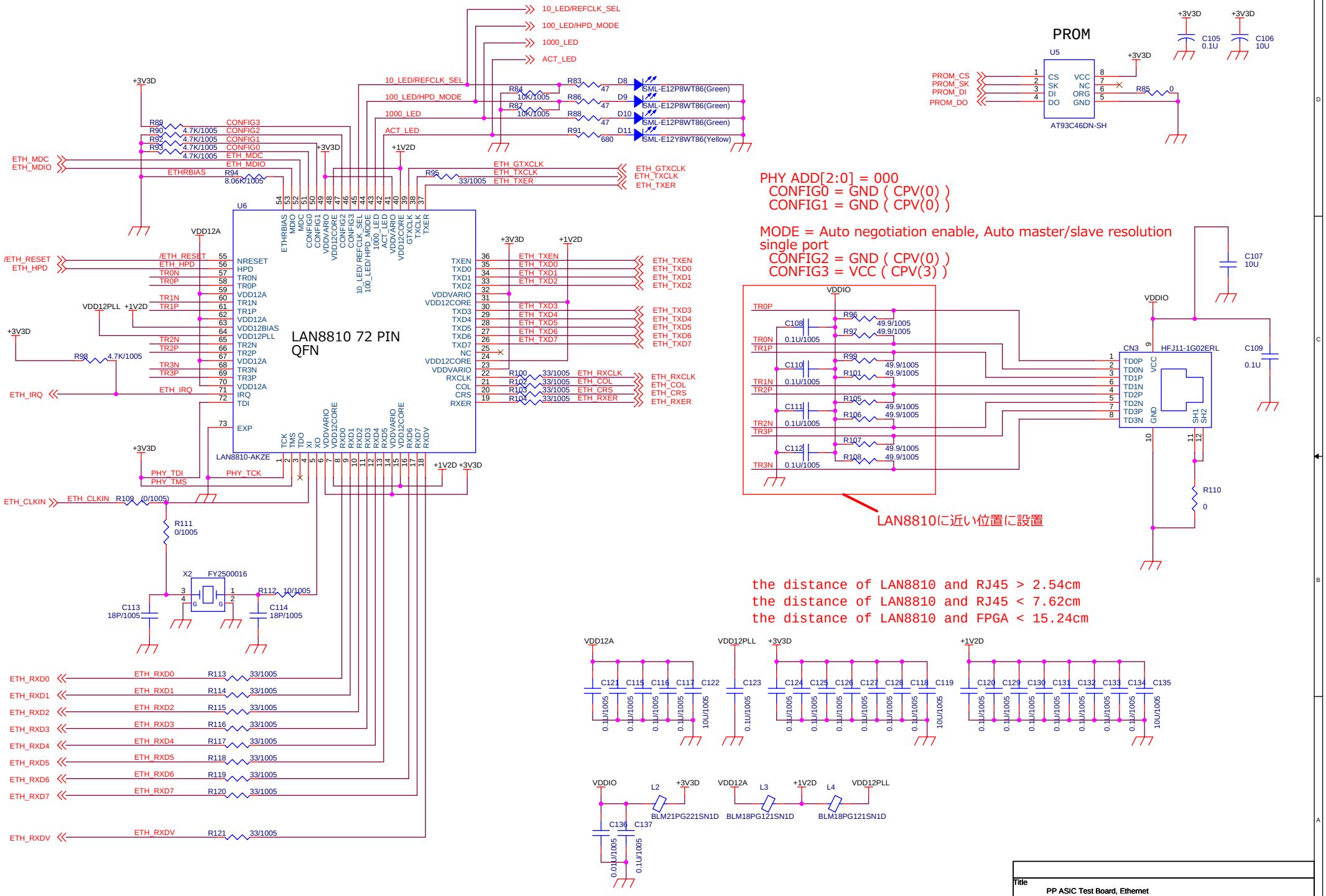

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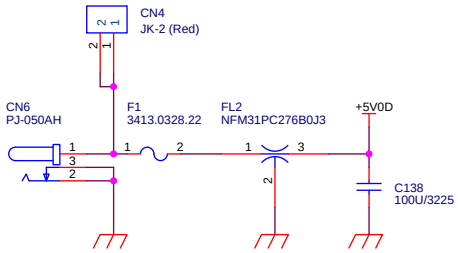
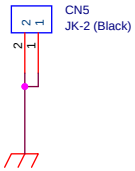
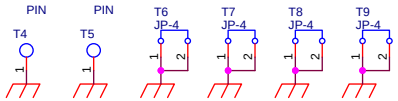
Connector for AC adapter



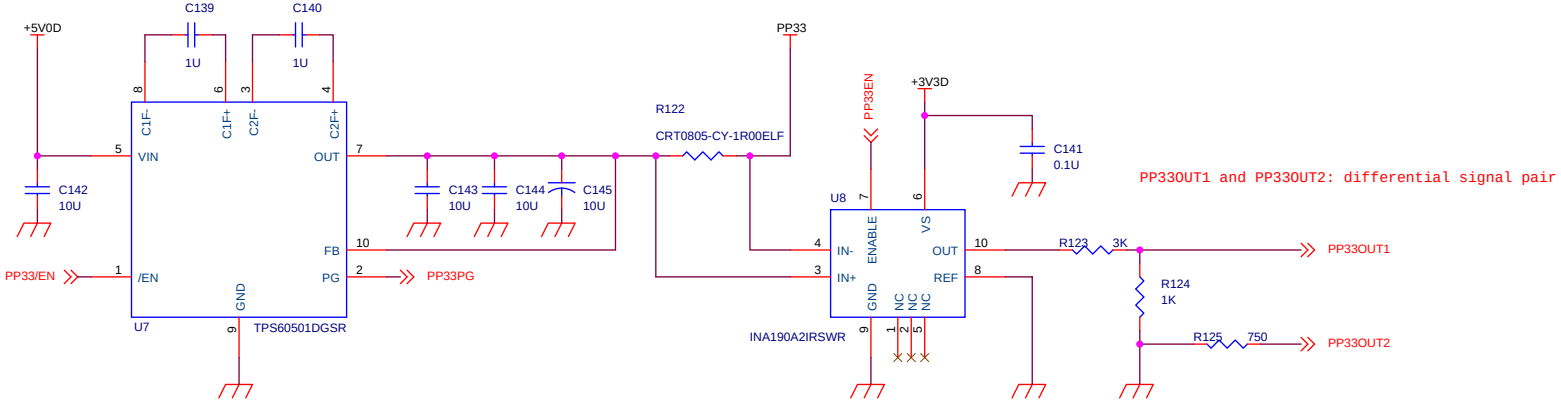
GND connector



Test pins

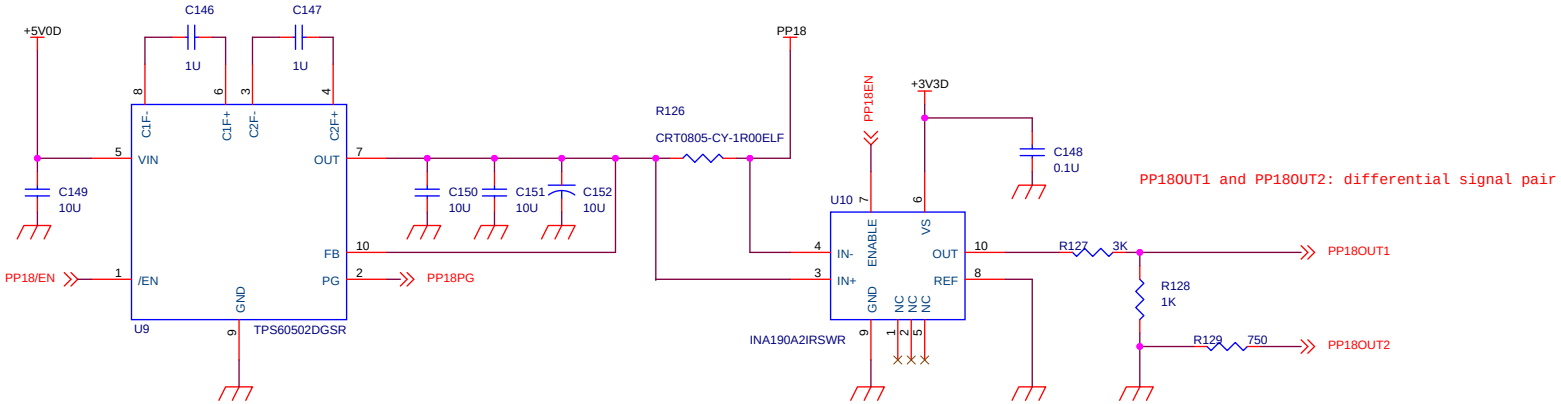


+3V3D for PP ASIC



PP33OUT1 and PP33OUT2: differential signal pair

+1V8D for PP ASIC



PP18OUT1 and PP18OUT2: differential signal pair

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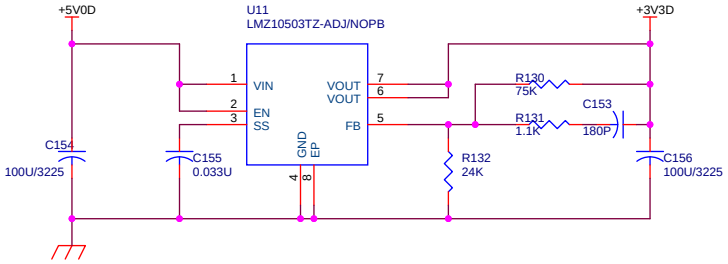
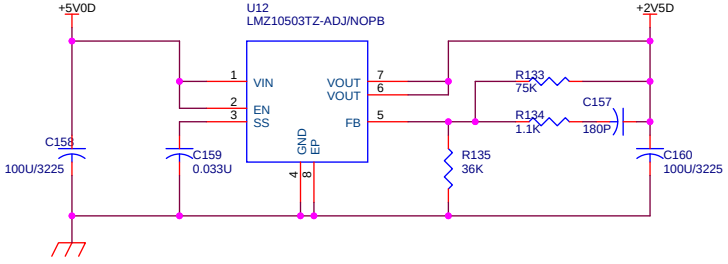
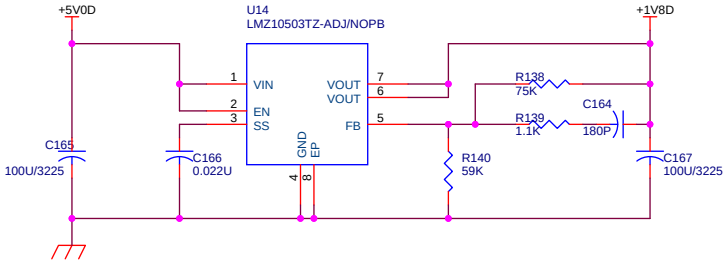
+3V3D for FPGA, etc.



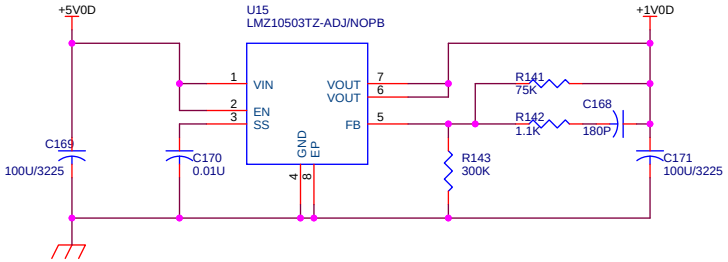
+2V5D for FPGA, etc.



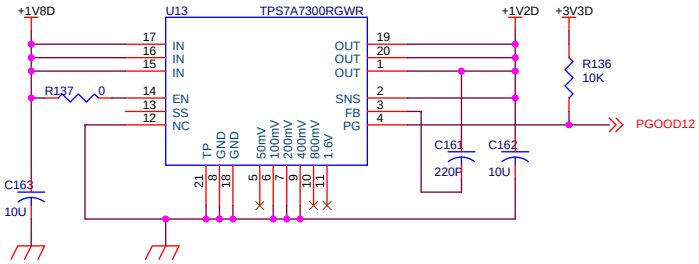
+1V8D for FPGA, etc.



+1V0D for FPGA



+1V2D for Ethernet



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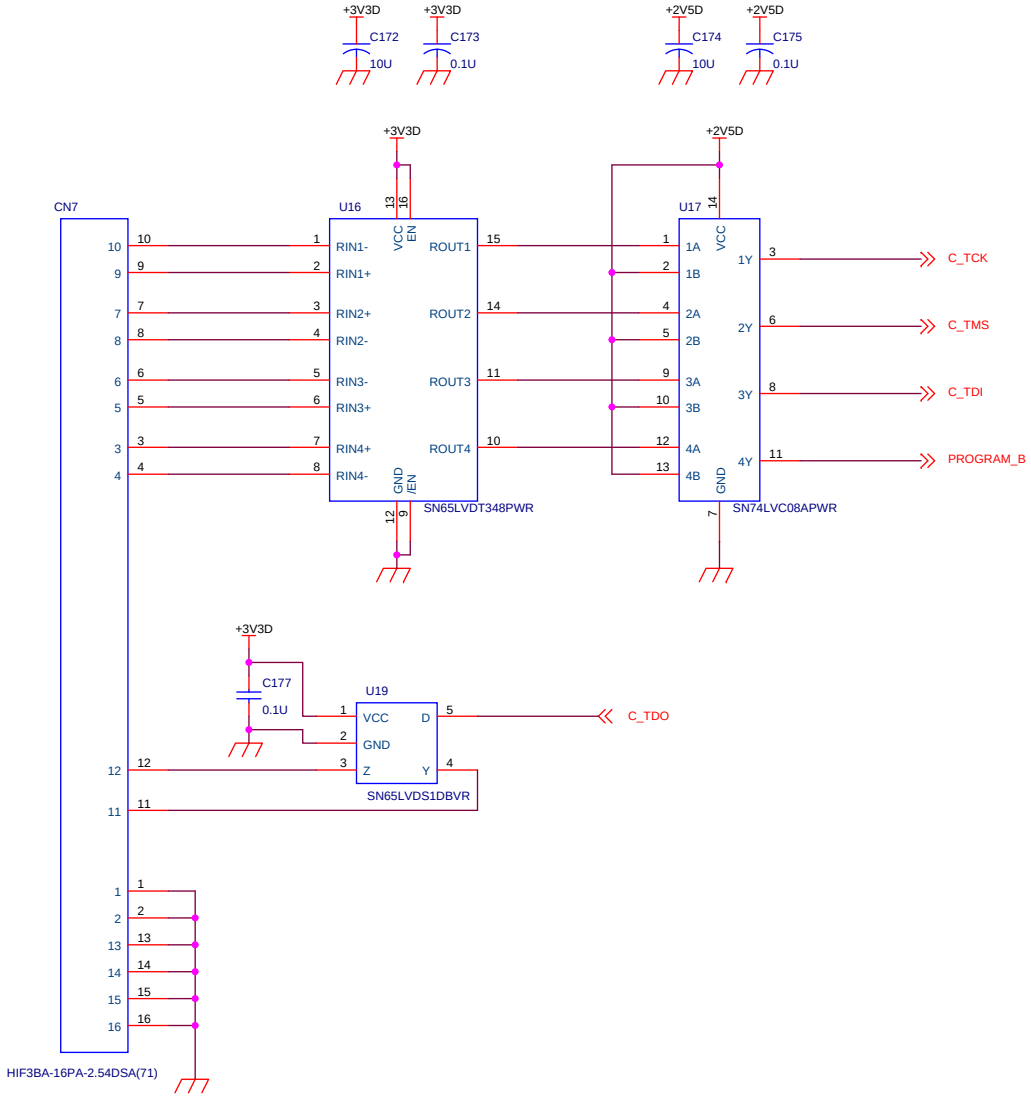
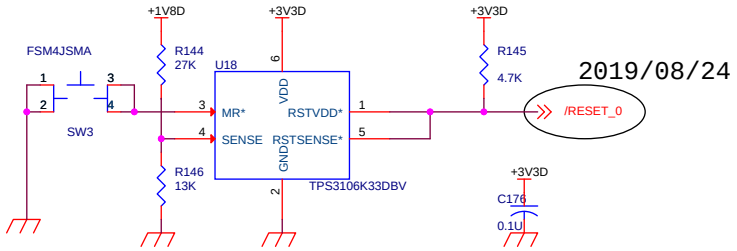
SPP Interface



Reset



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