Phase II TGC PP ASIC

Overview and Preproduction Test Results

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Production Readiness Review

27 Sep. 2019

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  - Full Tests for One Chip
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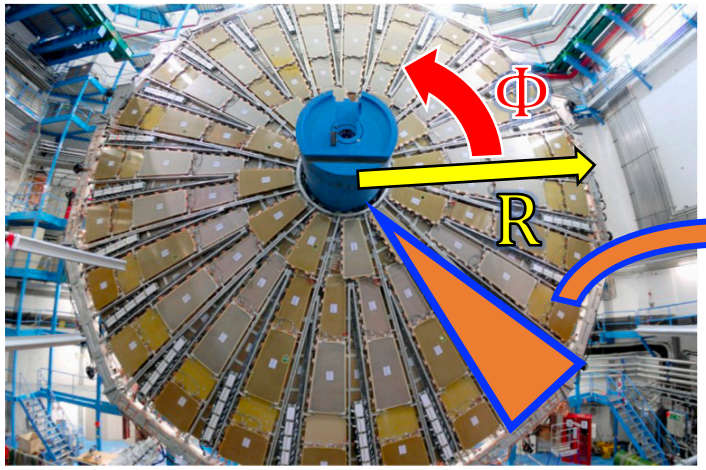
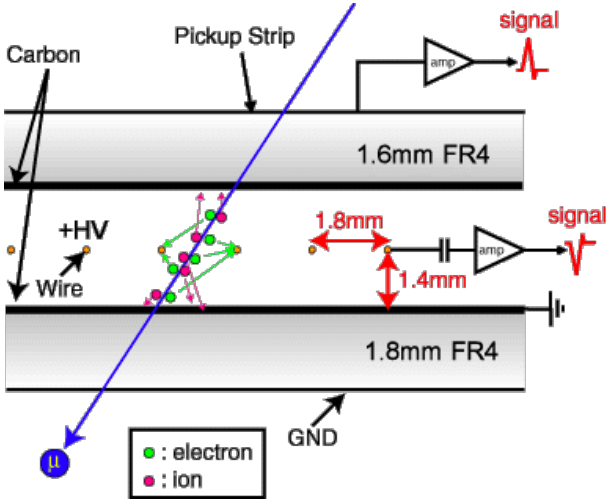
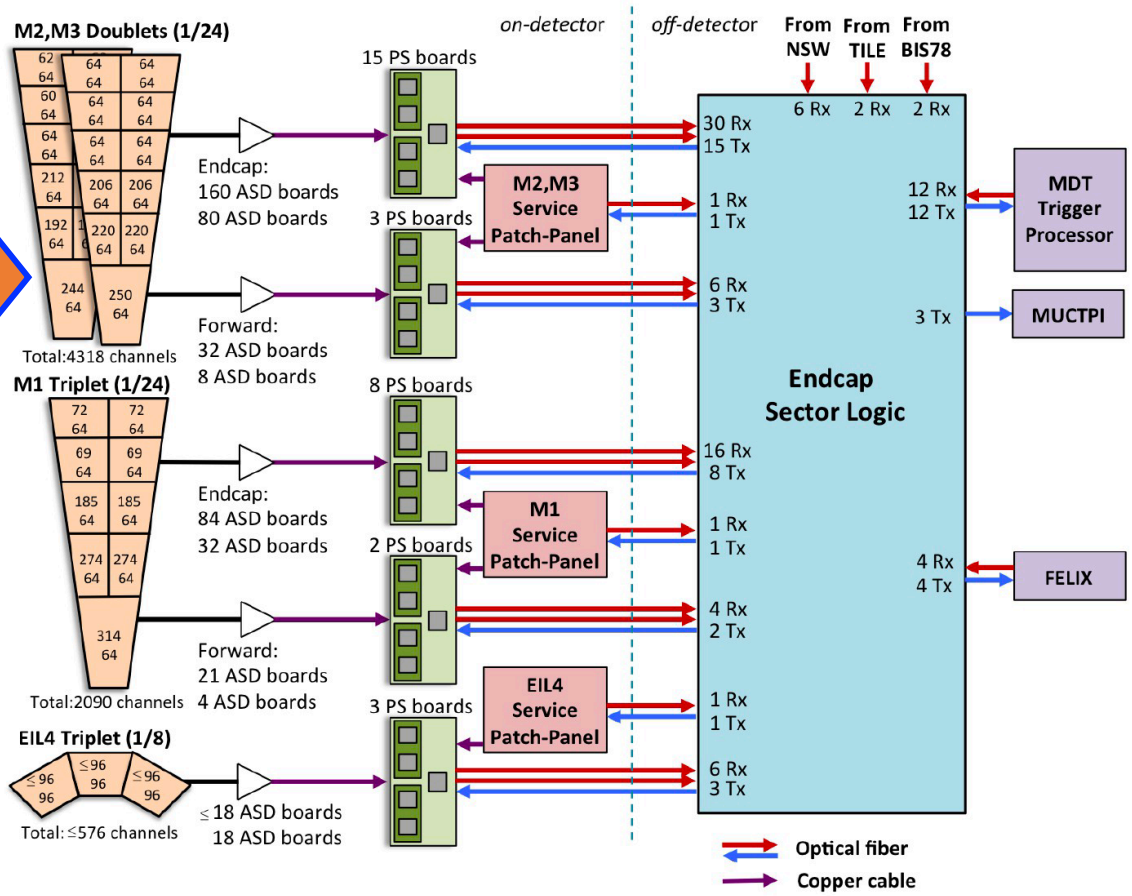
Phase II TGC Trigger and Readout System

Thin Gap Chamber (TGC)



Two-dimensional measurements by the wires and the strips



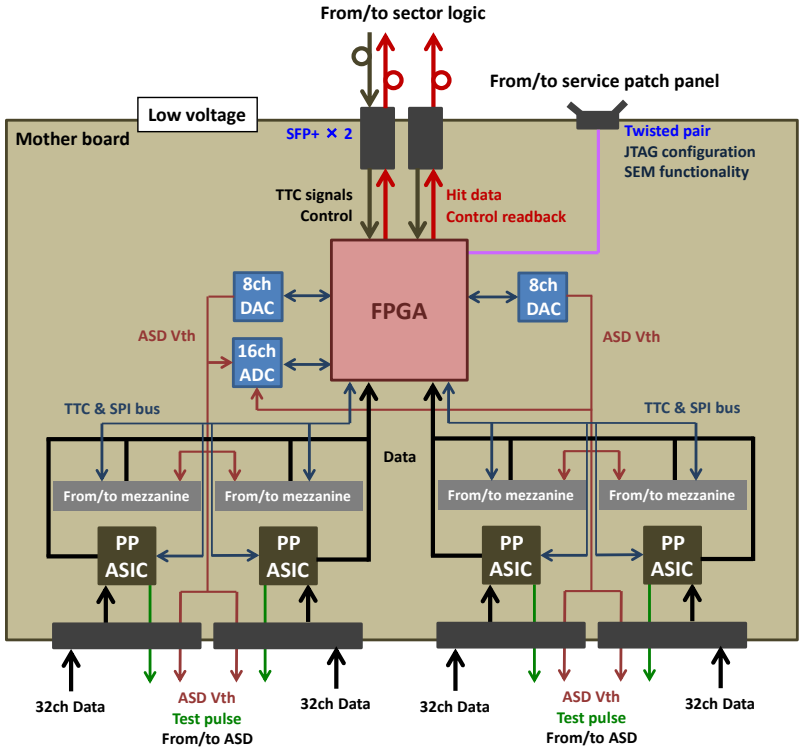


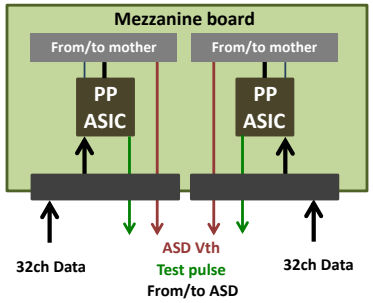
Replace all boards except for ASDs for an extension of the first-level trigger rate (1 MHz) and latency (10 μs).

All hit signals will be transferred to the off-detector boards.

PS Board Overview

PS board contains Patch-Panel (PP) ASICs, FPGA, etc.





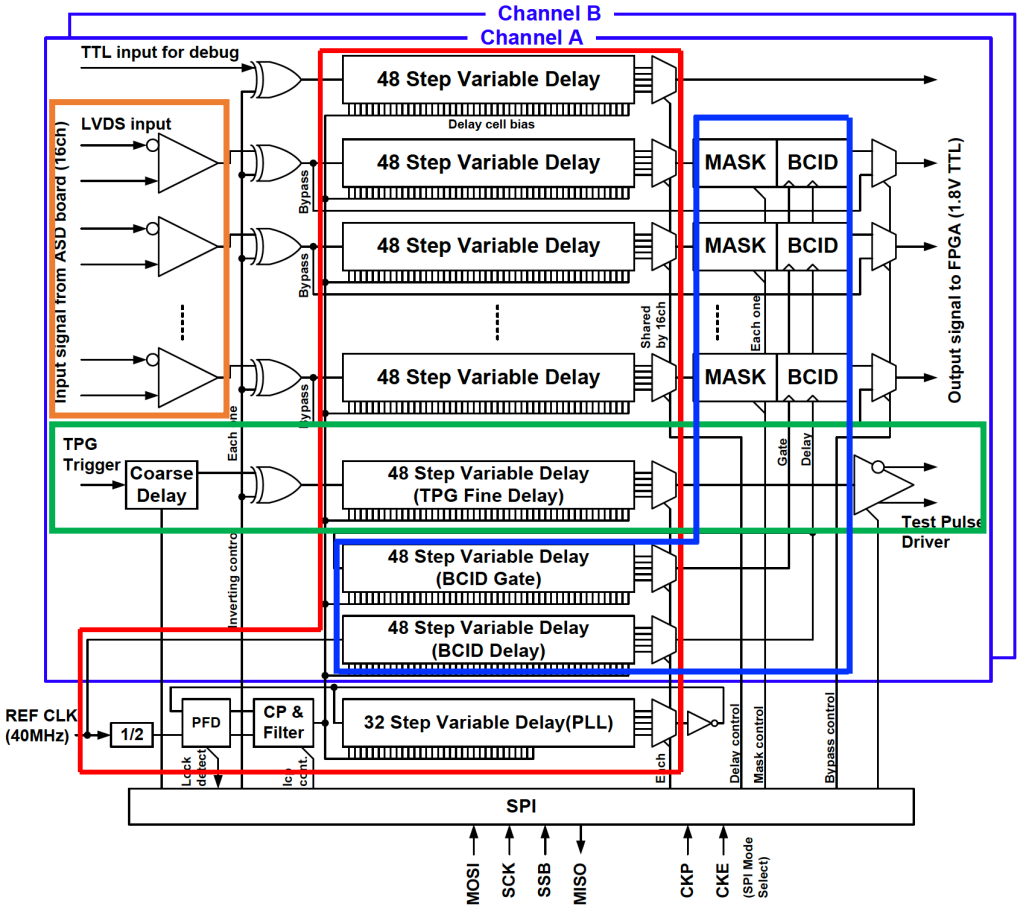
PP ASIC

- Receive LVDS signals from ASDs, and align the timing.
  Send the aligned signals to FPGA.
- Send test pulse to ASDs.

FPGA

- Collect signals from PP ASICs and transfer to off-detector
  (8 Gbps × 2 = 16 Gbps)
- Control threshold voltage of the discriminators of ASDs.

Overview of PP ASIC



Function of PP ASIC

- Receive LVDS signals from ASDs.
- Compensate for delay difference among channels due to time of flight and cable length using PLL and variable delay.
- Synchronize the signal with the 40 MHz clock and identify the bunch crossing.
- Generate test pulse to ASD for tests of readout chain.

PP ASIC Specification

Design process	Silterra 0.18 μm CMOS 6M1P
Supply voltage	3.3 V (LVDS receiver, test pulse generator) 1.8 V (PLL, delay line, CMOS input and output) Voltage tolerance : ± 10 %
# of channels	Group A (16 ch), Group B (16 ch)
Timing control resolution	< 1 ns
Timing control range	> 40 ns
Timing jitter	< 0.1 ns (RMS)
Temperature range	10 ~ 70 ℃
Power consumption	10 mW for data taking, 20~30 mW for test pulse runs (130 mW for the current PP ASICs)

Timeline for PP ASIC Development

- 6 Mar. 2018 : Preliminary Design Review (PDR) was held.
- 3 Oct. 2018 : 20 packaged prototype chips were delivered.

All functions were fine, but small modifications were suggested.

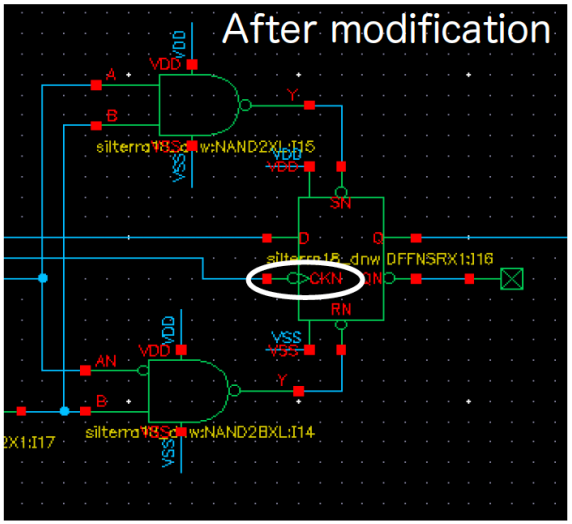
- 6 Dec. 2018 : Final Design Review (FDR) was held.
- Mar. 2019 : Production of ~25000 final chips was completed and 669 packaged chips were delivered.

Full measurement for one chip and simplified quality check for 200 chips were performed (see the following slides).

Design for Preproduction

Final chips were designed by applying two modifications to prototype chips.

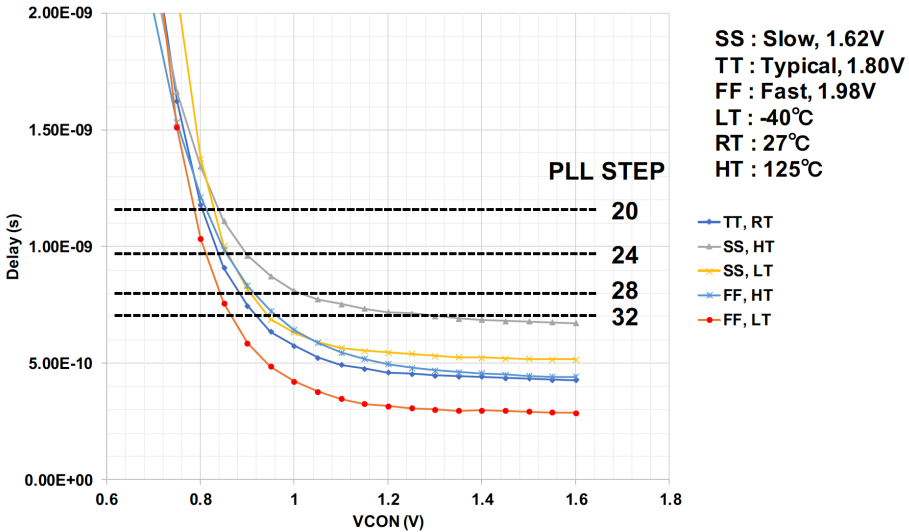
1) Prototype has a wrong edge setup of SPI MISO signal.
Although it is fine for the use if the device controlling the PP ASIC uses the corresponding edge,
as done for prototype measurement,
we corrected the edge for final chips.



2) Gate length of transistors in the delay units of PLL and variable delay was changed for lower delay time for an improved margin.

	Gate length of transistor
Prototype chip	1 μm
Final chip	0.5 μm

The target delay is covered even with SS, HT condition.



Test Items for Final Chips

All functions were confirmed for one chip. Analog specification in PLL was confirmed for ten chips. All channel outputs and power consumption were tested for 200 chips.

SPI-based configuration
- Confirmation of MISO edge*

LVDS Receiver
- Propagation delay depending on various parameters, e.g. amplitude of input signal

PLL and Variable Delay
- Relation between Delay and Control Voltage (V_{CON})*
- Comparison with the Simulation*
- Delay Dependence on Temperature*
- Linearity of the Variable Delay*
- Performance of the variable delay depending on VDD and temperature.

BCID
- Effective gate width of BCID
- BCID output for several delay setups

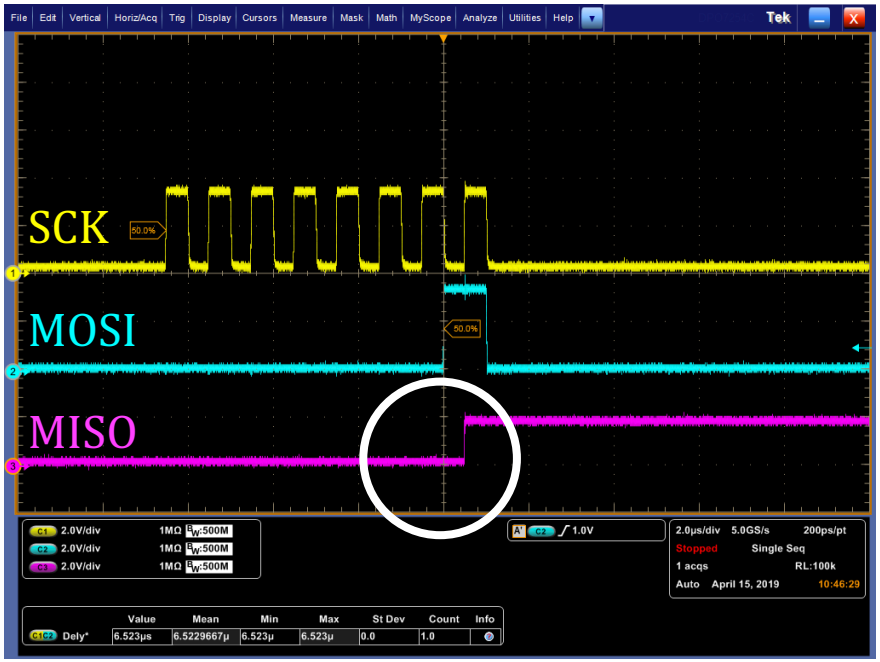
Test Pulse Generator
- Amplitude of the differential output of the test pulse generator for four bias control values
- Amplitude depending on temperature and VDD
- Coarse and fine delay

Power Consumption

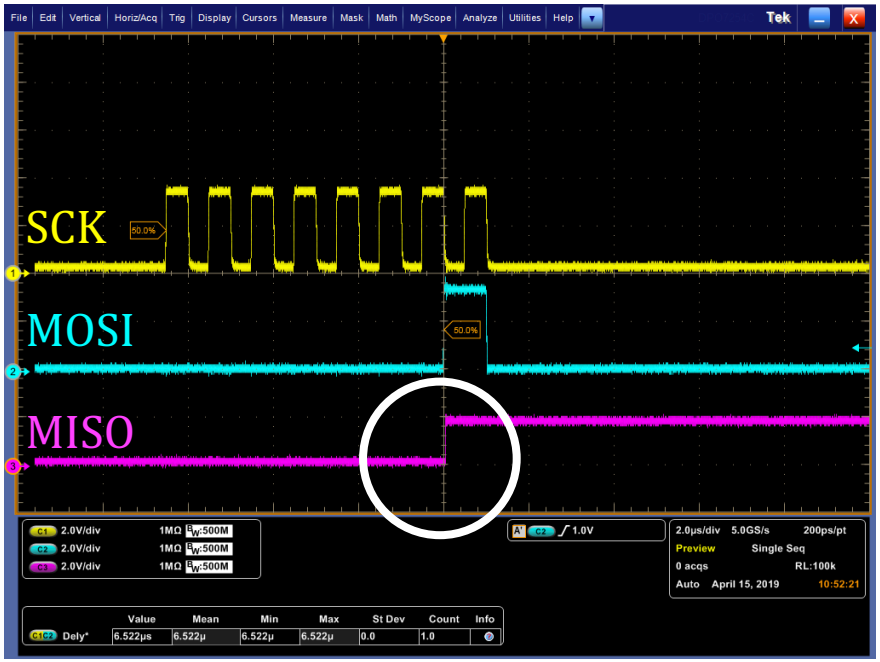
The red contents* will be shown in the following pages.

Confirmation of SPI MISO Correction

Prototype chip



Final chip



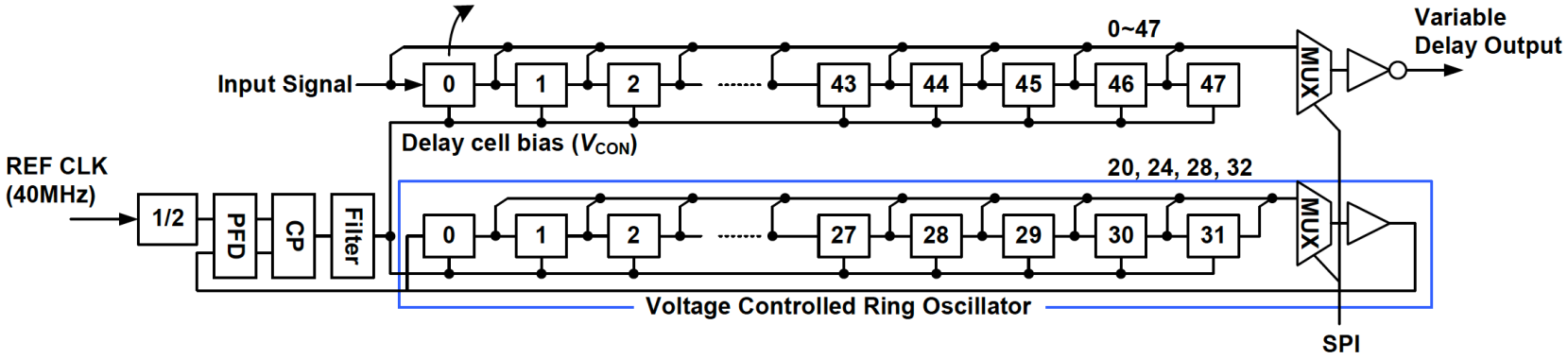
The correction of SPI MISO edge was confirmed with oscilloscope (see the above pictures).
In addition, SPI-based PP ASIC configuration was confirmed with various configuration setups.

PLL and Variable Delay Overview

- A common delay cell design is used in both PLL and variable delay lines. They are controlled by a common bias voltage (V_{CON}) which is generated from charge pump circuit in PLL.

- PLL keeps the signal propagation delay of the ring at 25 ns. The number of delay cells in PLL can be changed from 20 to 32 via SPI control signal.

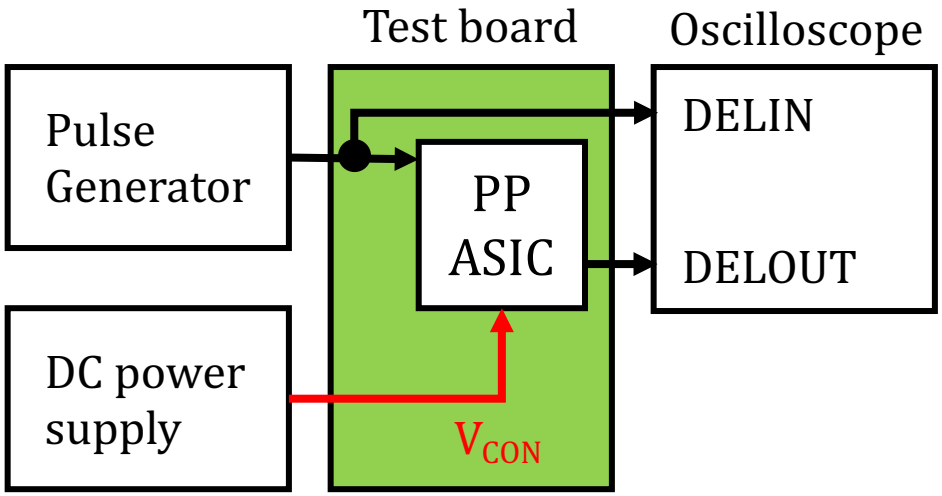
- The propagation delay of the variable delay will be kept constant against the changes of operation conditions.

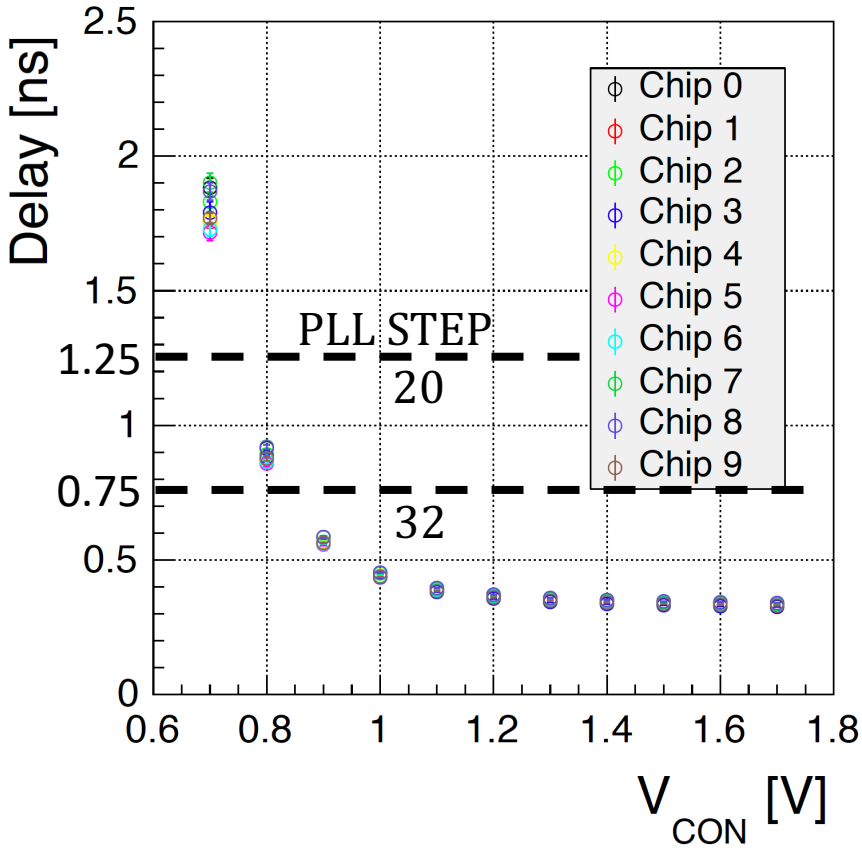


PLL and Variable Delay Result 1

Delay of a delay cell of 10 chips was measured depending on V_{CON}.

V_{CON} was supplied by DC power supply.

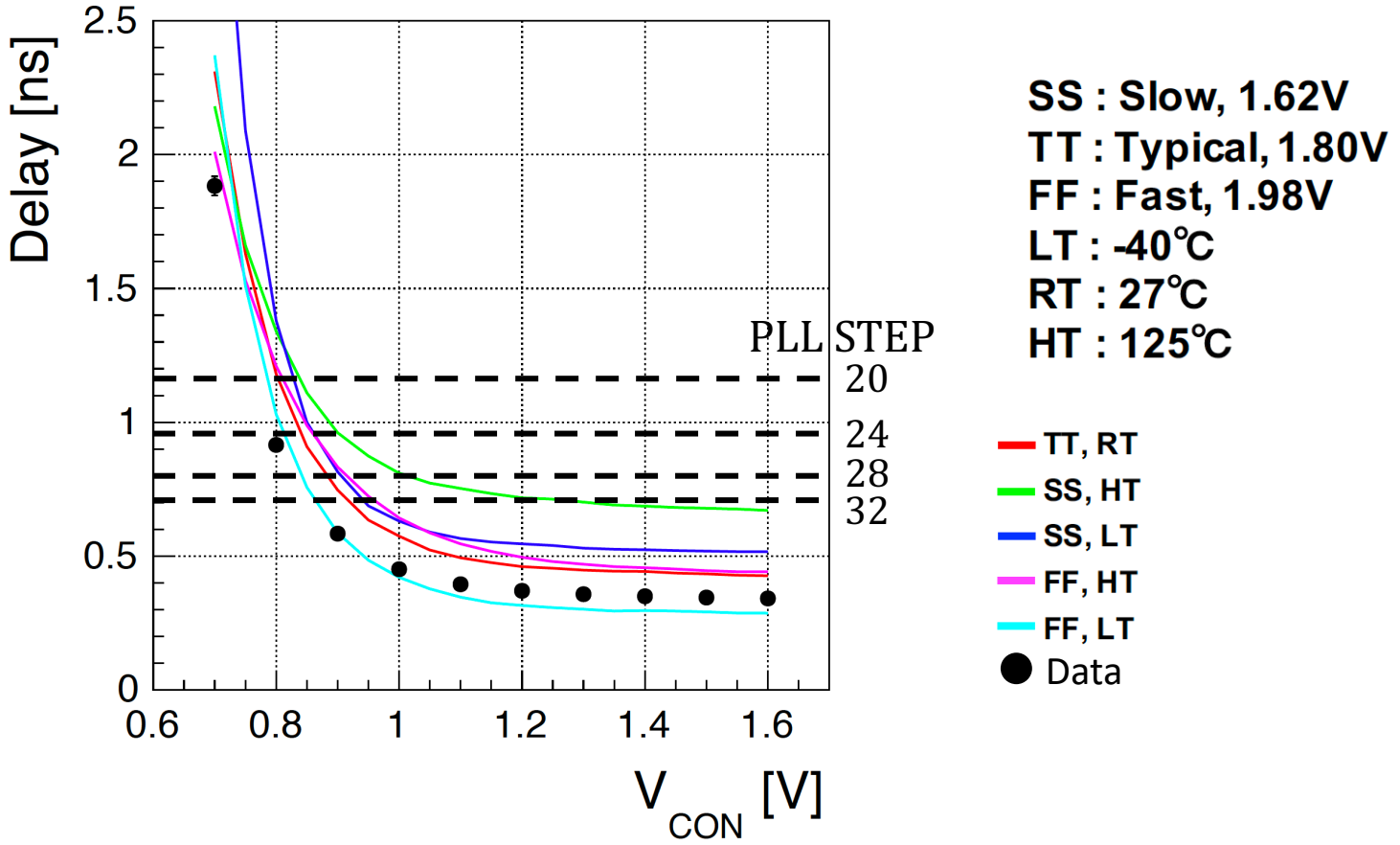




The delay can be changed from 0.3 ns to 1.9 ns.

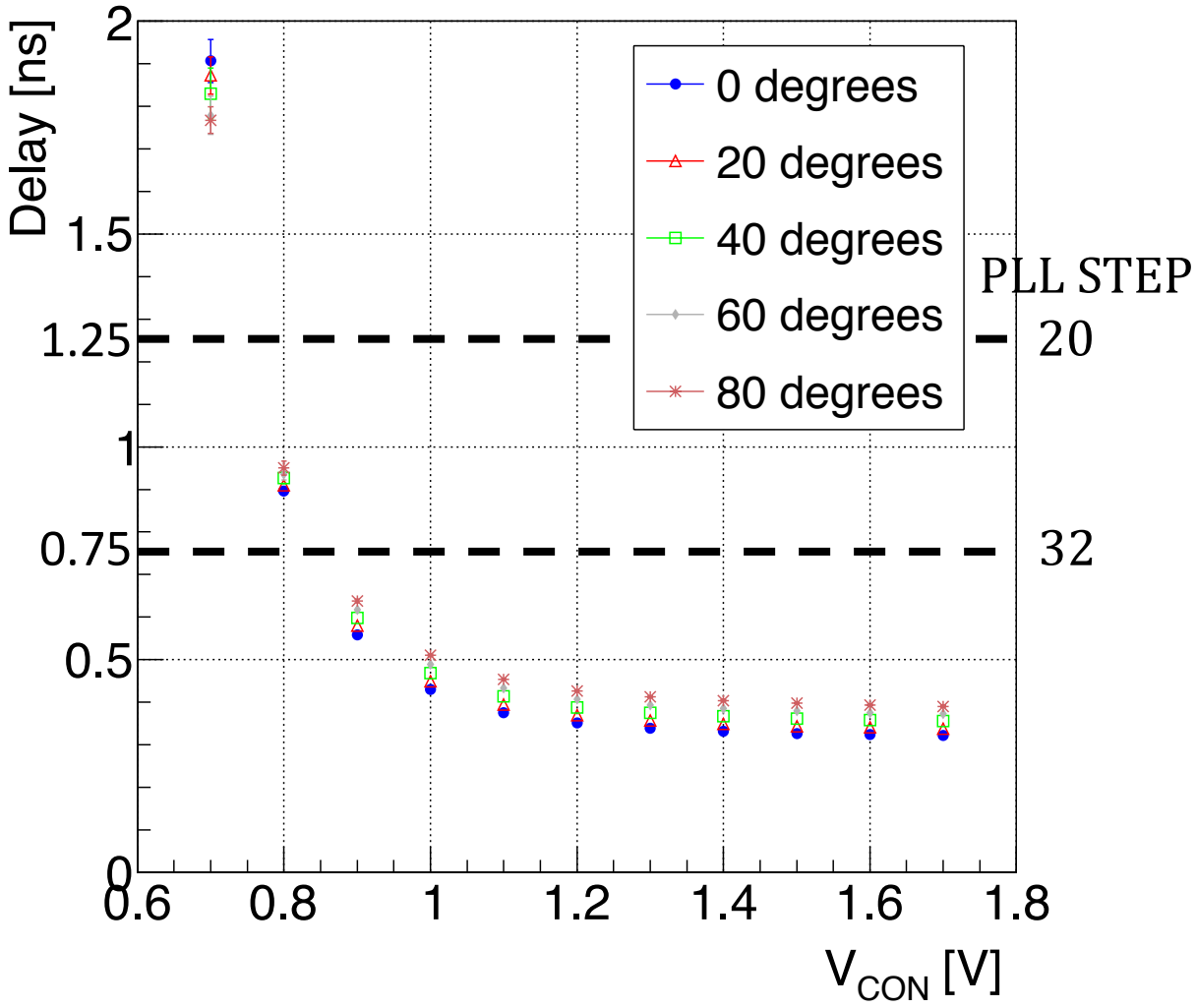
The requirement of timing control resolution < 1 ns is satisfied with margin.

PLL and Variable Delay Result 2



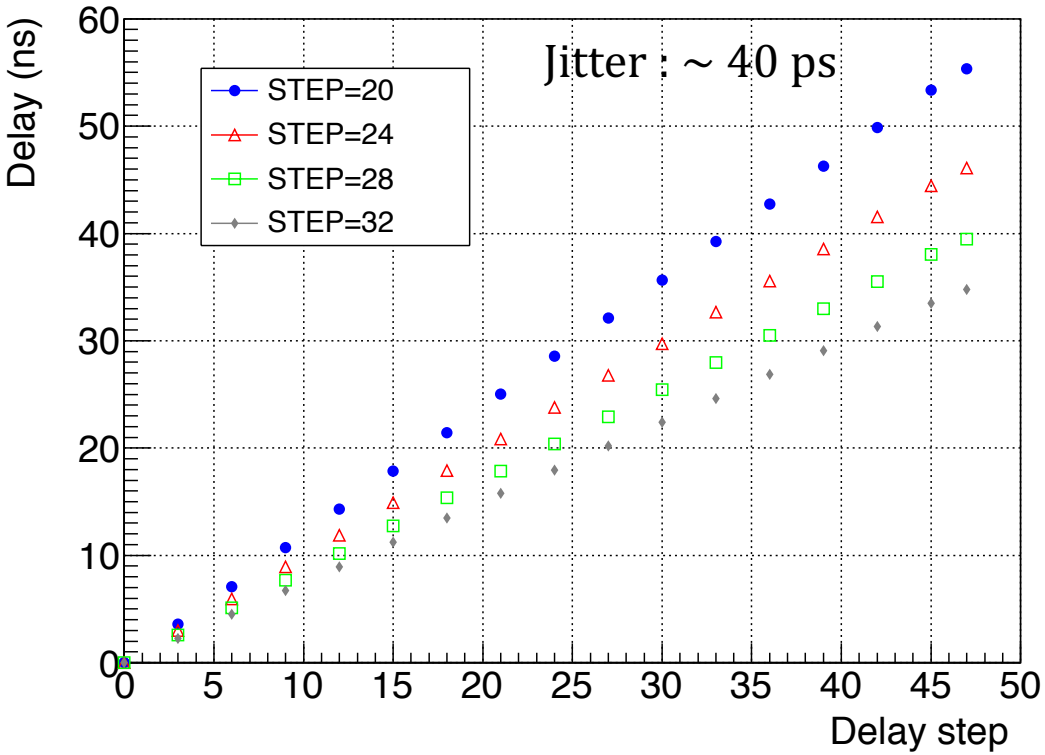
The measured delay is similar
to the Layout Parasitic Extraction (LPE) simulation with condition “FF,LT”.

PLL and Variable Delay Result 3



The delay < 1 ns is covered for 0-80 degrees.

PLL and Variable Delay Result 4

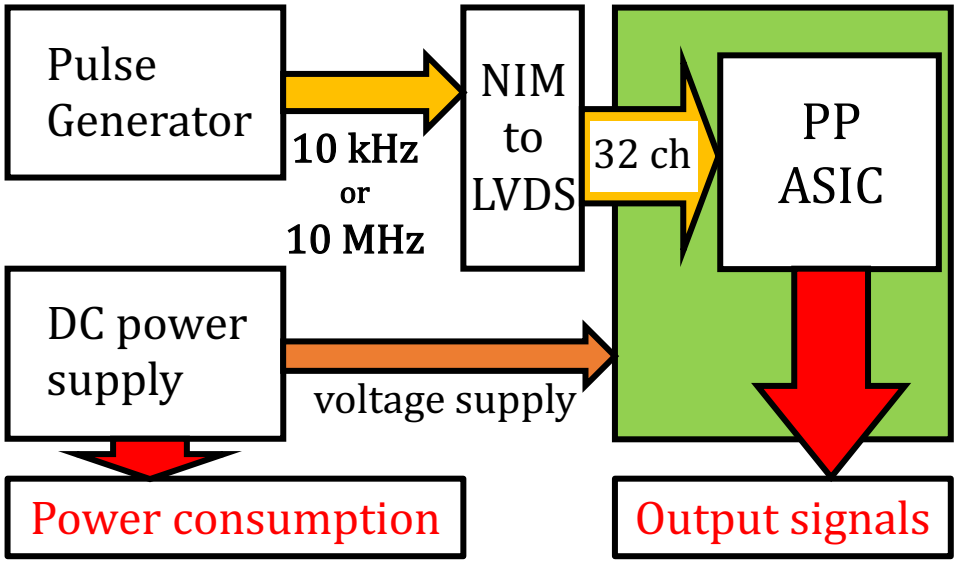


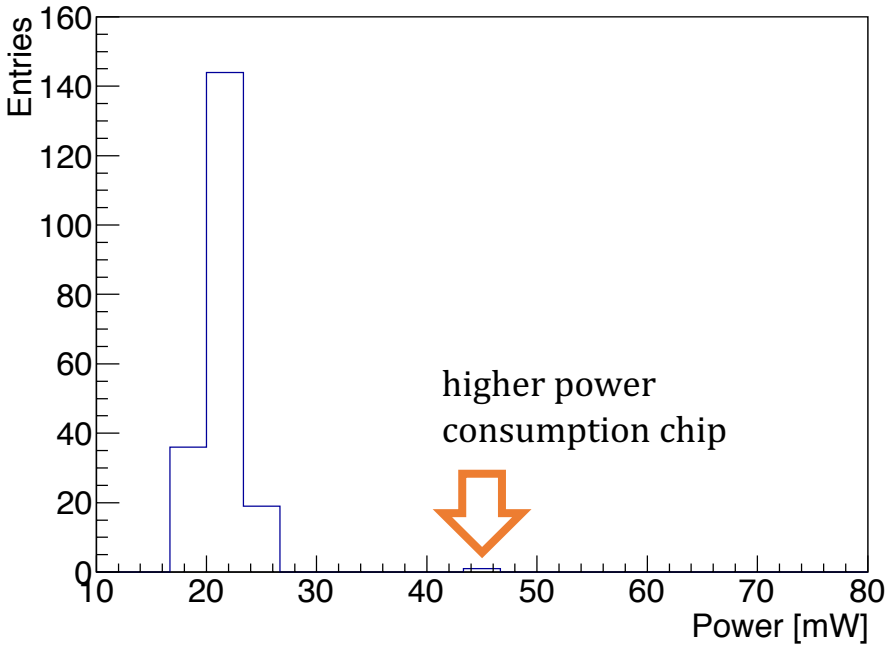
PLL STEP	Delay per step [ns]
20	1.2
24	0.99
28	0.84
32	0.74

- The linearity has been confirmed for all STEP configurations.
- The delay of single step is < 1 ns (target specification) for STEP $\geqq 24$.
- The dynamic range is greater than the target specification (40 ns).

Quality Checks for 200 Chips

For all channels of 200 chips, two sets of pulse input were provided:
10 kHz and 10 MHz.





Distribution of power consumption at 10 kHz

For all channels, output pulse width (25 ns or 50 ns) and height (LVCMOS 1.8 V) were confirmed.

The power consumption for 10 kHz (10 MHz) input ranges from 19 mW to 24 mW (from 44 mW to 49 mW) for 199 chips.

One chip had higher power consumption for 3.3 V supply. It was 44 mW (71 mW).

We concluded that 199 chips are fine among the tested 200 chips.

Summary

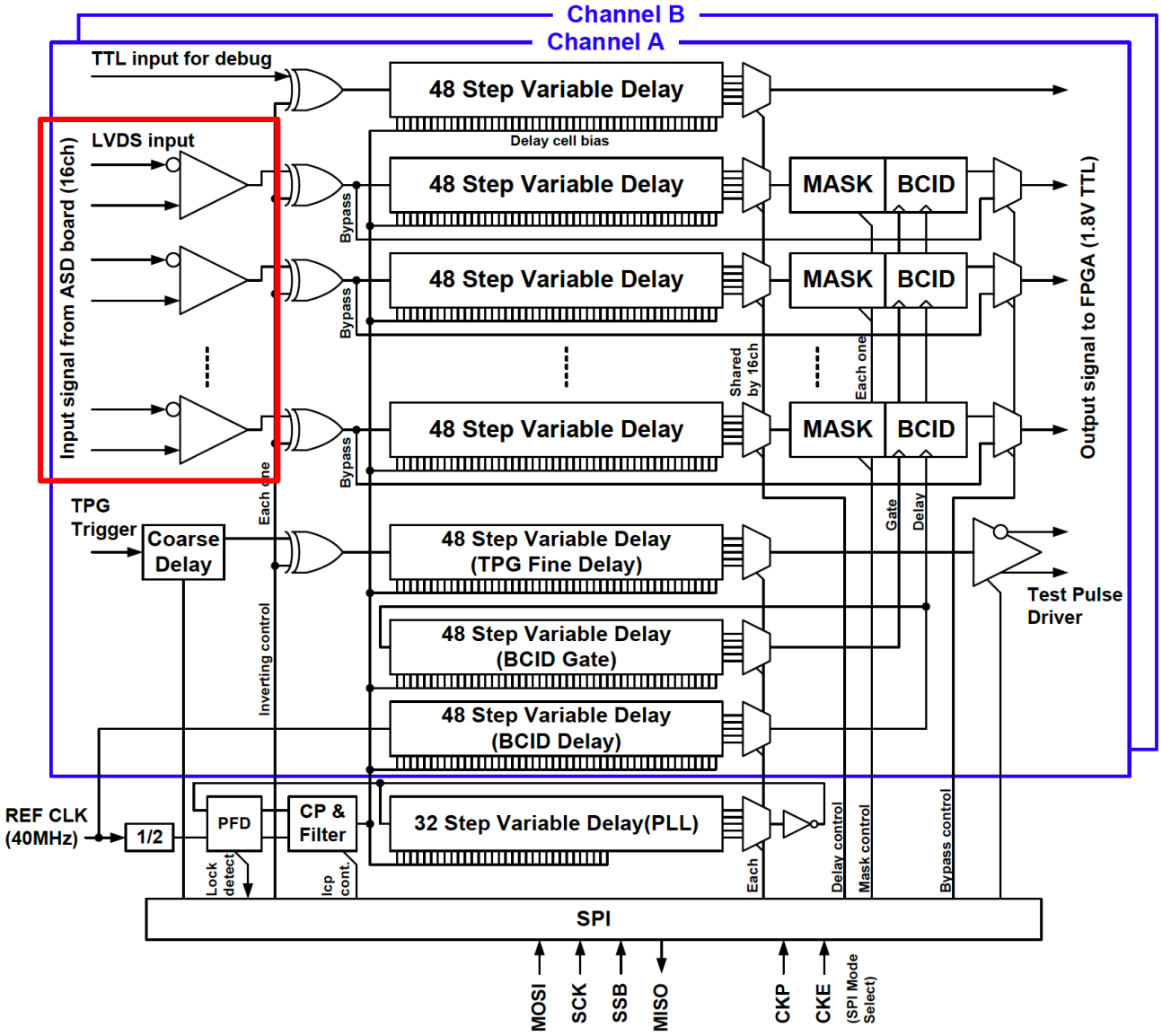
Production of ~25000 final chips and the packaging for 699 chips were completed in Mar. 2019.

Full test was performed for one chip, and analog specification of PLL was tested for ten chips. All the results were fine.

Simplified quality check was performed for 200 chips, and 199 chips were fine (99.5 % yield).

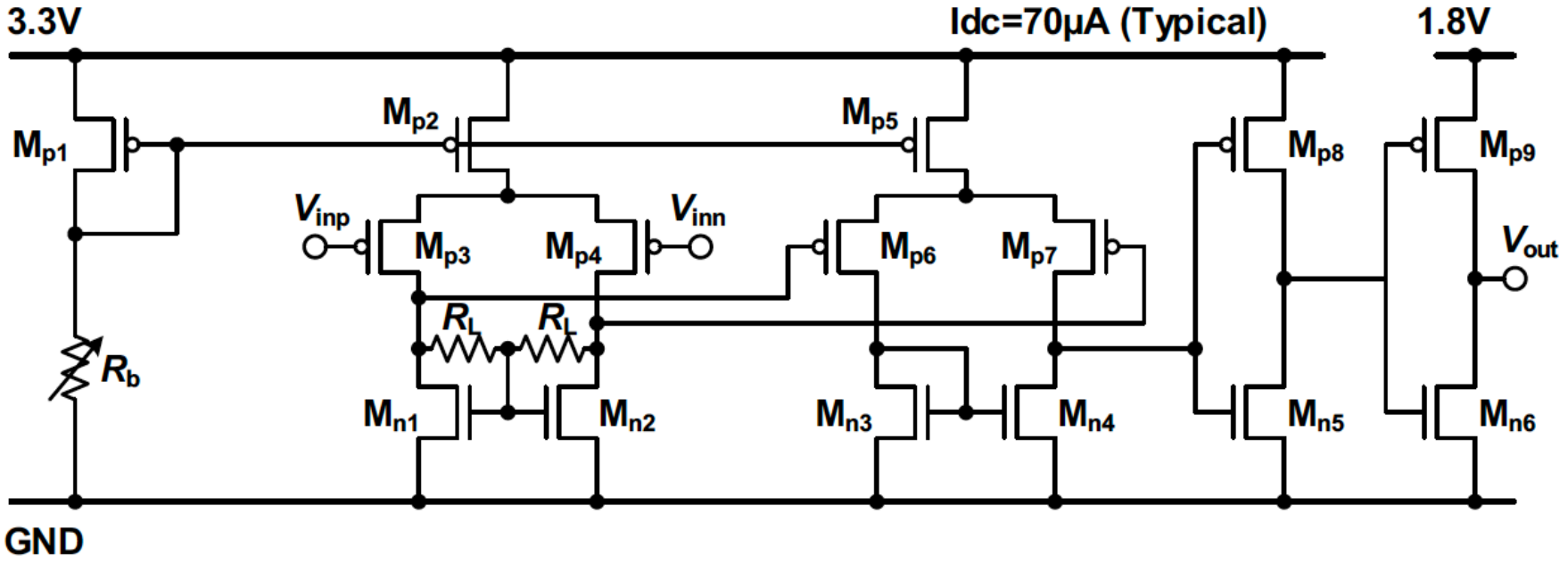
BACK UP

LVDS Receiver



Schematic of LVDS Receiver

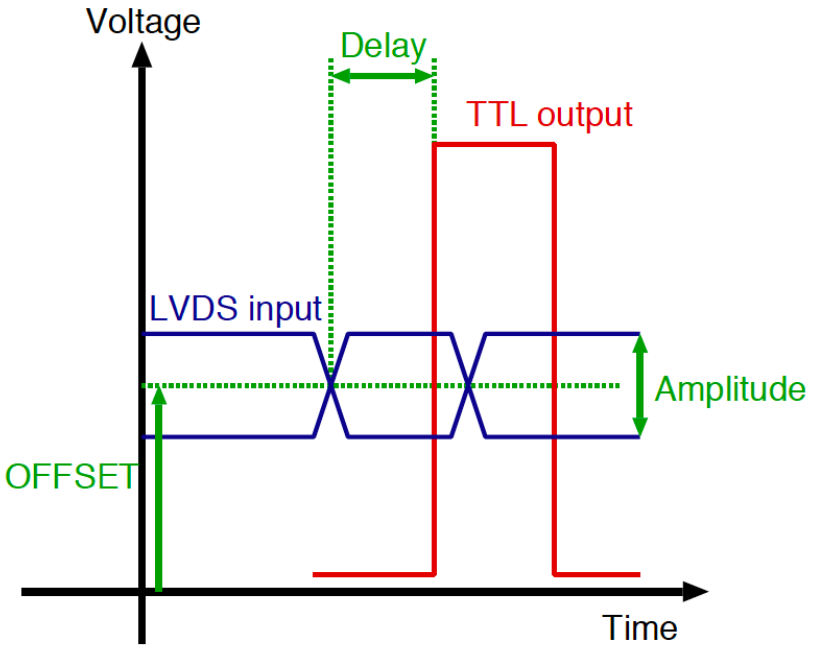
- LVDS receiver consists of two differential amplifiers and two stages of inverter.
- Level shifter is implemented in LVDS receiver. (3.3 V→1.8 V)
- LVDS Rx is not fully compatible with the LVDS receiver standard specification (IEEE 1596.3).

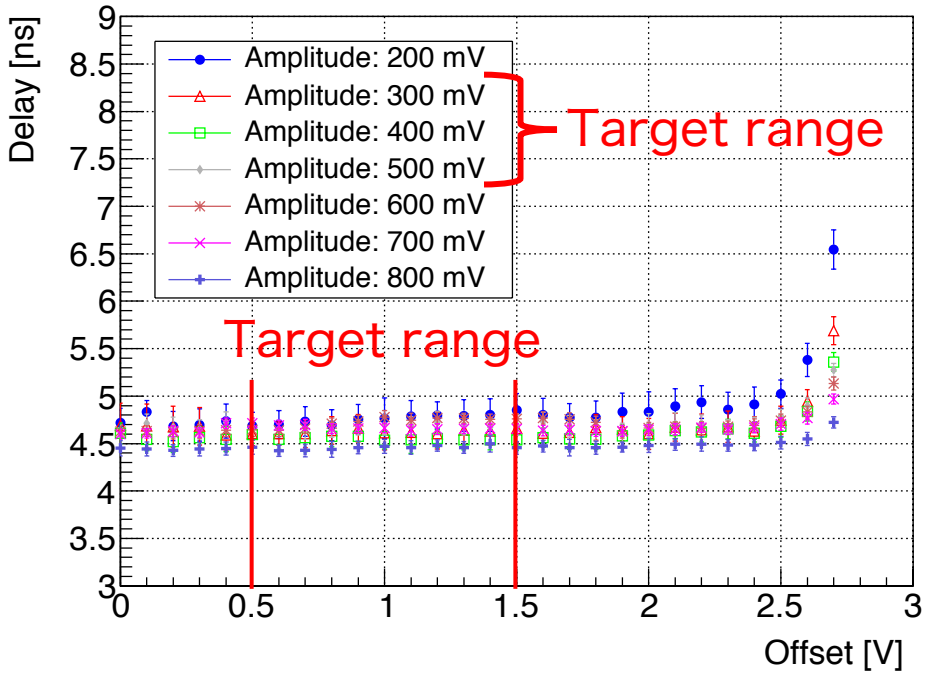


Delay Dependence on Offset and Amplitude

Delay of the LVDS receiver was measured depending on amplitude and offset.

Offset voltage is defined to be the central voltage of the input differential signals.



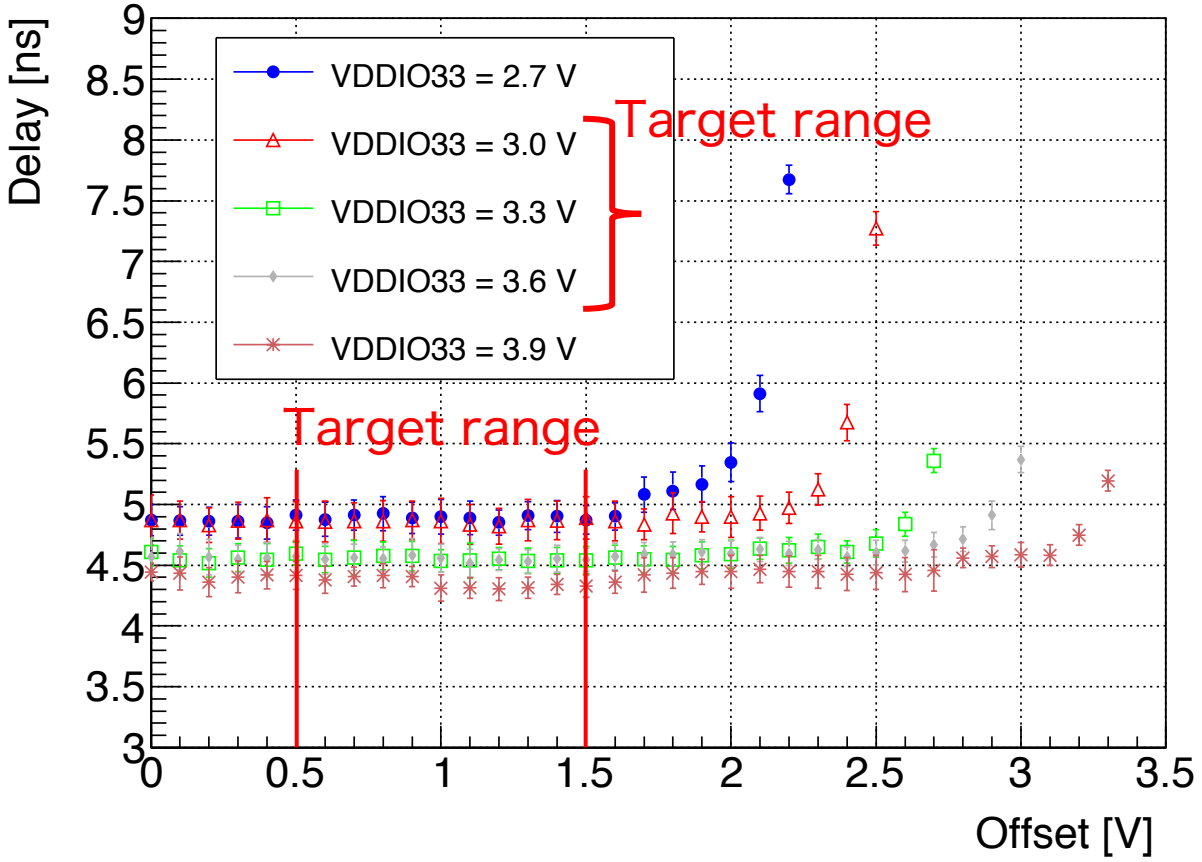


The measured delay is the sum of the propagation delay of the receiver, the multiplexer, and the output buffer.

The delay is 4.6 ± 0.2 ns for target ranges of amplitude and offset satisfies the requirement of timing control resolution < 1 ns.

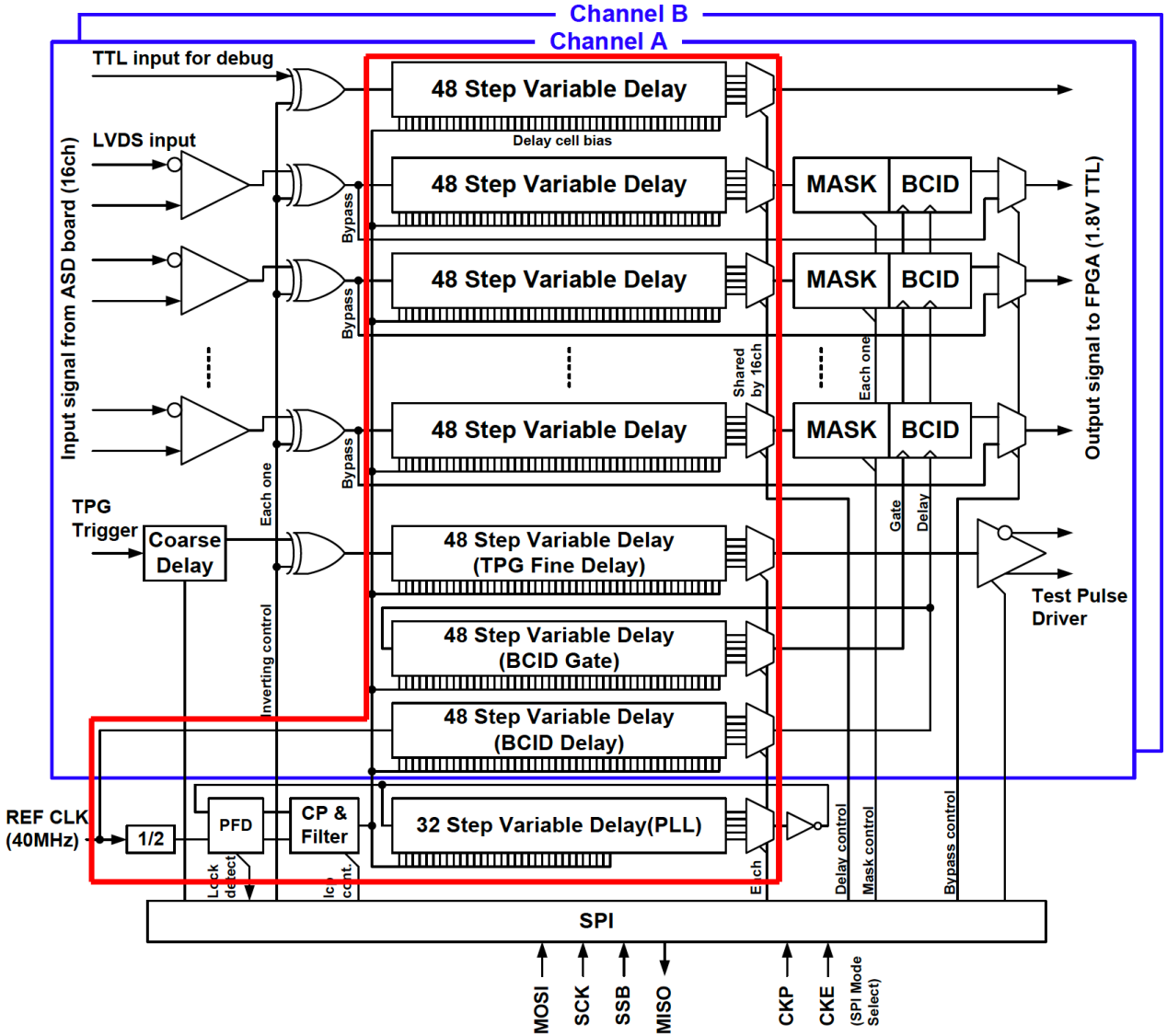
Delay Dependence on VDD and Offset

Delay of the LVDS receiver was measured depending on VDD and offset.



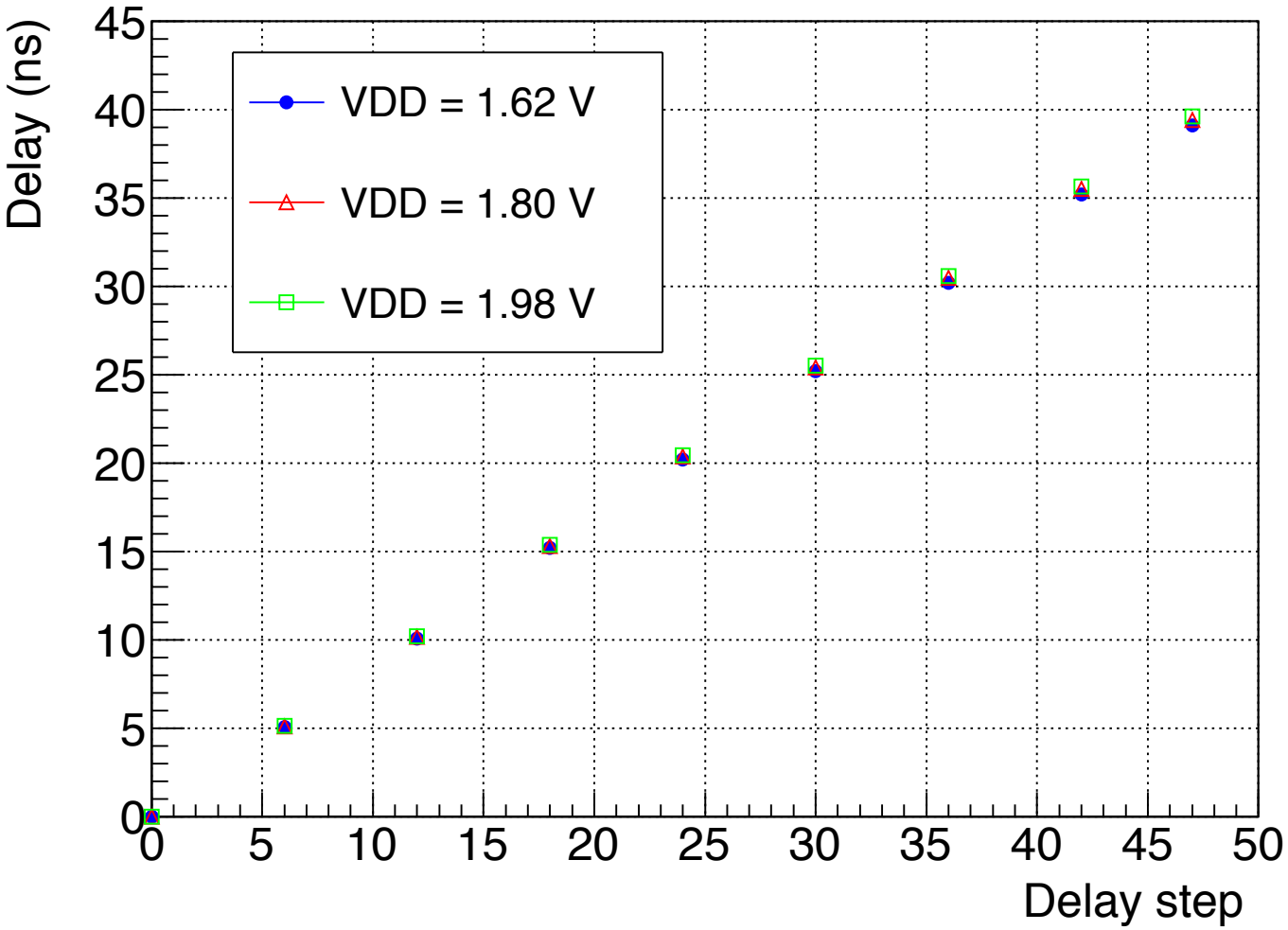
The delay is 4.6 ± 0.3 ns for target ranges of VDD
and offset satisfies the requirement of timing control resolution < 1 ns.

PLL and Variable Delay

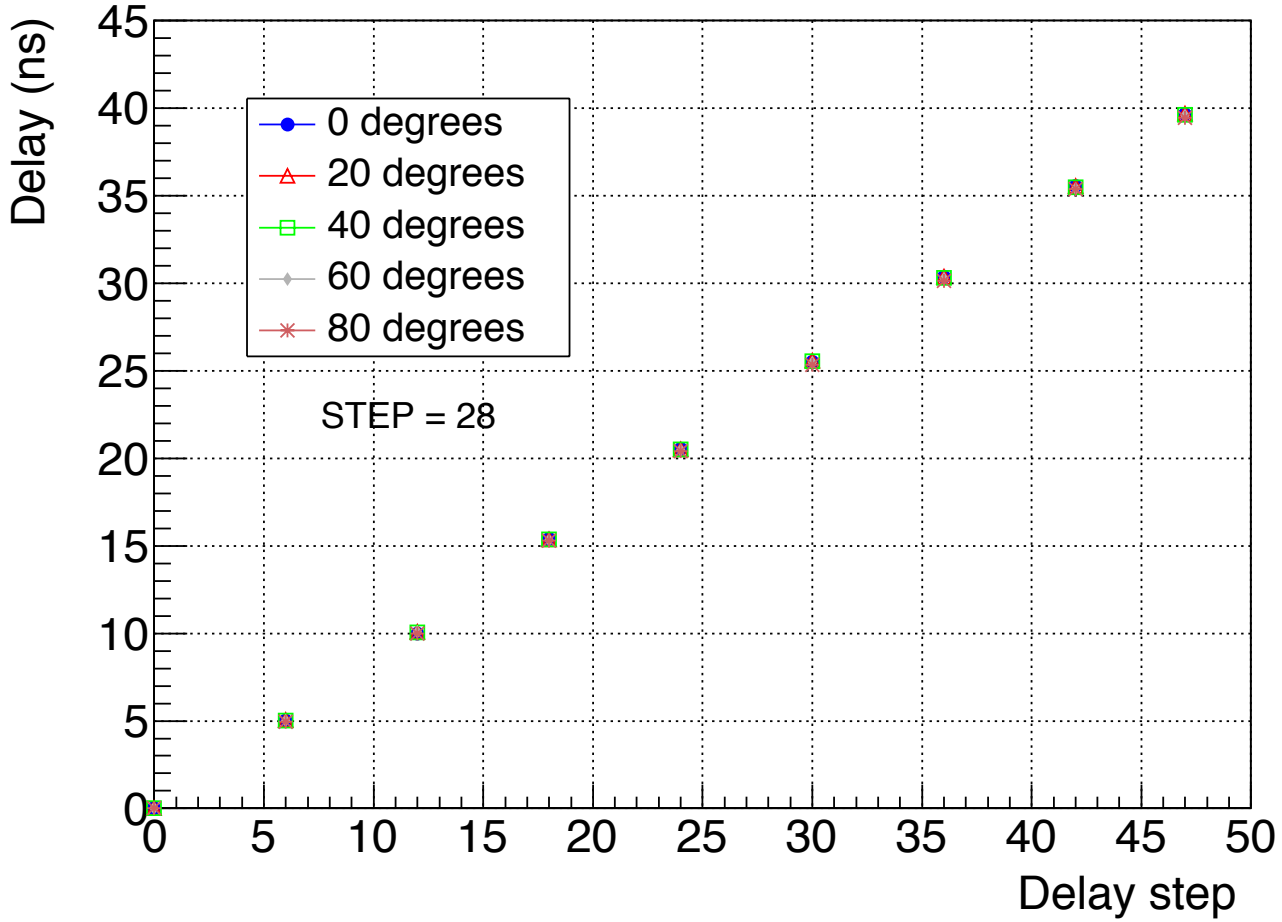


Performance of the Variable Delay Depending on VDD

The linearity of variable delay was confirmed for VDD = 1.62-1.98 V.

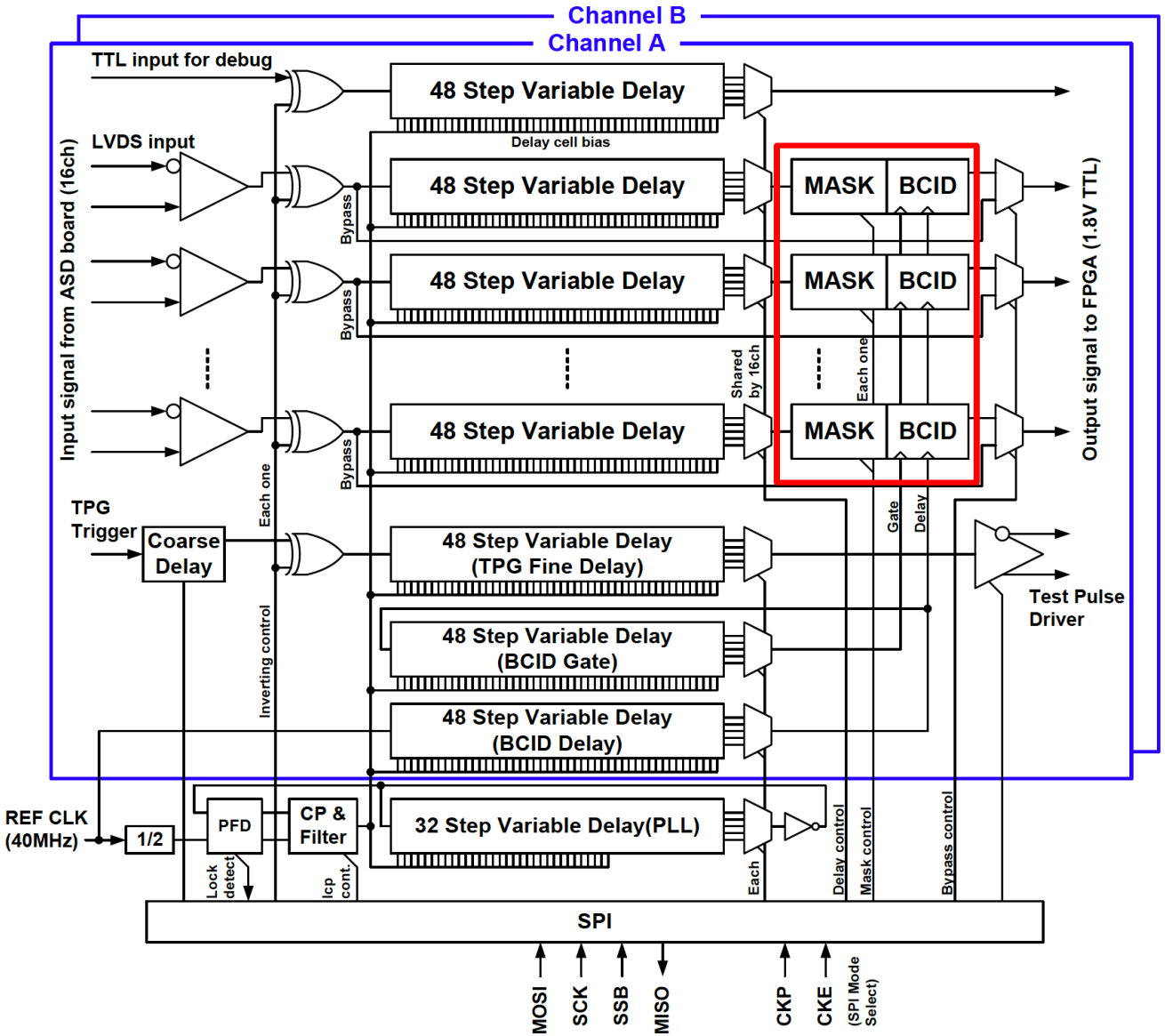


Performance of the Variable Delay Depending on Temperature

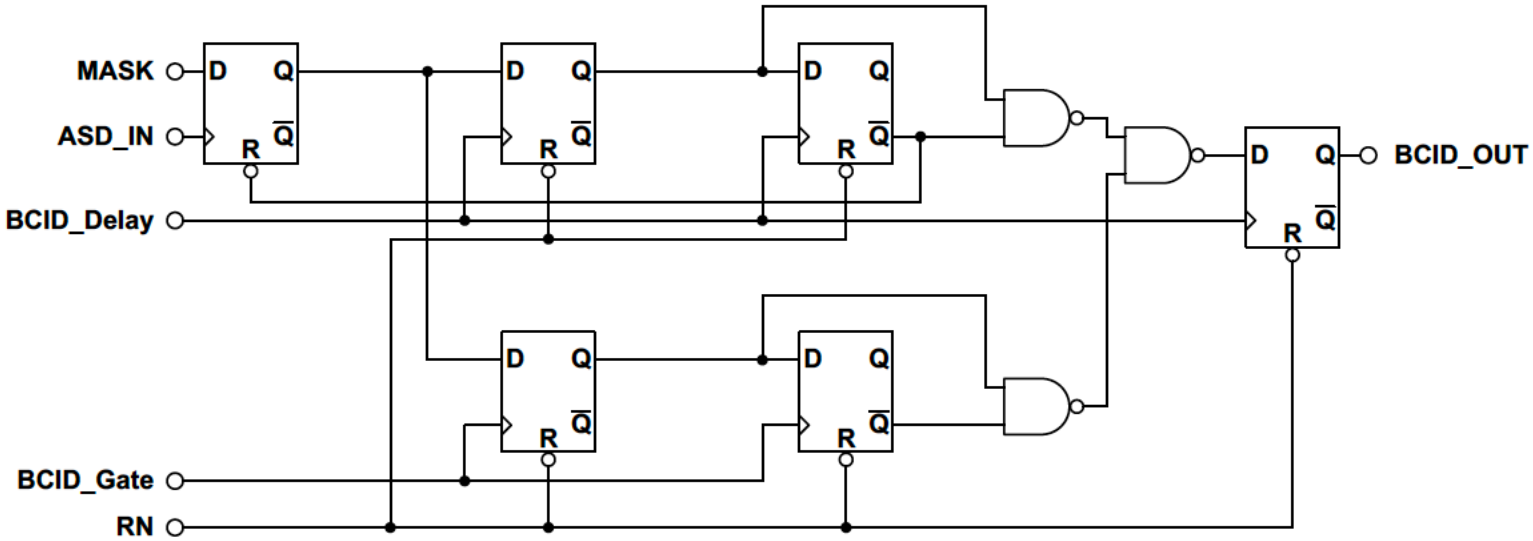


The linearity of variable delay was confirmed for 0-80 degrees.

BCID

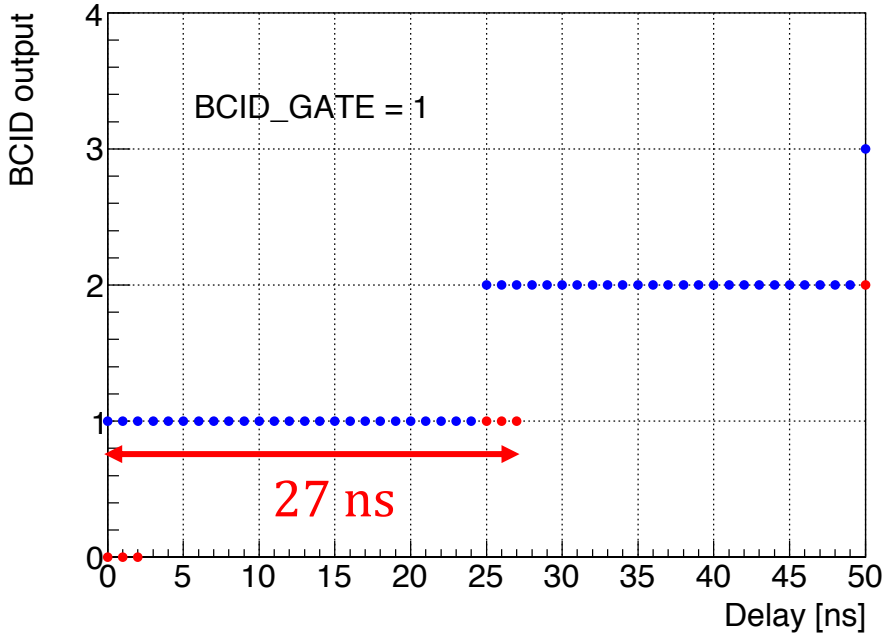

Channel B
Channel A
TTL input for debug
LVDS input
Input signal from ASD board (16ch)
48 Step Variable Delay
Delay cell bias
48 Step Variable Delay
48 Step Variable Delay
48 Step Variable Delay
Bypass
Bypass
Bypass
Shared by 16ch
Each one
MASK
BCID
MASK
BCID
MASK
BCID
Output signal to FPGA (1.8V TTL)
TPG Trigger
Coarse Delay
Each one
48 Step Variable Delay (TPG Fine Delay)
48 Step Variable Delay (BCID Gate)
48 Step Variable Delay (BCID Delay)
Gate
Delay
Test Pulse Driver
Inverting control
REF CLK (40MHz)
1/2
PFD
CP & Filter
32 Step Variable Delay(PLL)
Lock detect
Icp cont.
Each
Delay control
Mask control
Bypass control
SPI
MOSI
SCK
SSB
MISO
CKP
CKE
(SPI Mode Select)

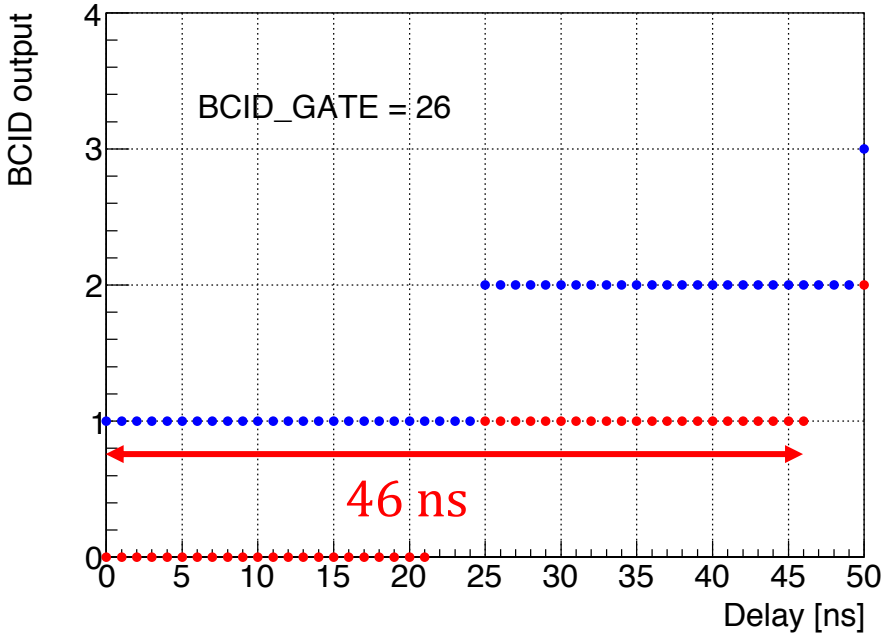
BCID



- The BCID circuit synchronizes the signals with 40 MHz clock.
- Each rising edge of the 40 MHz clock corresponds to a bunch crossing.
- BCID_Delay is used to adjust for the phase difference between the 40 MHz clock and the earliest arrival times of signals from ASDs.
- BCID_Gate is used to adjust the effective gate width. Each signal is assigned to either one or two bunch crossings depending on the timing.

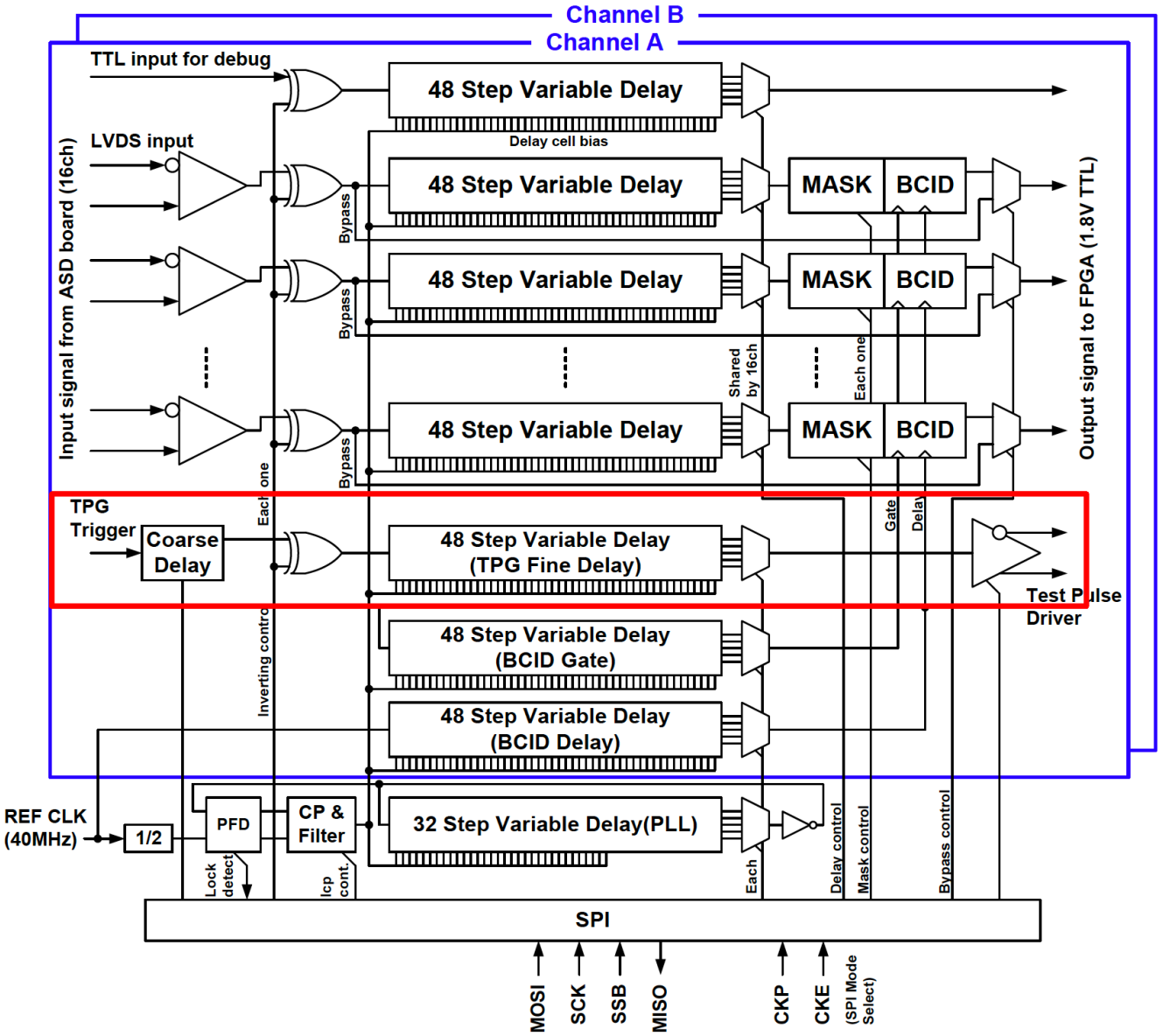
BCID Test Results



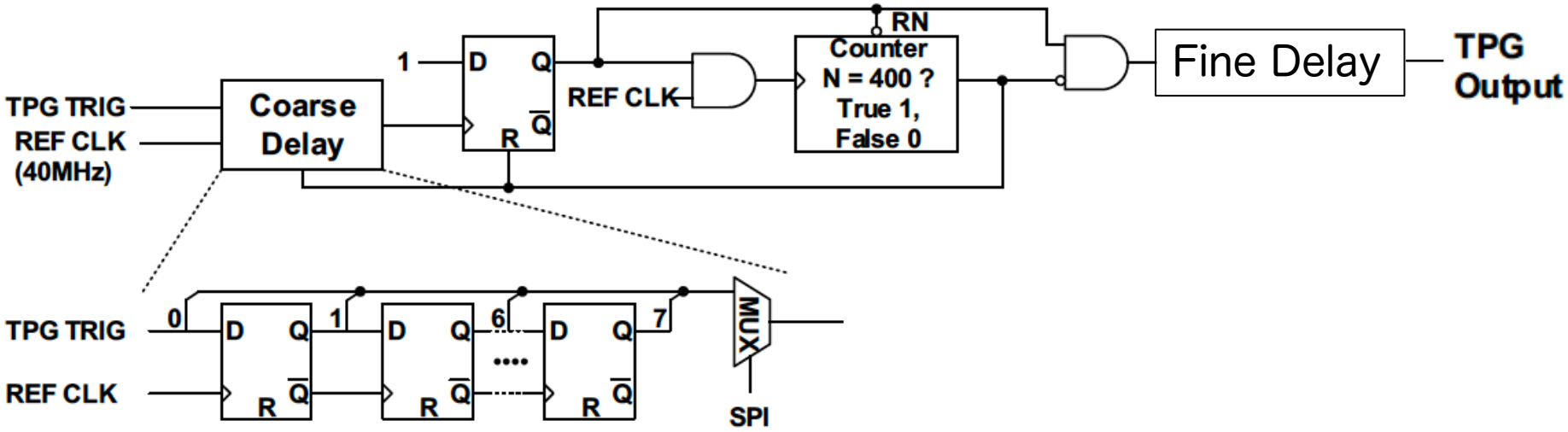


The functions of BCID circuit have been confirmed.

Test Pulse Generator (TPG)



Test Pulse Generator (TPG)



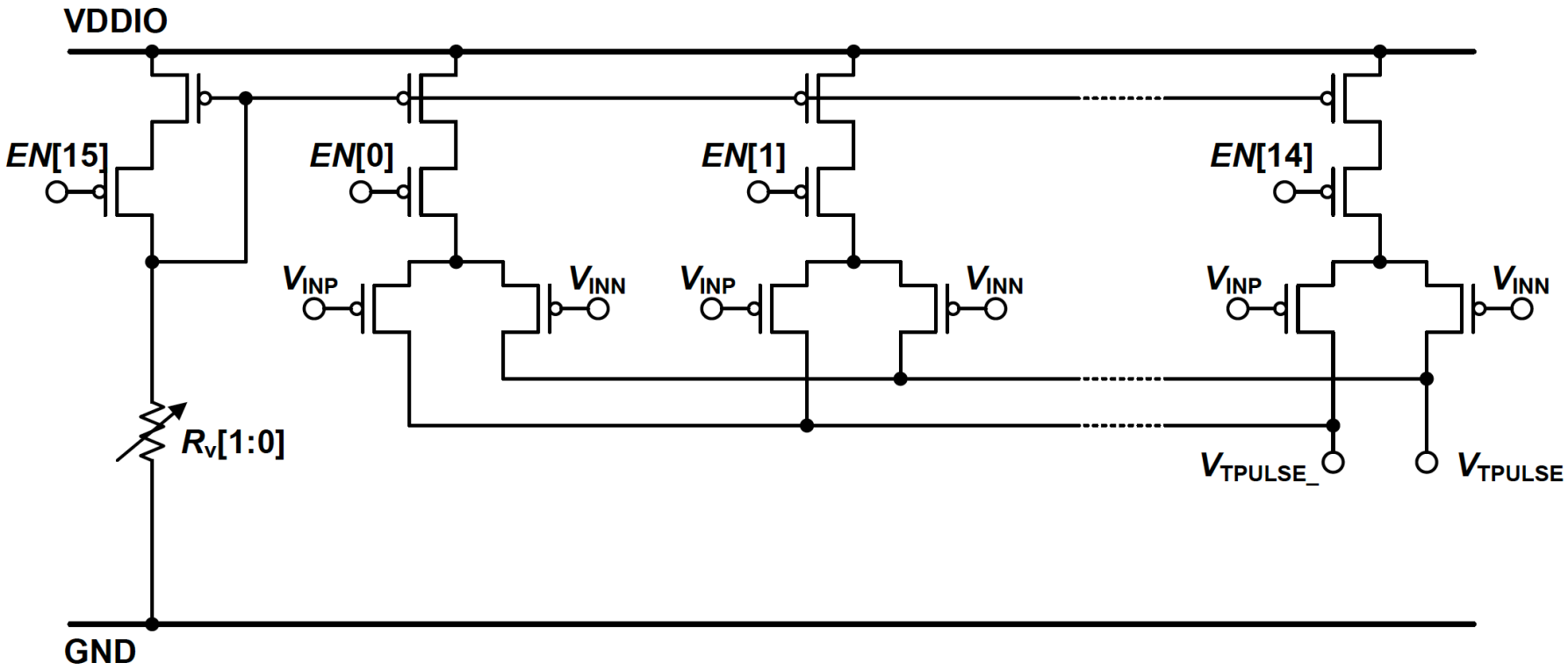
- TPG generates the pulse with coarse delay (0-7 CLK).
- The pulse is set via SPI in a range from 25 ns to 102.4 µs.
- TPG output delay time is controlled by another fine delay (0-40 ns, < 1 ns resolution).

TPG Driver

Drivability of TPG driver can be controlled by

- Changing the number of current sources (EN[0-14])
- Changing the bias current using variable resistor.

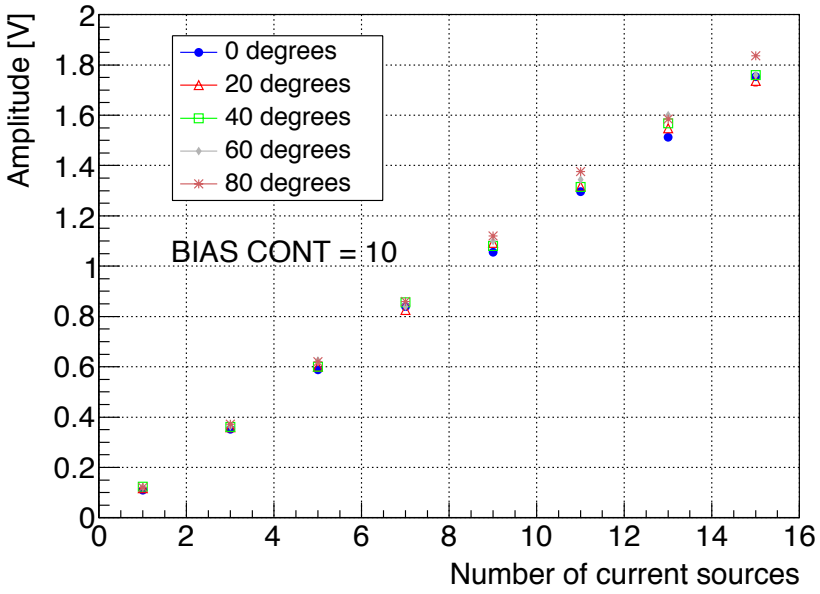
Load condition in measurements: 100 Ω/20 pF



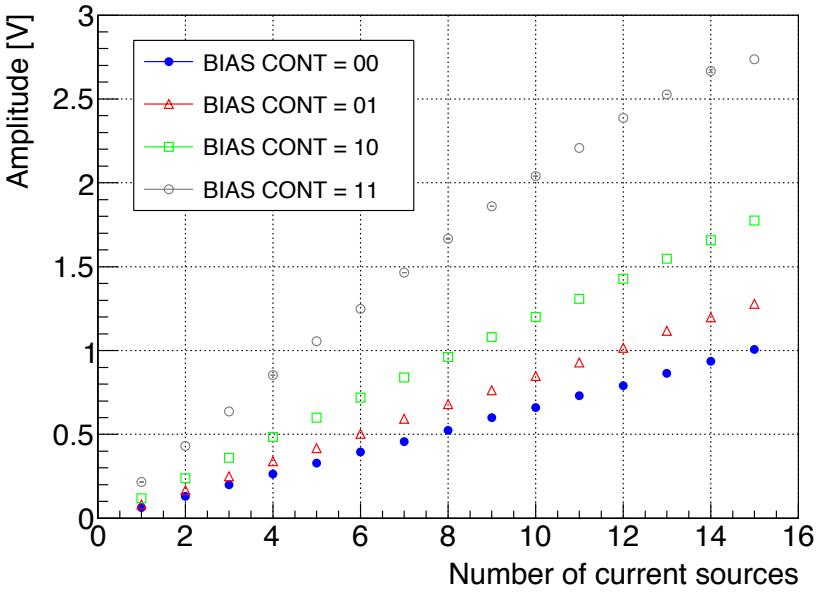
TPG Driver Test Results

The amplitude was measured depending on temperature and VDD.

・Dependence on temperature



・Dependence on VDD



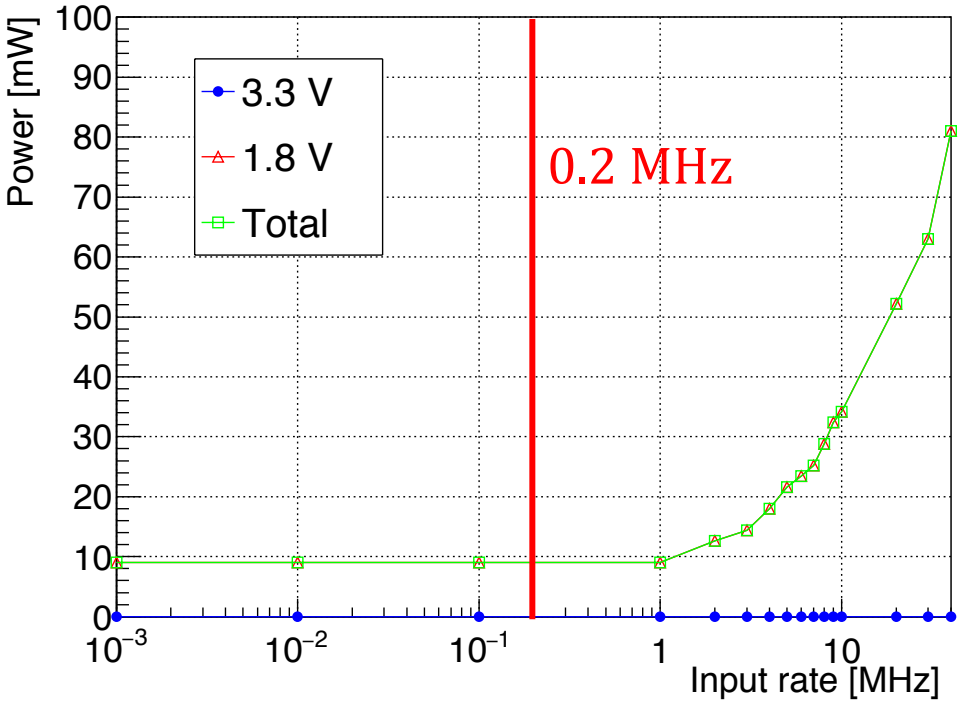
The amplitude used for daily calibration in Run 1 and Run 2 is ～300 mV.

A similar value is assumed for Run 4 and the beyond.

The dependence on VDD is safely small for the daily calibration.

Power Consumption

- 10 pF load capacitance at LVCMOS outputs
- Power consumption of TPG driver is not included.

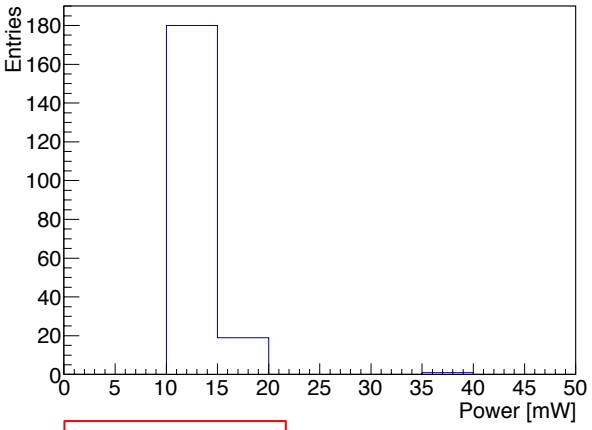


- The power consumption is ~ 10 mW under an expected hit rate of ~0.2 MHz per channel at a luminosity of 7.5 ± 10^{34} $cm^{-2}s^{-1}$.
- Note that the chip of the current system consumes ~130 mW.

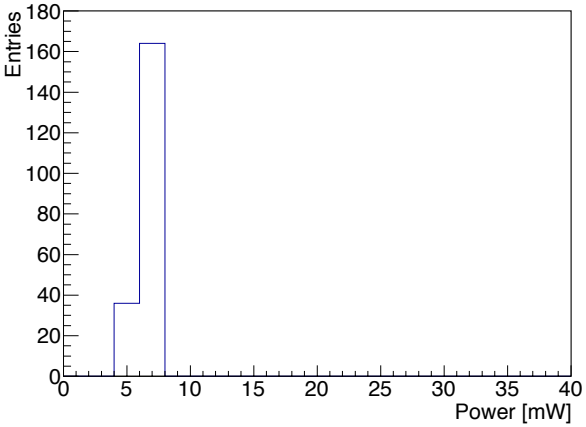
Yield

10 kHz

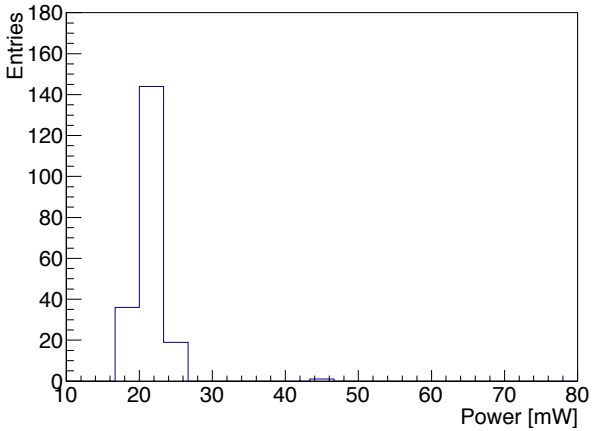
3.3 V



1.8 V

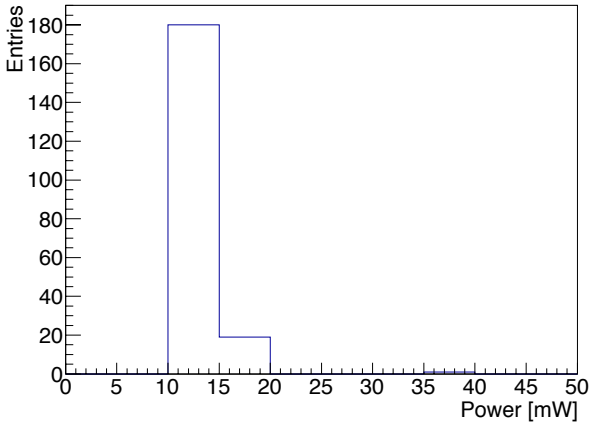


Total

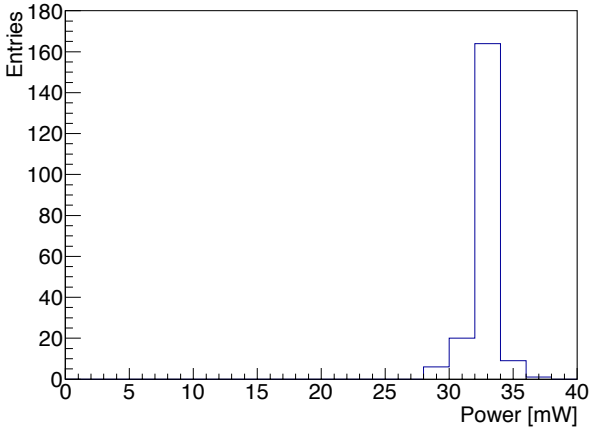


10 MHz

3.3 V



1.8 V



Total