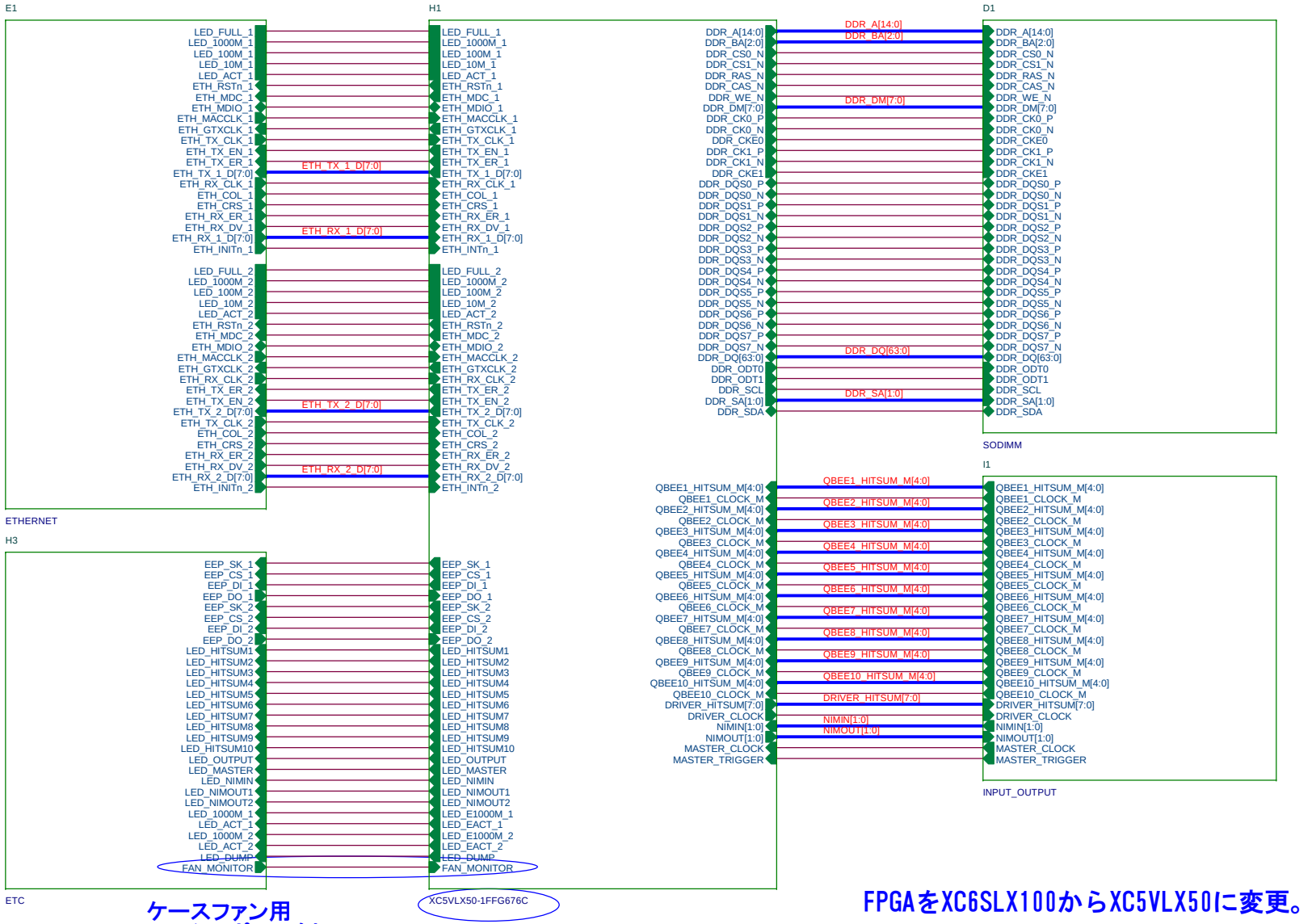
E1
LED_FULL_1
LED_1000M_1
LED_100M_1
LED_10M_1
LED_ACT_1
ETH_RSTn_1
ETH_MDC_1
ETH_MDIO_1
ETH_MACCLK_1
ETH_GTXCLK_1
ETH_TX_CLK_1
ETH_TX_EN_1
ETH_TX_ER_1
ETH_TX_1_D[7:0]
ETH_RX_CLK_1
ETH_COL_1
ETH_CRS_1
ETH_RX_ER_1
ETH_RX_DV_1
ETH_RX_1_D[7:0]
ETH_INITn_1
LED_FULL_2
LED_1000M_2
LED_100M_2
LED_10M_2
LED_ACT_2
ETH_RSTn_2
ETH_MDC_2
ETH_MDIO_2
ETH_MACCLK_2
ETH_GTXCLK_2
ETH_RX_CLK_2
ETH_TX_ER_2
ETH_TX_EN_2
ETH_TX_2_D[7:0]
ETH_TX_CLK_2
ETH_COL_2
ETH_CRS_2
ETH_RX_ER_2
ETH_RX_DV_2
ETH_RX_2_D[7:0]
ETH_INITn_2
ETHERNET
H3
EEP_SK_1
EEP_CS_1
EEP_DI_1
EEP_DO_1
EEP_SK_2
EEP_CS_2
EEP_DI_2
EEP_DO_2
LED_HITSUM1
LED_HITSUM2
LED_HITSUM3
LED_HITSUM4
LED_HITSUM5
LED_HITSUM6
LED_HITSUM7
LED_HITSUM8
LED_HITSUM9
LED_HITSUM10
LED_OUTPUT
LED_MASTER
LED_NIMIN
LED_NIMOUT1
LED_NIMOUT2
LED_1000M_1
LED_ACT_1
LED_1000M_2
LED_ACT_2
LED_DUMP
FAN_MONITOR
ETC
ケースファン用
モニターポート追加
H1
LED_E1000M_1
LED_EACT_1
LED_E1000M_2
LED_EACT_2
XC5VLX50-1FFG676C
POWER
POWER
DDR_A[14:0]
DDR_BA[2:0]
DDR_CS0_N
DDR_CS1_N
DDR_RAS_N
DDR_CAS_N
DDR_WE_N
DDR_DM[7:0]
DDR_CK0_P
DDR_CK0_N
DDR_CKE0
DDR_CK1_P
DDR_CK1_N
DDR_CKE1
DDR_DQS0_P
DDR_DQS0_N
DDR_DQS1_P
DDR_DQS1_N
DDR_DQS2_P
DDR_DQS2_N
DDR_DQS3_P
DDR_DQS3_N
DDR_DQS4_P
DDR_DQS4_N
DDR_DQS5_P
DDR_DQS5_N
DDR_DQS6_P
DDR_DQS6_N
DDR_DQS7_P
DDR_DQS7_N
DDR_DQ[63:0]
DDR_ODT0
DDR_ODT1
DDR_SCL
DDR_SA[1:0]
DDR_SDA
D1
SODIMM
I1
QBEE1_HITSUM_M[4:0]
QBEE1_CLOCK_M
QBEE2_HITSUM_M[4:0]
QBEE2_CLOCK_M
QBEE3_HITSUM_M[4:0]
QBEE3_CLOCK_M
QBEE4_HITSUM_M[4:0]
QBEE4_CLOCK_M
QBEE5_HITSUM_M[4:0]
QBEE5_CLOCK_M
QBEE6_HITSUM_M[4:0]
QBEE6_CLOCK_M
QBEE7_HITSUM_M[4:0]
QBEE7_CLOCK_M
QBEE8_HITSUM_M[4:0]
QBEE8_CLOCK_M
QBEE9_HITSUM_M[4:0]
QBEE9_CLOCK_M
QBEE10_HITSUM_M[4:0]
QBEE10_CLOCK_M
DRIVER_HITSUM[7:0]
DRIVER_CLOCK
NIMIN[1:0]
NIMOUT[1:0]
MASTER_CLOCK
MASTER_TRIGGER
INPUT_OUTPUT
FPGAをXC6SLX100からXC5VLX50に変更。
Title
SN_MONITOR
Size
A3
Document Number
<Doc>
Rev
5
Date:
Sunday, February 03, 2013
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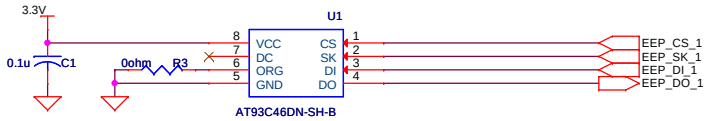
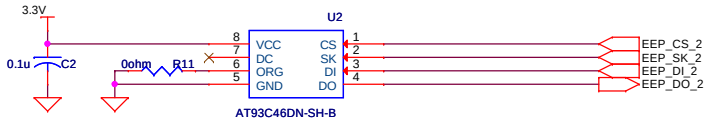
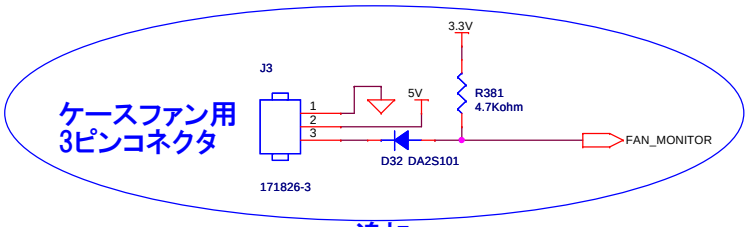
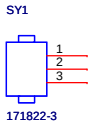
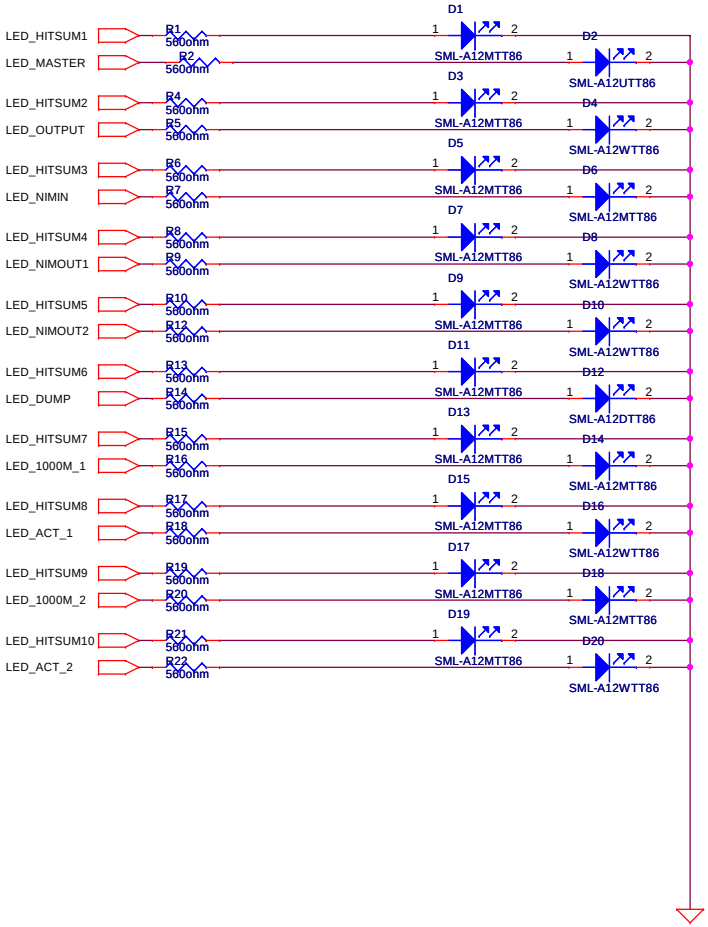


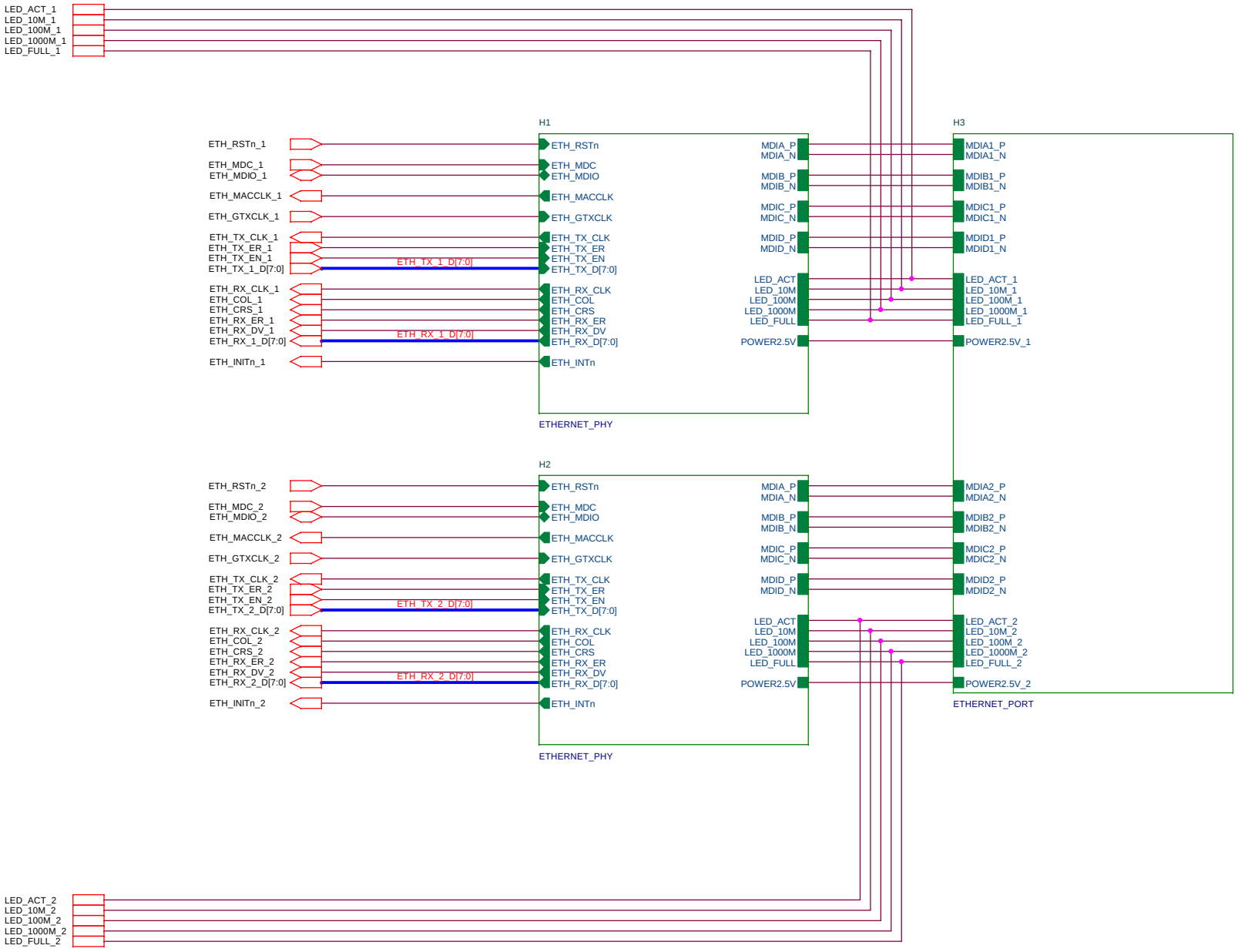




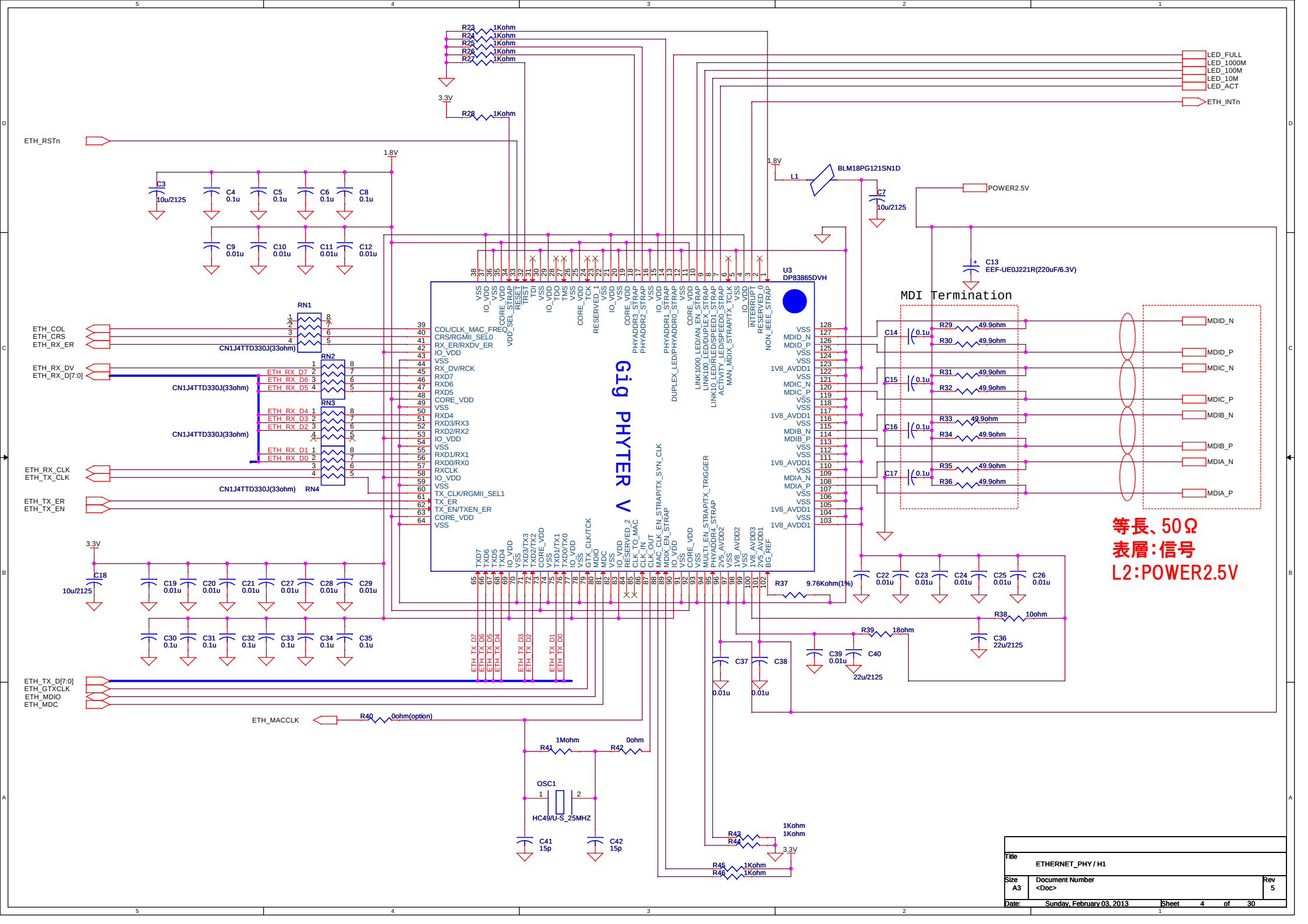




Title: ETC		
Size: A3	Document Number: <Doc>	Rev: 5
Date: Sunday, February 03, 2013	Sheet 2 of 30	



Title	ETHERNET	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 3 of 30	


U3
DP83865DVH
Gig PHYTER V
MDI Termination
等長、50Ω
表層:信号
L2:POWER2.5V
ETH_RSTn
ETH_INTn
LED_FULL
LED_1000M
LED_100M
LED_10M
LED_ACT
POWER2.5V
BLM18PG121SN1D
ETH_COL
ETH_CRS
ETH_RX_ER
ETH_RX_DV
ETH_RX_D[7:0]
ETH_RX_CLK
ETH_TX_CLK
ETH_TX_ER
ETH_TX_EN
ETH_TX_D[7:0]
ETH_GTXCLK
ETH_MDIO
ETH_MDC
ETH_MACCLK
MDID_N
MDID_P
MDIC_N
MDIC_P
MDIB_N
MDIB_P
MDIA_N
MDIA_P
OSC1
HC49/U-S_25MHZ
CN1J4TTD330J(33ohm)
Title
ETHERNET_PHY / H1
Size
A3
Document Number
<Doc>
Rev
5
Date:
Sunday, February 03, 2013
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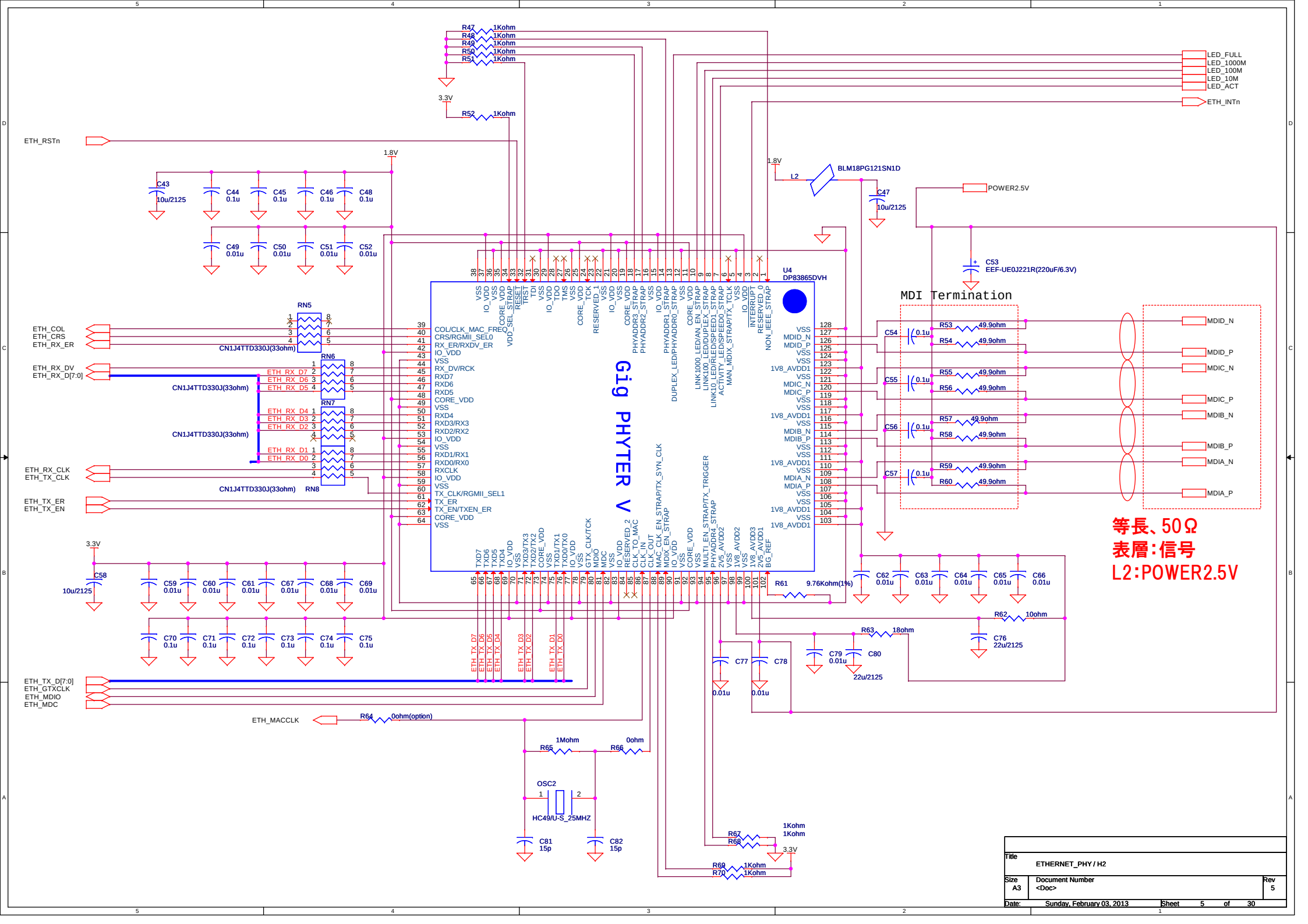
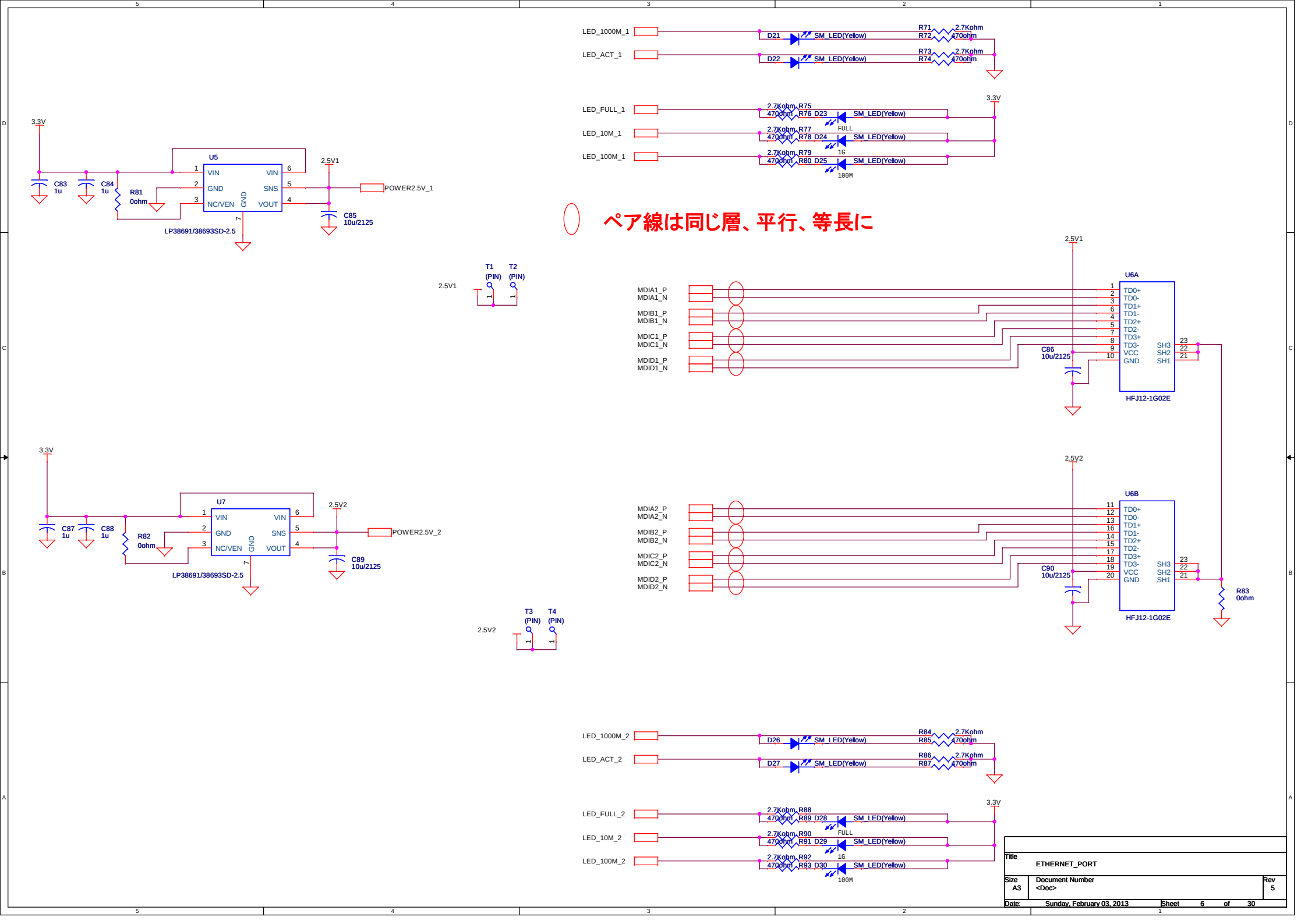
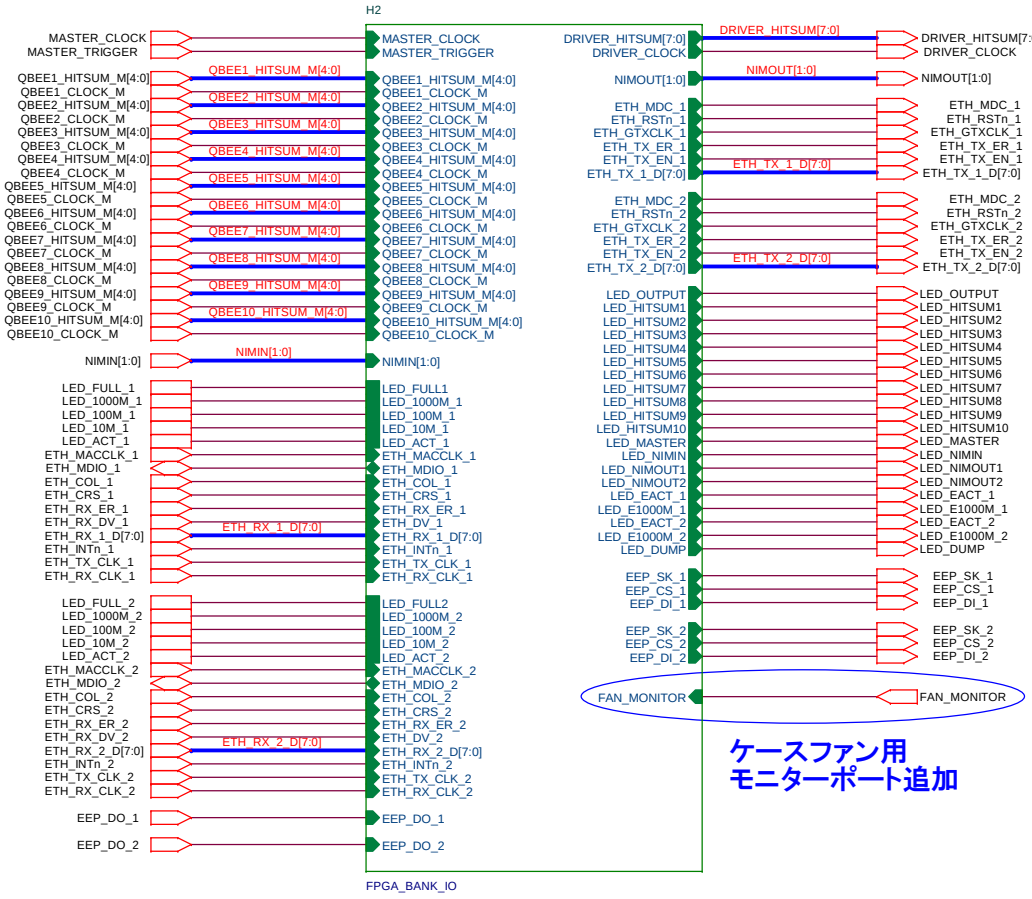
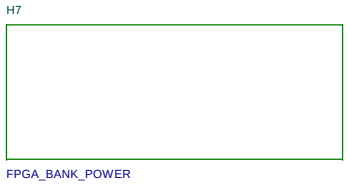
30

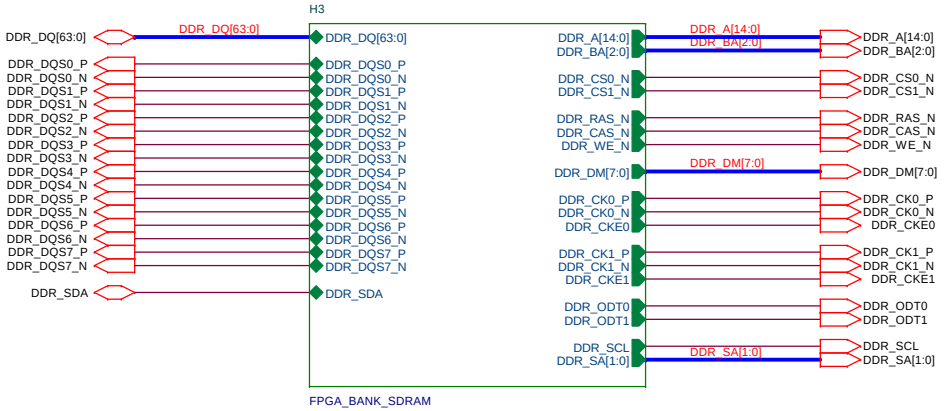

R47 1Kohm
R48 1Kohm
R49 1Kohm
R50 1Kohm
R51 1Kohm
3.3V
R52 1Kohm
LED_FULL
LED_1000M
LED_100M
LED_10M
LED_ACT
ETH_INTn
ETH_RSTn
1.8V
C43 10u/2125
C44 0.1u
C45 0.1u
C46 0.1u
C48 0.1u
C49 0.01u
C50 0.01u
C51 0.01u
C52 0.01u
L2 BLM18PG121SN1D
C47 10u/2125
POWER2.5V
C53 EEF-UE0J221R(220uF/6.3V)
U4
DP83865DVH
Gig PHYTER V
MDI Termination
RN5
RN6
RN7
RN8
CN1J4TTD330J(33ohm)
ETH_COL
ETH_CRS
ETH_RX_ER
ETH_RX_DV
ETH_RX_D[7:0]
ETH_RX_CLK
ETH_TX_CLK
ETH_TX_ER
ETH_TX_EN
ETH_TX_D[7:0]
ETH_GTXCLK
ETH_MDIO
ETH_MDC
ETH_MACCLK
R64 0ohm(option)
R65 1Mohm
R66 0ohm
OSC2
HC49/U-S_25MHZ
C81 15p
C82 15p
R67 1Kohm
R68 1Kohm
R69 1Kohm
R70 1Kohm
R53 49.9ohm
R54 49.9ohm
R55 49.9ohm
R56 49.9ohm
R57 49.9ohm
R58 49.9ohm
R59 49.9ohm
R60 49.9ohm
C54 0.1u
C55 0.1u
C56 0.1u
C57 0.1u
MDID_N
MDID_P
MDIC_N
MDIC_P
MDIB_N
MDIB_P
MDIA_N
MDIA_P
R61 9.76Kohm(1%)
C62 0.01u
C63 0.01u
C64 0.01u
C65 0.01u
C66 0.01u
R62 10ohm
R63 18ohm
C76 22u/2125
C77 0.01u
C78 0.01u
C79 0.01u
C80 22u/2125
C58 10u/2125
C59 0.01u
C60 0.01u
C61 0.01u
C67 0.01u
C68 0.01u
C69 0.01u
C70 0.1u
C71 0.1u
C72 0.1u
C73 0.1u
C74 0.1u
C75 0.1u
等長、50Ω
表層:信号
L2:POWER2.5V
Title
ETHERNET_PHY / H2
Size A3
Document Number <Doc>
Rev 5
Date: Sunday, February 03, 2013
Sheet 5 of 30

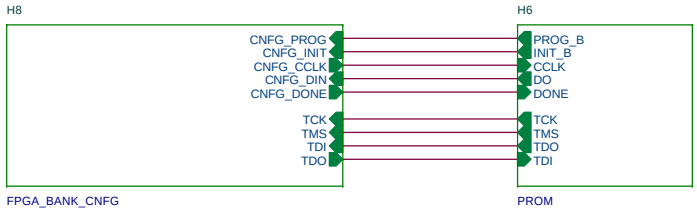


Title	ETHERNET_PORT	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 6 of 30	



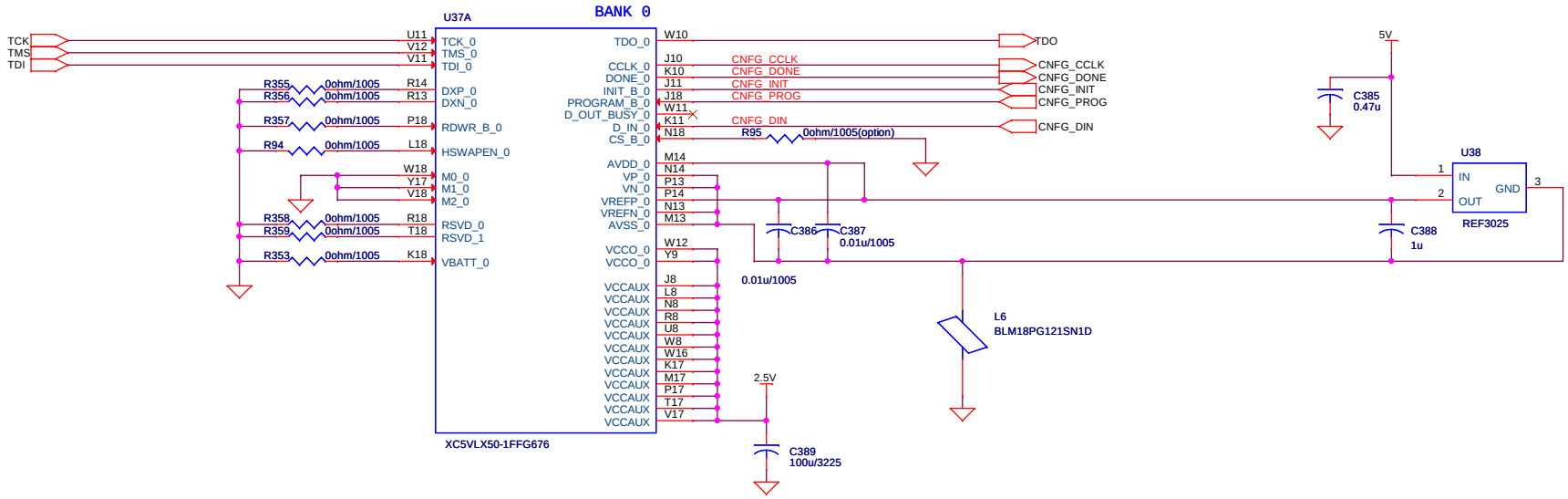






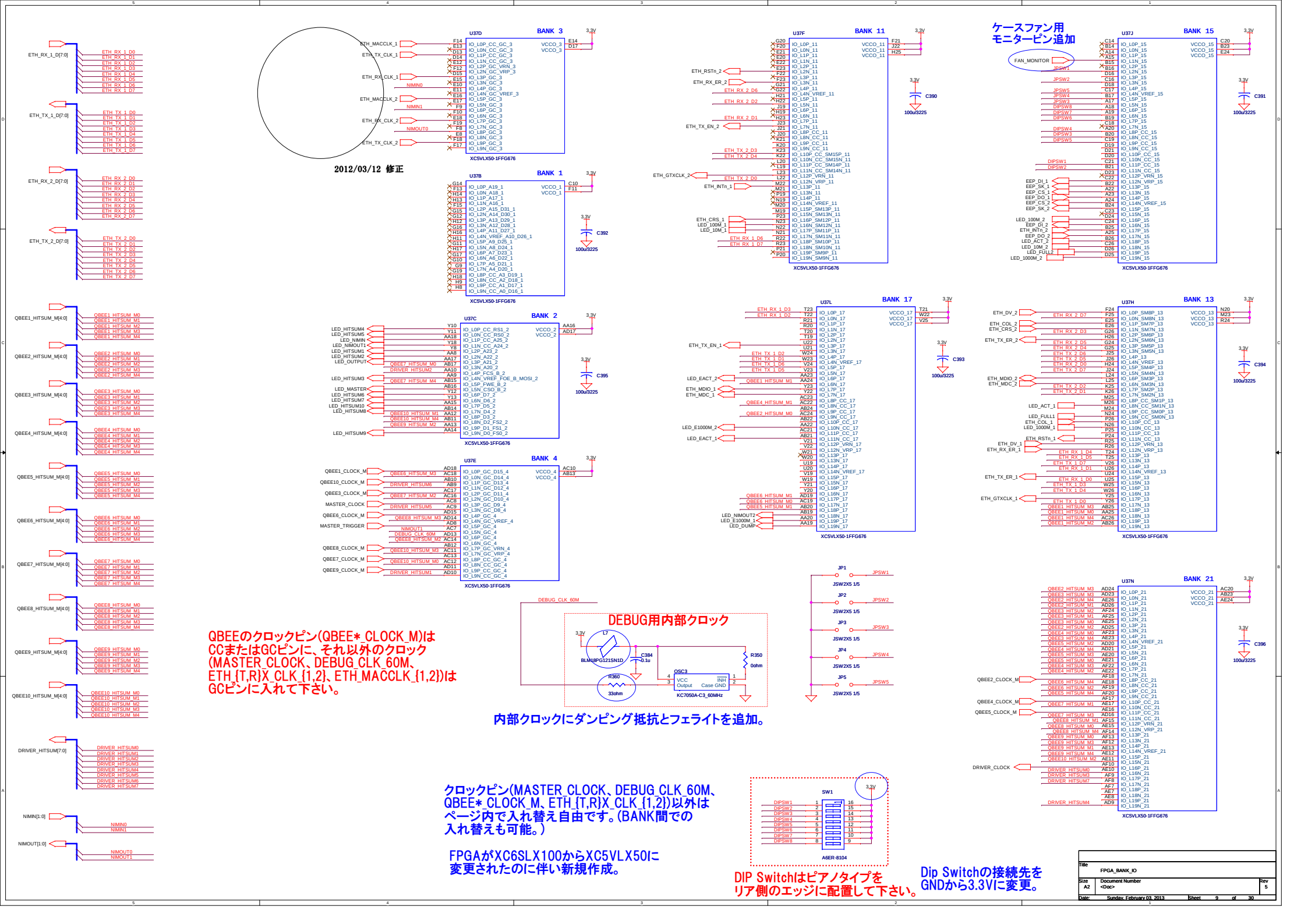
FPGAがXC6SLX100からXC5VLX50に
変更されたのに伴い修正。

Title: FPGA		
Size: A3	Document Number: <Doc>	Rev: 5
Date: Sunday, February 03, 2013	Sheet 7 of 30	



FPGAがXC6SLX100からXC5VLX50に
変更されたのに伴い新規作成。

Title	FPGA_BANK_CNFG	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 8 of 30	


ETH_RX_1_D[7:0]
ETH_RX_1_D0
ETH_RX_1_D1
ETH_RX_1_D2
ETH_RX_1_D3
ETH_RX_1_D4
ETH_RX_1_D5
ETH_RX_1_D6
ETH_RX_1_D7
ETH_TX_1_D[7:0]
ETH_TX_1_D0
ETH_TX_1_D1
ETH_TX_1_D2
ETH_TX_1_D3
ETH_TX_1_D4
ETH_TX_1_D5
ETH_TX_1_D6
ETH_TX_1_D7
ETH_RX_2_D[7:0]
ETH_RX_2_D0
ETH_RX_2_D1
ETH_RX_2_D2
ETH_RX_2_D3
ETH_RX_2_D4
ETH_RX_2_D5
ETH_RX_2_D6
ETH_RX_2_D7
ETH_TX_2_D[7:0]
ETH_TX_2_D0
ETH_TX_2_D1
ETH_TX_2_D2
ETH_TX_2_D3
ETH_TX_2_D4
ETH_TX_2_D5
ETH_TX_2_D6
ETH_TX_2_D7
QBEE1_HITSUM_M[4:0]
QBEE1_HITSUM_M0
QBEE1_HITSUM_M1
QBEE1_HITSUM_M2
QBEE1_HITSUM_M3
QBEE1_HITSUM_M4
QBEE2_HITSUM_M[4:0]
QBEE2_HITSUM_M0
QBEE2_HITSUM_M1
QBEE2_HITSUM_M2
QBEE2_HITSUM_M3
QBEE2_HITSUM_M4
QBEE3_HITSUM_M[4:0]
QBEE3_HITSUM_M0
QBEE3_HITSUM_M1
QBEE3_HITSUM_M2
QBEE3_HITSUM_M3
QBEE3_HITSUM_M4
QBEE4_HITSUM_M[4:0]
QBEE4_HITSUM_M0
QBEE4_HITSUM_M1
QBEE4_HITSUM_M2
QBEE4_HITSUM_M3
QBEE4_HITSUM_M4
QBEE5_HITSUM_M[4:0]
QBEE5_HITSUM_M0
QBEE5_HITSUM_M1
QBEE5_HITSUM_M2
QBEE5_HITSUM_M3
QBEE5_HITSUM_M4
QBEE6_HITSUM_M[4:0]
QBEE6_HITSUM_M0
QBEE6_HITSUM_M1
QBEE6_HITSUM_M2
QBEE6_HITSUM_M3
QBEE6_HITSUM_M4
QBEE7_HITSUM_M[4:0]
QBEE7_HITSUM_M0
QBEE7_HITSUM_M1
QBEE7_HITSUM_M2
QBEE7_HITSUM_M3
QBEE7_HITSUM_M4
QBEE8_HITSUM_M[4:0]
QBEE8_HITSUM_M0
QBEE8_HITSUM_M1
QBEE8_HITSUM_M2
QBEE8_HITSUM_M3
QBEE8_HITSUM_M4
QBEE9_HITSUM_M[4:0]
QBEE9_HITSUM_M0
QBEE9_HITSUM_M1
QBEE9_HITSUM_M2
QBEE9_HITSUM_M3
QBEE9_HITSUM_M4
QBEE10_HITSUM_M[4:0]
QBEE10_HITSUM_M0
QBEE10_HITSUM_M1
QBEE10_HITSUM_M2
QBEE10_HITSUM_M3
QBEE10_HITSUM_M4
DRIVER_HITSUM[7:0]
DRIVER_HITSUM0
DRIVER_HITSUM1
DRIVER_HITSUM2
DRIVER_HITSUM3
DRIVER_HITSUM4
DRIVER_HITSUM5
DRIVER_HITSUM6
DRIVER_HITSUM7
NIMIN[1:0]
NIMIN0
NIMIN1
NIMOUT[1:0]
NIMOUT0
NIMOUT1
2012/03/12 修正
U37D
BANK 3
XC5VLX50-1FFG676
ETH_MACCLK_1
ETH_TX_CLK_1
ETH_RX_CLK_1
NIMIN0
ETH_MACCLK_2
NIMIN1
ETH_RX_CLK_2
NIMOUT0
ETH_TX_CLK_2
U37B
BANK 1
XC5VLX50-1FFG676
C392
100u/3225
U37C
BANK 2
XC5VLX50-1FFG676
C395
100u/3225
LED_HITSUM4
LED_HITSUM5
LED_NIMIN
LED_NIMOUT1
LED_HITSUM1
LED_HITSUM2
LED_OUTPUT
LED_HITSUM3
LED_MASTER
LED_HITSUM6
LED_HITSUM7
LED_HITSUM10
LED_HITSUM8
LED_HITSUM9
U37E
BANK 4
XC5VLX50-1FFG676
QBEE1_CLOCK_M
QBEE10_CLOCK_M
QBEE3_CLOCK_M
MASTER_CLOCK
QBEE6_CLOCK_M
MASTER_TRIGGER
QBEE8_CLOCK_M
QBEE7_CLOCK_M
QBEE9_CLOCK_M
U37F
BANK 11
XC5VLX50-1FFG676
C390
100u/3225
ETH_RSTn_2
ETH_RX_ER_2
ETH_TX_EN_2
ETH_GTXCLK_2
ETH_INTn_1
ETH_CRS_1
LED_100M_1
LED_10M_1
U37L
BANK 17
XC5VLX50-1FFG676
C393
100u/3225
ETH_TX_EN_1
LED_EACT_2
ETH_MDIO_1
ETH_MDC_1
LED_E1000M_2
LED_EACT_1
LED_NIMOUT2
LED_E1000M_1
LED_DUMP
ケースファン用
モニターピン追加
U37J
BANK 15
XC5VLX50-1FFG676
C391
100u/3225
FAN_MONITOR
JPSW1
JPSW2
JPSW5
JPSW4
JPSW3
DIPSW8
DIPSW7
DIPSW6
DIPSW4
DIPSW3
DIPSW5
DIPSW1
DIPSW2
EEP_DI_1
EEP_SK_1
EEP_CS_1
EEP_DO_1
EEP_CS_2
EEP_SK_2
LED_100M_2
EEP_DI_2
ETH_INTn_2
EEP_DO_2
LED_ACT_2
LED_10M_2
LED_FULL2
LED_1000M_2
U37H
BANK 13
XC5VLX50-1FFG676
C394
100u/3225
ETH_DV_2
ETH_COL_2
ETH_CRS_2
ETH_TX_ER_2
ETH_MDIO_2
ETH_MDC_2
LED_ACT_1
LED_FULL1
ETH_COL_1
LED_1000M_1
ETH_RSTn_1
ETH_DV_1
ETH_RX_ER_1
ETH_TX_ER_1
ETH_GTXCLK_1
U37N
BANK 21
XC5VLX50-1FFG676
C396
100u/3225
QBEE2_CLOCK_M
QBEE4_CLOCK_M
QBEE5_CLOCK_M
DRIVER_CLOCK
JP1
JP2
JP3
JP4
JP5
JSW2X5 1/5
JPSW1
JPSW2
JPSW3
JPSW4
JPSW5
DEBUG_CLK_60M
DEBUG用内部クロック
L7
BLM18PG121SN1D
C384
0.1u
R350
0ohm
R360
33ohm
OSC3
KC7050A-C3_60MHz
SW1
A6ER-8104
QBEEのクロックピン(QBEE*_CLOCK_M)は
CCまたはGCピンに、それ以外のクロック
(MASTER_CLOCK、DEBUG_CLK_60M、
ETH_{T,R}X_CLK_{1,2}、ETH_MACCLK_{1,2})は
GCピンに入れて下さい。
内部クロックにダンピング抵抗とフェライトを追加。
クロックピン(MASTER_CLOCK、DEBUG_CLK_60M、
QBEE*_CLOCK_M、ETH_{T,R}X_CLK_{1,2})以外は
ページ内で入れ替え自由です。(BANK間での
入れ替えも可能。)
FPGAがXC6SLX100からXC5VLX50に
変更されたのに伴い新規作成。
DIP Switchはピアノタイプを
リア側のエッジに配置して下さい。
Dip Switchの接続先を
GNDから3.3Vに変更。
Title
FPGA_BANK_IO
Size
A2
Document Number
<Doc>
Rev
5
Date:
Sunday, February 03, 2013
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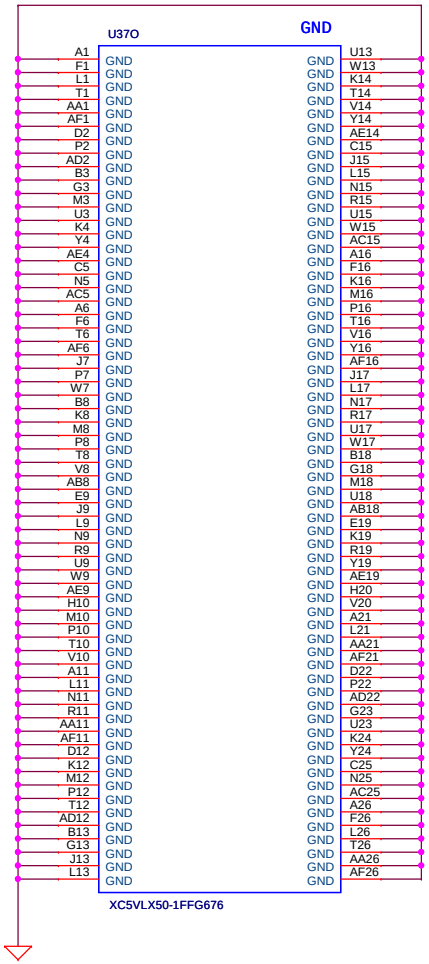
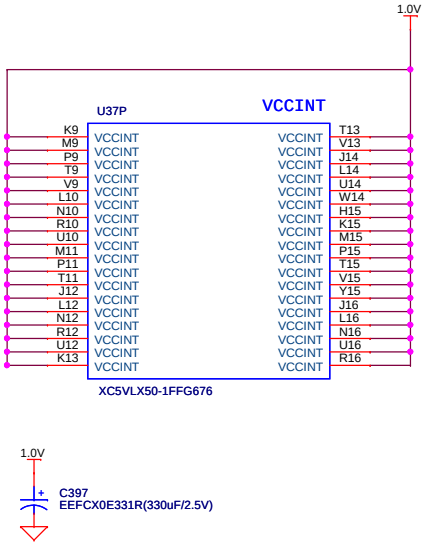
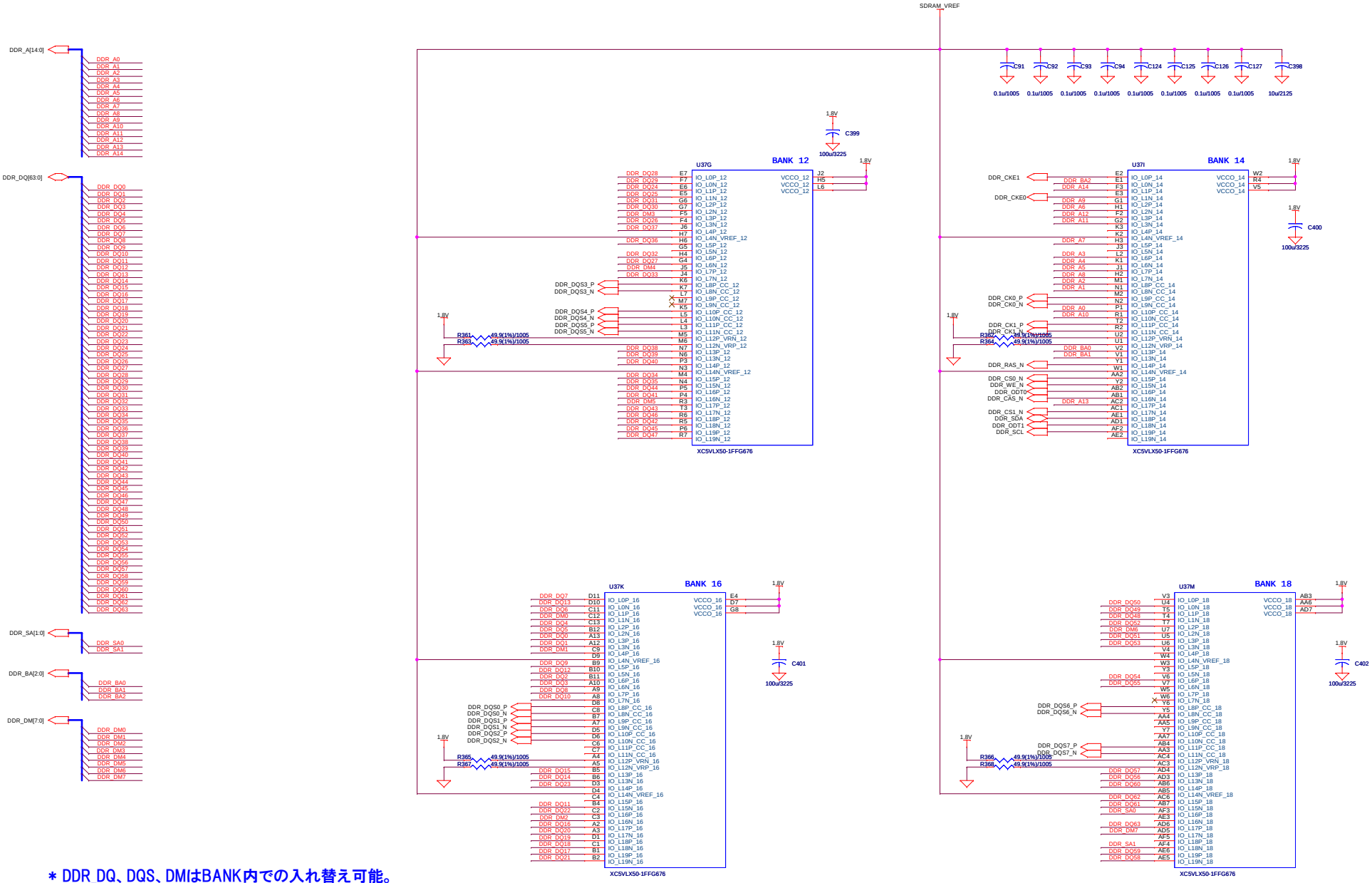




FPGAがXC6SLX100からXC5VLX50に
変更されたのに伴い新規作成。

Title	FPGA_BANK_POWER	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 10 of 30	

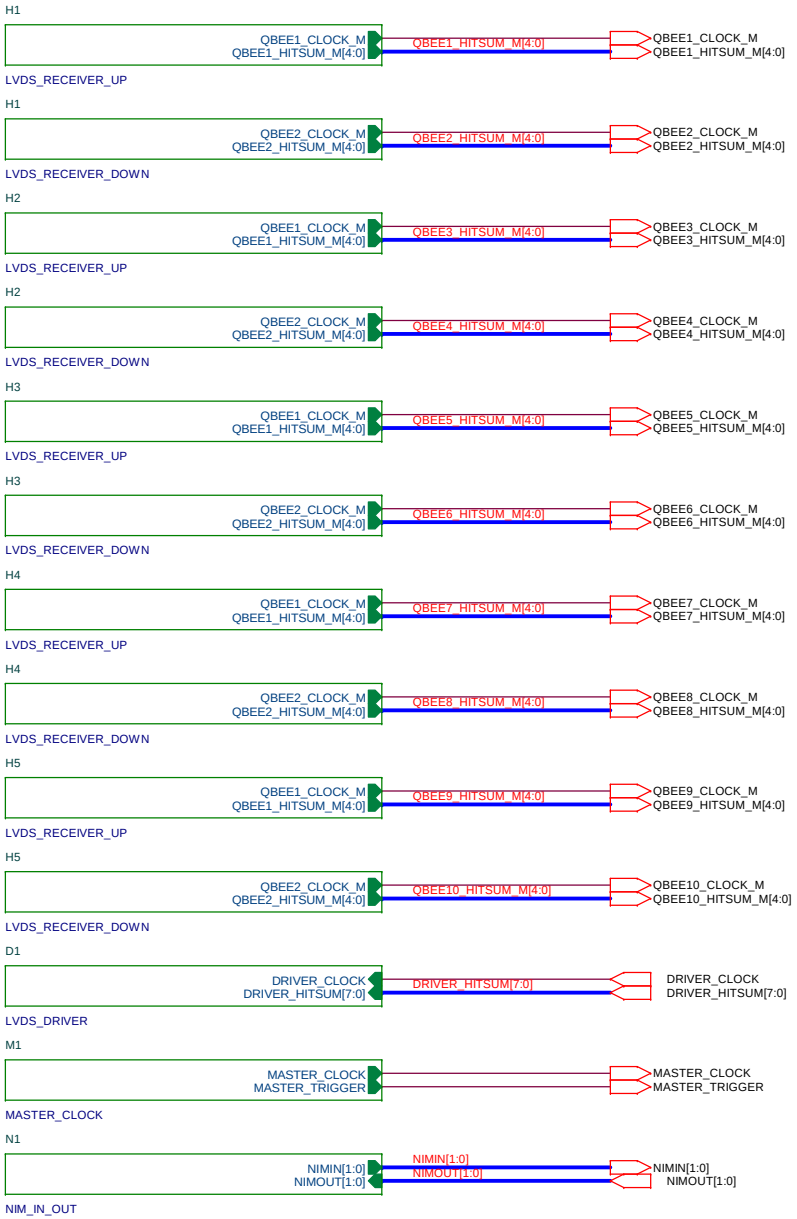


* DDR_DQ、DQS、DMはBANK内での入れ替え可能。
BANK間でこれらのピンを入れ替える場合は、1Byte単位
(8つのDQ、1ペアのDQS、1つのDM)をまとめて入れ替える。
* AddressとControl信号(DDR_A、BA、RAS_N、CAS_N、
WE_N、CS_N、ODT、CK、CKE)は出来れば同じBANKにする。
* DQSとCKはCCピンにのみ入れられる。

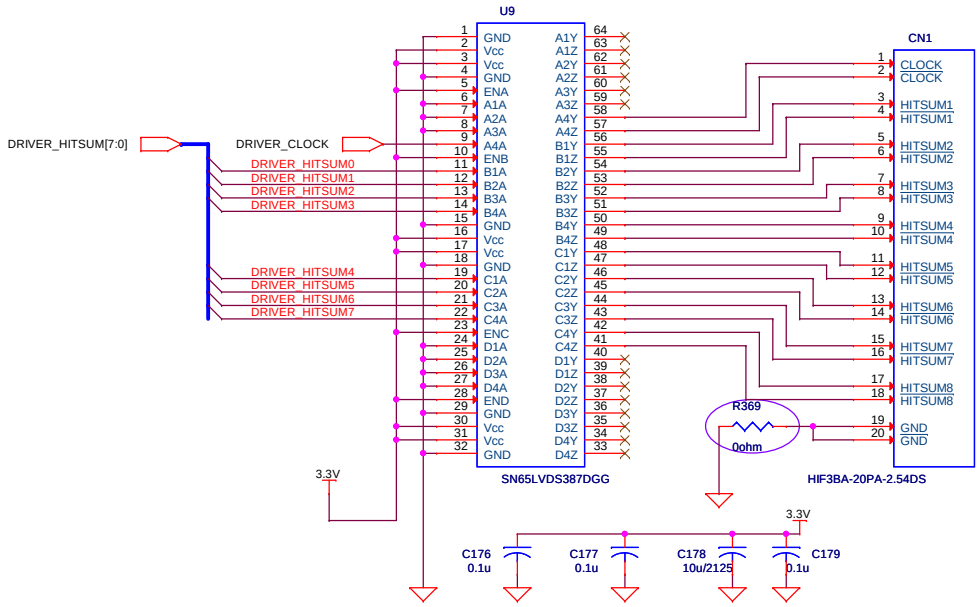
FPGAがXC6SLX100からXC5VLX50に
変更されたのに伴い新規作成。

FPGA <--> SODIMM間の等長配線:
* クロックのペアは+-10mil以内
* 同一Byte内のDQとDQS信号は+-25ps以内
* AddressおよびControl信号と対応するCK信号は+-50ps以内
* DQS信号とCK信号同士は+-100ps以内

Title	FPGA_BANK_SDRAM	
Size A2	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 11 of 30	

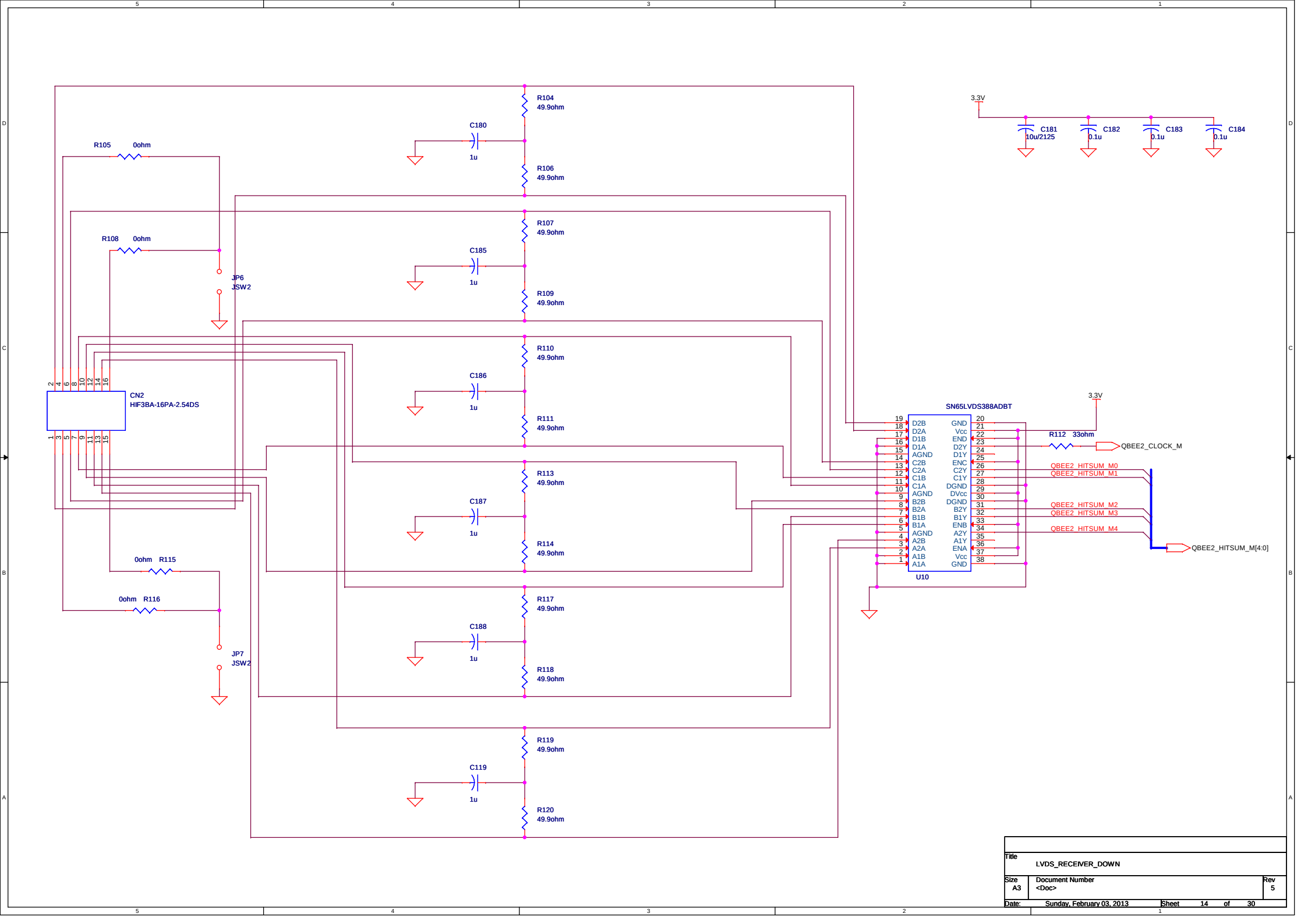


Title	INPUT_OUTPUT	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 12 of 30	

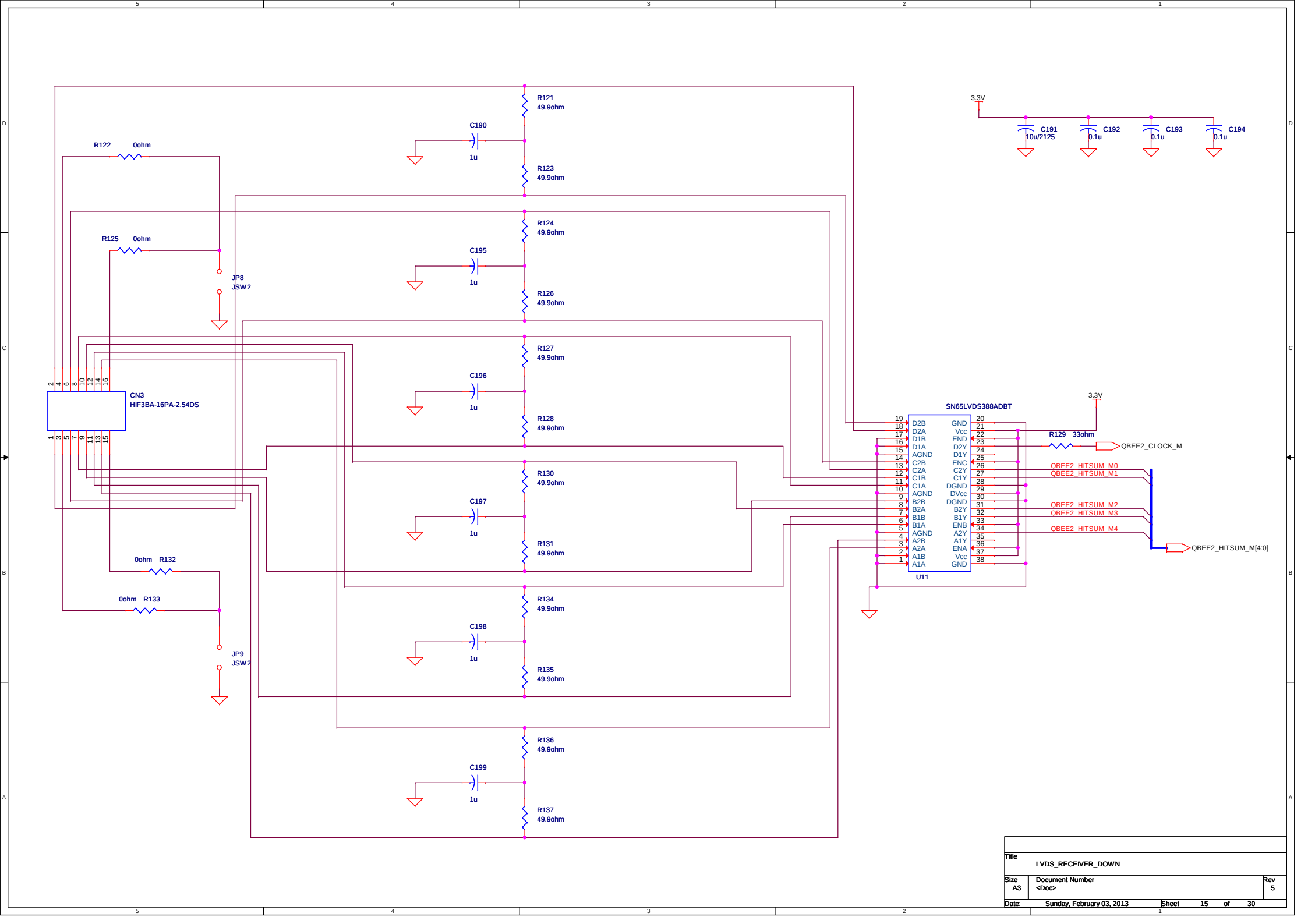


コネクターのGNDの配線に0ohm抵抗を追加。

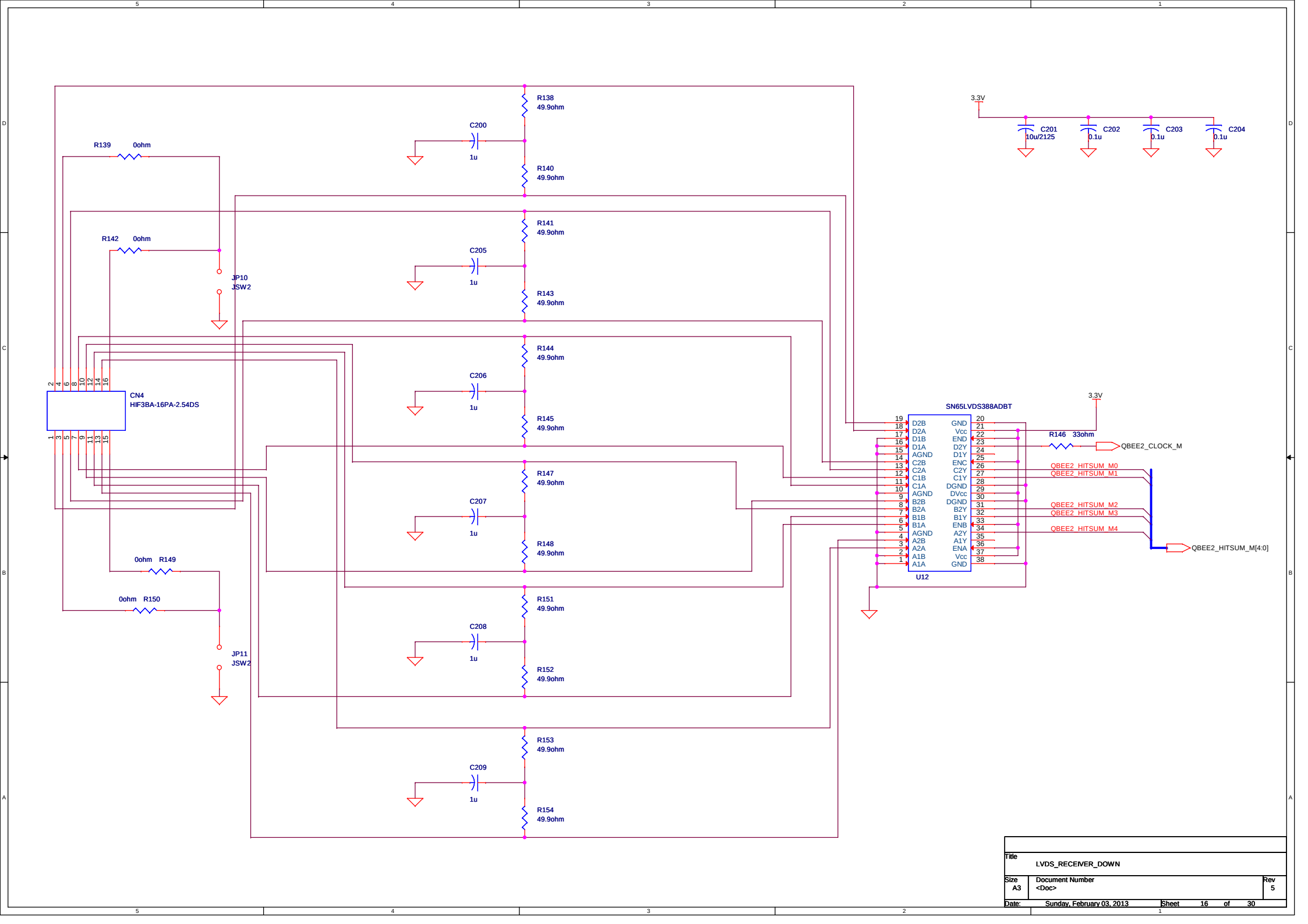
Title	LVDS_DRIVER	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 13 of 30	



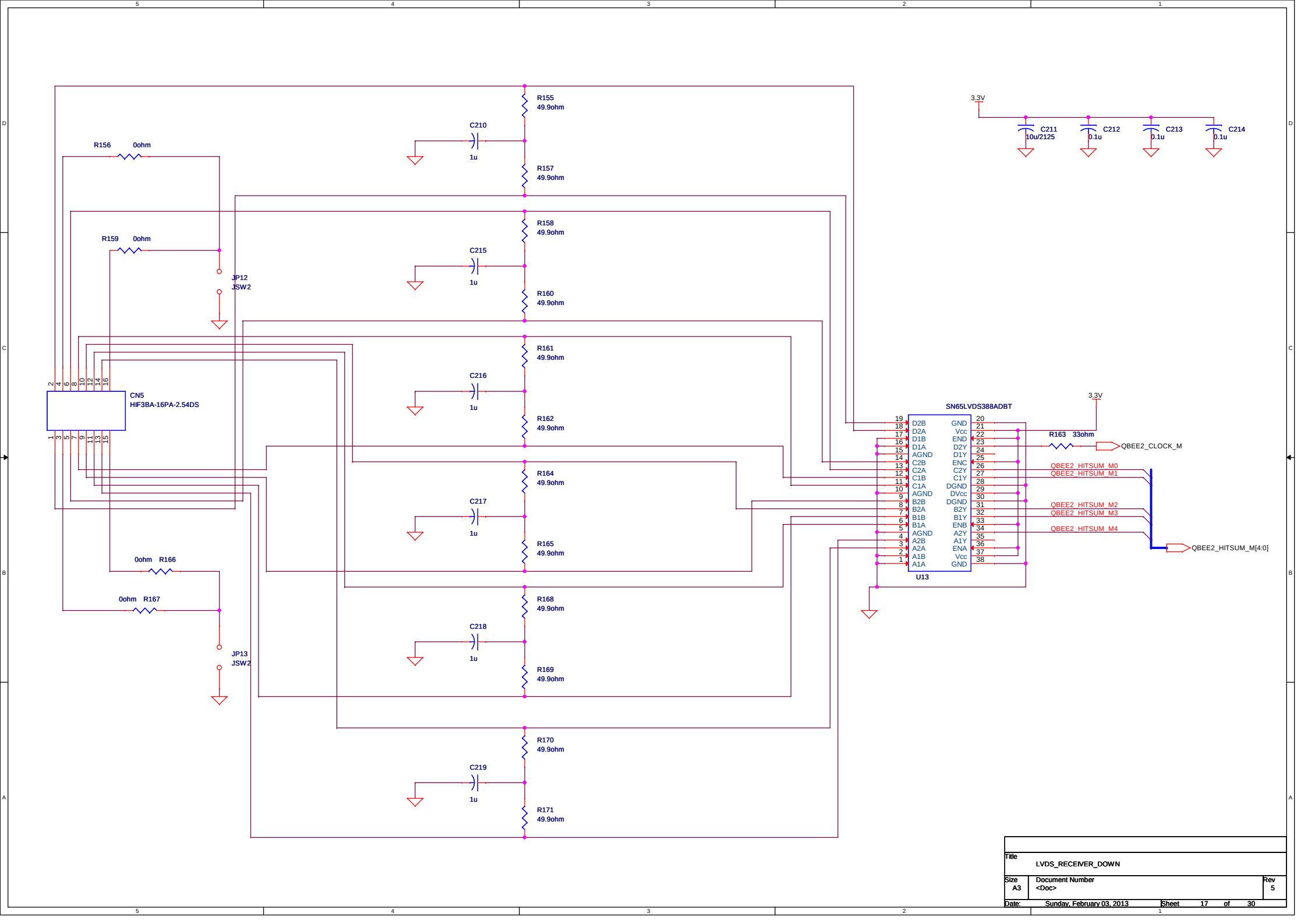
Title	LVDS_RECEIVER_DOWN	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 14 of 30	



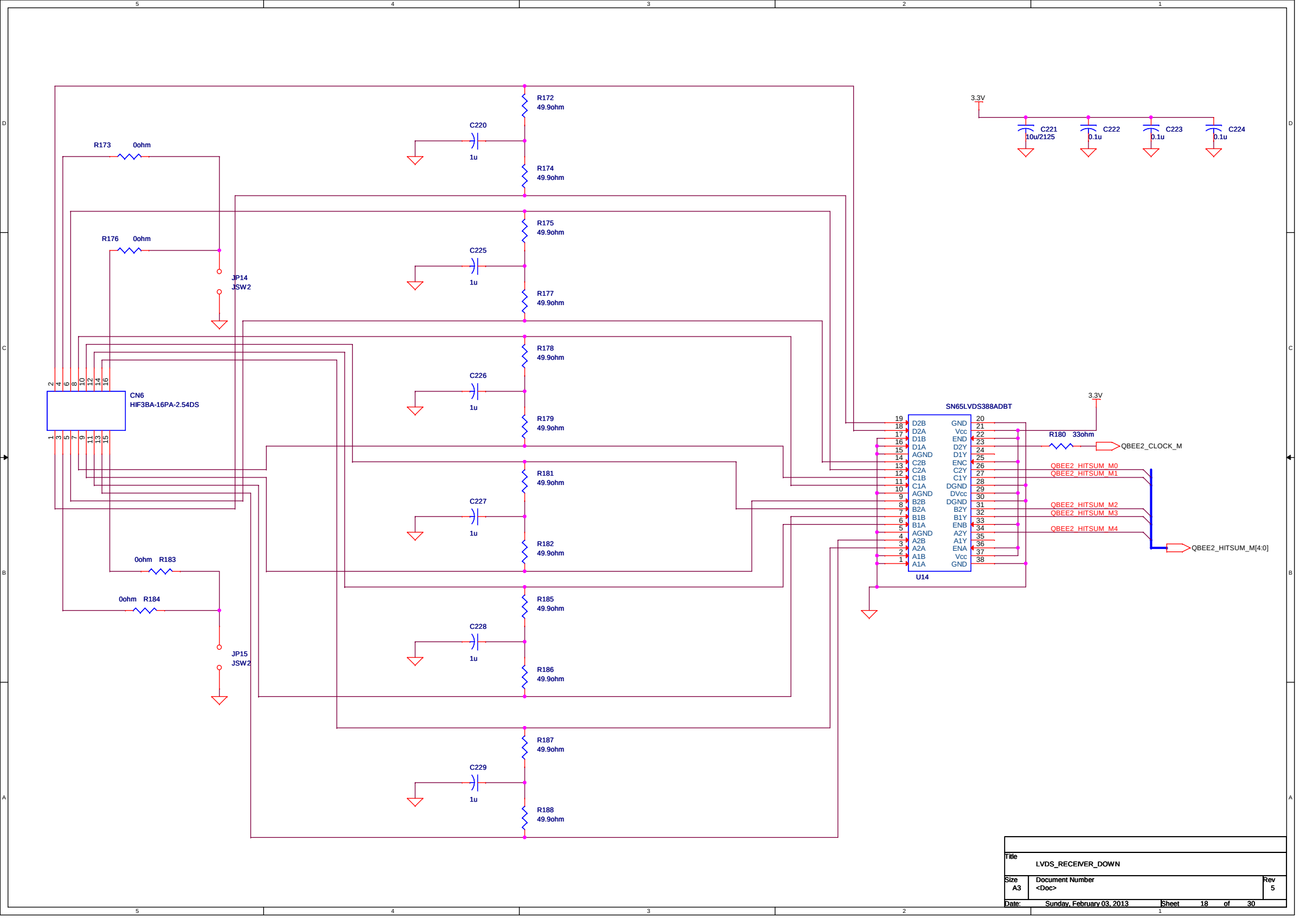
Title	LVDS_RECEIVER_DOWN	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 15 of 30	



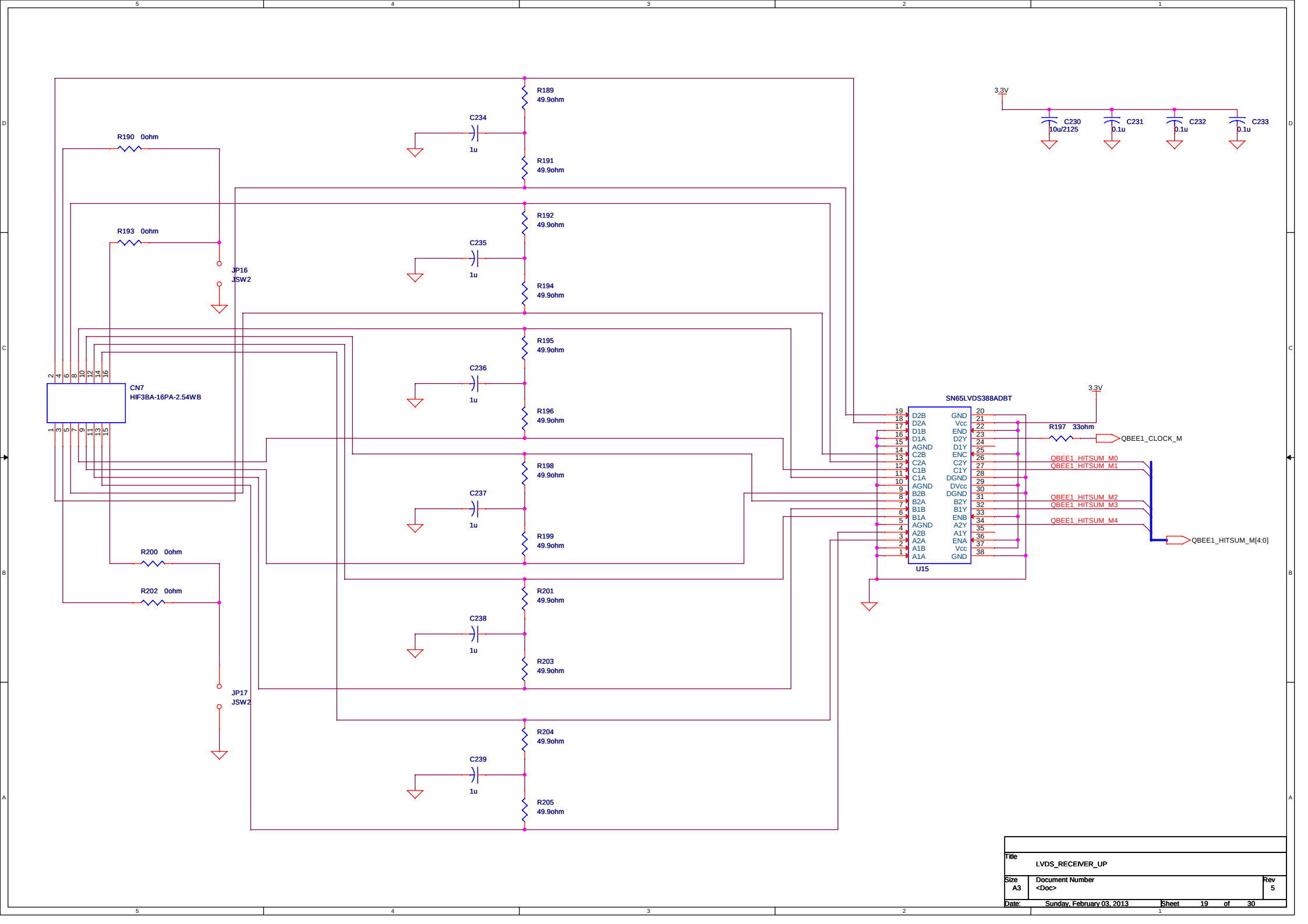
Title	LVDS_RECEIVER_DOWN	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 16 of 30	



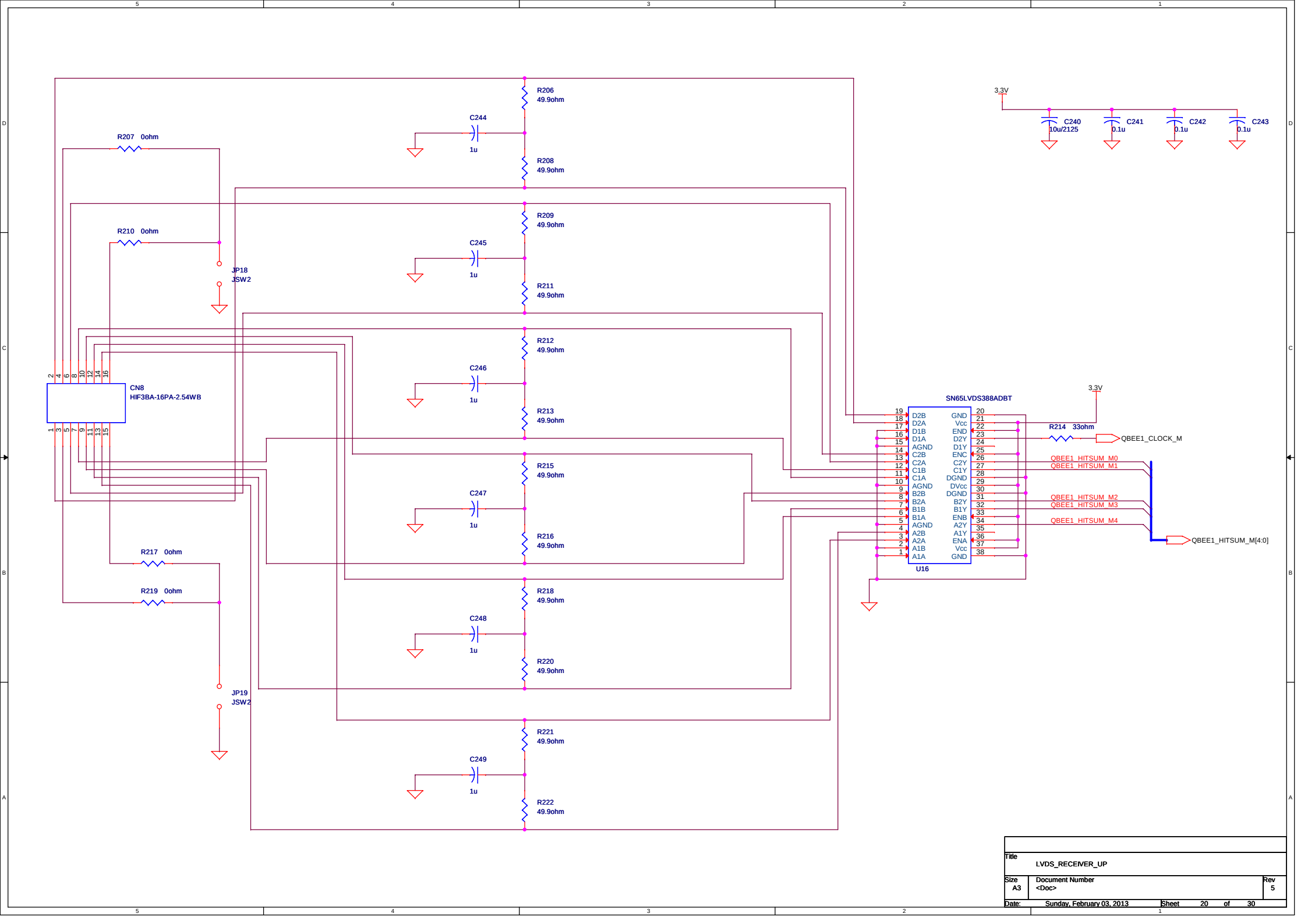
Title	LVDS_RECEIVER_DOWN	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 17 of 30	



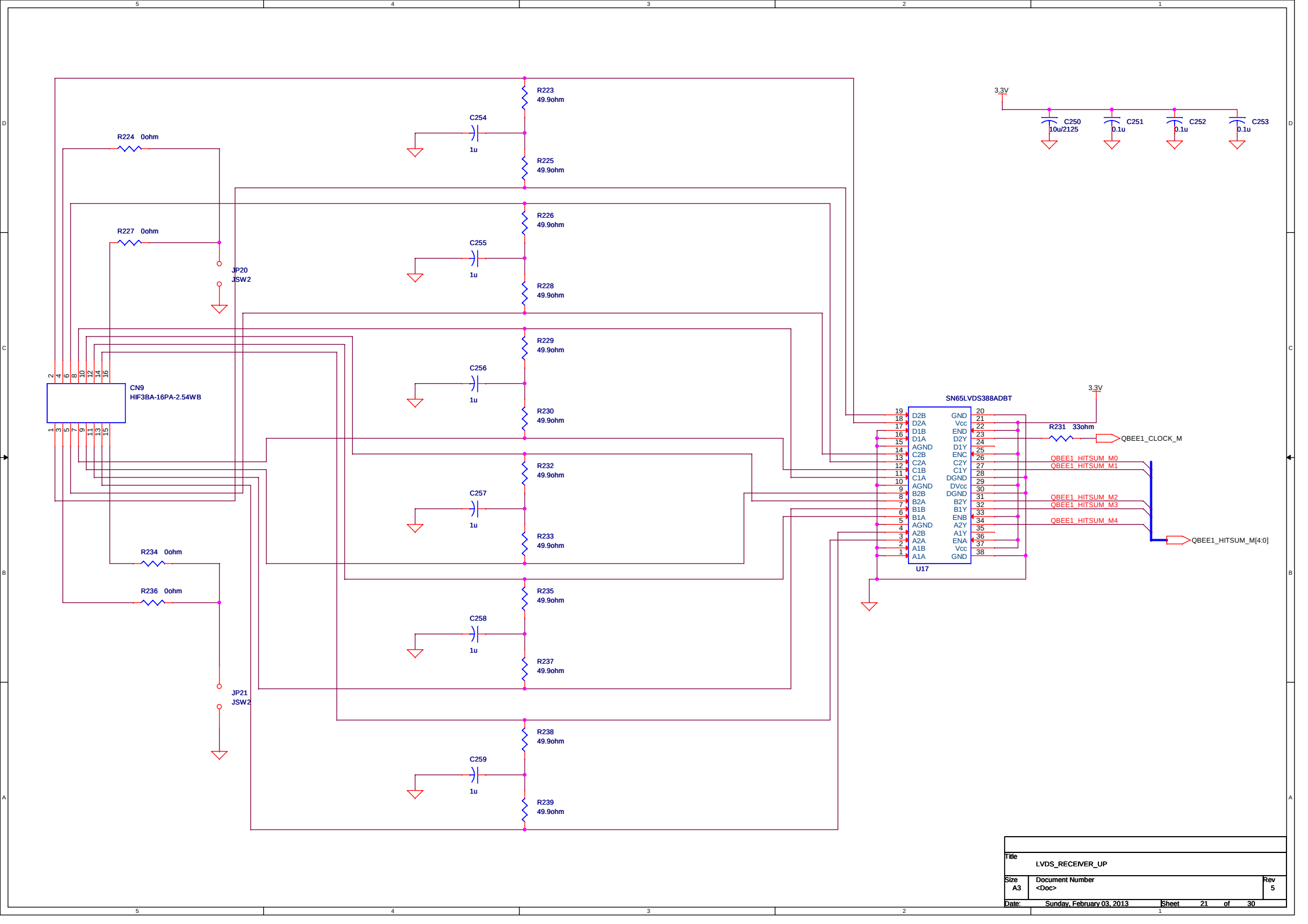
Title	LVDS_RECEIVER_DOWN	
Size: A3	Document Number: <Doc>	Rev: 5
Date: Sunday, February 03, 2013	Sheet 18 of 30	



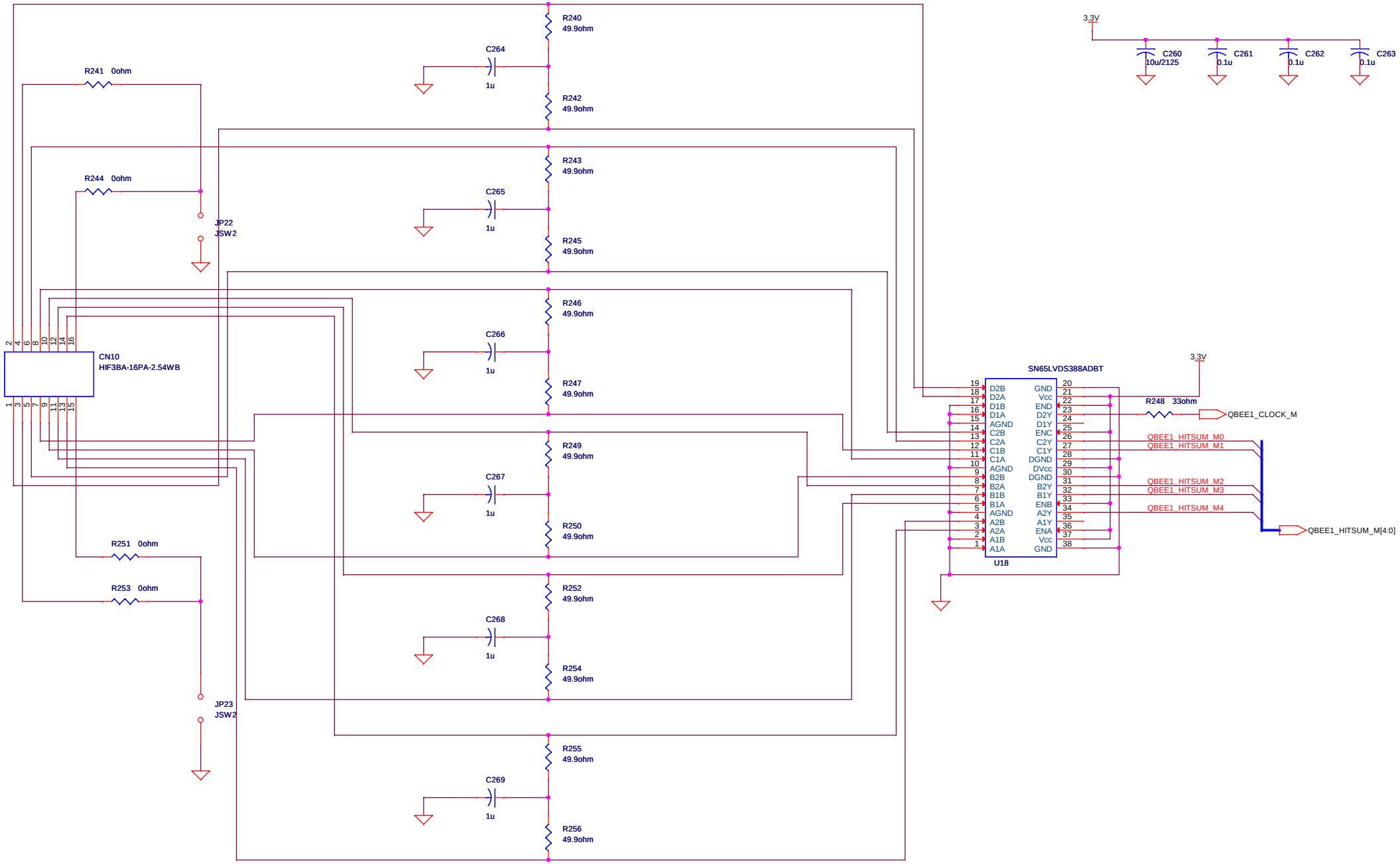
Title	LVDS_RECEIVER_UP	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 19 of 30	



Title	LVDS_RECEIVER_UP	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 20 of 30	



Title	LVDS_RECEIVER_UP	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 21 of 30	



Title	LVDS_RECEIVER_UP	
Size A3	Document Number <Doc>	Rev 5
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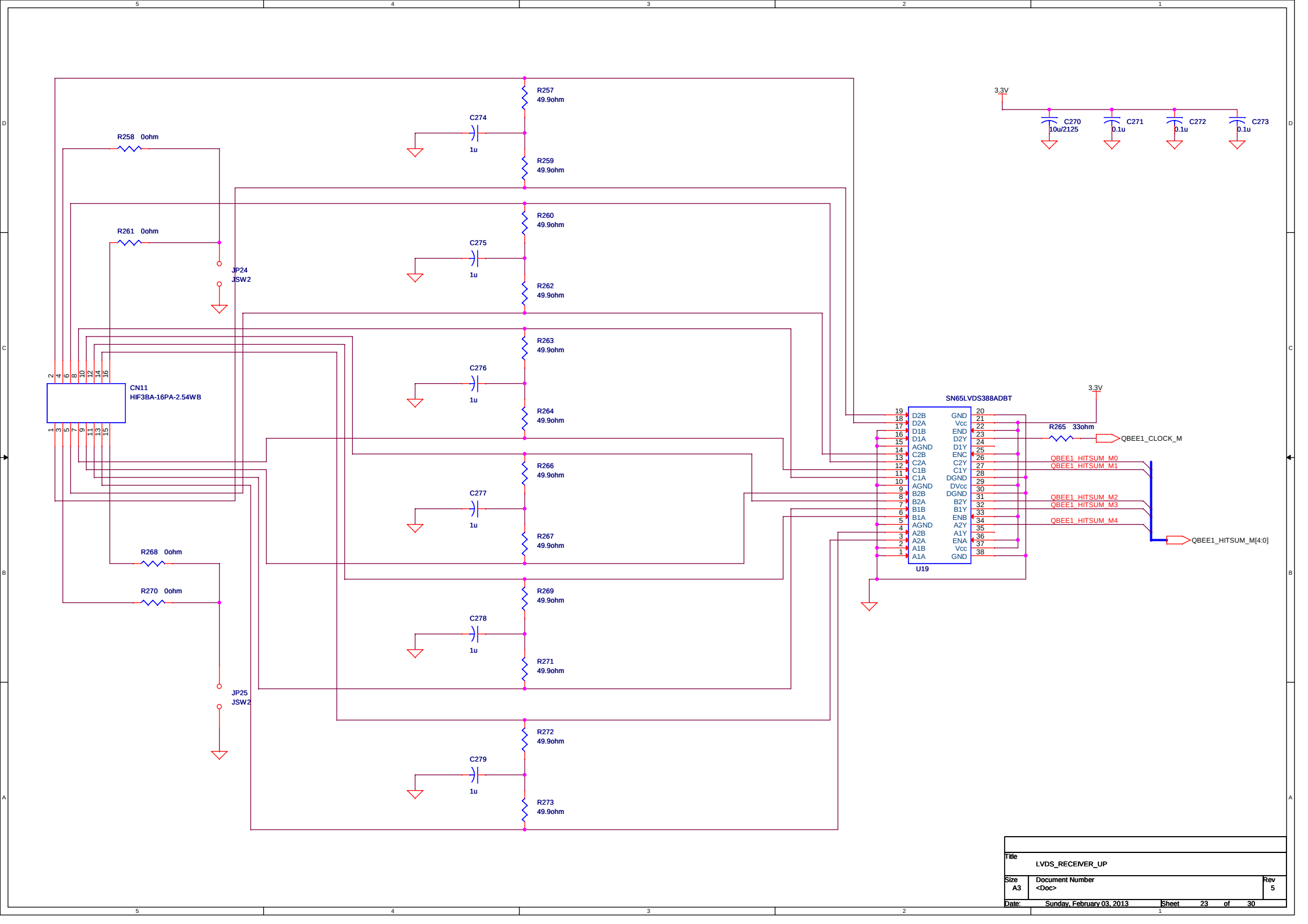

Title	LVDS_RECEIVER_UP	
Size A3	Document Number <Doc>	Rev 5
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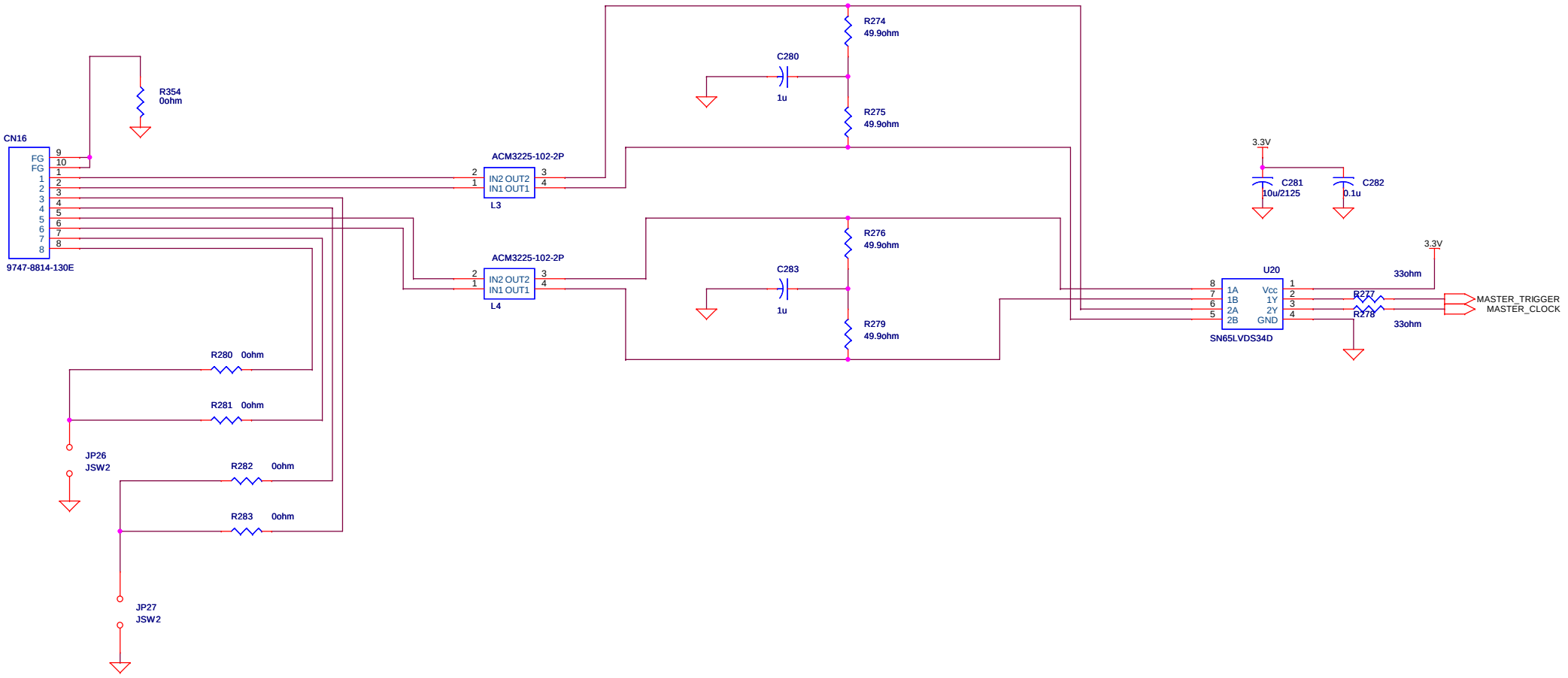

Title	MASTER_CLOCK	
Size A3	Document Number <Doc>	Rev 5
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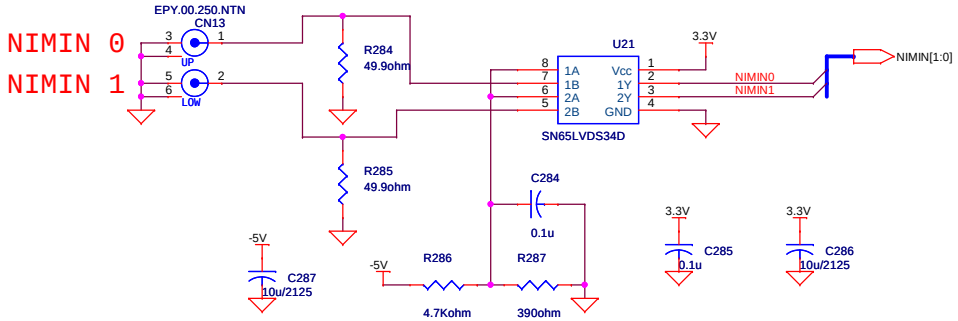

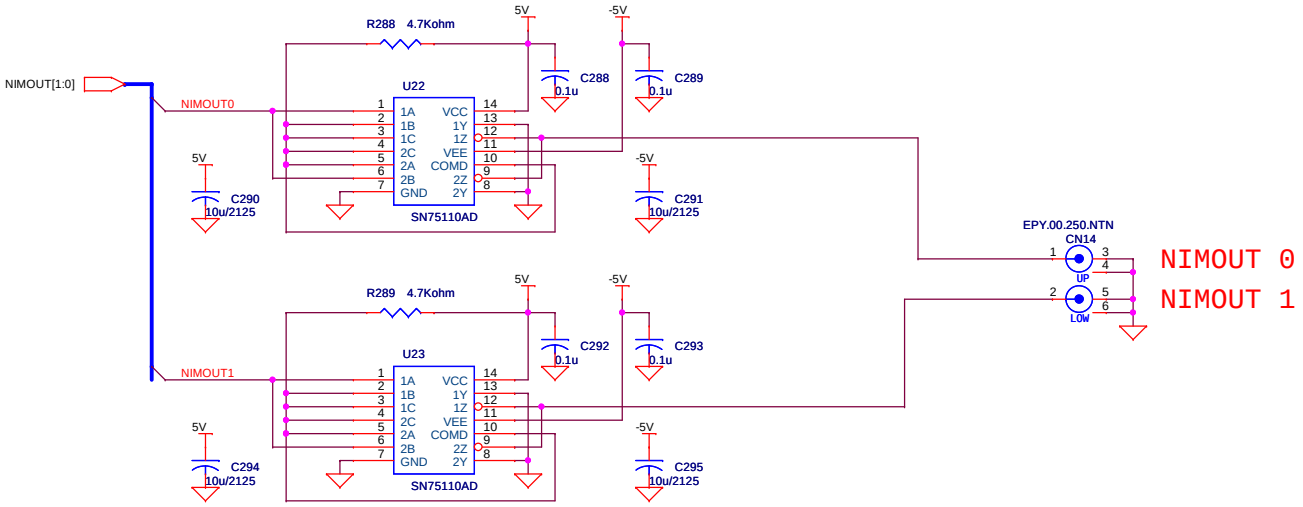

Title: NIM_IN_OUT		
Size: A3	Document Number: <Doc>	Rev: 5
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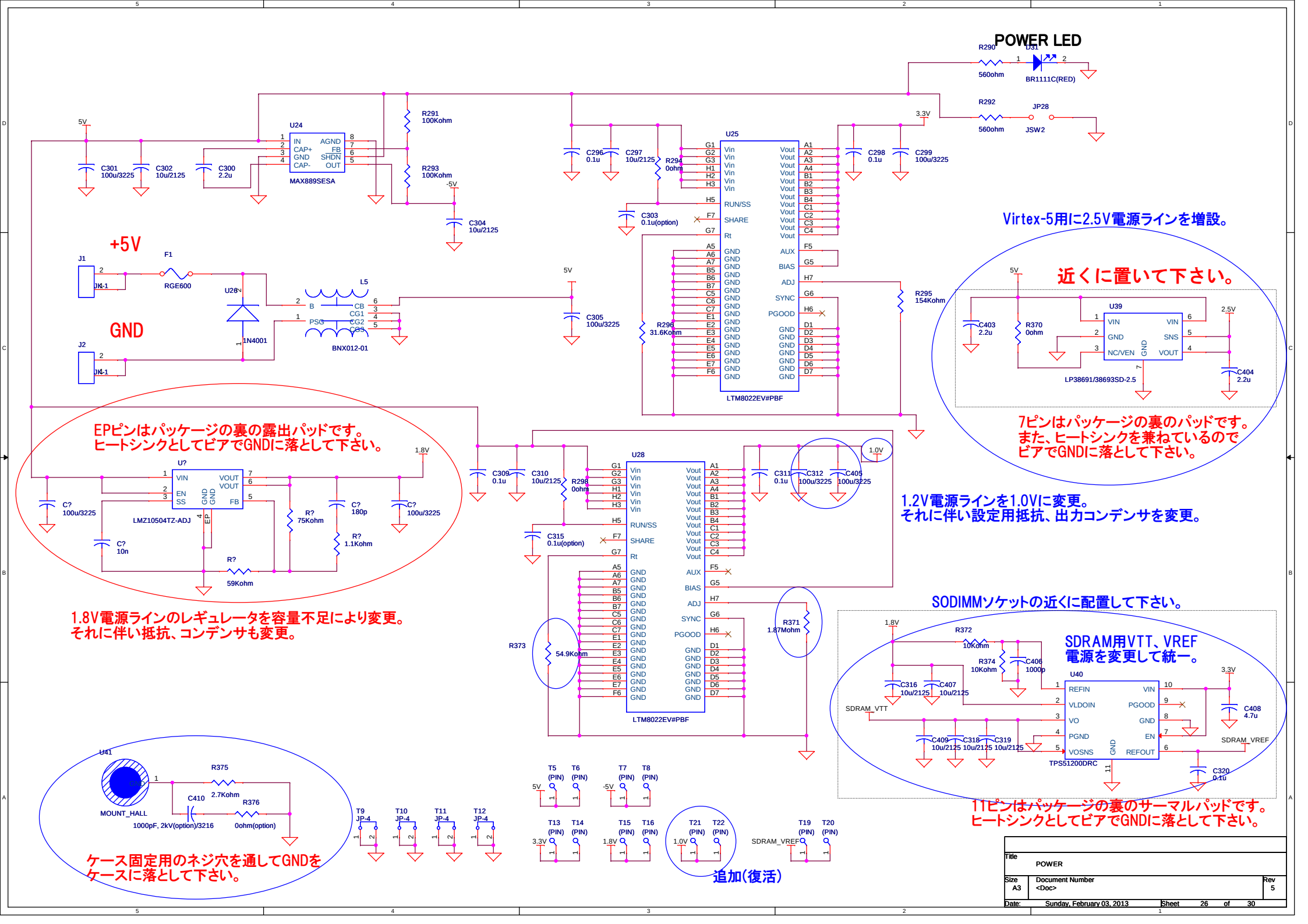
POWER LED
R290
560ohm
D31
BR1111C(RED)
R292
560ohm
JP28
JSW2
3.3V
R291
100Kohm
R293
100Kohm
U24
MAX889SESA
IN
CAP+
GND
CAP-
AGND
FB
SHDN
OUT
5V
-5V
C301
100u/3225
C302
10u/2125
C300
2.2u
C304
10u/2125
C296
0.1u
C297
10u/2125
R294
0ohm
C303
0.1u(option)
U25
LTM8022EV#PBF
RUN/SS
SHARE
Rt
AUX
BIAS
ADJ
SYNC
PGOOD
Vin
Vout
GND
C298
0.1u
C299
100u/3225
R295
154Kohm
R296
31.6Kohm
+5V
GND
J1
J2
JM-1
F1
RGE600
U26
1N4001
L5
BNX012-01
B
PSG
CB
CG1
CG2
CG3
C305
100u/3225
Virtex-5用に2.5V電源ラインを増設。
近くに置いて下さい。
U39
LP38691/38693SD-2.5
VIN
GND
NC/VEN
SNS
VOUT
2.5V
C403
2.2u
R370
0ohm
C404
2.2u
7ピンはパッケージの裏のパッドです。
また、ヒートシンクを兼ねているので
ビアでGNDに落として下さい。
EPピンはパッケージの裏の露出パッドです。
ヒートシンクとしてビアでGNDに落として下さい。
U?
LMZ10504TZ-ADJ
EN
SS
FB
EP
1.8V
C?
100u/3225
C?
10n
R?
75Kohm
C?
180p
R?
1.1Kohm
R?
59Kohm
1.8Vの電源ラインのレギュレータを容量不足により変更。
それに伴い抵抗、コンデンサも変更。
U28
LTM8022EV#PBF
C309
0.1u
C310
10u/2125
R298
0ohm
C315
0.1u(option)
C311
0.1u
C312
100u/3225
C405
100u/3225
1.0V
R373
54.9Kohm
R371
1.87Mohm
1.2V電源ラインを1.0Vに変更。
それに伴い設定用抵抗、出力コンデンサを変更。
SODIMMソケットの近くに配置して下さい。
SDRAM用VTT、VREF
電源を変更して統一。
U40
TPS51200DRC
REFIN
VLDOIN
VO
PGOOD
EN
REFOUT
VIN
R372
10Kohm
R374
10Kohm
C406
1000p
C316
10u/2125
C407
10u/2125
C409
10u/2125
C318
10u/2125
C319
10u/2125
C408
4.7u
C320
0.1u
SDRAM_VTT
SDRAM_VREF
11ピンはパッケージの裏のサーマルパッドです。
ヒートシンクとしてビアでGNDに落として下さい。
U41
MOUNT_HALL
R375
2.7Kohm
C410
1000pF, 2kV(option)/3216
R376
0ohm(option)
ケース固定用のネジ穴を通してGNDを
ケースに落として下さい。
T5 (PIN)
T6 (PIN)
T7 (PIN)
T8 (PIN)
T9 JP-4
T10 JP-4
T11 JP-4
T12 JP-4
T13 (PIN)
T14 (PIN)
T15 (PIN)
T16 (PIN)
T21 (PIN)
T22 (PIN)
T19 (PIN)
T20 (PIN)
追加(復活)
Title
POWER
Size
A3
Document Number
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Rev
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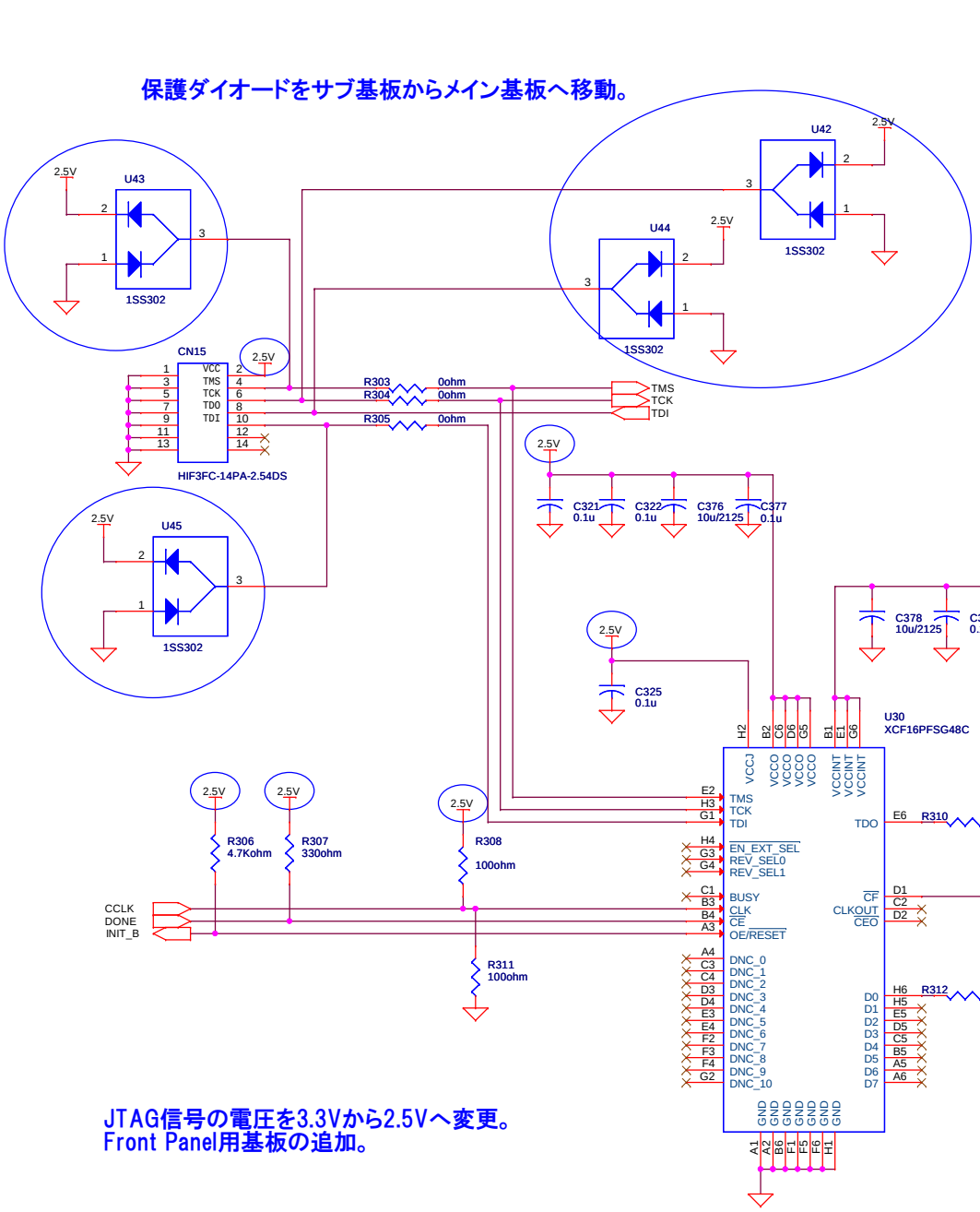
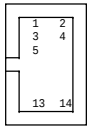
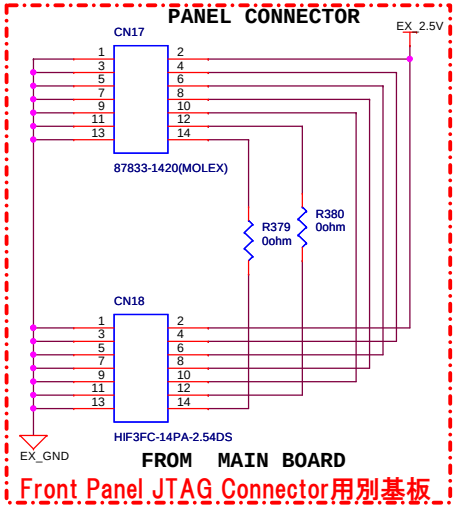
保護ダイオードをサブ基板からメイン基板へ移動。



Top View





JTAG信号の電圧を3.3Vから2.5Vへ変更。
Front Panel用基板の追加。

Title	PROM	
Size A3	Document Number <Doc>	Rev 5
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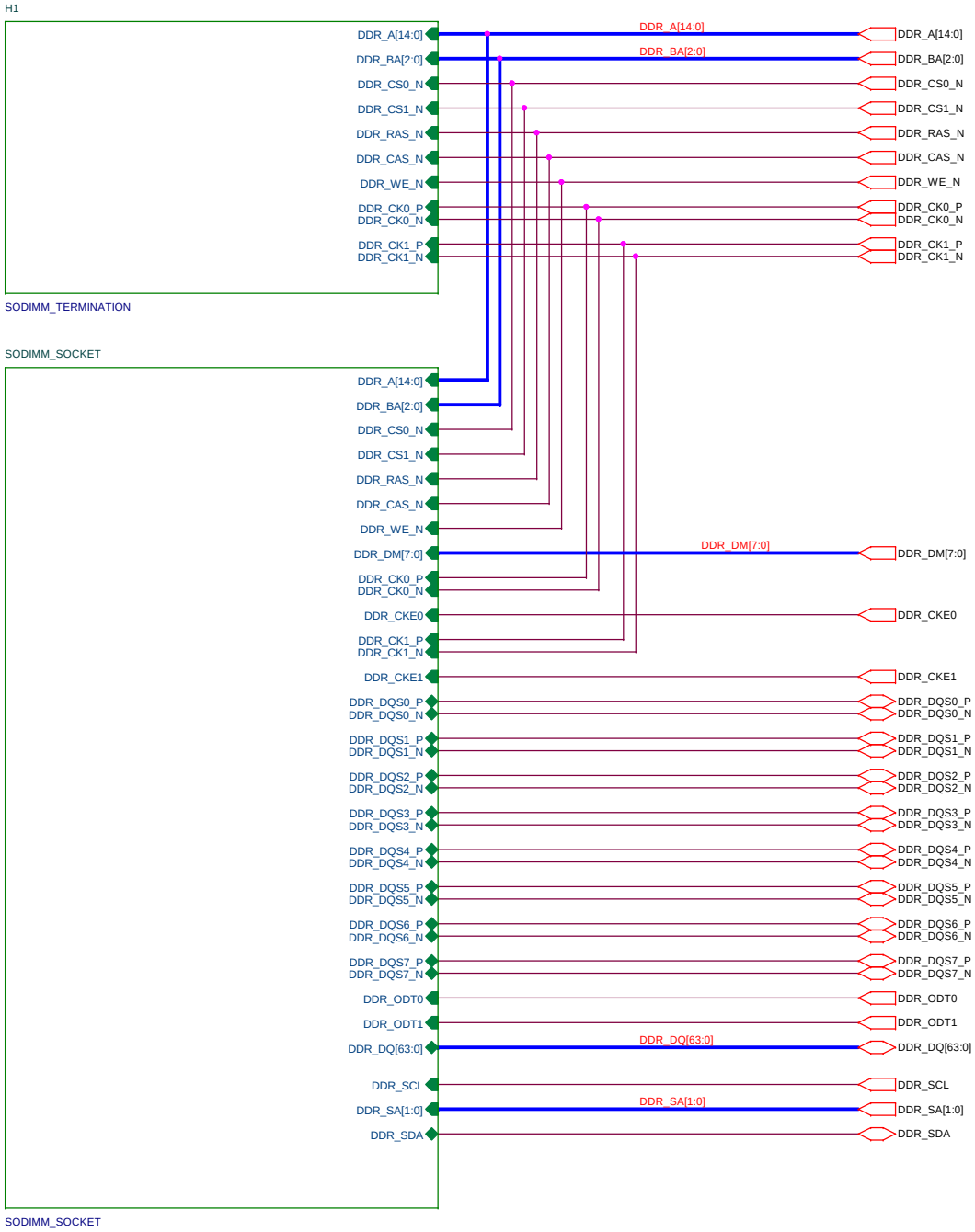
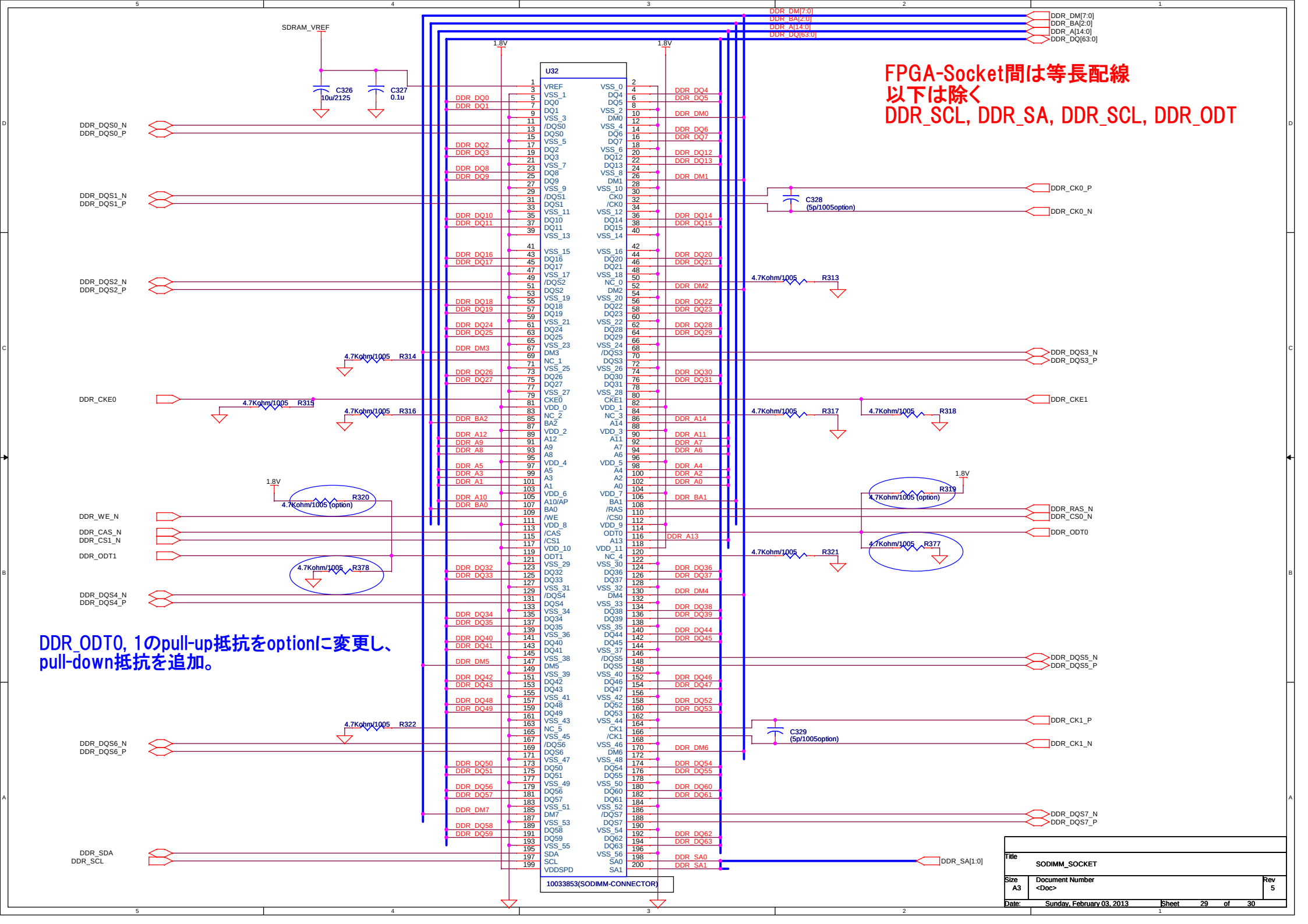


Title	SODIMM	
Size A3	Document Number <Doc>	Rev 5
Date: Sunday, February 03, 2013	Sheet 28 of 30	


FPGA-Socket間は等長配線
以下は除く
DDR_SCL, DDR_SA, DDR_SCL, DDR_ODT
DDR_ODT0, 1のpull-up抵抗をoptionに変更し、
pull-down抵抗を追加。
U32
10033853(SODIMM-CONNECTOR)
SDRAM_VREF
1.8V
C326
10u/2125
C327
0.1u
C328
(5p/1005option)
C329
(5p/1005option)
4.7Kohm/1005 R313
4.7Kohm/1005 R314
4.7Kohm/1005 R315
4.7Kohm/1005 R316
4.7Kohm/1005 R317
4.7Kohm/1005 R318
4.7Kohm/1005 (option) R319
4.7Kohm/1005 (option) R320
4.7Kohm/1005 R321
4.7Kohm/1005 R322
4.7Kohm/1005 R377
4.7Kohm/1005 R378
DDR_DM[7:0]
DDR_BA[2:0]
DDR_A[14:0]
DDR_DQ[63:0]
DDR_DQS0_N
DDR_DQS0_P
DDR_DQS1_N
DDR_DQS1_P
DDR_DQS2_N
DDR_DQS2_P
DDR_DQS3_N
DDR_DQS3_P
DDR_DQS4_N
DDR_DQS4_P
DDR_DQS5_N
DDR_DQS5_P
DDR_DQS6_N
DDR_DQS6_P
DDR_DQS7_N
DDR_DQS7_P
DDR_CK0_P
DDR_CK0_N
DDR_CK1_P
DDR_CK1_N
DDR_CKE0
DDR_CKE1
DDR_WE_N
DDR_CAS_N
DDR_CS1_N
DDR_ODT1
DDR_RAS_N
DDR_CS0_N
DDR_ODT0
DDR_SDA
DDR_SCL
DDR_SA[1:0]
Title
SODIMM_SOCKET
Size A3
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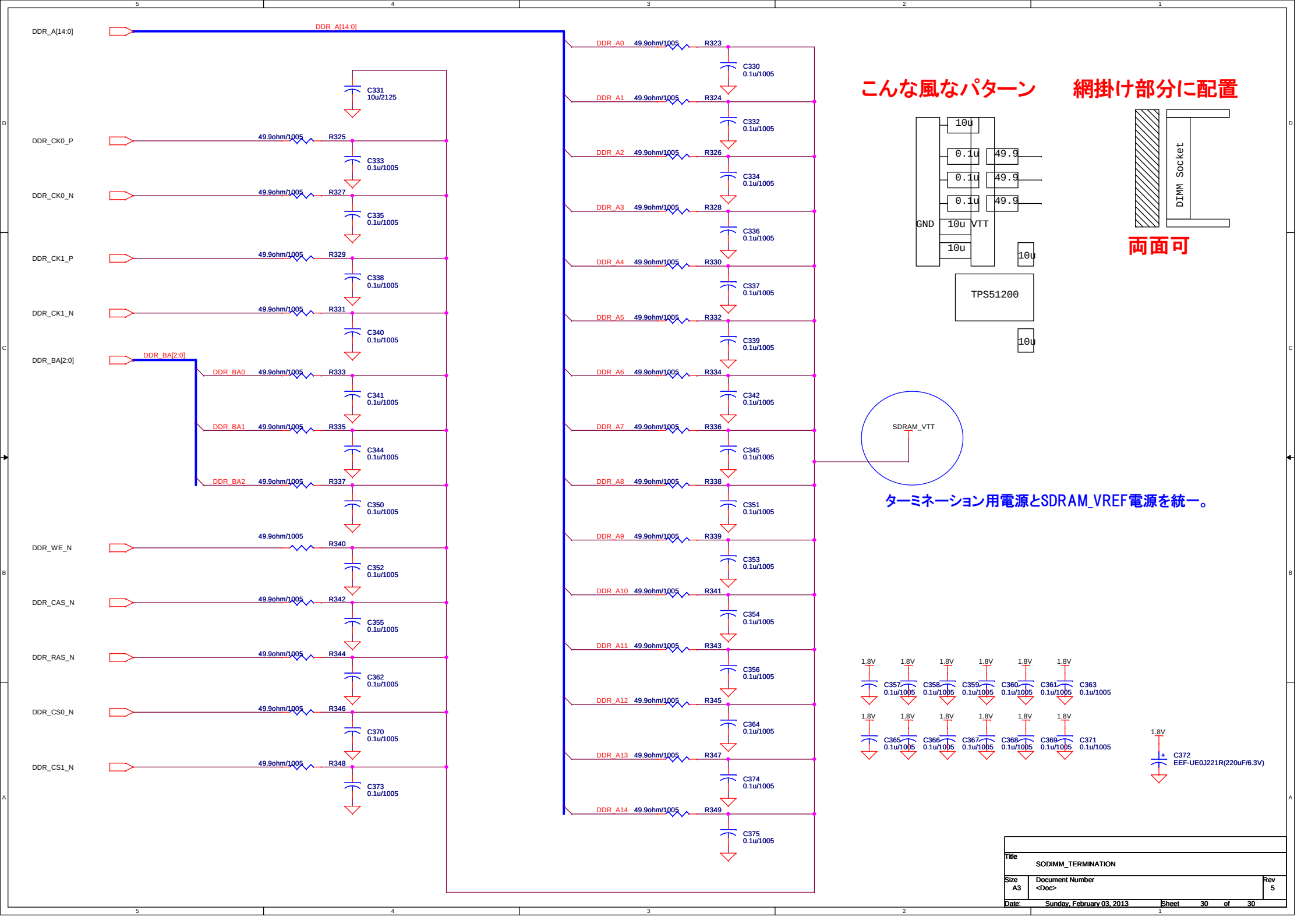
DDR_A[14:0]
DDR_A[14:0]
DDR_CK0_P
DDR_CK0_N
DDR_CK1_P
DDR_CK1_N
DDR_BA[2:0]
DDR_BA[2:0]
DDR_WE_N
DDR_CAS_N
DDR_RAS_N
DDR_CS0_N
DDR_CS1_N
DDR_BA0
DDR_BA1
DDR_BA2
DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_A13
DDR_A14
49.9ohm/1005
R323
R324
R325
R326
R327
R328
R329
R330
R331
R332
R333
R334
R335
R336
R337
R338
R339
R340
R341
R342
R343
R344
R345
R346
R347
R348
R349
C330 0.1u/1005
C331 10u/2125
C332 0.1u/1005
C333 0.1u/1005
C334 0.1u/1005
C335 0.1u/1005
C336 0.1u/1005
C337 0.1u/1005
C338 0.1u/1005
C339 0.1u/1005
C340 0.1u/1005
C341 0.1u/1005
C342 0.1u/1005
C344 0.1u/1005
C345 0.1u/1005
C350 0.1u/1005
C351 0.1u/1005
C352 0.1u/1005
C353 0.1u/1005
C354 0.1u/1005
C355 0.1u/1005
C356 0.1u/1005
C362 0.1u/1005
C364 0.1u/1005
C370 0.1u/1005
C373 0.1u/1005
C374 0.1u/1005
C375 0.1u/1005
こんな風なパターン
網掛け部分に配置
10u
0.1u
0.1u
0.1u
49.9
49.9
49.9
GND
10u
VTT
10u
10u
TPS51200
DIMM Socket
両面可
SDRAM_VTT
ターミネーション用電源とSDRAM_VREF電源を統一。
1.8V
C357 0.1u/1005
C358 0.1u/1005
C359 0.1u/1005
C360 0.1u/1005
C361 0.1u/1005
C363 0.1u/1005
C365 0.1u/1005
C366 0.1u/1005
C367 0.1u/1005
C368 0.1u/1005
C369 0.1u/1005
C371 0.1u/1005
C372
EEF-UE0J221R(220uF/6.3V)
Title
SODIMM_TERMINATION
Size
A3
Document Number
<Doc>
Rev
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