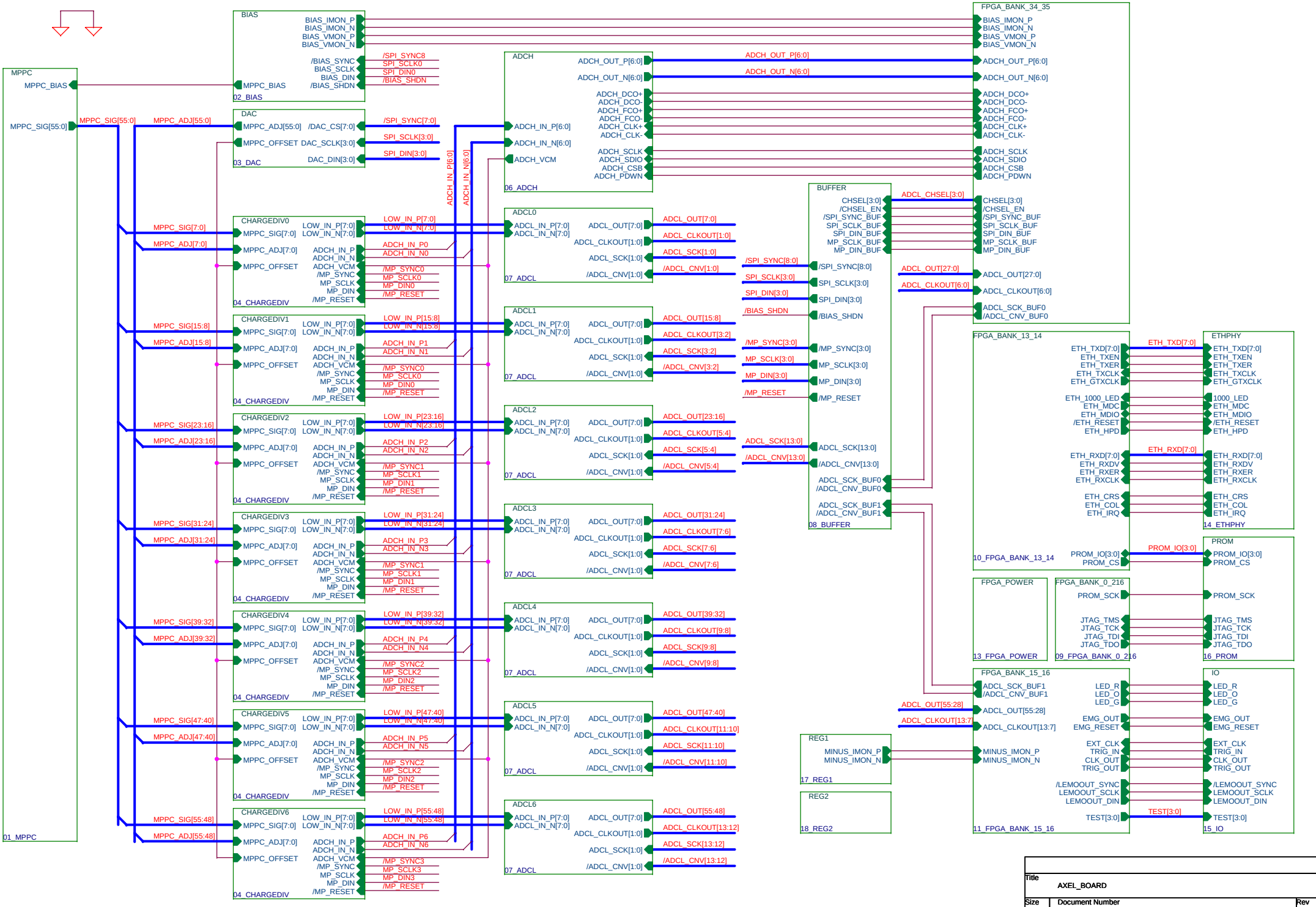
MPPC
MPPC_BIAS
MPPC_SIG[55:0]
01_MPPC
BIAS
BIAS_IMON_P
BIAS_IMON_N
BIAS_VMON_P
BIAS_VMON_N
/BIAS_SYNC
BIAS_SCLK
BIAS_DIN
/BIAS_SHDN
MPPC_BIAS
02_BIAS
/SPI_SYNC8
SPI_SCLK0
SPI_DIN0
/BIAS_SHDN
DAC
MPPC_ADJ[55:0]
MPPC_OFFSET
/DAC_CS[7:0]
DAC_SCLK[3:0]
DAC_DIN[3:0]
03_DAC
/SPI_SYNC[7:0]
SPI_SCLK[3:0]
SPI_DIN[3:0]
CHARGEDIV0
CHARGEDIV1
CHARGEDIV2
CHARGEDIV3
CHARGEDIV4
CHARGEDIV5
CHARGEDIV6
LOW_IN_P[7:0]
LOW_IN_N[7:0]
MPPC_SIG[7:0]
MPPC_ADJ[7:0]
ADCH_IN_P
ADCH_IN_N
ADCH_VCM
/MP_SYNC
MP_SCLK
MP_DIN
/MP_RESET
04_CHARGEDIV
LOW_IN_P[15:8]
LOW_IN_N[15:8]
MPPC_SIG[15:8]
MPPC_ADJ[15:8]
LOW_IN_P[23:16]
LOW_IN_N[23:16]
MPPC_SIG[23:16]
MPPC_ADJ[23:16]
LOW_IN_P[31:24]
LOW_IN_N[31:24]
MPPC_SIG[31:24]
MPPC_ADJ[31:24]
LOW_IN_P[39:32]
LOW_IN_N[39:32]
MPPC_SIG[39:32]
MPPC_ADJ[39:32]
LOW_IN_P[47:40]
LOW_IN_N[47:40]
MPPC_SIG[47:40]
MPPC_ADJ[47:40]
LOW_IN_P[55:48]
LOW_IN_N[55:48]
MPPC_SIG[55:48]
MPPC_ADJ[55:48]
ADCH_IN_P0
ADCH_IN_N0
/MP_SYNC0
MP_SCLK0
MP_DIN0
/MP_RESET
ADCH_IN_P1
ADCH_IN_N1
/MP_SYNC1
MP_SCLK1
MP_DIN1
ADCH_IN_P2
ADCH_IN_N2
ADCH_IN_P3
ADCH_IN_N3
ADCH_IN_P4
ADCH_IN_N4
/MP_SYNC2
MP_SCLK2
MP_DIN2
ADCH_IN_P5
ADCH_IN_N5
/MP_SYNC3
MP_SCLK3
MP_DIN3
ADCH_IN_P6
ADCH_IN_N6
ADCH_IN_P[6:0]
ADCH_IN_N[6:0]
ADCH
ADCH_OUT_P[6:0]
ADCH_OUT_N[6:0]
ADCH_DCO+
ADCH_DCO-
ADCH_FCO+
ADCH_FCO-
ADCH_CLK+
ADCH_CLK-
ADCH_VCM
ADCH_SCLK
ADCH_SDIO
ADCH_CSB
ADCH_PDWN
06_ADCH
ADCL0
ADCL1
ADCL2
ADCL3
ADCL4
ADCL5
ADCL6
ADCL_IN_P[7:0]
ADCL_IN_N[7:0]
ADCL_OUT[7:0]
ADCL_CLKOUT[1:0]
ADCL_SCK[1:0]
/ADCL_CNV[1:0]
07_ADCL
ADCL_OUT[15:8]
ADCL_CLKOUT[3:2]
ADCL_SCK[3:2]
/ADCL_CNV[3:2]
ADCL_OUT[23:16]
ADCL_CLKOUT[5:4]
ADCL_SCK[5:4]
/ADCL_CNV[5:4]
ADCL_OUT[31:24]
ADCL_CLKOUT[7:6]
ADCL_SCK[7:6]
/ADCL_CNV[7:6]
ADCL_OUT[39:32]
ADCL_CLKOUT[9:8]
ADCL_SCK[9:8]
/ADCL_CNV[9:8]
ADCL_OUT[47:40]
ADCL_CLKOUT[11:10]
ADCL_SCK[11:10]
/ADCL_CNV[11:10]
ADCL_OUT[55:48]
ADCL_CLKOUT[13:12]
ADCL_SCK[13:12]
/ADCL_CNV[13:12]
BUFFER
CHSEL[3:0]
/CHSEL_EN
/SPI_SYNC_BUF
SPI_SCLK_BUF
SPI_DIN_BUF
MP_SCLK_BUF
MP_DIN_BUF
/SPI_SYNC[8:0]
SPI_SCLK[3:0]
SPI_DIN[3:0]
/BIAS_SHDN
/MP_SYNC[3:0]
MP_SCLK[3:0]
MP_DIN[3:0]
/MP_RESET
ADCL_SCK[13:0]
/ADCL_CNV[13:0]
ADCL_SCK_BUF0
/ADCL_CNV_BUF0
ADCL_SCK_BUF1
/ADCL_CNV_BUF1
08_BUFFER
ADCL_CHSEL[3:0]
ADCL_OUT[27:0]
ADCL_CLKOUT[6:0]
ADCL_SCK_BUF0
/ADCL_CNV_BUF0
ADCL_OUT[55:28]
ADCL_CLKOUT[13:7]
REG1
MINUS_IMON_P
MINUS_IMON_N
17_REG1
REG2
18_REG2
FPGA_BANK_34_35
11_FPGA_BANK_15_16
FPGA_BANK_13_14
10_FPGA_BANK_13_14
FPGA_POWER
13_FPGA_POWER
FPGA_BANK_0_216
09_FPGA_BANK_0_216
ETHPHY
ETH_TXD[7:0]
ETH_TXEN
ETH_TXER
ETH_TXCLK
ETH_GTXCLK
ETH_1000_LED
ETH_MDC
ETH_MDIO
/ETH_RESET
ETH_HPD
ETH_RXD[7:0]
ETH_RXDV
ETH_RXER
ETH_RXCLK
ETH_CRS
ETH_COL
ETH_IRQ
14_ETHPHY
PROM
PROM_IO[3:0]
PROM_CS
PROM_SCK
JTAG_TMS
JTAG_TCK
JTAG_TDI
JTAG_TDO
16_PROM
IO
LED_R
LED_O
LED_G
EMG_OUT
EMG_RESET
EXT_CLK
TRIG_IN
CLK_OUT
TRIG_OUT
/LEMOOUT_SYNC
LEMOOUT_SCLK
LEMOOUT_DIN
TEST[3:0]
15_IO
GN-1806-1
Title
AXEL_BOARD
Size
A3
Document Number
<Doc>
Rev
1
Date:
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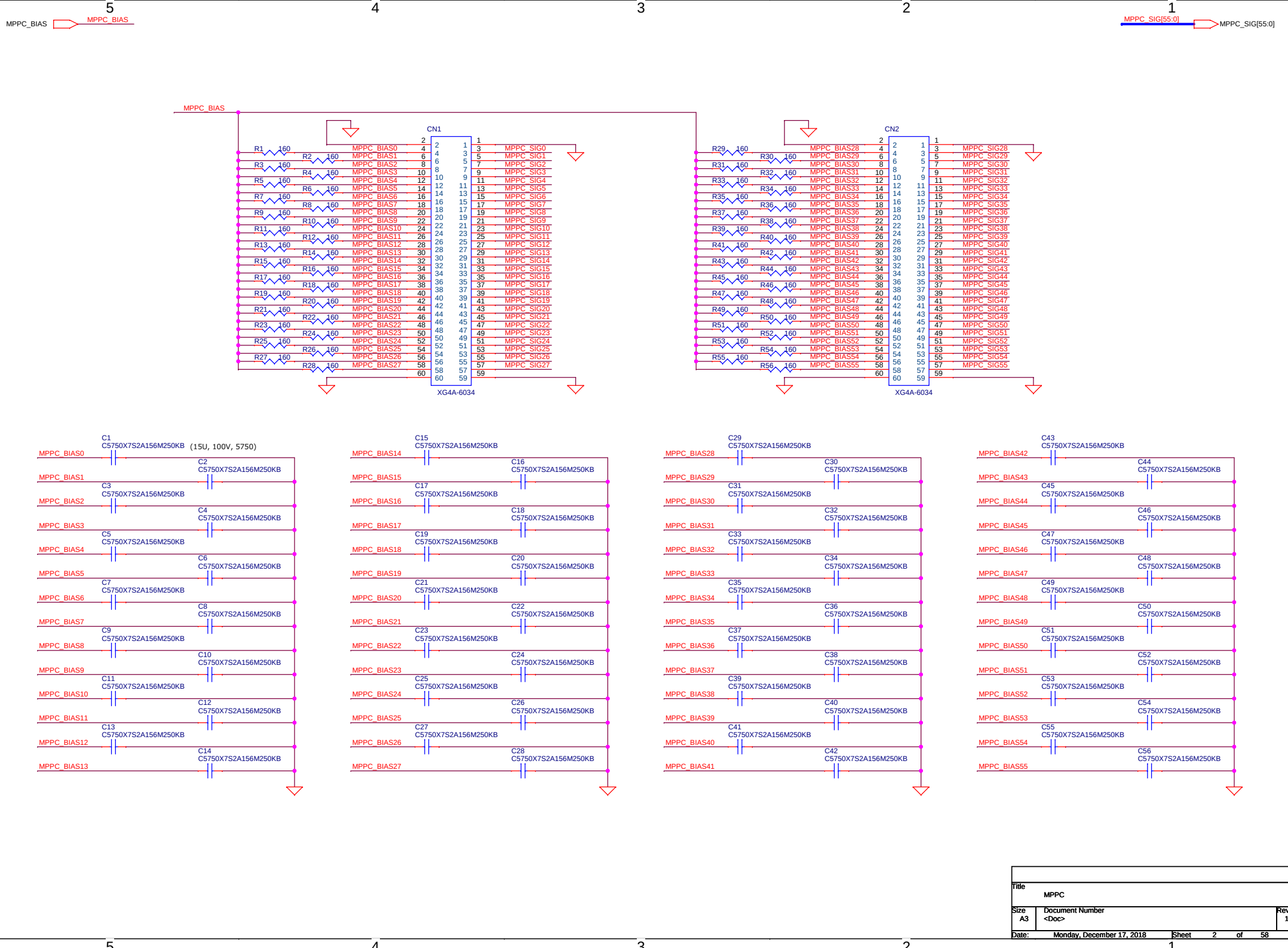
MPPC_BIAS
MPPC_BIAS
MPPC_SIG[55:0]
MPPC_SIG[55:0]
CN1
CN2
XG4A-6034
XG4A-6034
C1
C5750X7S2A156M250KB
(15U, 100V, 5750)
Title
MPPC
Size
A3
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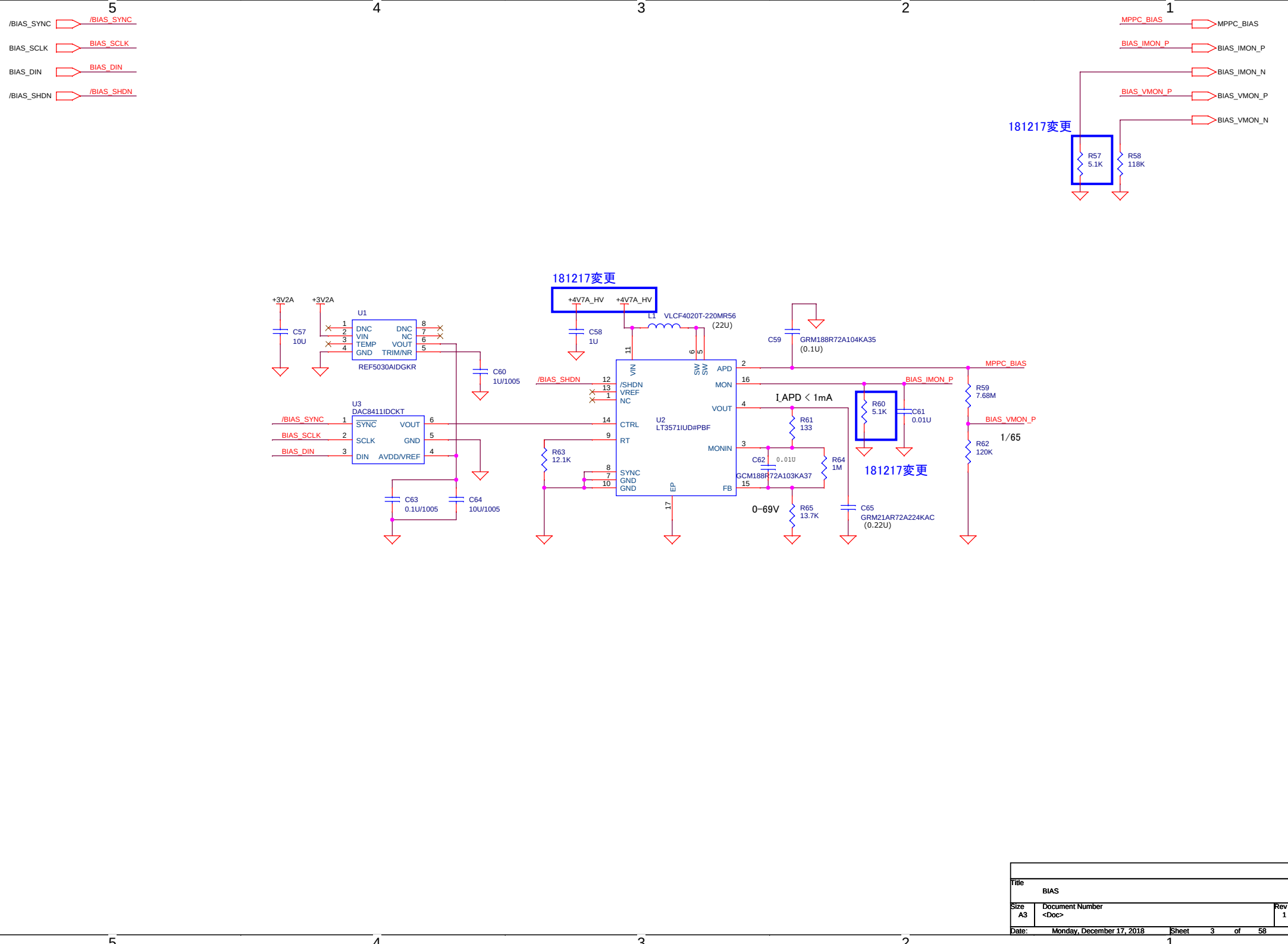

Title	BIAS		
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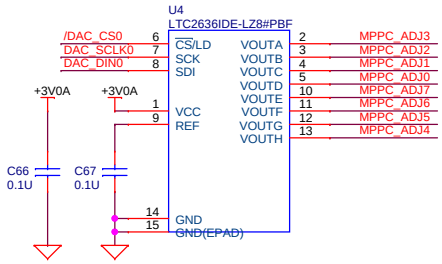
/DAC_CS[7:0] /DAC_CS[7:0]

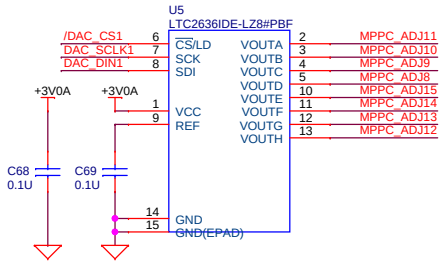
DAC_SCLK[3:0] DAC_SCLK[3:0]

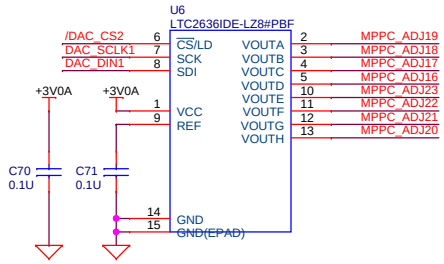
DAC_DIN[3:0] DAC_DIN[3:0]

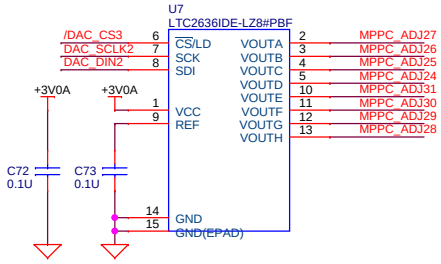
MPPC_ADJ[55:0] MPPC_ADJ[55:0]

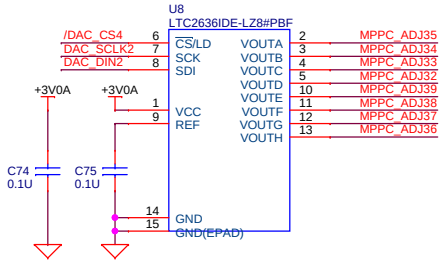
MPPC_OFFSET MPPC_OFFSET

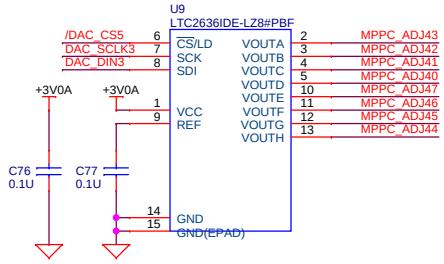


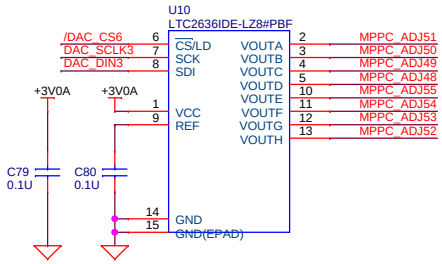


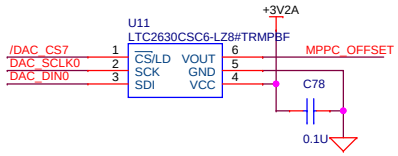












Title: DAC			
Size: A3	Document Number: <Doc>		Rev: 1
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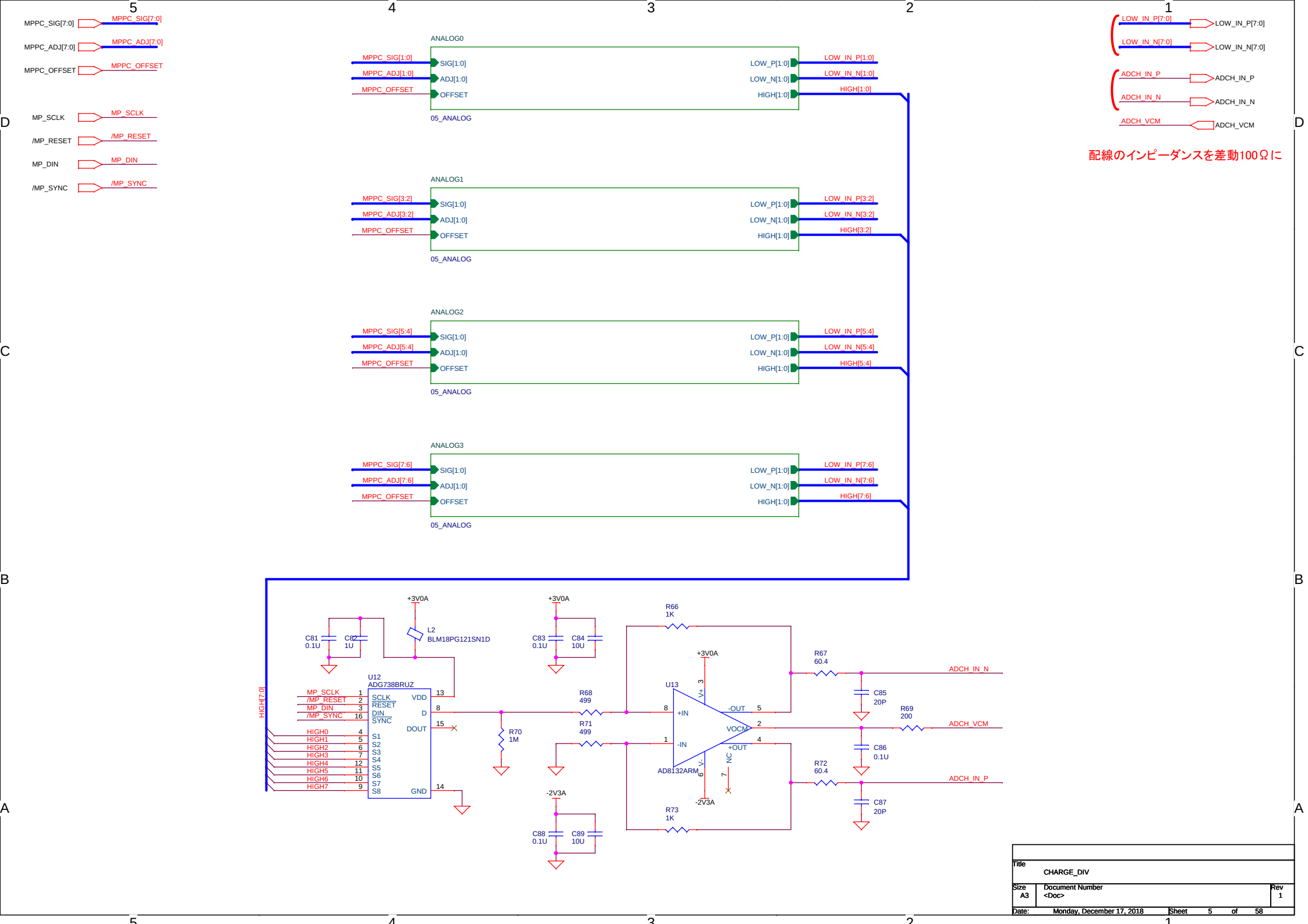
MPPC_SIG[7:0]
MPPC_ADJ[7:0]
MPPC_OFFSET
MP_SCLK
/MP_RESET
MP_DIN
/MP_SYNC
ANALOG0
SIG[1:0]
ADJ[1:0]
OFFSET
LOW_P[1:0]
LOW_N[1:0]
HIGH[1:0]
05_ANALOG
ANALOG1
ANALOG2
ANALOG3
LOW_IN_P[7:0]
LOW_IN_N[7:0]
ADCH_IN_P
ADCH_IN_N
ADCH_VCM
配線のインピーダンスを差動100Ωに
+3V0A
L2
BLM18PG121SN1D
C81
0.1U
C82
1U
C83
0.1U
C84
10U
U12
ADG738BRUZ
SCLK
RESET
DIN
SYNC
VDD
D
DOUT
S1
S2
S3
S4
S5
S6
S7
S8
GND
HIGH0
HIGH1
HIGH2
HIGH3
HIGH4
HIGH5
HIGH6
HIGH7
R70
1M
R66
1K
R67
60.4
R68
499
R69
200
R71
499
R72
60.4
R73
1K
U13
AD8132ARM
+IN
-IN
-OUT
+OUT
VOCM
V+
V-
NC
-2V3A
C85
20P
C86
0.1U
C87
20P
C88
0.1U
C89
10U
Title
CHARGE_DIV
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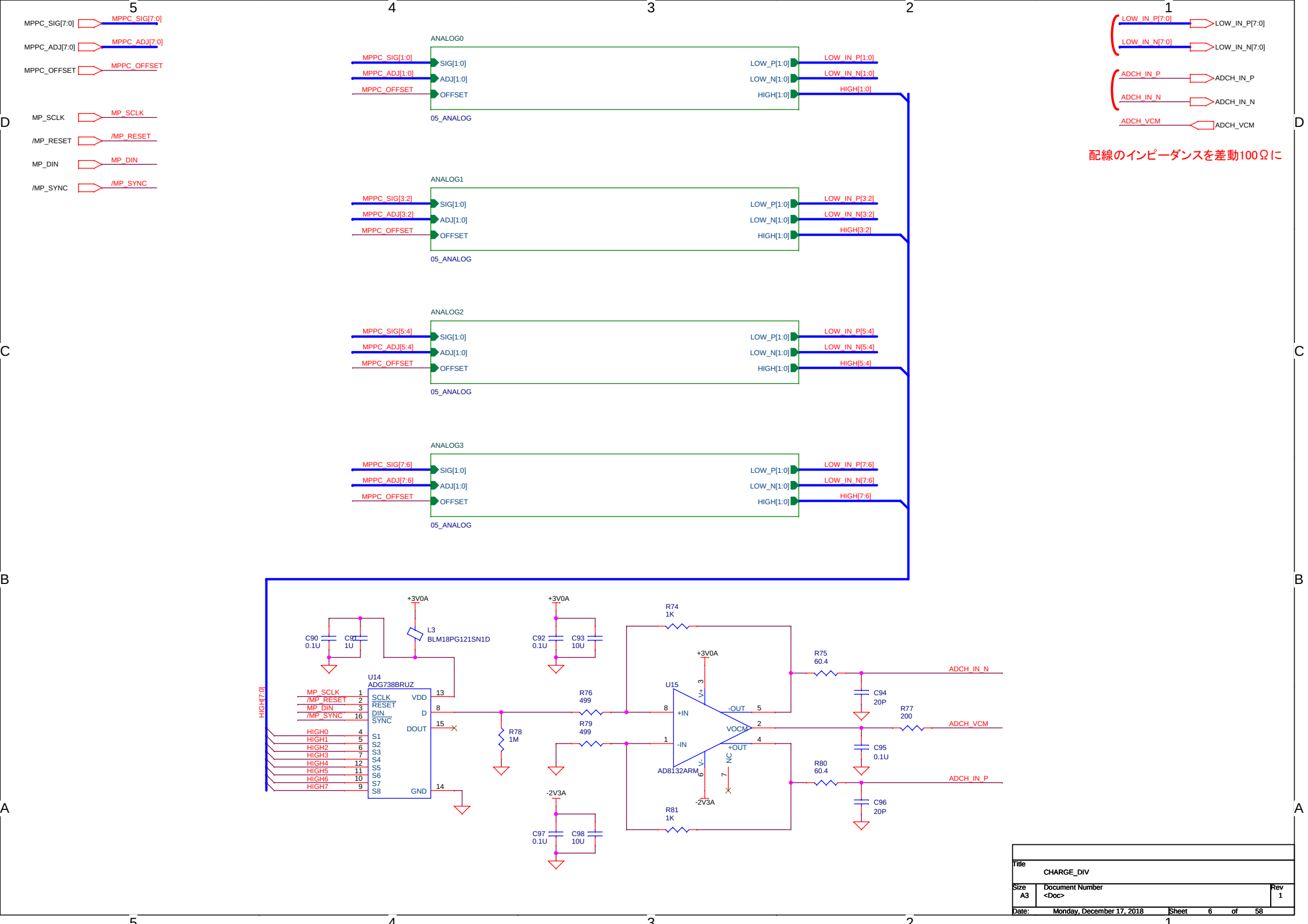
MPPC_SIG[7:0]
MPPC_ADJ[7:0]
MPPC_OFFSET
MP_SCLK
/MP_RESET
MP_DIN
/MP_SYNC
ANALOG0
SIG[1:0]
ADJ[1:0]
OFFSET
LOW_P[1:0]
LOW_N[1:0]
HIGH[1:0]
05_ANALOG
ANALOG1
ANALOG2
ANALOG3
LOW_IN_P[7:0]
LOW_IN_N[7:0]
ADCH_IN_P
ADCH_IN_N
ADCH_VCM
配線のインピーダンスを差動100Ωに
+3V0A
L3
BLM18PG121SN1D
C90
0.1U
C91
1U
C92
C93
10U
U14
ADG738BRUZ
SCLK
RESET
DIN
SYNC
VDD
D
DOUT
S1
S2
S3
S4
S5
S6
S7
S8
GND
HIGH0
HIGH1
HIGH2
HIGH3
HIGH4
HIGH5
HIGH6
HIGH7
R78
1M
R74
1K
R75
60.4
R76
499
R79
499
R77
200
R80
60.4
R81
1K
U15
AD8132ARM
+IN
-IN
-OUT
+OUT
VOCM
V+
V-
NC
-2V3A
C94
20P
C95
0.1U
C96
20P
C97
0.1U
C98
10U
ADCH_IN_N
ADCH_VCM
ADCH_IN_P
Title
CHARGE_DIV
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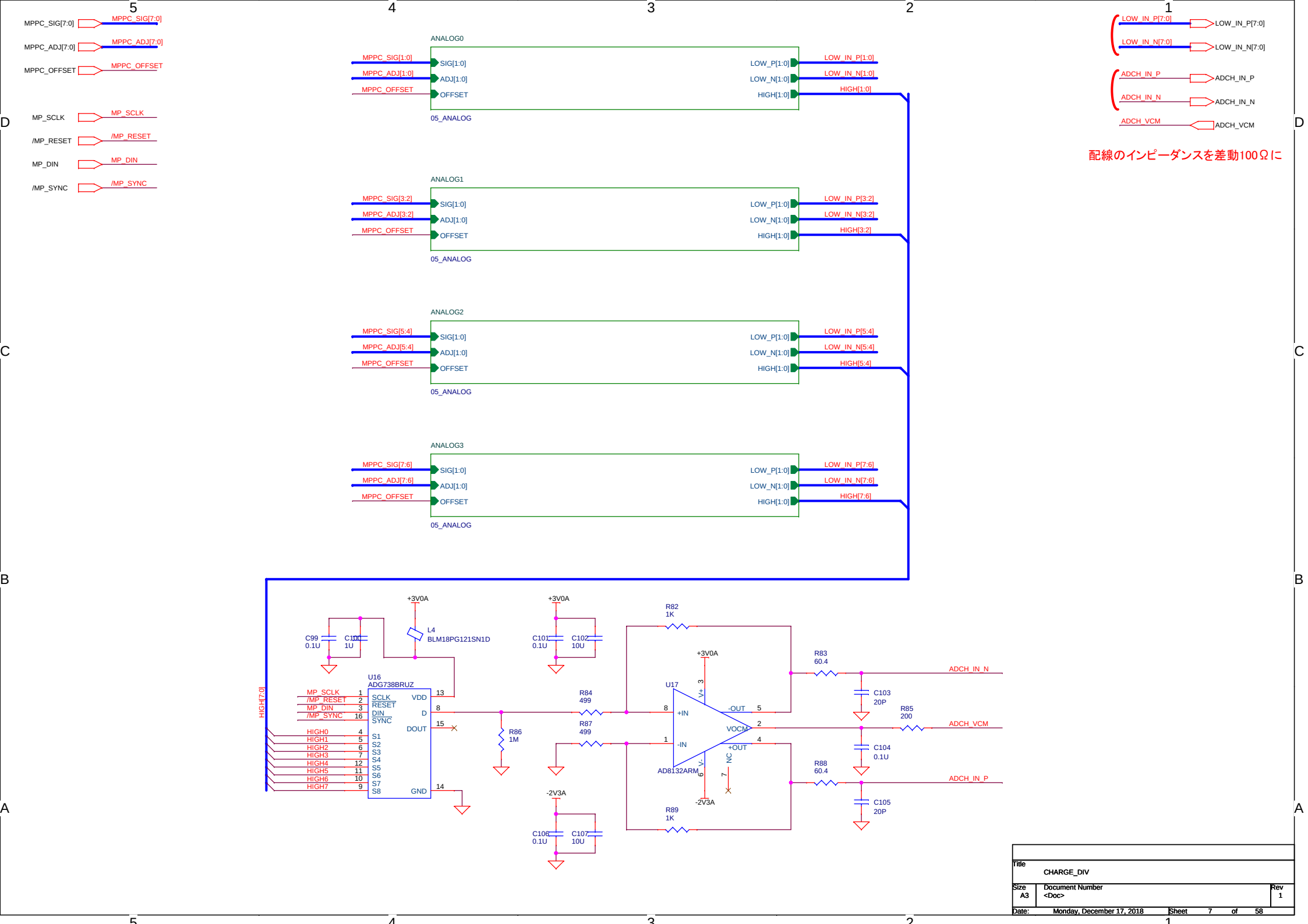
MPPC_SIG[7:0]
MPPC_ADJ[7:0]
MPPC_OFFSET
MP_SCLK
/MP_RESET
MP_DIN
/MP_SYNC
ANALOG0
MPPC_SIG[1:0]
MPPC_ADJ[1:0]
MPPC_OFFSET
SIG[1:0]
ADJ[1:0]
OFFSET
LOW_P[1:0]
LOW_N[1:0]
HIGH[1:0]
LOW_IN_P[1:0]
LOW_IN_N[1:0]
HIGH[1:0]
05_ANALOG
ANALOG1
MPPC_SIG[3:2]
MPPC_ADJ[3:2]
LOW_IN_P[3:2]
LOW_IN_N[3:2]
HIGH[3:2]
ANALOG2
MPPC_SIG[5:4]
MPPC_ADJ[5:4]
LOW_IN_P[5:4]
LOW_IN_N[5:4]
HIGH[5:4]
ANALOG3
MPPC_SIG[7:6]
MPPC_ADJ[7:6]
LOW_IN_P[7:6]
LOW_IN_N[7:6]
HIGH[7:6]
LOW_IN_P[7:0]
LOW_IN_N[7:0]
ADCH_IN_P
ADCH_IN_N
ADCH_VCM
配線のインピーダンスを差動100Ωに
+3V0A
C99 0.1U
C100 1U
L4 BLM18PG121SN1D
C101 0.1U
C102 10U
U16 ADG738BRUZ
SCLK
RESET
DIN
SYNC
VDD
D
DOUT
S1
S2
S3
S4
S5
S6
S7
S8
GND
R86 1M
R82 1K
R84 499
R87 499
R89 1K
U17 AD8132ARM
+IN
-IN
-OUT
+OUT
VOCM
V+
V-
NC
-2V3A
C106 0.1U
C107 10U
R83 60.4
R85 200
R88 60.4
C103 20P
C104 0.1U
C105 20P
Title
CHARGE_DIV
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MPPC_SIG[7:0]
MPPC_ADJ[7:0]
MPPC_OFFSET
MP_SCLK
/MP_RESET
MP_DIN
/MP_SYNC

ANALOG0
MPPC_SIG[1:0] → SIG[1:0]
MPPC_ADJ[1:0] → ADJ[1:0]
MPPC_OFFSET → OFFSET
LOW_P[1:0] → LOW_IN_P[1:0]
LOW_N[1:0] → LOW_IN_N[1:0]
HIGH[1:0] → HIGH[1:0]
05_ANALOG

ANALOG1
MPPC_SIG[3:2] → SIG[1:0]
MPPC_ADJ[3:2] → ADJ[1:0]
MPPC_OFFSET → OFFSET
LOW_P[1:0] → LOW_IN_P[3:2]
LOW_N[1:0] → LOW_IN_N[3:2]
HIGH[1:0] → HIGH[3:2]
05_ANALOG

ANALOG2
MPPC_SIG[5:4] → SIG[1:0]
MPPC_ADJ[5:4] → ADJ[1:0]
MPPC_OFFSET → OFFSET
LOW_P[1:0] → LOW_IN_P[5:4]
LOW_N[1:0] → LOW_IN_N[5:4]
HIGH[1:0] → HIGH[5:4]
05_ANALOG

ANALOG3
MPPC_SIG[7:6] → SIG[1:0]
MPPC_ADJ[7:6] → ADJ[1:0]
MPPC_OFFSET → OFFSET
LOW_P[1:0] → LOW_IN_P[7:6]
LOW_N[1:0] → LOW_IN_N[7:6]
HIGH[1:0] → HIGH[7:6]
05_ANALOG

LOW_IN_P[7:0] → LOW_IN_P[7:0]
LOW_IN_N[7:0] → LOW_IN_N[7:0]
ADCH_IN_P → ADCH_IN_P
ADCH_IN_N → ADCH_IN_N
ADCH_VCM → ADCH_VCM

配線のインピーダンスを差動100Ωに

HIGH[7:0]
+3V0A
C108 0.1U
C109 1U
L5 BLM18PG121SN1D
U18 ADG738BRUZ
MP_SCLK 1 → SCLK
/MP_RESET 2 → RESET
MP_DIN 3 → DIN
/MP_SYNC 16 → SYNC
HIGH0 4 → S1
HIGH1 5 → S2
HIGH2 6 → S3
HIGH3 7 → S4
HIGH4 12 → S5
HIGH5 11 → S6
HIGH6 10 → S7
HIGH7 9 → S8
VDD 13
D 8
DOUT 15
GND 14
R94 1M
C110 0.1U
C111 10U
R92 499
R95 499
R90 1K
R97 1K
-2V3A
C115 0.1U
C116 10U
U19 AD8132ARM
+IN 8
-IN 1
-OUT 5
+OUT 4
VOCM 2
V+ 3
V- 6
NC 7
R91 60.4
R96 60.4
R93 200
C112 20P
C113 0.1U
C114 20P
ADCH_IN_N
ADCH_VCM
ADCH_IN_P

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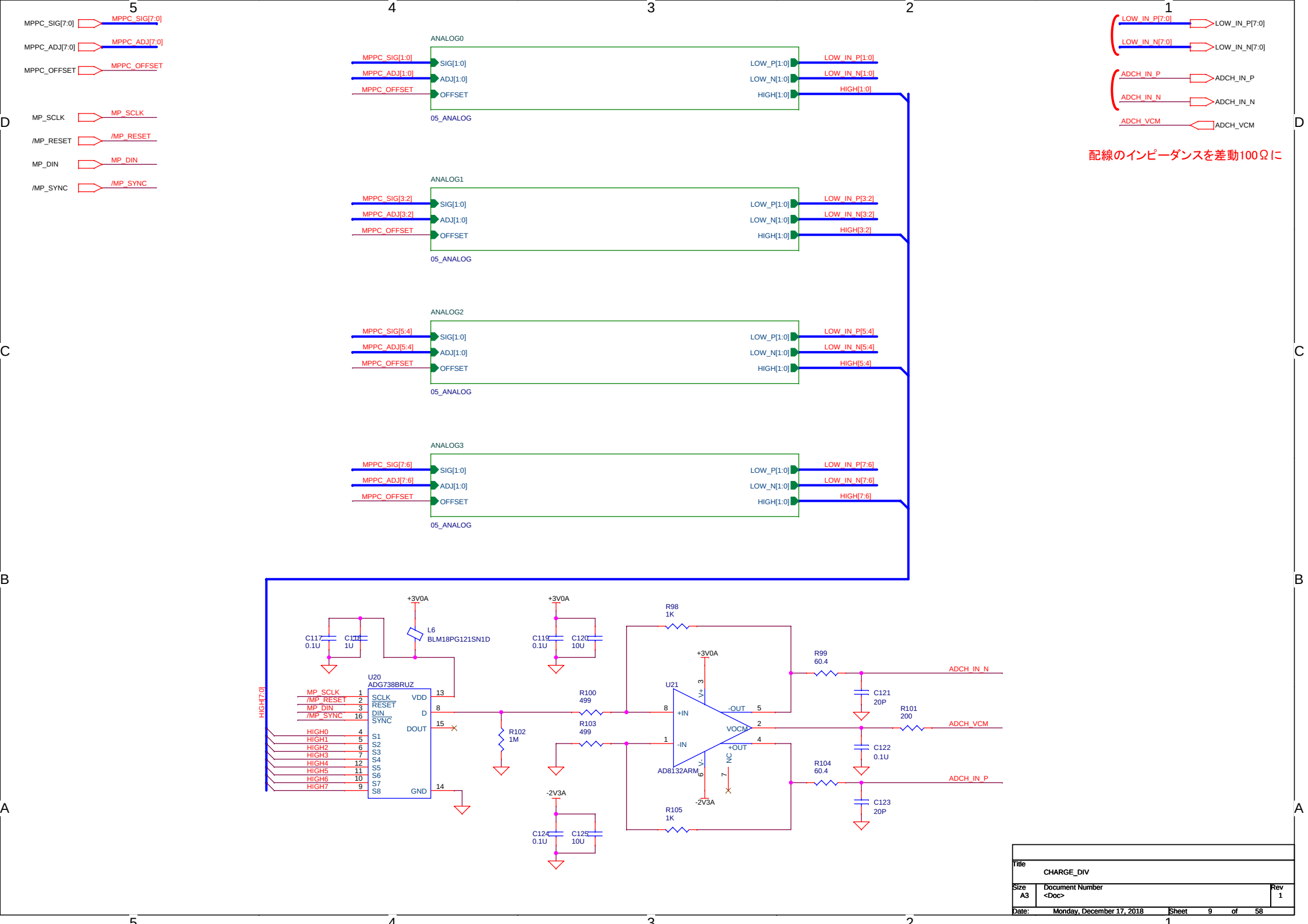
MPPC_SIG[7:0]
MPPC_ADJ[7:0]
MPPC_OFFSET
MP_SCLK
/MP_RESET
MP_DIN
/MP_SYNC
ANALOG0
MPPC_SIG[1:0]
MPPC_ADJ[1:0]
MPPC_OFFSET
SIG[1:0]
ADJ[1:0]
OFFSET
LOW_P[1:0]
LOW_N[1:0]
HIGH[1:0]
LOW_IN_P[1:0]
LOW_IN_N[1:0]
HIGH[1:0]
05_ANALOG
ANALOG1
MPPC_SIG[3:2]
MPPC_ADJ[3:2]
LOW_IN_P[3:2]
LOW_IN_N[3:2]
HIGH[3:2]
ANALOG2
MPPC_SIG[5:4]
MPPC_ADJ[5:4]
LOW_IN_P[5:4]
LOW_IN_N[5:4]
HIGH[5:4]
ANALOG3
MPPC_SIG[7:6]
MPPC_ADJ[7:6]
LOW_IN_P[7:6]
LOW_IN_N[7:6]
HIGH[7:6]
LOW_IN_P[7:0]
LOW_IN_N[7:0]
ADCH_IN_P
ADCH_IN_N
ADCH_VCM
配線のインピーダンスを差動100Ωに
+3V0A
C117
0.1U
C118
1U
L6
BLM18PG121SN1D
C119
0.1U
C120
10U
U20
ADG738BRUZ
SCLK
RESET
DIN
SYNC
VDD
D
DOUT
S1
S2
S3
S4
S5
S6
S7
S8
GND
HIGH0
HIGH1
HIGH2
HIGH3
HIGH4
HIGH5
HIGH6
HIGH7
R102
1M
R100
499
R103
499
R98
1K
R105
1K
U21
AD8132ARM
+IN
-IN
-OUT
+OUT
VOCM
V+
V-
NC
-2V3A
C124
0.1U
C125
10U
R99
60.4
R104
60.4
R101
200
C121
20P
C122
0.1U
C123
20P
Title
CHARGE_DIV
Size
A3
Document Number
<Doc>
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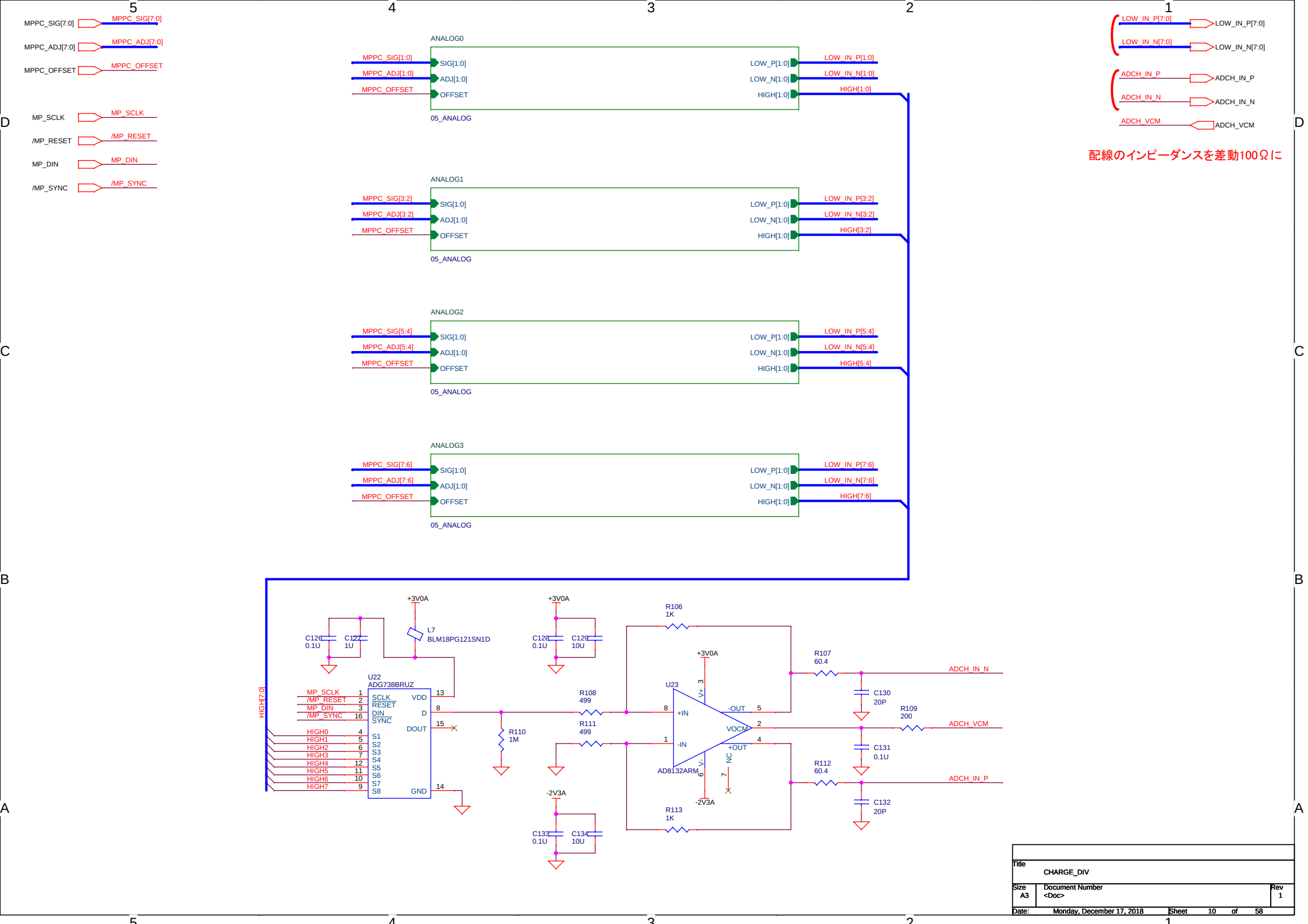

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MPPC_SIG[7:0]
MPPC_ADJ[7:0]
MPPC_OFFSET
MP_SCLK
/MP_RESET
MP_DIN
/MP_SYNC

ANALOG0
MPPC_SIG[1:0] → SIG[1:0]
MPPC_ADJ[1:0] → ADJ[1:0]
MPPC_OFFSET → OFFSET
LOW_P[1:0] → LOW_IN_P[1:0]
LOW_N[1:0] → LOW_IN_N[1:0]
HIGH[1:0] → HIGH[1:0]
05_ANALOG

ANALOG1
MPPC_SIG[3:2] → SIG[1:0]
MPPC_ADJ[3:2] → ADJ[1:0]
MPPC_OFFSET → OFFSET
LOW_P[1:0] → LOW_IN_P[3:2]
LOW_N[1:0] → LOW_IN_N[3:2]
HIGH[1:0] → HIGH[3:2]
05_ANALOG

ANALOG2
MPPC_SIG[5:4] → SIG[1:0]
MPPC_ADJ[5:4] → ADJ[1:0]
MPPC_OFFSET → OFFSET
LOW_P[1:0] → LOW_IN_P[5:4]
LOW_N[1:0] → LOW_IN_N[5:4]
HIGH[1:0] → HIGH[5:4]
05_ANALOG

ANALOG3
MPPC_SIG[7:6] → SIG[1:0]
MPPC_ADJ[7:6] → ADJ[1:0]
MPPC_OFFSET → OFFSET
LOW_P[1:0] → LOW_IN_P[7:6]
LOW_N[1:0] → LOW_IN_N[7:6]
HIGH[1:0] → HIGH[7:6]
05_ANALOG

LOW_IN_P[7:0] → LOW_IN_P[7:0]
LOW_IN_N[7:0] → LOW_IN_N[7:0]
ADCH_IN_P → ADCH_IN_P
ADCH_IN_N → ADCH_IN_N
ADCH_VCM → ADCH_VCM

配線のインピーダンスを差動100Ωに

HIGH[7:0]
+3V0A
C135 0.1U
C136 1U
L8 BLM18PG121SN1D
C137 0.1U
C138 10U
U24 ADG738BRUZ
MP_SCLK 1 SCLK
/MP_RESET 2 RESET
MP_DIN 3 DIN
/MP_SYNC 16 SYNC
VDD 13
D 8
DOUT 15
GND 14
HIGH0 4 S1
HIGH1 5 S2
HIGH2 6 S3
HIGH3 7 S4
HIGH4 12 S5
HIGH5 11 S6
HIGH6 10 S7
HIGH7 9 S8
R118 1M
R114 1K
R116 499
R119 499
R121 1K
U25 AD8132ARM
+IN 3
-IN 6
+OUT 5
-OUT 4
VOCM 2
V+ 8
V- 7
NC 1
-2V3A
C142 0.1U
C143 10U
R115 60.4
R120 60.4
R117 200
C139 20P
C140 0.1U
C141 20P
ADCH_IN_N
ADCH_VCM
ADCH_IN_P

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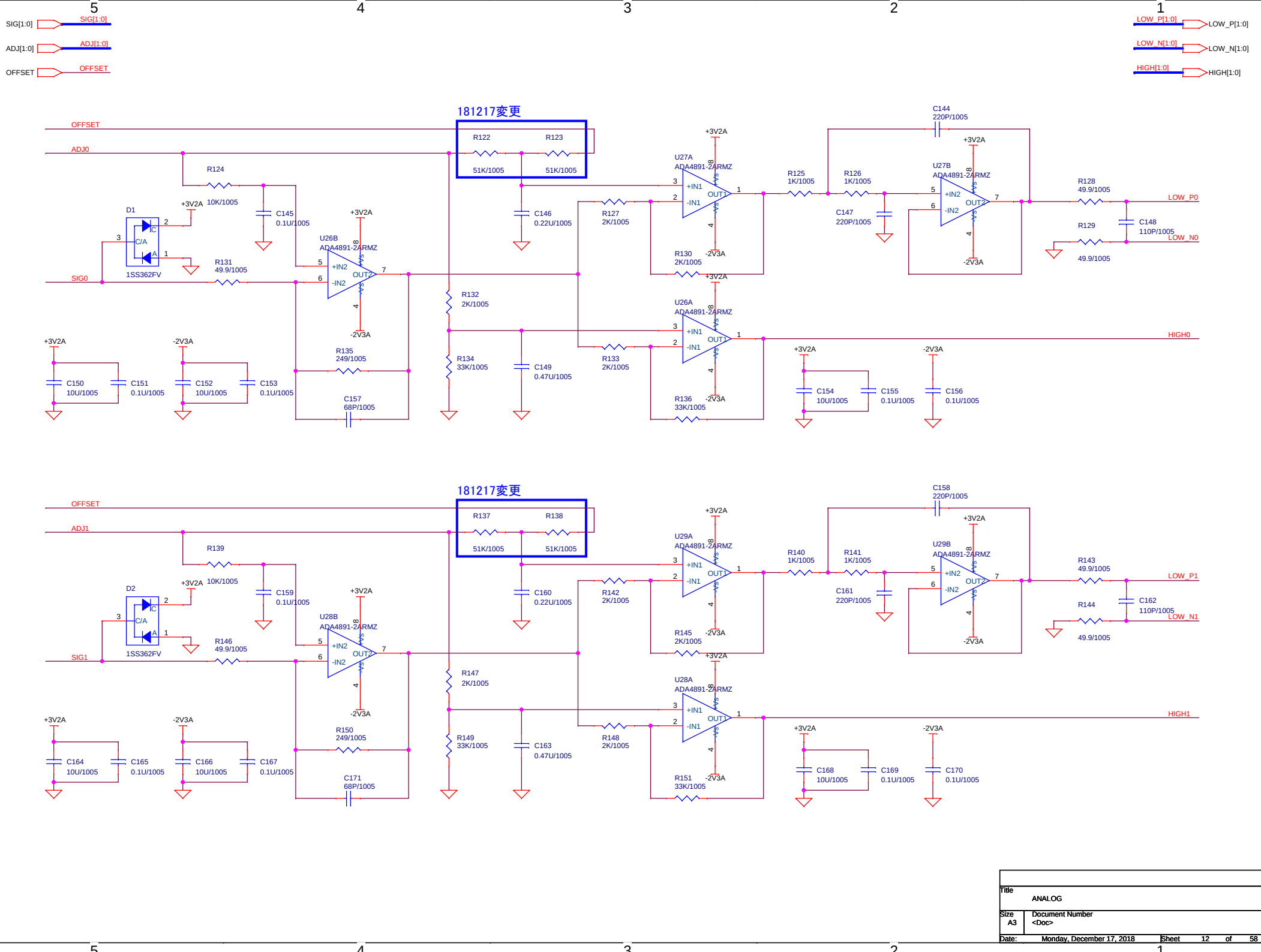
SIG[1:0]
ADJ[1:0]
OFFSET
LOW_P[1:0]
LOW_N[1:0]
HIGH[1:0]
181217变更
R122
R123
51K/1005
R124
10K/1005
D1
1SS362FV
R131
49.9/1005
SIG0
U26B
ADA4891-2ARMZ
R132
2K/1005
R133
2K/1005
R134
33K/1005
R135
249/1005
C157
68P/1005
U27A
ADA4891-2ARMZ
R125
1K/1005
R126
1K/1005
C144
220P/1005
C147
220P/1005
U27B
ADA4891-2ARMZ
R128
49.9/1005
R129
49.9/1005
C148
110P/1005
LOW_P0
LOW_N0
R127
2K/1005
R130
2K/1005
U26A
ADA4891-2ARMZ
R136
33K/1005
HIGH0
C145
0.1U/1005
C146
0.22U/1005
C149
0.47U/1005
C150
10U/1005
C151
0.1U/1005
C152
10U/1005
C153
0.1U/1005
C154
10U/1005
C155
0.1U/1005
C156
0.1U/1005
+3V2A
-2V3A
181217变更
R137
R138
51K/1005
R139
10K/1005
D2
1SS362FV
R146
49.9/1005
SIG1
U28B
ADA4891-2ARMZ
R147
2K/1005
R148
2K/1005
R149
33K/1005
R150
249/1005
C171
68P/1005
U29A
ADA4891-2ARMZ
R140
1K/1005
R141
1K/1005
C158
220P/1005
C161
220P/1005
U29B
ADA4891-2ARMZ
R143
49.9/1005
R144
49.9/1005
C162
110P/1005
LOW_P1
LOW_N1
R142
2K/1005
R145
2K/1005
U28A
ADA4891-2ARMZ
R151
33K/1005
HIGH1
C159
0.1U/1005
C160
0.22U/1005
C163
0.47U/1005
C164
10U/1005
C165
0.1U/1005
C166
10U/1005
C167
0.1U/1005
C168
10U/1005
C169
0.1U/1005
C170
0.1U/1005
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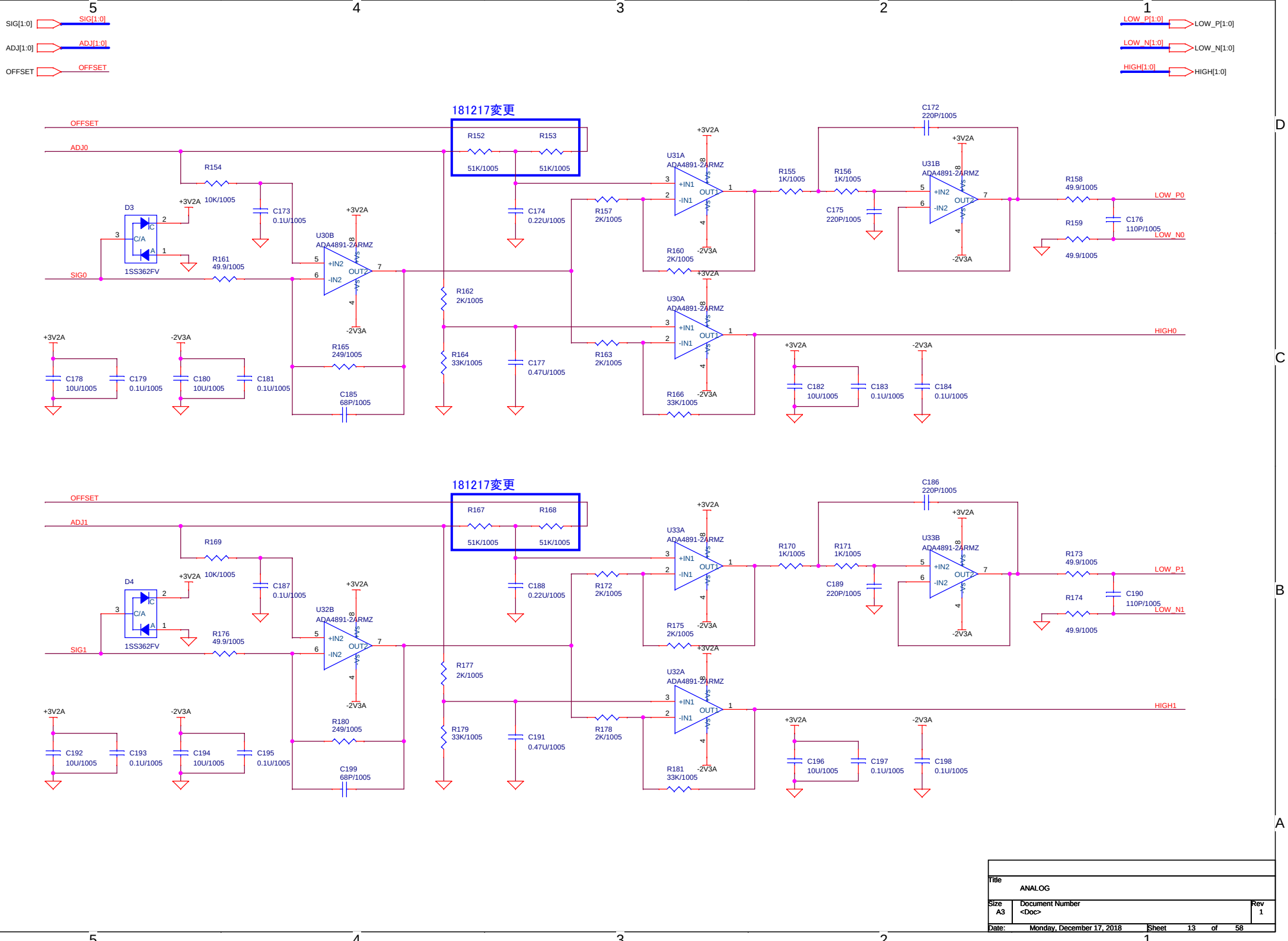
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ADJ[1:0]
OFFSET
LOW_P[1:0]
LOW_N[1:0]
HIGH[1:0]
181217変更
OFFSET
ADJ0
R152
R153
51K/1005
51K/1005
R154
10K/1005
D3
1SS362FV
C173
0.1U/1005
SIG0
R161
49.9/1005
U30B
ADA4891-2ARMZ
R165
249/1005
C185
68P/1005
C174
0.22U/1005
R157
2K/1005
U31A
ADA4891-2ARMZ
R155
1K/1005
R156
1K/1005
C175
220P/1005
C172
220P/1005
U31B
ADA4891-2ARMZ
R158
49.9/1005
R159
49.9/1005
C176
110P/1005
LOW_P0
LOW_N0
R160
2K/1005
R162
2K/1005
R164
33K/1005
C177
0.47U/1005
R163
2K/1005
U30A
ADA4891-2ARMZ
R166
33K/1005
HIGH0
C178
10U/1005
C179
0.1U/1005
C180
10U/1005
C181
0.1U/1005
C182
10U/1005
C183
0.1U/1005
C184
0.1U/1005
+3V2A
-2V3A
181217変更
OFFSET
ADJ1
R167
R168
51K/1005
51K/1005
R169
10K/1005
D4
1SS362FV
C187
0.1U/1005
SIG1
R176
49.9/1005
U32B
ADA4891-2ARMZ
R180
249/1005
C199
68P/1005
C188
0.22U/1005
R172
2K/1005
U33A
ADA4891-2ARMZ
R170
1K/1005
R171
1K/1005
C189
220P/1005
C186
220P/1005
U33B
ADA4891-2ARMZ
R173
49.9/1005
R174
49.9/1005
C190
110P/1005
LOW_P1
LOW_N1
R175
2K/1005
R177
2K/1005
R179
33K/1005
C191
0.47U/1005
R178
2K/1005
U32A
ADA4891-2ARMZ
R181
33K/1005
HIGH1
C192
10U/1005
C193
0.1U/1005
C194
10U/1005
C195
0.1U/1005
C196
10U/1005
C197
0.1U/1005
C198
0.1U/1005
+3V2A
-2V3A
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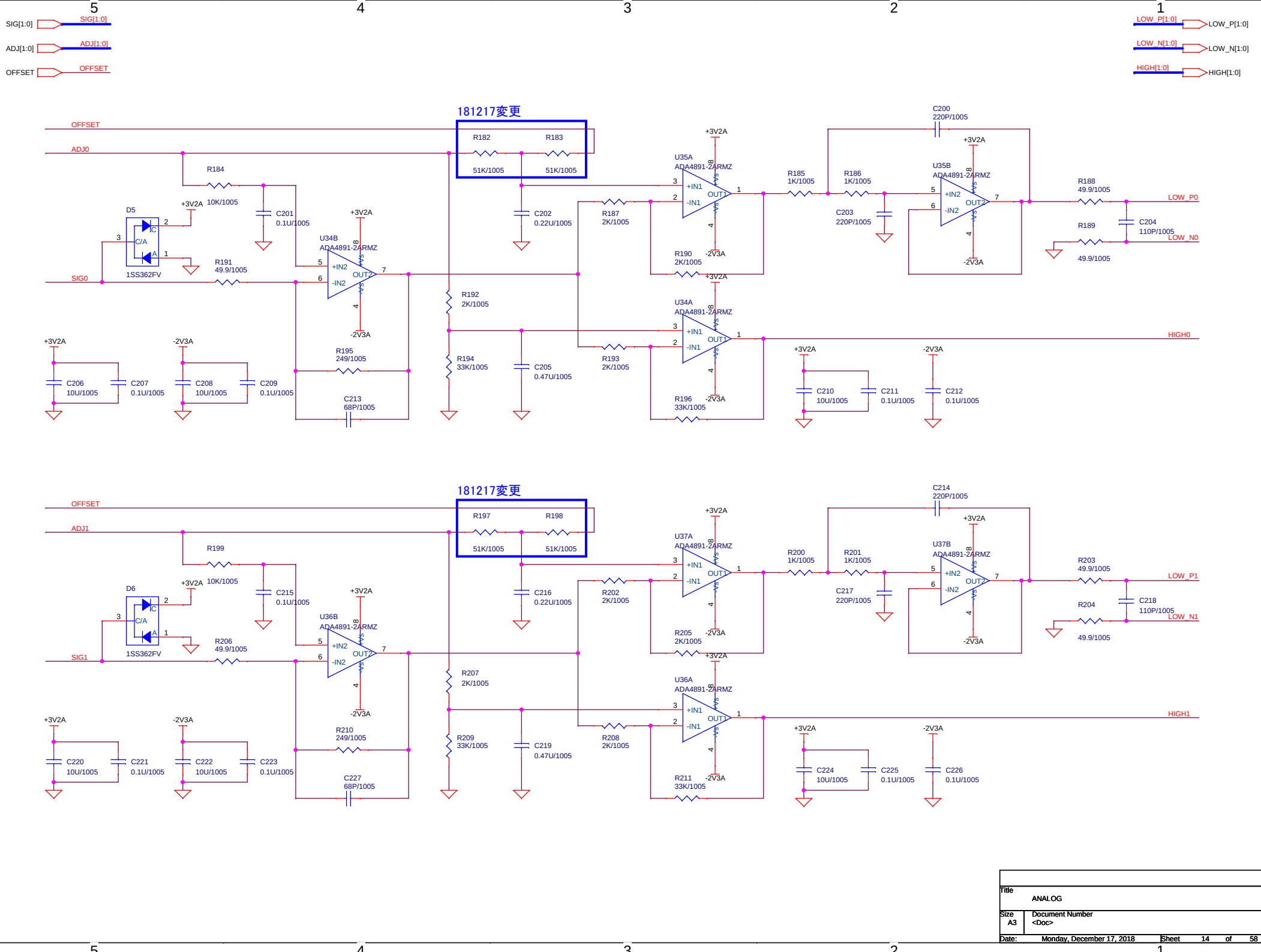
SIG[1:0]
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OFFSET
LOW_P[1:0]
LOW_N[1:0]
HIGH[1:0]
181217变更
OFFSET
ADJ0
SIG0
R182
R183
51K/1005
R184
10K/1005
D5
1SS362FV
C201
0.1U/1005
R191
49.9/1005
U34B
ADA4891-2ARMZ
R192
2K/1005
R194
33K/1005
C205
0.47U/1005
R195
249/1005
C213
68P/1005
C206
10U/1005
C207
0.1U/1005
C208
10U/1005
C209
0.1U/1005
C202
0.22U/1005
R187
2K/1005
U35A
ADA4891-2ARMZ
R190
2K/1005
U34A
ADA4891-2ARMZ
R193
2K/1005
R196
33K/1005
R185
1K/1005
R186
1K/1005
C203
220P/1005
C200
220P/1005
U35B
ADA4891-2ARMZ
R188
49.9/1005
R189
49.9/1005
C204
110P/1005
LOW_P0
LOW_N0
HIGH0
C210
10U/1005
C211
0.1U/1005
C212
0.1U/1005
+3V2A
-2V3A
181217变更
OFFSET
ADJ1
SIG1
R197
R198
51K/1005
R199
10K/1005
D6
1SS362FV
C215
0.1U/1005
R206
49.9/1005
U36B
ADA4891-2ARMZ
R207
2K/1005
R209
33K/1005
C219
0.47U/1005
R210
249/1005
C227
68P/1005
C220
10U/1005
C221
0.1U/1005
C222
10U/1005
C223
0.1U/1005
C216
0.22U/1005
R202
2K/1005
U37A
ADA4891-2ARMZ
R205
2K/1005
U36A
ADA4891-2ARMZ
R208
2K/1005
R211
33K/1005
R200
1K/1005
R201
1K/1005
C217
220P/1005
C214
220P/1005
U37B
ADA4891-2ARMZ
R203
49.9/1005
R204
49.9/1005
C218
110P/1005
LOW_P1
LOW_N1
HIGH1
C224
10U/1005
C225
0.1U/1005
C226
0.1U/1005
+3V2A
-2V3A
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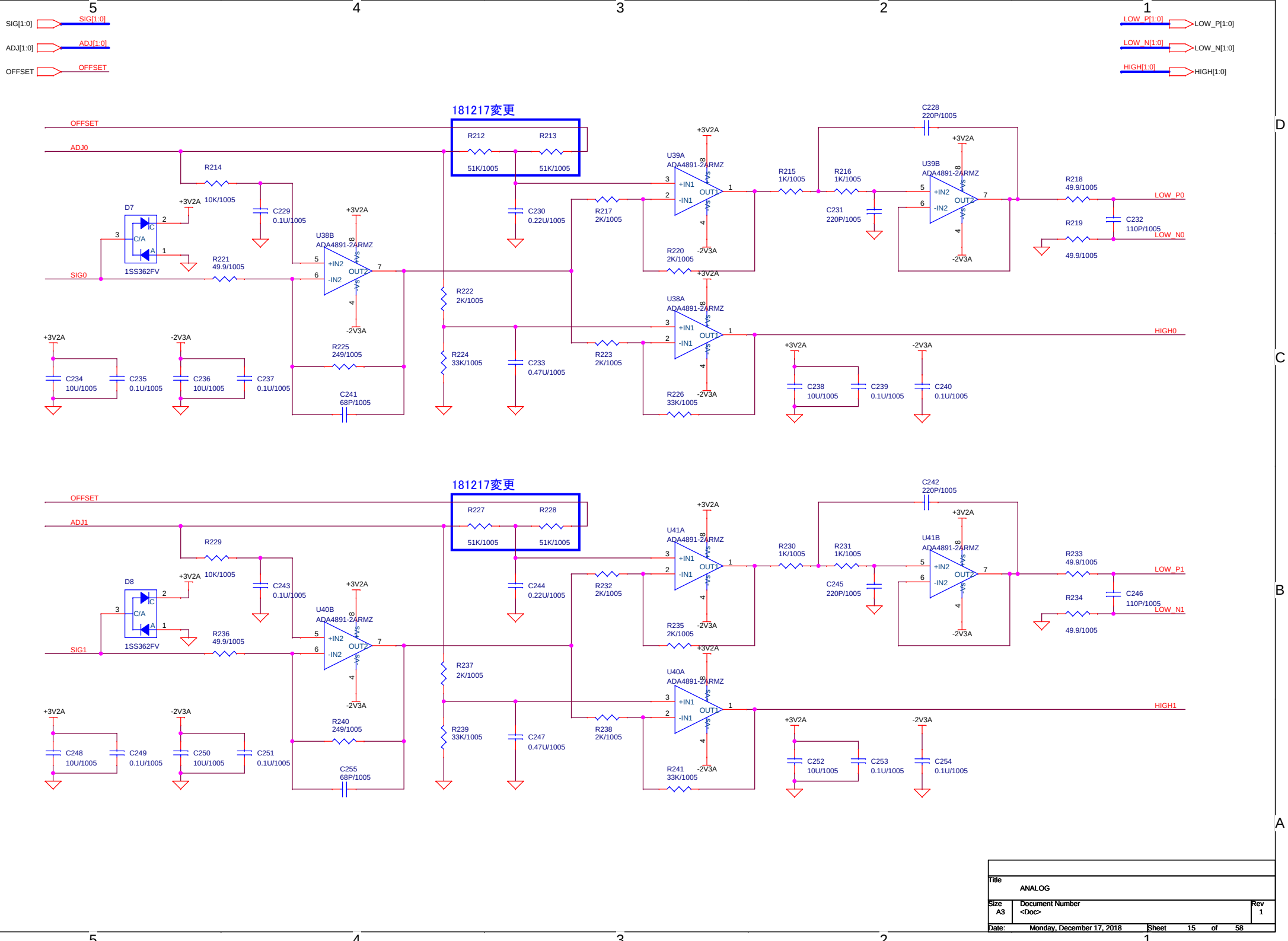

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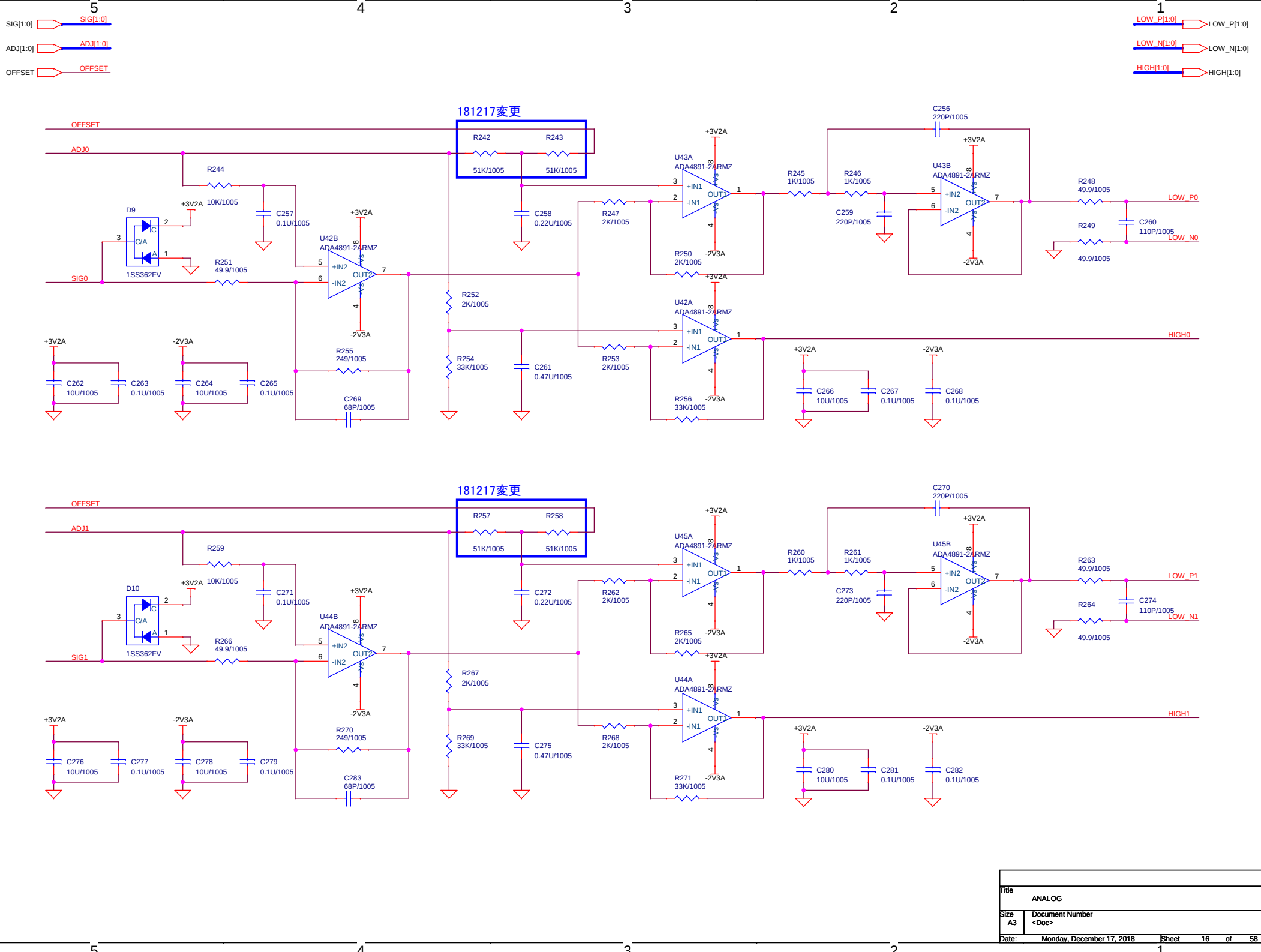
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ADJ[1:0]
OFFSET
LOW_P[1:0]
LOW_N[1:0]
HIGH[1:0]
181217变更
OFFSET
ADJ0
SIG0
R242
R243
51K/1005
R244
10K/1005
D9
1SS362FV
R251
49.9/1005
C257
0.1U/1005
U42B
ADA4891-2ARMZ
R252
2K/1005
R254
33K/1005
C261
0.47U/1005
R253
2K/1005
U43A
ADA4891-2ARMZ
R250
2K/1005
R245
1K/1005
R246
1K/1005
C259
220P/1005
C256
220P/1005
U43B
ADA4891-2ARMZ
R248
49.9/1005
R249
49.9/1005
C260
110P/1005
LOW_P0
LOW_N0
C258
0.22U/1005
R247
2K/1005
U42A
ADA4891-2ARMZ
R256
33K/1005
HIGH0
R255
249/1005
C269
68P/1005
C262
10U/1005
C263
0.1U/1005
C264
10U/1005
C265
0.1U/1005
C266
10U/1005
C267
0.1U/1005
C268
0.1U/1005
+3V2A
-2V3A
181217变更
OFFSET
ADJ1
SIG1
R257
R258
51K/1005
R259
10K/1005
D10
1SS362FV
R266
49.9/1005
C271
0.1U/1005
U44B
ADA4891-2ARMZ
R267
2K/1005
R269
33K/1005
C275
0.47U/1005
R268
2K/1005
U45A
ADA4891-2ARMZ
R265
2K/1005
R260
1K/1005
R261
1K/1005
C273
220P/1005
C270
220P/1005
U45B
ADA4891-2ARMZ
R263
49.9/1005
R264
49.9/1005
C274
110P/1005
LOW_P1
LOW_N1
C272
0.22U/1005
R262
2K/1005
U44A
ADA4891-2ARMZ
R271
33K/1005
HIGH1
R270
249/1005
C283
68P/1005
C276
10U/1005
C277
0.1U/1005
C278
10U/1005
C279
0.1U/1005
C280
10U/1005
C281
0.1U/1005
C282
0.1U/1005
+3V2A
-2V3A
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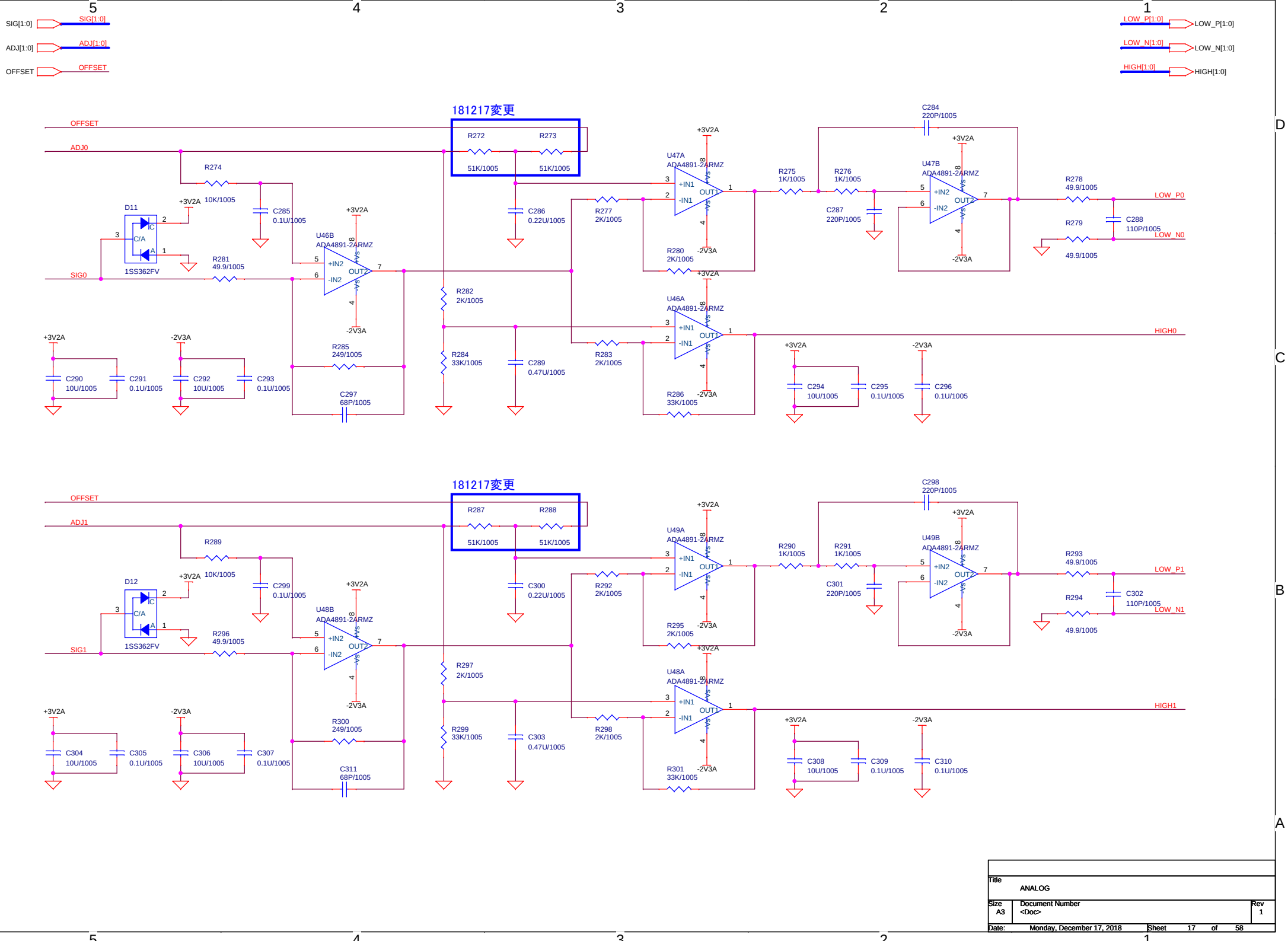

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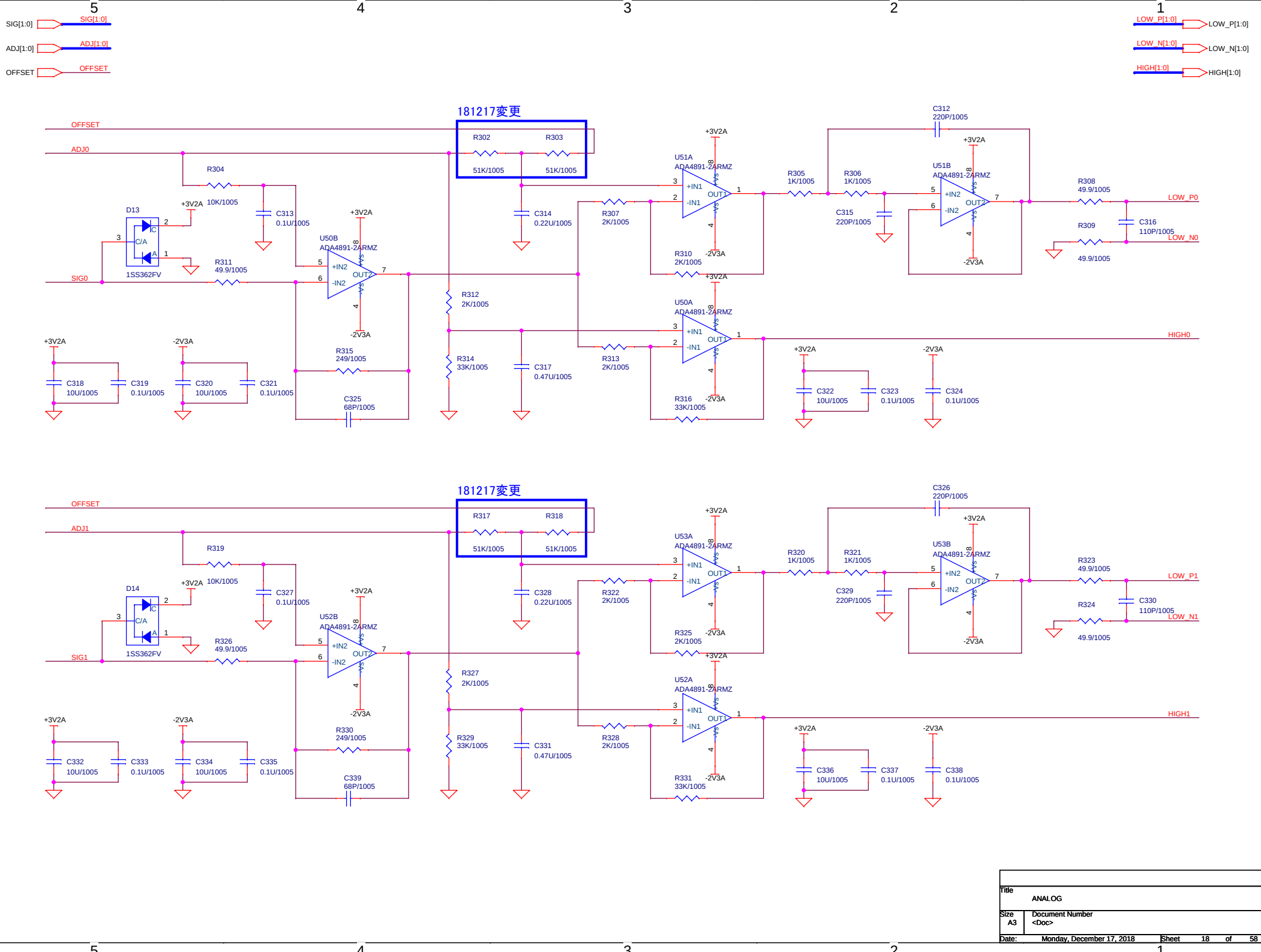
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ADJ[1:0]
OFFSET
LOW_P[1:0]
LOW_N[1:0]
HIGH[1:0]
181217变更
R302
R303
51K/1005
R304
10K/1005
D13
1SS362FV
R311
49.9/1005
U50B
ADA4891-2ARMZ
U50A
U51A
U51B
R305
1K/1005
R306
1K/1005
C312
220P/1005
C315
220P/1005
R307
2K/1005
R308
49.9/1005
R309
C316
110P/1005
R310
2K/1005
R312
2K/1005
R313
2K/1005
R314
33K/1005
R315
249/1005
R316
33K/1005
C313
0.1U/1005
C314
0.22U/1005
C317
0.47U/1005
C318
10U/1005
C319
0.1U/1005
C320
10U/1005
C321
0.1U/1005
C322
10U/1005
C323
0.1U/1005
C324
0.1U/1005
C325
68P/1005
+3V2A
-2V3A
OFFSET
ADJ0
SIG0
LOW_P0
LOW_N0
HIGH0
181217变更
R317
R318
51K/1005
R319
10K/1005
D14
1SS362FV
R326
49.9/1005
U52B
ADA4891-2ARMZ
U52A
U53A
U53B
R320
1K/1005
R321
1K/1005
C326
220P/1005
C329
220P/1005
R322
2K/1005
R323
49.9/1005
R324
C330
110P/1005
R325
2K/1005
R327
2K/1005
R328
2K/1005
R329
33K/1005
R330
249/1005
R331
33K/1005
C327
0.1U/1005
C328
0.22U/1005
C331
0.47U/1005
C332
10U/1005
C333
0.1U/1005
C334
10U/1005
C335
0.1U/1005
C336
10U/1005
C337
0.1U/1005
C338
0.1U/1005
C339
68P/1005
OFFSET
ADJ1
SIG1
LOW_P1
LOW_N1
HIGH1
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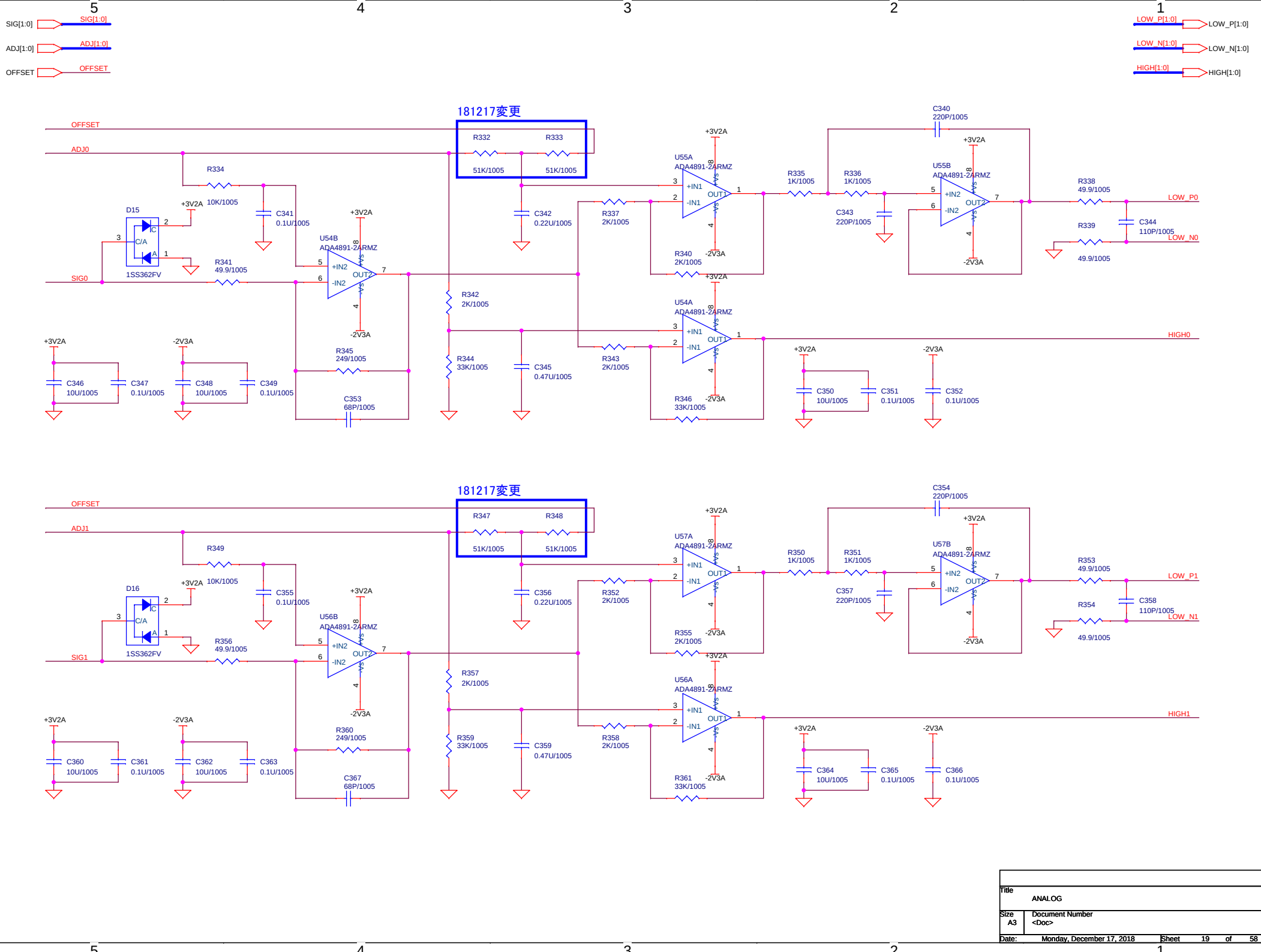
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ADJ[1:0]
OFFSET
LOW_P[1:0]
LOW_N[1:0]
HIGH[1:0]
181217変更
OFFSET
ADJ0
SIG0
R332 51K/1005
R333 51K/1005
R334 10K/1005
D15
1SS362FV
R341 49.9/1005
C341 0.1U/1005
U54B ADA4891-2ARMZ
R342 2K/1005
R344 33K/1005
C345 0.47U/1005
R345 249/1005
C353 68P/1005
C342 0.22U/1005
R337 2K/1005
U55A ADA4891-2ARMZ
R340 2K/1005
R335 1K/1005
R336 1K/1005
C343 220P/1005
C340 220P/1005
U55B ADA4891-2ARMZ
R338 49.9/1005
R339 49.9/1005
C344 110P/1005
LOW_P0
LOW_N0
U54A ADA4891-2ARMZ
R343 2K/1005
R346 33K/1005
HIGH0
C346 10U/1005
C347 0.1U/1005
C348 10U/1005
C349 0.1U/1005
C350 10U/1005
C351 0.1U/1005
C352 0.1U/1005
+3V2A
-2V3A
181217変更
OFFSET
ADJ1
SIG1
R347 51K/1005
R348 51K/1005
R349 10K/1005
D16
1SS362FV
R356 49.9/1005
C355 0.1U/1005
U56B ADA4891-2ARMZ
R357 2K/1005
R359 33K/1005
C359 0.47U/1005
R360 249/1005
C367 68P/1005
C356 0.22U/1005
R352 2K/1005
U57A ADA4891-2ARMZ
R355 2K/1005
R350 1K/1005
R351 1K/1005
C357 220P/1005
C354 220P/1005
U57B ADA4891-2ARMZ
R353 49.9/1005
R354 49.9/1005
C358 110P/1005
LOW_P1
LOW_N1
U56A ADA4891-2ARMZ
R358 2K/1005
R361 33K/1005
HIGH1
C360 10U/1005
C361 0.1U/1005
C362 10U/1005
C363 0.1U/1005
C364 10U/1005
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C366 0.1U/1005
+3V2A
-2V3A
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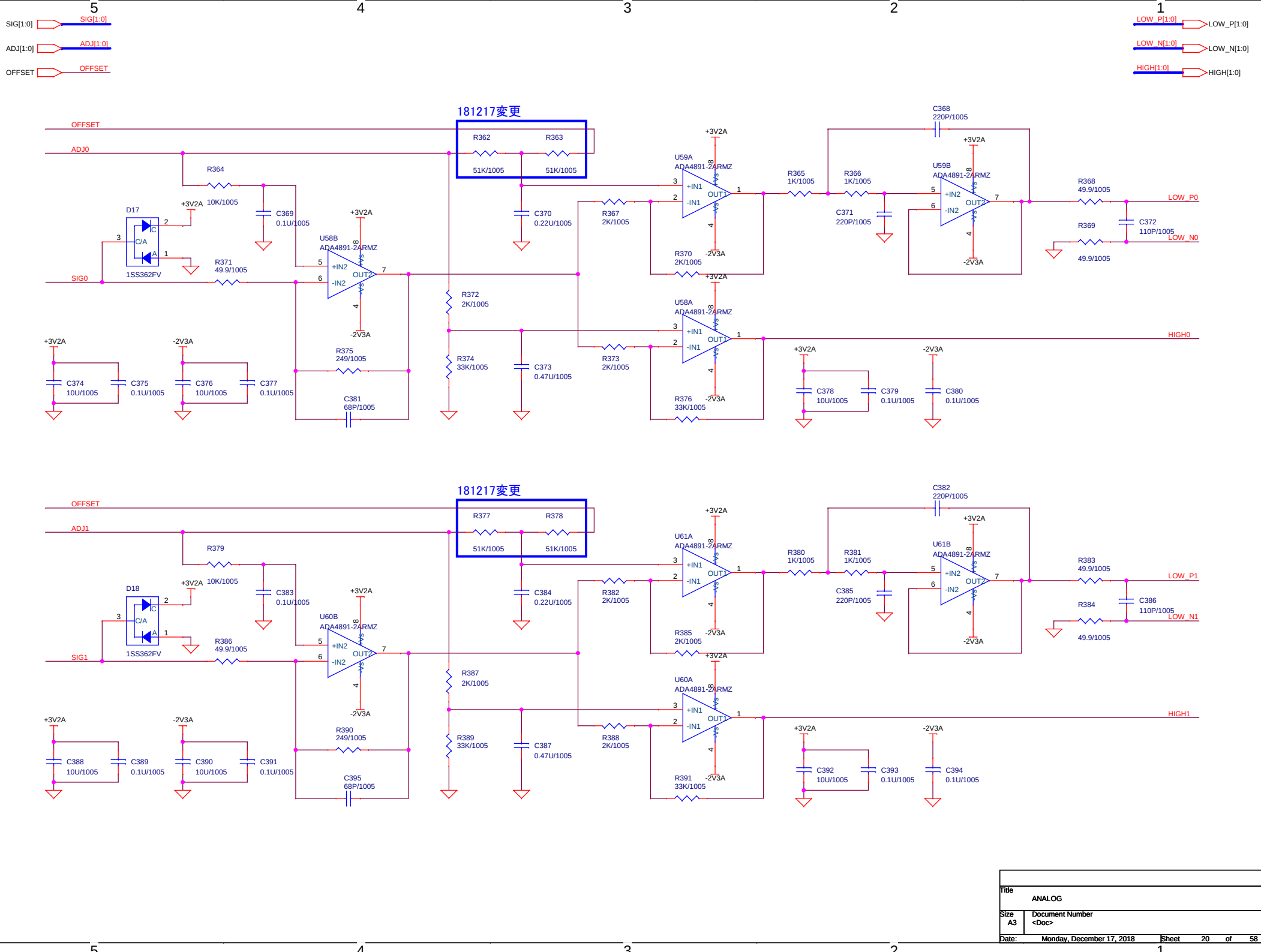
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ADJ[1:0]
OFFSET
LOW_P[1:0]
LOW_N[1:0]
HIGH[1:0]
181217变更
OFFSET
ADJ0
SIG0
R362
R363
51K/1005
R364
10K/1005
D17
1SS362FV
R371
49.9/1005
C369
0.1U/1005
U58B
ADA4891-2ARMZ
R372
2K/1005
R374
33K/1005
C373
0.47U/1005
C370
0.22U/1005
R367
2K/1005
U59A
ADA4891-2ARMZ
R365
1K/1005
R366
1K/1005
C371
220P/1005
C368
220P/1005
U59B
ADA4891-2ARMZ
R368
49.9/1005
R369
49.9/1005
C372
110P/1005
LOW_P0
LOW_N0
R370
2K/1005
U58A
ADA4891-2ARMZ
R373
2K/1005
R376
33K/1005
HIGH0
R375
249/1005
C381
68P/1005
C374
10U/1005
C375
0.1U/1005
C376
10U/1005
C377
0.1U/1005
C378
10U/1005
C379
0.1U/1005
C380
0.1U/1005
+3V2A
-2V3A
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R377
R378
51K/1005
R379
10K/1005
D18
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49.9/1005
C383
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R387
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0.22U/1005
R382
2K/1005
U61A
ADA4891-2ARMZ
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1K/1005
R381
1K/1005
C385
220P/1005
C382
220P/1005
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ADA4891-2ARMZ
R383
49.9/1005
R384
49.9/1005
C386
110P/1005
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LOW_N1
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2K/1005
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ADA4891-2ARMZ
R388
2K/1005
R391
33K/1005
HIGH1
R390
249/1005
C395
68P/1005
C388
10U/1005
C389
0.1U/1005
C390
10U/1005
C391
0.1U/1005
C392
10U/1005
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C394
0.1U/1005
+3V2A
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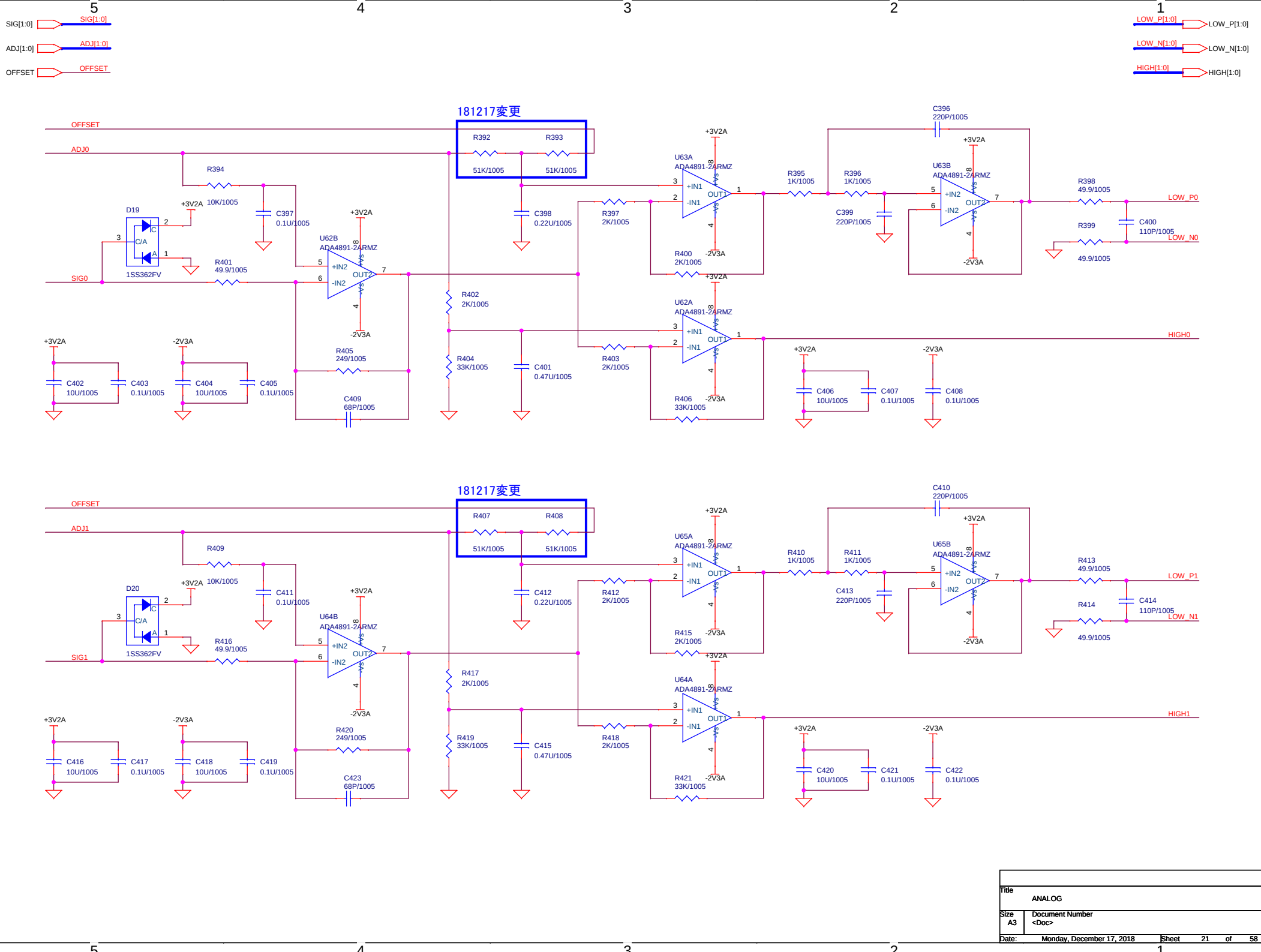

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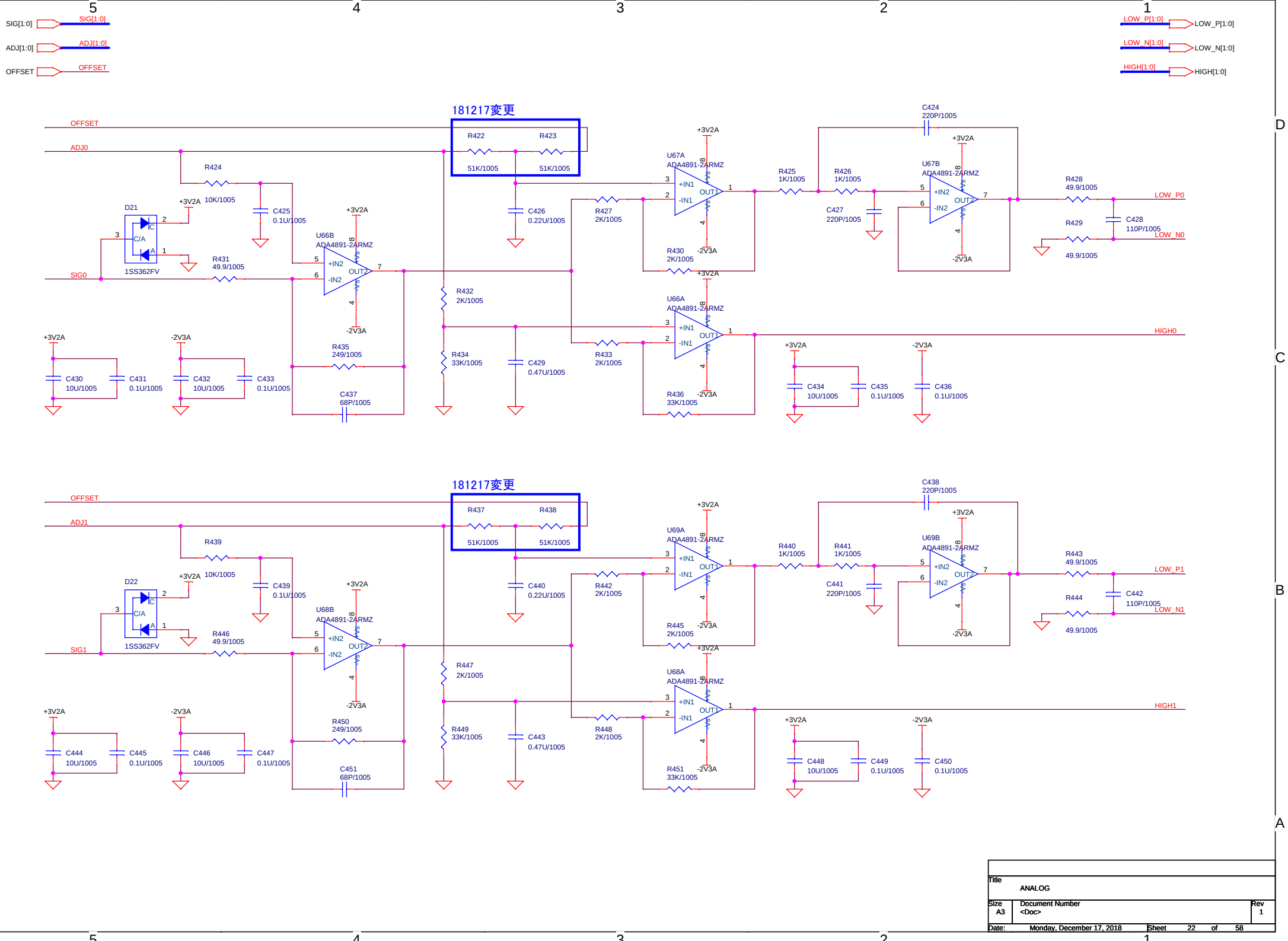
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R423 51K/1005
R424 10K/1005
D21 1SS362FV
C425 0.1U/1005
R431 49.9/1005
U66B ADA4891-2ARMZ
R432 2K/1005
R433 2K/1005
R434 33K/1005
C426 0.22U/1005
C429 0.47U/1005
R435 249/1005
C437 68P/1005
U67A ADA4891-2ARMZ
R425 1K/1005
R426 1K/1005
C427 220P/1005
R427 2K/1005
R430 2K/1005
C424 220P/1005
U67B ADA4891-2ARMZ
R428 49.9/1005
R429 49.9/1005
C428 110P/1005
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LOW_N0
U66A ADA4891-2ARMZ
HIGH0
R436 33K/1005
C430 10U/1005
C431 0.1U/1005
C432 10U/1005
C433 0.1U/1005
C434 10U/1005
C435 0.1U/1005
C436 0.1U/1005
+3V2A
-2V3A
181217变更
OFFSET
ADJ1
SIG1
R437 51K/1005
R438 51K/1005
R439 10K/1005
D22 1SS362FV
C439 0.1U/1005
R446 49.9/1005
U68B ADA4891-2ARMZ
R447 2K/1005
R448 2K/1005
R449 33K/1005
C440 0.22U/1005
C443 0.47U/1005
R450 249/1005
C451 68P/1005
U69A ADA4891-2ARMZ
R440 1K/1005
R441 1K/1005
C441 220P/1005
R442 2K/1005
R445 2K/1005
C438 220P/1005
U69B ADA4891-2ARMZ
R443 49.9/1005
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C442 110P/1005
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LOW_N1
U68A ADA4891-2ARMZ
HIGH1
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C444 10U/1005
C445 0.1U/1005
C446 10U/1005
C447 0.1U/1005
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C449 0.1U/1005
C450 0.1U/1005
+3V2A
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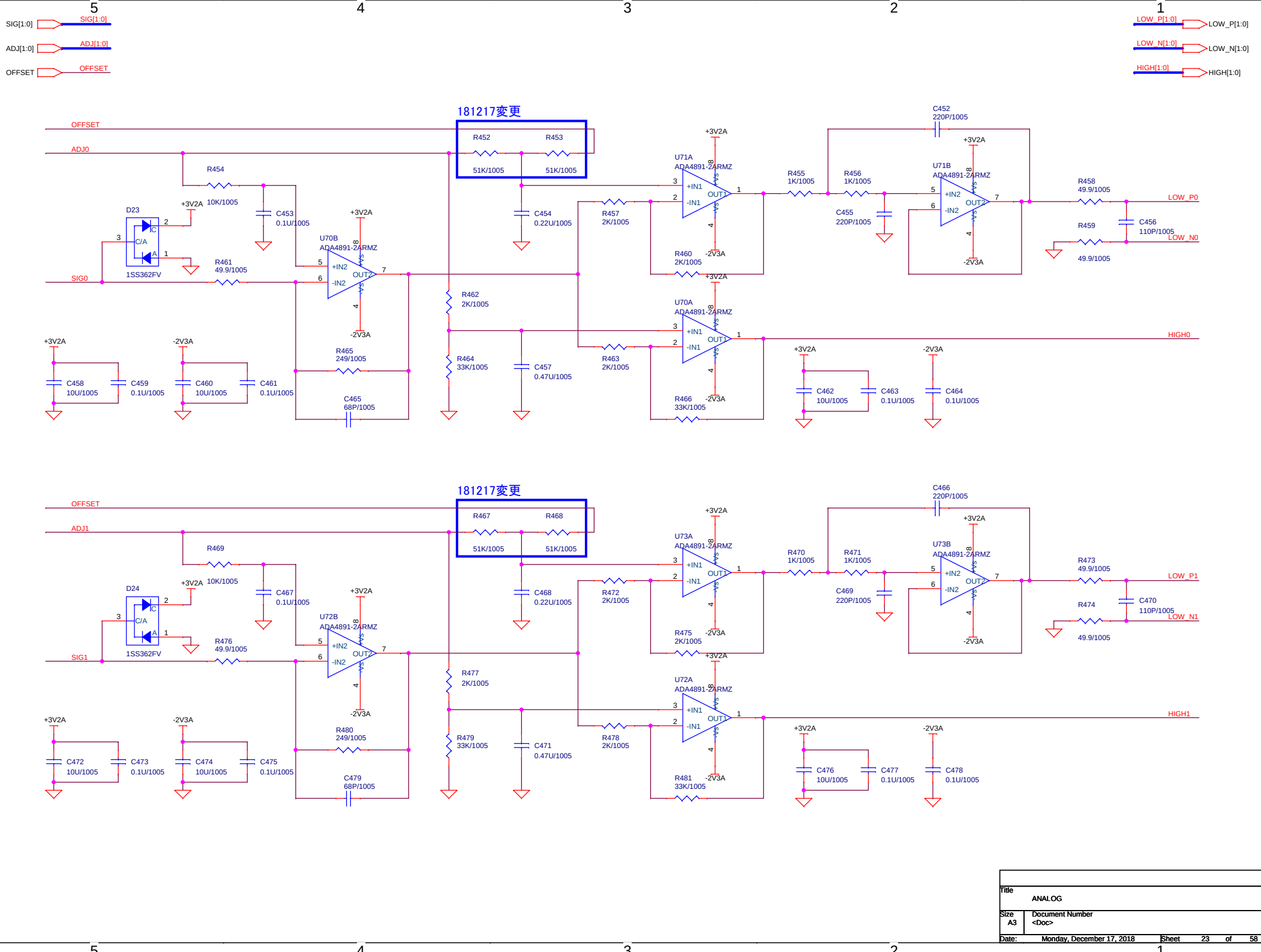

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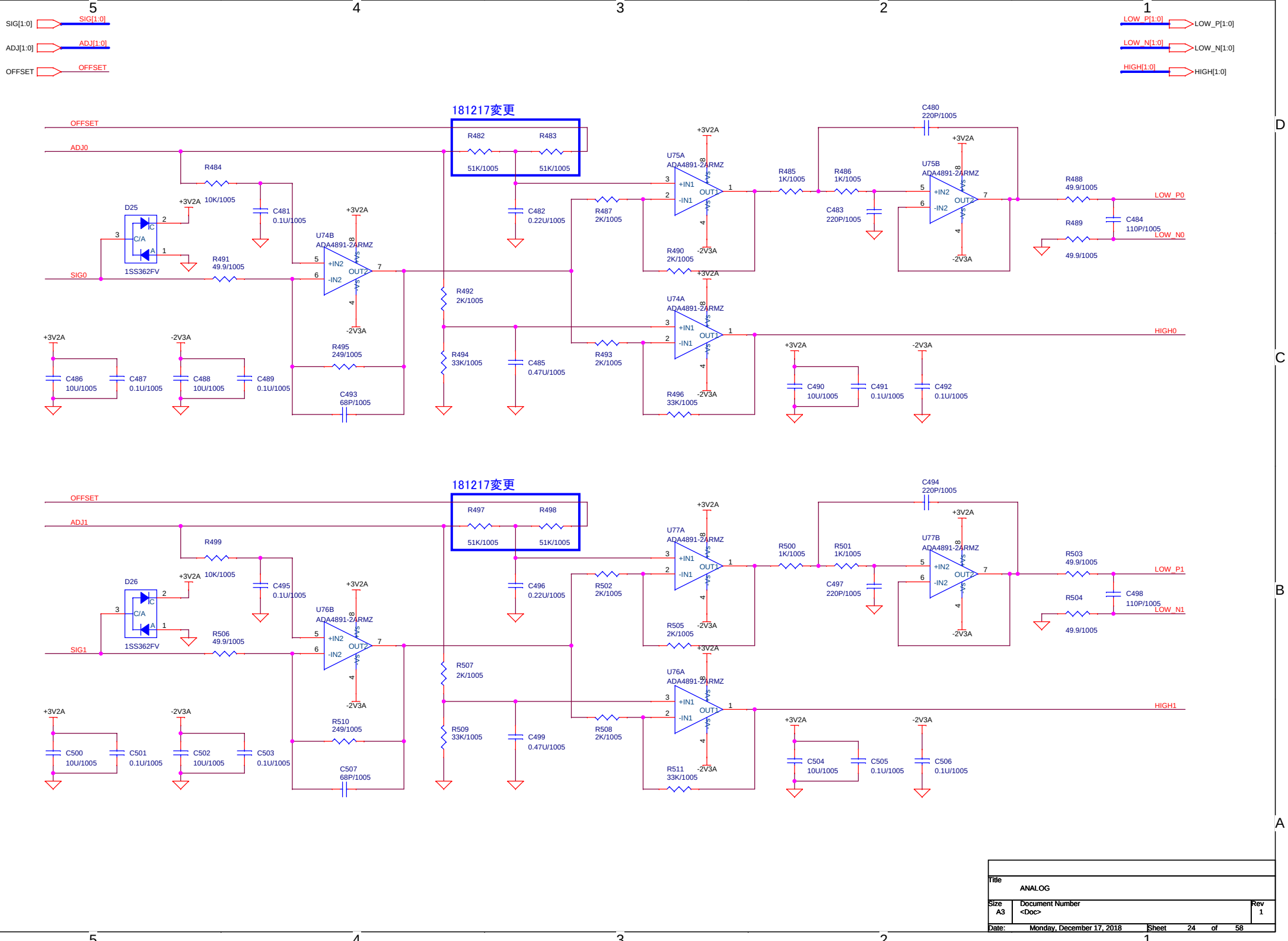
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R484
10K/1005
C481
0.1U/1005
D25
1SS362FV
R491
49.9/1005
U74B
ADA4891-2ARMZ
R495
249/1005
C493
68P/1005
C482
0.22U/1005
R487
2K/1005
U75A
ADA4891-2ARMZ
R485
1K/1005
R486
1K/1005
C483
220P/1005
C480
220P/1005
U75B
ADA4891-2ARMZ
R488
49.9/1005
R489
49.9/1005
C484
110P/1005
LOW_P0
LOW_N0
R490
2K/1005
R492
2K/1005
R494
33K/1005
C485
0.47U/1005
U74A
ADA4891-2ARMZ
R493
2K/1005
R496
33K/1005
HIGH0
C486
10U/1005
C487
0.1U/1005
C488
10U/1005
C489
0.1U/1005
C490
10U/1005
C491
0.1U/1005
C492
0.1U/1005
+3V2A
-2V3A
181217变更
R497
R498
51K/1005
R499
10K/1005
C495
0.1U/1005
D26
1SS362FV
R506
49.9/1005
U76B
ADA4891-2ARMZ
R510
249/1005
C507
68P/1005
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0.22U/1005
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2K/1005
U77A
ADA4891-2ARMZ
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1K/1005
R501
1K/1005
C497
220P/1005
C494
220P/1005
U77B
ADA4891-2ARMZ
R503
49.9/1005
R504
49.9/1005
C498
110P/1005
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LOW_N1
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2K/1005
R507
2K/1005
R509
33K/1005
C499
0.47U/1005
U76A
ADA4891-2ARMZ
R508
2K/1005
R511
33K/1005
HIGH1
C500
10U/1005
C501
0.1U/1005
C502
10U/1005
C503
0.1U/1005
C504
10U/1005
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0.1U/1005
C506
0.1U/1005
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ADJ1
SIG0
SIG1
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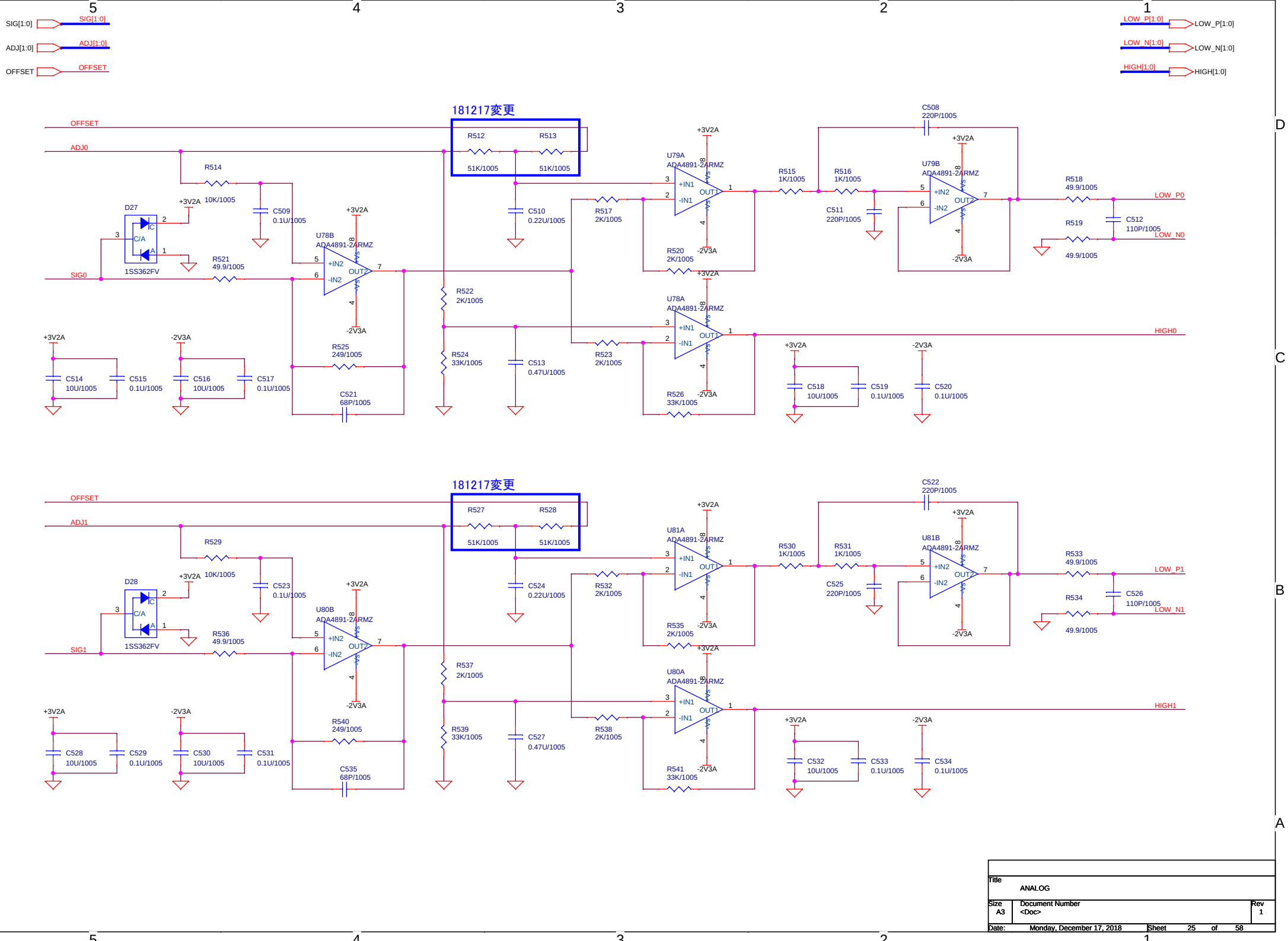
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51K/1005
R514
10K/1005
D27
1SS362FV
R521
49.9/1005
C509
0.1U/1005
U78B
ADA4891-2ARMZ
R522
2K/1005
R524
33K/1005
C513
0.47U/1005
R525
249/1005
C521
68P/1005
C510
0.22U/1005
R517
2K/1005
U79A
ADA4891-2ARMZ
R520
2K/1005
U78A
ADA4891-2ARMZ
R523
2K/1005
R526
33K/1005
R515
1K/1005
R516
1K/1005
C511
220P/1005
C508
220P/1005
U79B
ADA4891-2ARMZ
R518
49.9/1005
R519
49.9/1005
C512
110P/1005
LOW_P0
LOW_N0
HIGH0
C514
10U/1005
C515
0.1U/1005
C516
10U/1005
C517
0.1U/1005
C518
10U/1005
C519
0.1U/1005
C520
0.1U/1005
+3V2A
-2V3A
181217変更
OFFSET
ADJ1
SIG1
R527
R528
51K/1005
R529
10K/1005
D28
1SS362FV
R536
49.9/1005
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0.1U/1005
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R537
2K/1005
R539
33K/1005
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0.47U/1005
R540
249/1005
C535
68P/1005
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0.22U/1005
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2K/1005
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ADA4891-2ARMZ
R535
2K/1005
U80A
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R538
2K/1005
R541
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C522
220P/1005
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ADA4891-2ARMZ
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49.9/1005
R534
49.9/1005
C526
110P/1005
LOW_P1
LOW_N1
HIGH1
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10U/1005
C529
0.1U/1005
C530
10U/1005
C531
0.1U/1005
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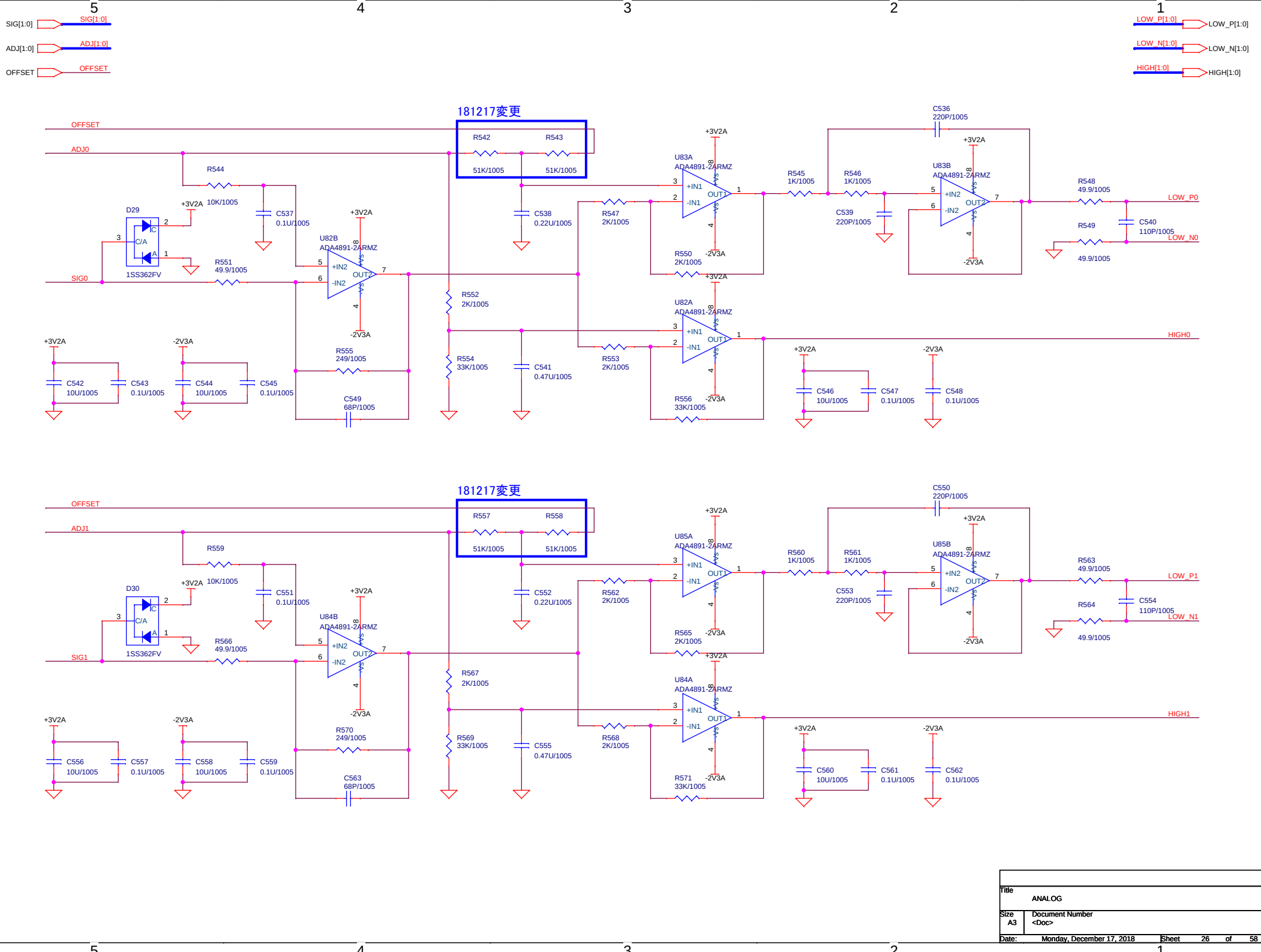
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10K/1005
D29
1SS362FV
C537
0.1U/1005
R551
49.9/1005
U82B
ADA4891-2ARMZ
R555
249/1005
C549
68P/1005
C538
0.22U/1005
R547
2K/1005
U83A
ADA4891-2ARMZ
R545
1K/1005
R546
1K/1005
C539
220P/1005
C536
220P/1005
U83B
ADA4891-2ARMZ
R548
49.9/1005
R549
49.9/1005
C540
110P/1005
LOW_P0
LOW_N0
R550
2K/1005
R552
2K/1005
R554
33K/1005
C541
0.47U/1005
R553
2K/1005
U82A
ADA4891-2ARMZ
R556
33K/1005
HIGH0
C542
10U/1005
C543
0.1U/1005
C544
10U/1005
C545
0.1U/1005
C546
10U/1005
C547
0.1U/1005
C548
0.1U/1005
+3V2A
-2V3A
181217变更
OFFSET
ADJ1
SIG1
R557
R558
51K/1005
R559
10K/1005
D30
1SS362FV
C551
0.1U/1005
R566
49.9/1005
U84B
ADA4891-2ARMZ
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249/1005
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68P/1005
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0.22U/1005
R562
2K/1005
U85A
ADA4891-2ARMZ
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1K/1005
R561
1K/1005
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220P/1005
C550
220P/1005
U85B
ADA4891-2ARMZ
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49.9/1005
R564
49.9/1005
C554
110P/1005
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LOW_N1
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2K/1005
R567
2K/1005
R569
33K/1005
C555
0.47U/1005
R568
2K/1005
U84A
ADA4891-2ARMZ
R571
33K/1005
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C556
10U/1005
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0.1U/1005
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10U/1005
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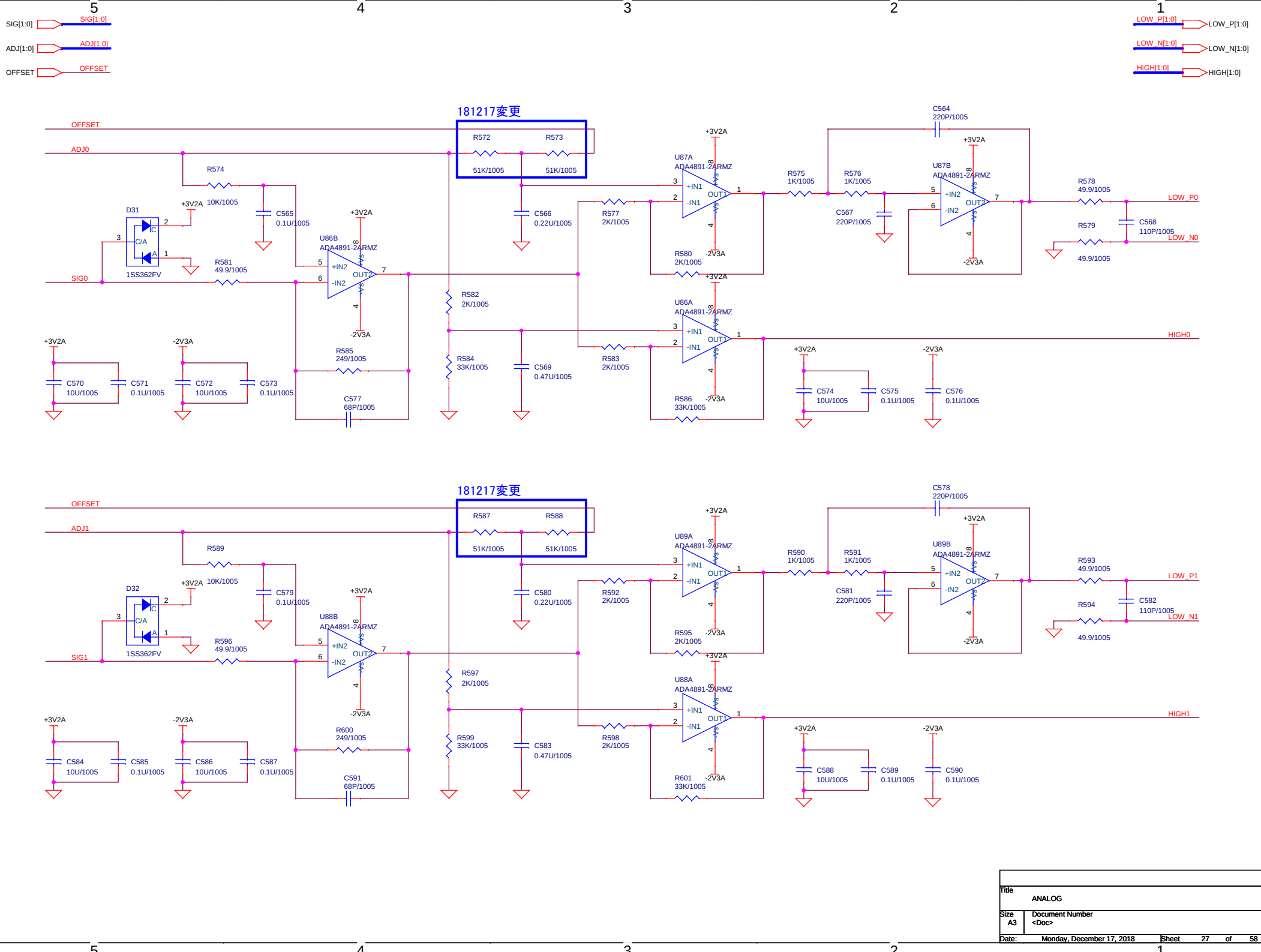
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R574 10K/1005
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R582 2K/1005
R584 33K/1005
C569 0.47U/1005
R585 249/1005
C577 68P/1005
C566 0.22U/1005
R577 2K/1005
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R580 2K/1005
R575 1K/1005
R576 1K/1005
C567 220P/1005
C564 220P/1005
U87B ADA4891-2ARMZ
R578 49.9/1005
R579 49.9/1005
C568 110P/1005
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LOW_N0
U86A ADA4891-2ARMZ
R583 2K/1005
R586 33K/1005
HIGH0
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C571 0.1U/1005
C572 10U/1005
C573 0.1U/1005
C574 10U/1005
C575 0.1U/1005
C576 0.1U/1005
+3V2A
-2V3A
181217变更
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SIG1
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R588 51K/1005
R589 10K/1005
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1SS362FV
R596 49.9/1005
C579 0.1U/1005
U88B ADA4891-2ARMZ
R597 2K/1005
R599 33K/1005
C583 0.47U/1005
R600 249/1005
C591 68P/1005
C580 0.22U/1005
R592 2K/1005
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R590 1K/1005
R591 1K/1005
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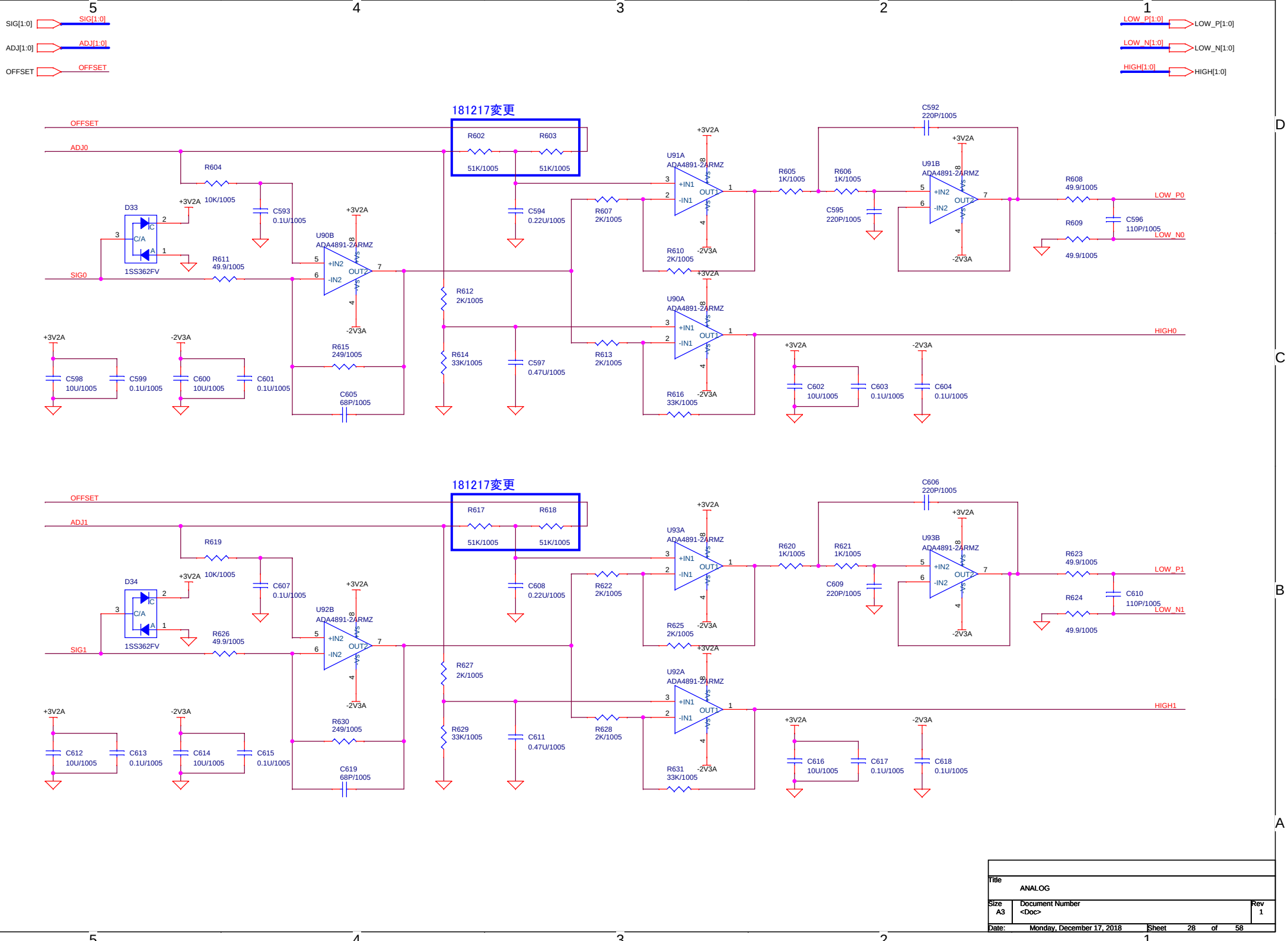

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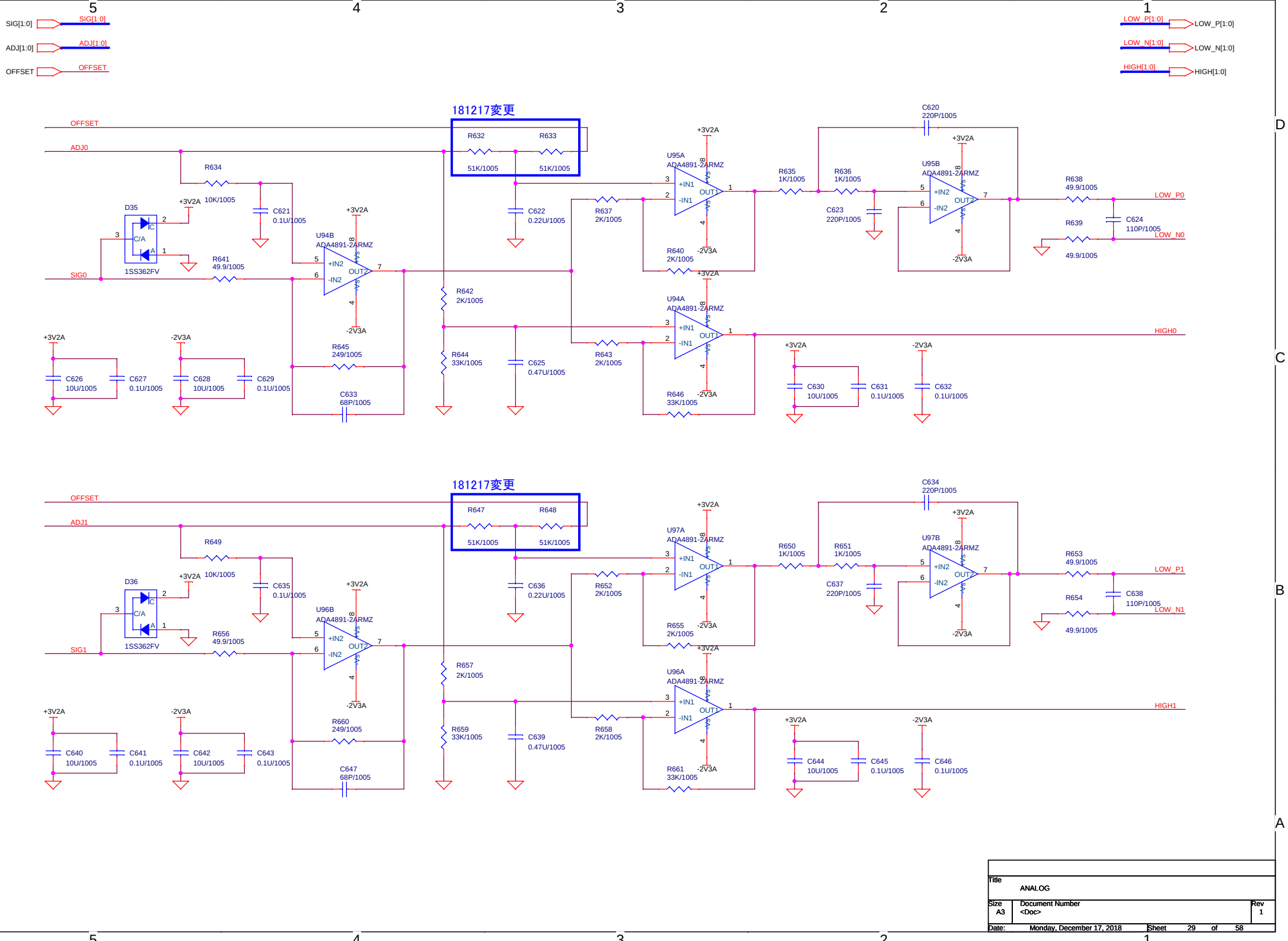
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R636 1K/1005
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R639 49.9/1005
R640 2K/1005
R642 2K/1005
R643 2K/1005
R644 33K/1005
R645 249/1005
R646 33K/1005
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C623 220P/1005
C624 110P/1005
C625 0.47U/1005
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C627 0.1U/1005
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C632 0.1U/1005
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LOW_N0
HIGH0
+3V2A
-2V3A
181217变更
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ADJ1
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R648 51K/1005
R649 10K/1005
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D36 1SS362FV
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C636 0.22U/1005
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U97A ADA4891-2ARMZ
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U96A ADA4891-2ARMZ
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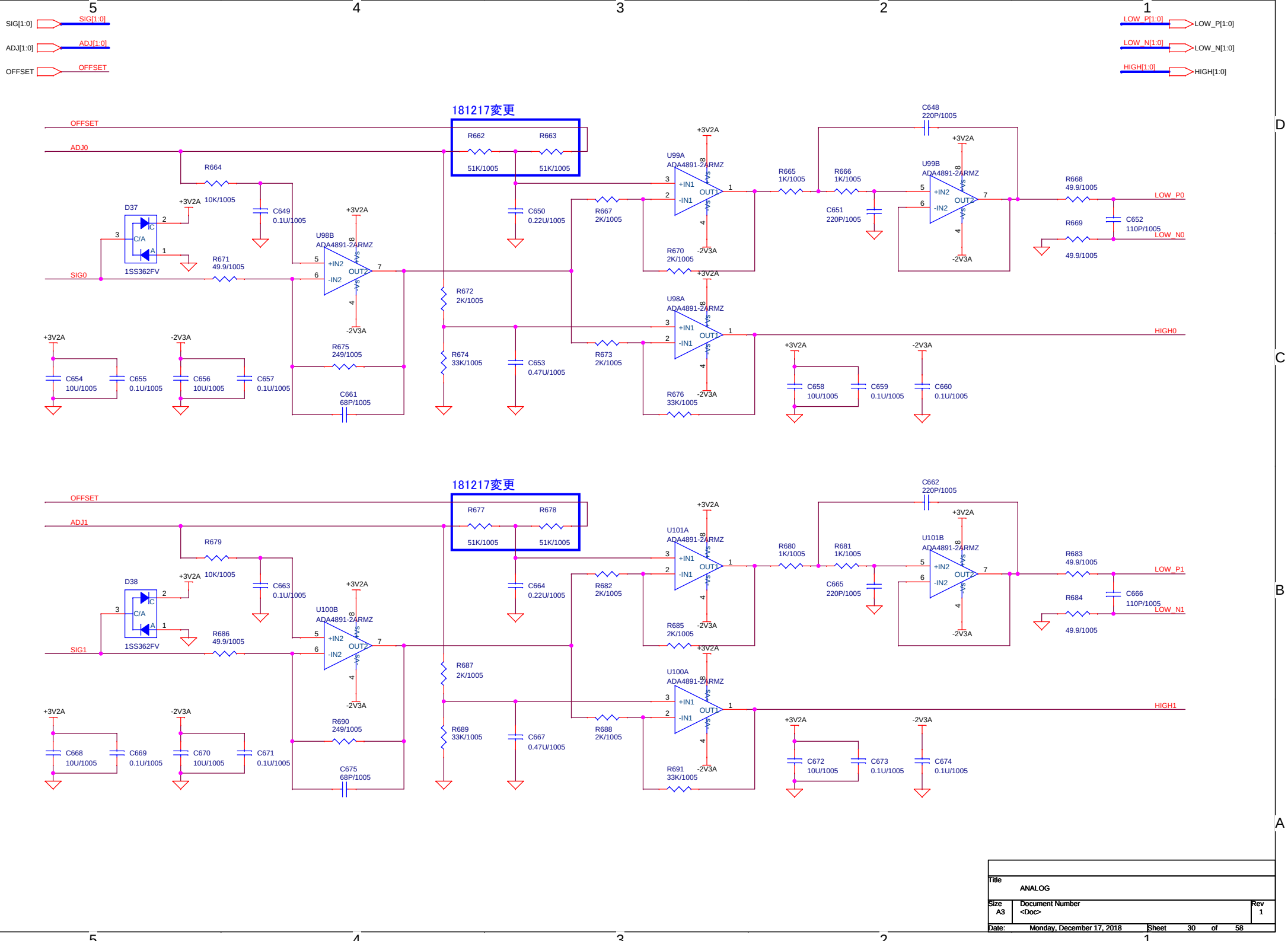

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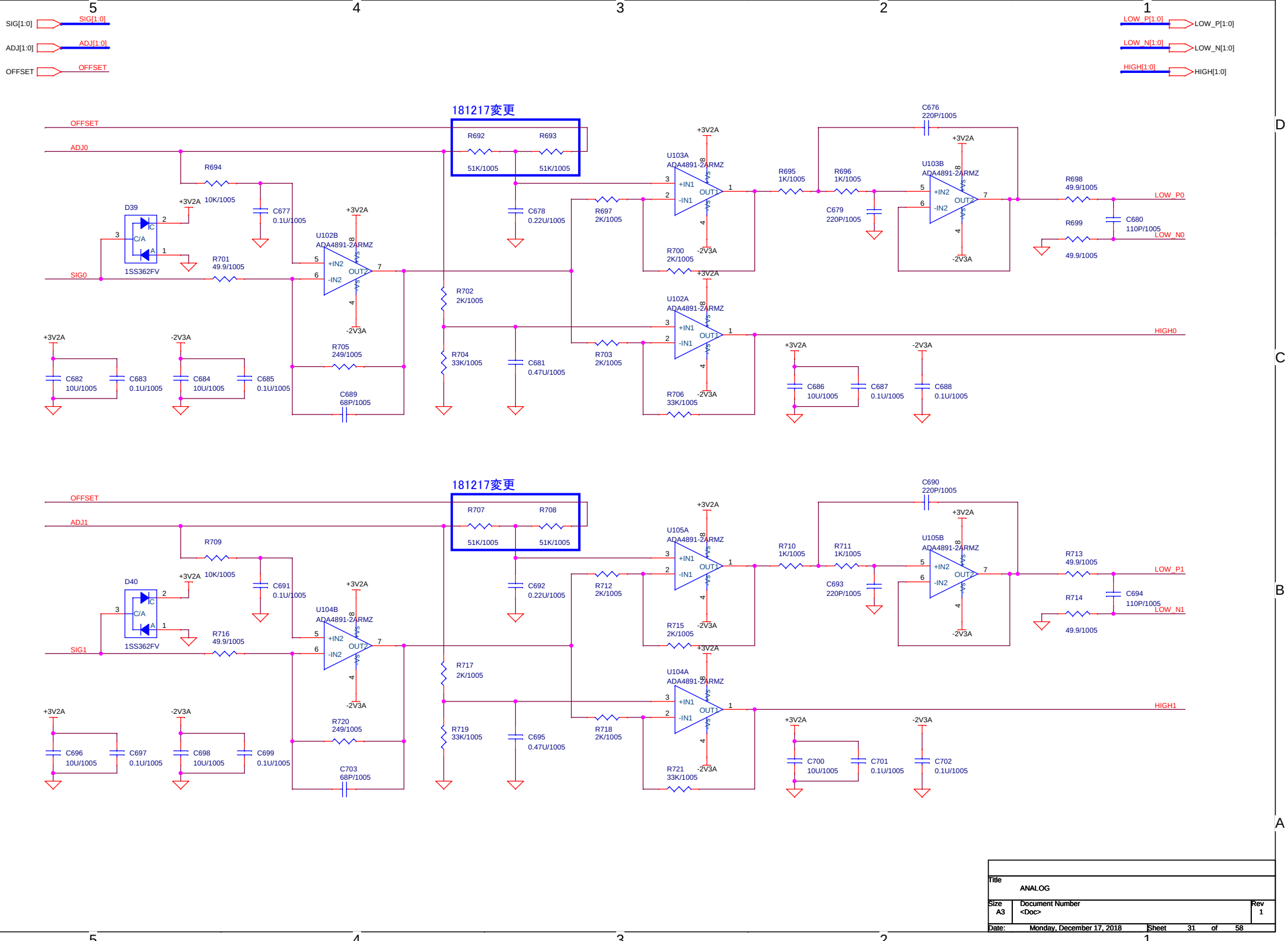
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R693
51K/1005
R694
10K/1005
D39
1SS362FV
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49.9/1005
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ADA4891-2ARMZ
R705
249/1005
C689
68P/1005
R702
2K/1005
R704
33K/1005
C681
0.47U/1005
C678
0.22U/1005
R697
2K/1005
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ADA4891-2ARMZ
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2K/1005
U102A
ADA4891-2ARMZ
R703
2K/1005
R706
33K/1005
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C676
220P/1005
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ADA4891-2ARMZ
R698
49.9/1005
R699
49.9/1005
C680
110P/1005
LOW_P0
LOW_N0
HIGH0
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-2V3A
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0.1U/1005
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51K/1005
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10K/1005
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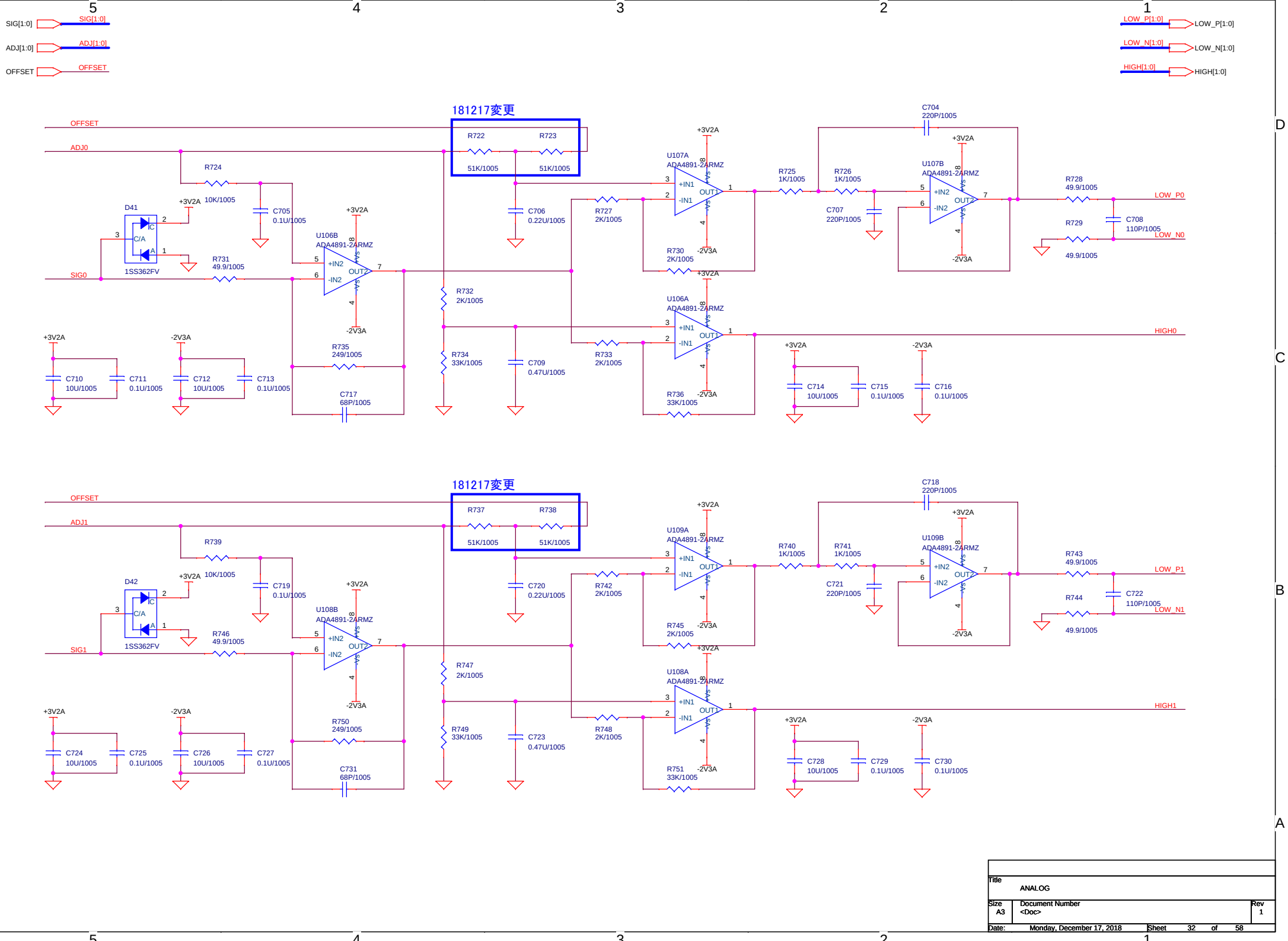
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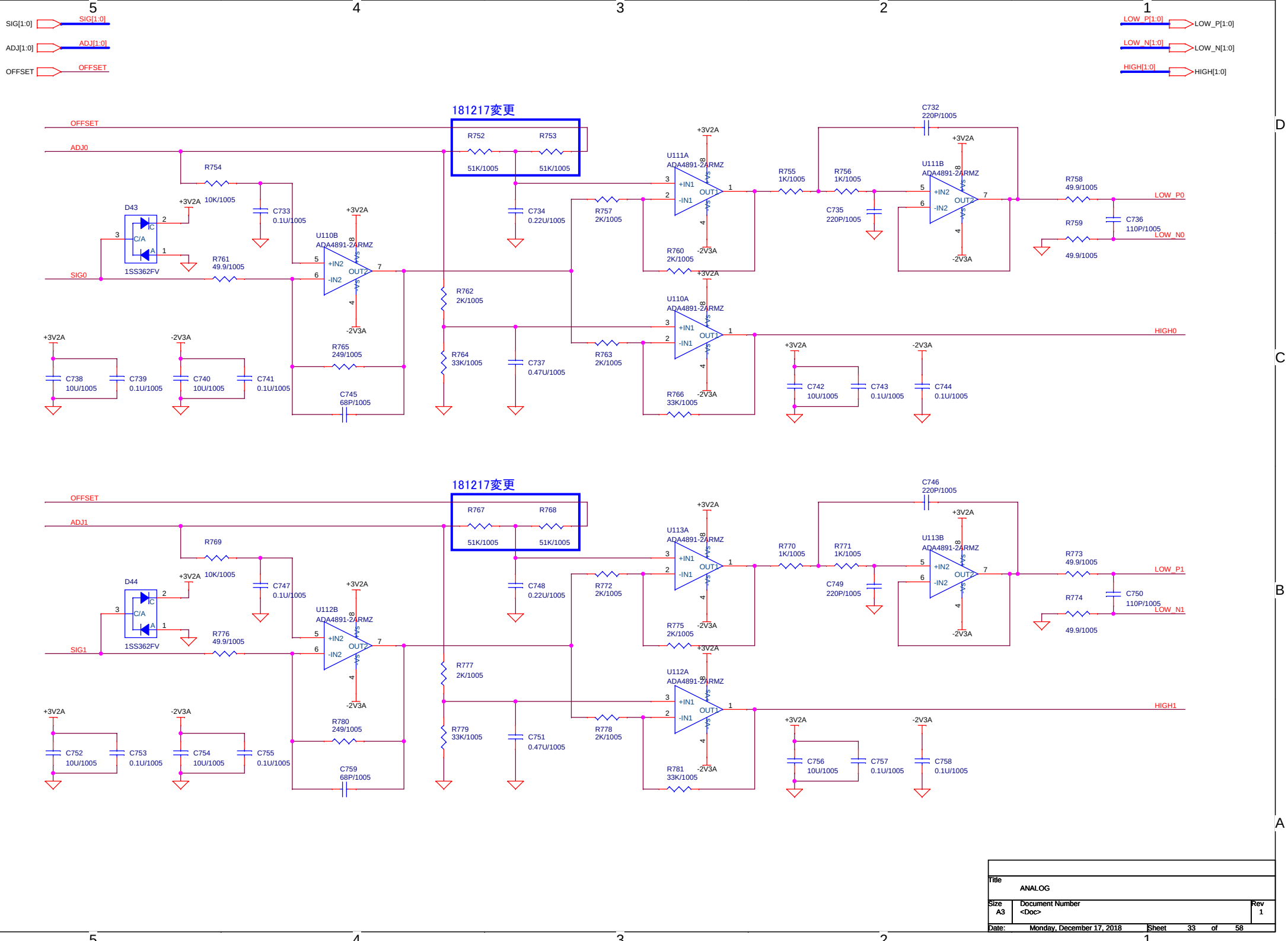
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R756
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ADA4891-2ARMZ
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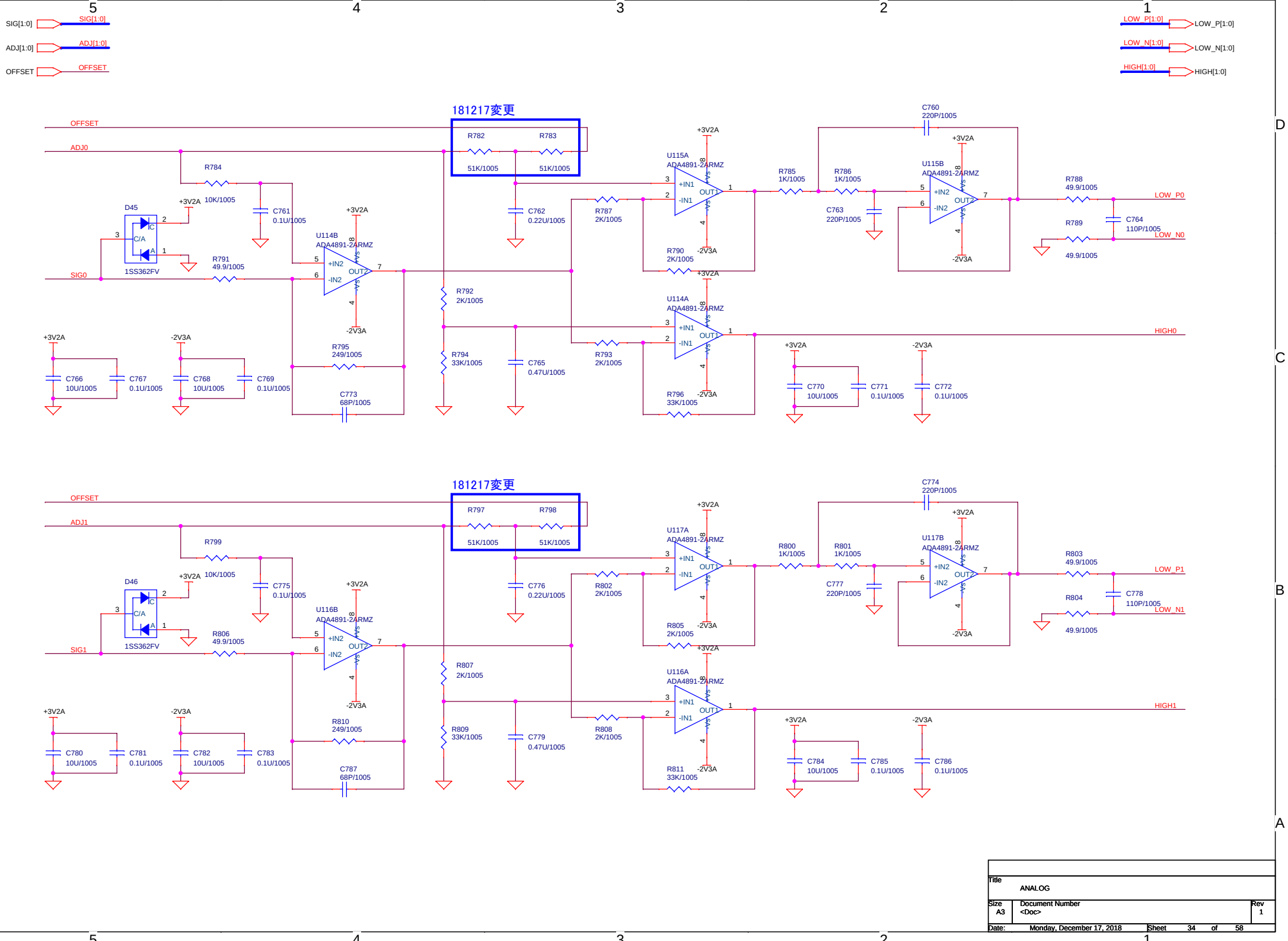
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R785 1K/1005
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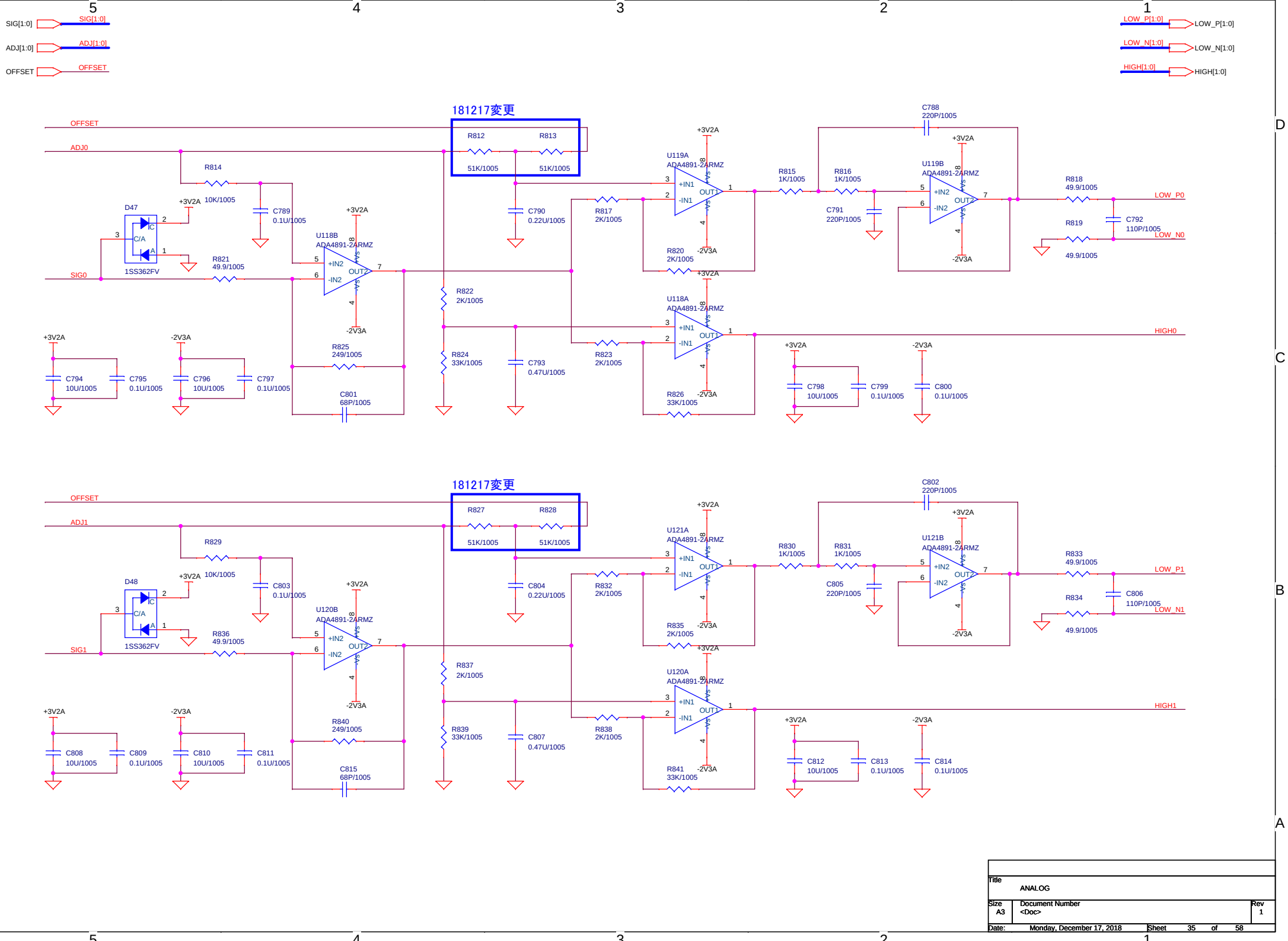
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R831 1K/1005
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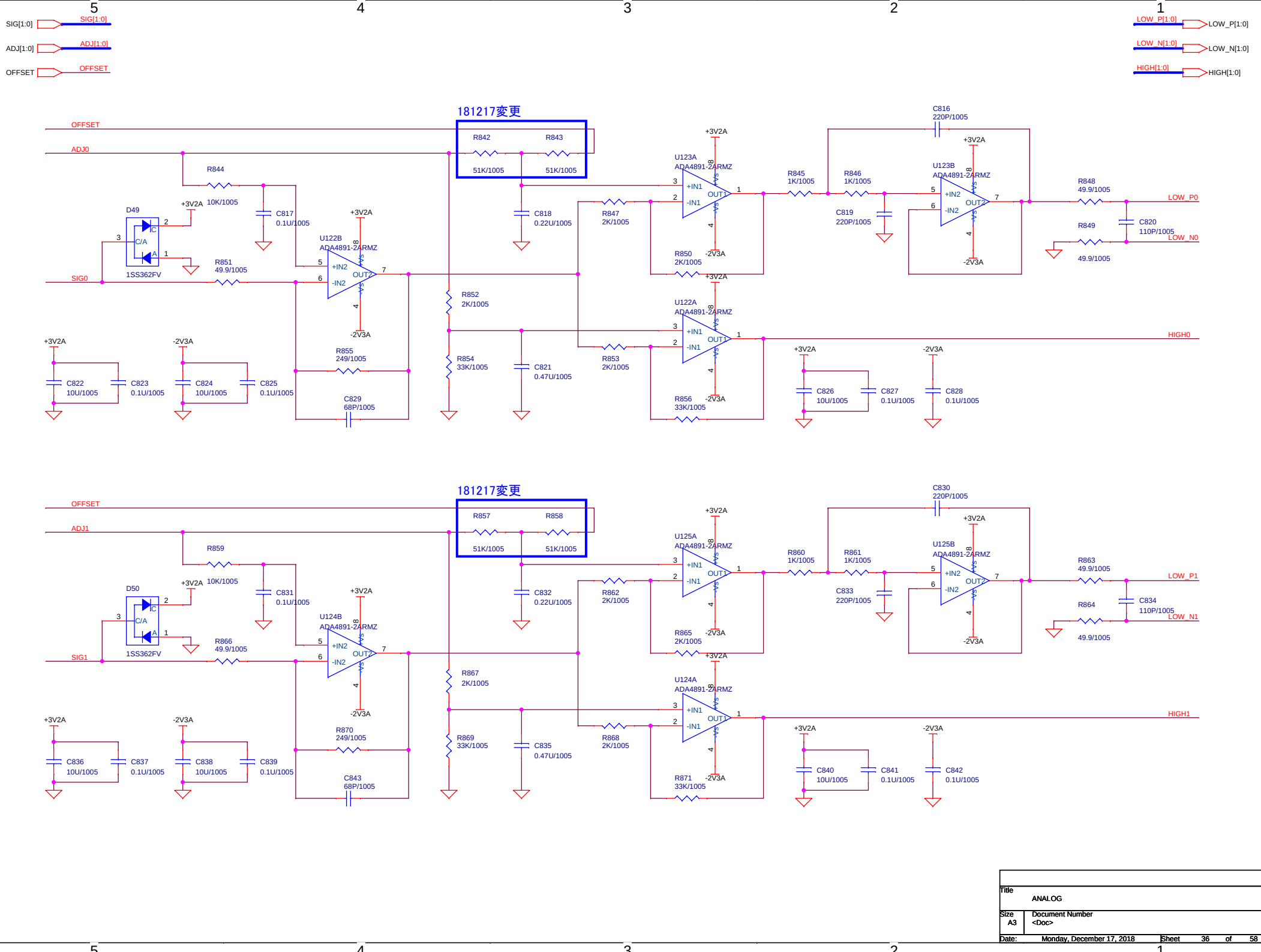
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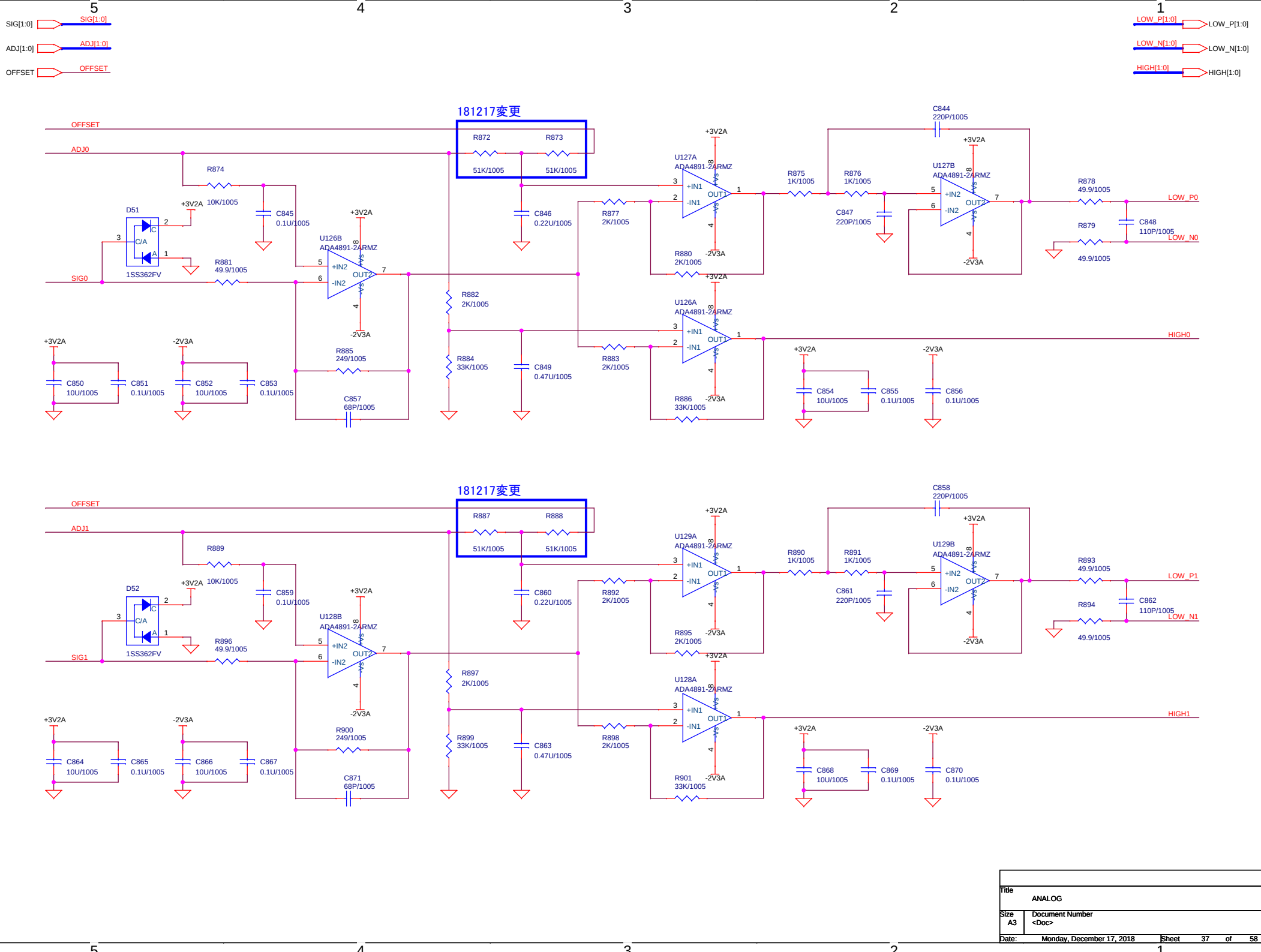
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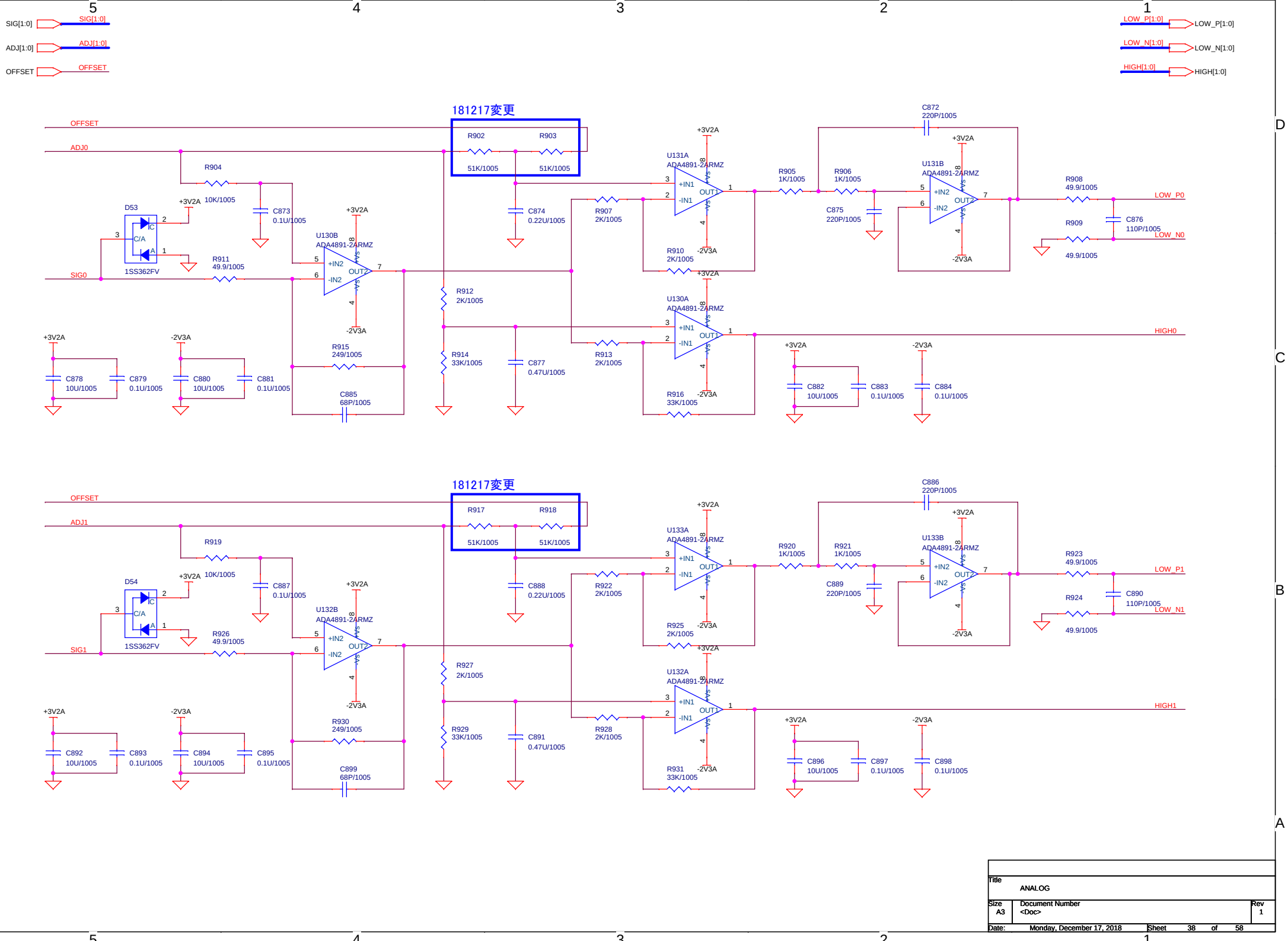
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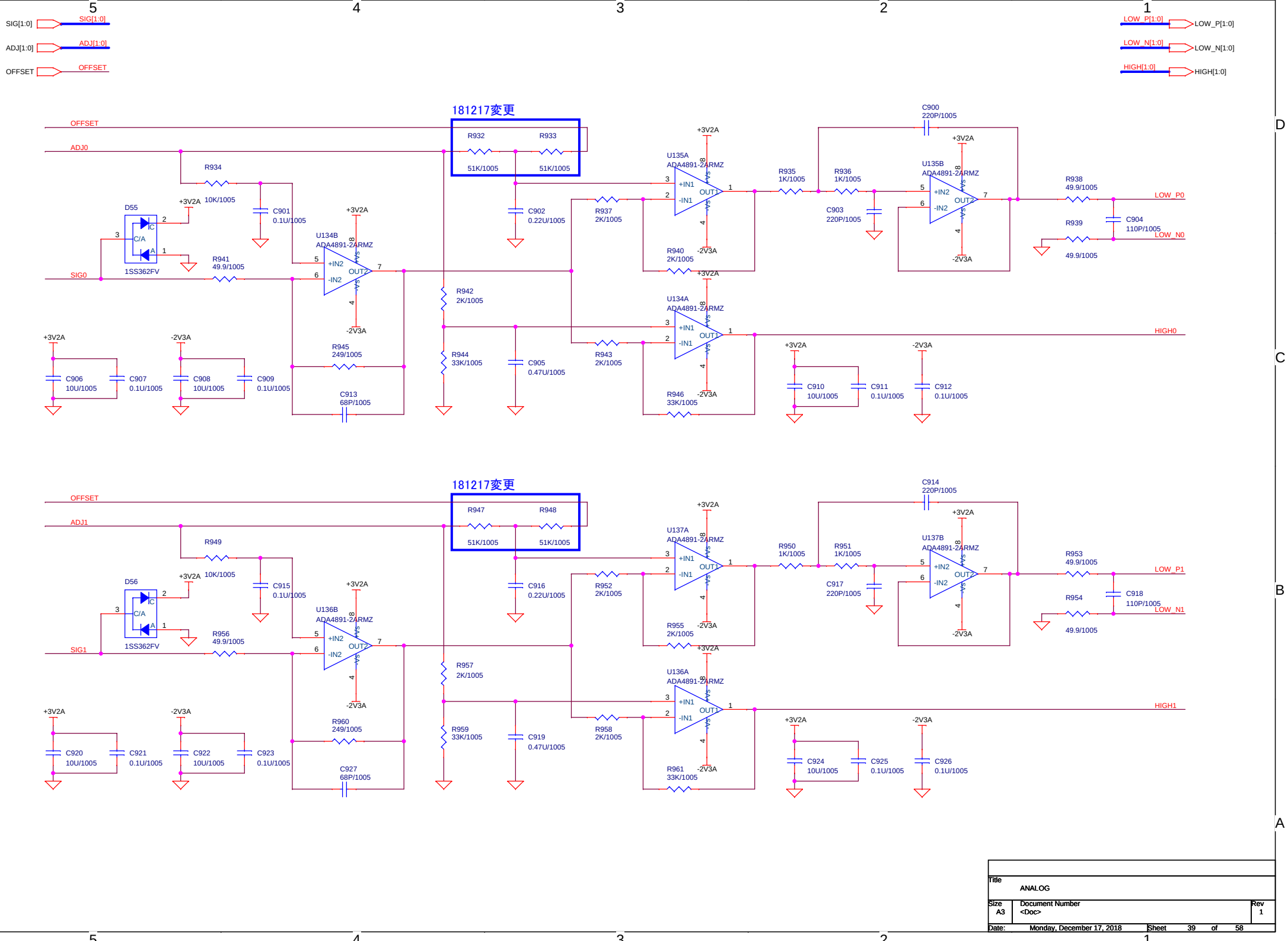
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C921 0.1U/1005
C922 10U/1005
C923 0.1U/1005
C924 10U/1005
C925 0.1U/1005
C926 0.1U/1005
C927 68P/1005
C914 220P/1005
D56
1SS362FV
U136A ADA4891-2ARMZ
U136B ADA4891-2ARMZ
U137A ADA4891-2ARMZ
U137B ADA4891-2ARMZ
+3V2A
-2V3A
HIGH1
LOW_P1
LOW_N1
Title
ANALOG
Size
A3
Document Number
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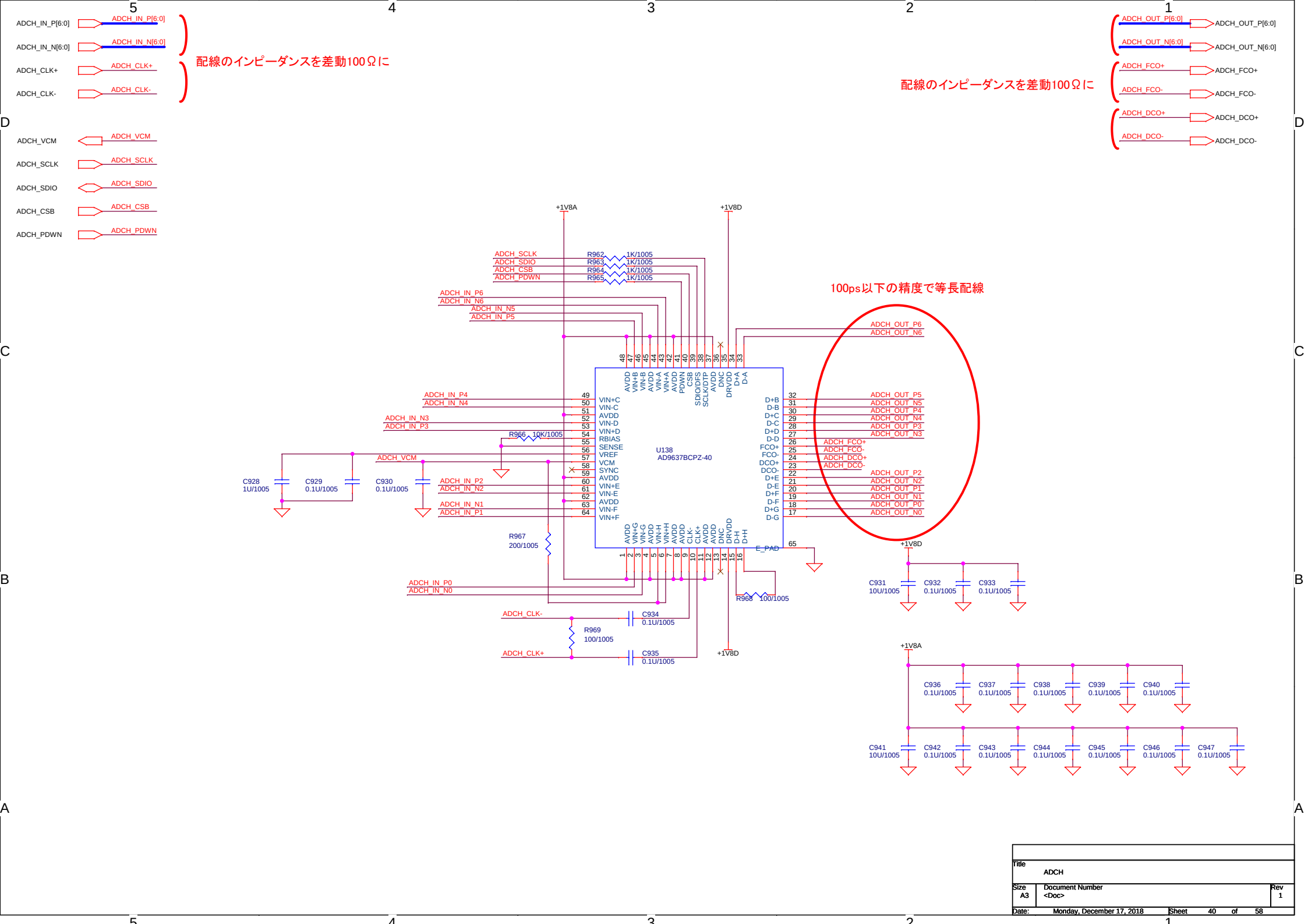
ADCH_IN_P[6:0]
ADCH_IN_N[6:0]
ADCH_CLK+
ADCH_CLK-
配線のインピーダンスを差動100Ωに
ADCH_VCM
ADCH_SCLK
ADCH_SDIO
ADCH_CSB
ADCH_PDWN
ADCH_OUT_P[6:0]
ADCH_OUT_N[6:0]
ADCH_FCO+
ADCH_FCO-
ADCH_DCO+
ADCH_DCO-
配線のインピーダンスを差動100Ωに
100ps以下の精度で等長配線
+1V8A
+1V8D
U138
AD9637BCPZ-40
R962 1K/1005
R963 1K/1005
R964 1K/1005
R965 1K/1005
R966 10K/1005
R967 200/1005
R968 100/1005
R969 100/1005
C928 1U/1005
C929 0.1U/1005
C930 0.1U/1005
C931 10U/1005
C932 0.1U/1005
C933 0.1U/1005
C934 0.1U/1005
C935 0.1U/1005
C936 0.1U/1005
C937 0.1U/1005
C938 0.1U/1005
C939 0.1U/1005
C940 0.1U/1005
C941 10U/1005
C942 0.1U/1005
C943 0.1U/1005
C944 0.1U/1005
C945 0.1U/1005
C946 0.1U/1005
C947 0.1U/1005
Title
ADCH
Size
A3
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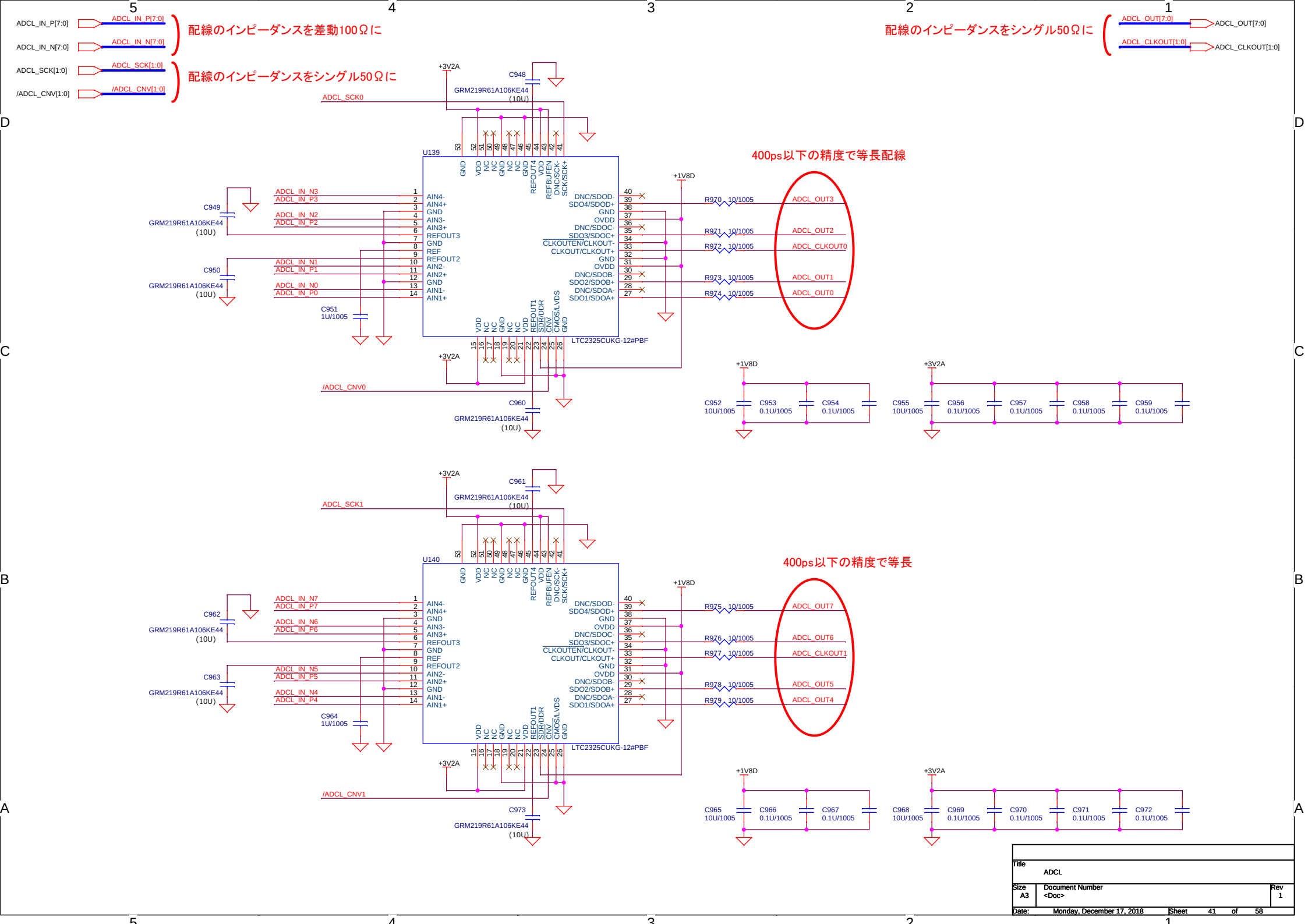
ADCL_IN_P[7:0]
ADCL_IN_N[7:0]
ADCL_SCK[1:0]
/ADCL_CNV[1:0]
配線のインピーダンスを差動100Ωに
配線のインピーダンスをシングル50Ωに
ADCL_OUT[7:0]
ADCL_CLKOUT[1:0]
配線のインピーダンスをシングル50Ωに
+3V2A
+1V8D
ADCL_SCK0
/ADCL_CNV0
U139
LTC2325CUKG-12#PBF
400ps以下の精度で等長配線
ADCL_OUT3
ADCL_OUT2
ADCL_CLKOUT0
ADCL_OUT1
ADCL_OUT0
ADCL_SCK1
/ADCL_CNV1
U140
400ps以下の精度で等長
ADCL_OUT7
ADCL_OUT6
ADCL_CLKOUT1
ADCL_OUT5
ADCL_OUT4
Title
ADCL
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A3
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ADCL_IN_P[7:0]
ADCL_IN_N[7:0]
ADCL_SCK[1:0]
/ADCL_CNV[1:0]
配線のインピーダンスを差動100Ωに
配線のインピーダンスをシングル50Ωに
ADCL_OUT[7:0]
ADCL_CLKOUT[1:0]
配線のインピーダンスをシングル50Ωに
400ps以下の精度で等長配線
400ps以下の精度で等長
U141
U142
LTC2325CUKG-12#PBF
GRM219R61A106KE44
C974
C975
C976
C977
C978
C979
C980
C981
C982
C983
C984
C985
C986
C987
C988
C989
C990
C991
C992
C993
C994
C995
C996
C997
C998
C999
R980
R981
R982
R983
R984
R985
R986
R987
R988
R989
+3V2A
+1V8D
ADCL_SCK0
ADCL_SCK1
/ADCL_CNV0
/ADCL_CNV1
ADCL_OUT3
ADCL_OUT2
ADCL_CLKOUT0
ADCL_OUT1
ADCL_OUT0
ADCL_OUT7
ADCL_OUT6
ADCL_CLKOUT1
ADCL_OUT5
ADCL_OUT4

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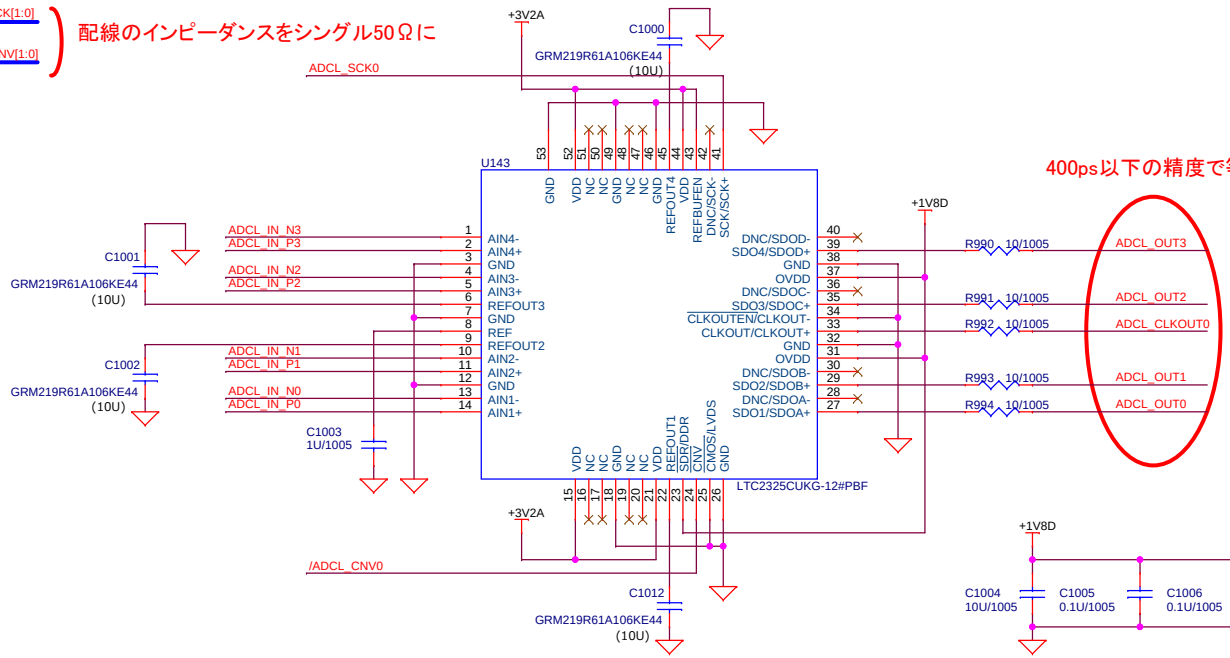
ADCL_IN_P[7:0]
ADCL_IN_N[7:0]
ADCL_SCK[1:0]
/ADCL_CNV[1:0]

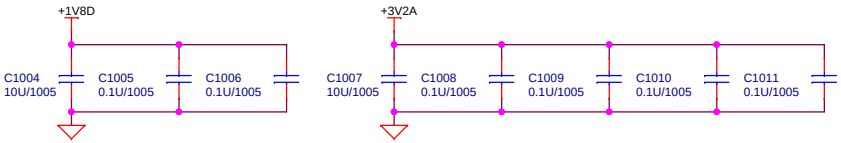
配線のインピーダンスを差動100Ωに

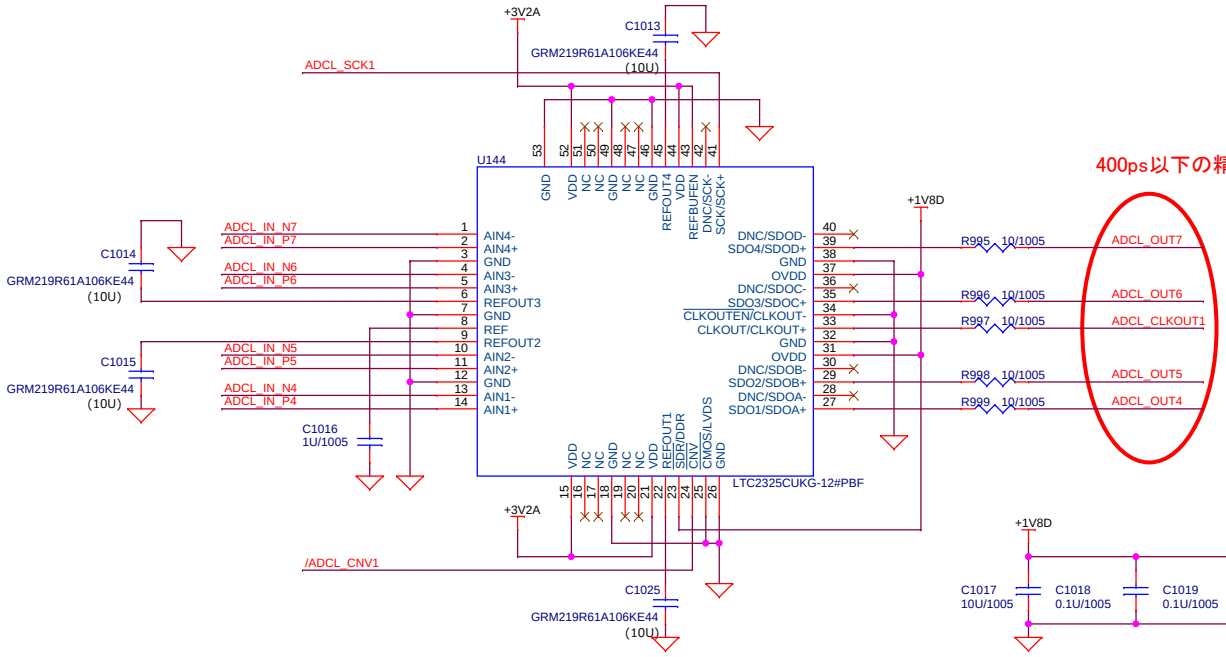
配線のインピーダンスをシングル50Ωに

ADCL_OUT[7:0]
ADCL_CLKOUT[1:0]

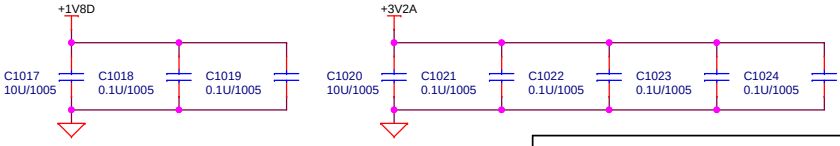


400ps以下の精度で等長配線





400ps以下の精度で等長



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ADCL_IN_P[7:0]
ADCL_IN_P[7:0]
ADCL_IN_N[7:0]
ADCL_IN_N[7:0]
配線のインピーダンスを差動100Ωに
ADCL_SCK[1:0]
ADCL_SCK[1:0]
/ADCL_CNV[1:0]
/ADCL_CNV[1:0]
配線のインピーダンスをシングル50Ωに
配線のインピーダンスをシングル50Ωに
ADCL_OUT[7:0]
ADCL_OUT[7:0]
ADCL_CLKOUT[1:0]
ADCL_CLKOUT[1:0]
+3V2A
C1026
GRM219R61A106KE44
(10U)
ADCL_SCK0
U145
GND VDD NC NC GND NC NC GND REFOUT4 VDD REFBUFEN DNC/SCK- SCK/SCK+
53 52 51 50 49 48 47 46 45 44 43 42 41
400ps以下の精度で等長配線
+1V8D
ADCL_IN_N3
ADCL_IN_P3
ADCL_IN_N2
ADCL_IN_P2
ADCL_IN_N1
ADCL_IN_P1
ADCL_IN_N0
ADCL_IN_P0
1 2 3 4 5 6 7 8 9 10 11 12 13 14
AIN4- AIN4+ GND AIN3- AIN3+ REFOUT3 GND REF REFOUT2 AIN2- AIN2+ GND AIN1- AIN1+
DNC/SDOD- SDO4/SDOD+ GND OVDD DNC/SDOC- SDO3/SDOC+ CLKOUTEN/CLKOUT- CLKOUT/CLKOUT+ GND OVDD DNC/SDOB- SDO2/SDOB+ DNC/SDOA- SDO1/SDOA+
40 39 38 37 36 35 34 33 32 31 30 29 28 27
C1027
C1028
C1029
GRM219R61A106KE44
(10U)
1U/1005
R1000 10/1005
R1001 10/1005
R1002 10/1005
R1003 10/1005
R1004 10/1005
ADCL_OUT3
ADCL_OUT2
ADCL_CLKOUT0
ADCL_OUT1
ADCL_OUT0
VDD NC NC GND NC NC VDD REFOUT1 SDR/DDR CNV CMOS/LVDS GND
15 16 17 18 19 20 21 22 23 24 25 26
LTC2325CUKG-12#PBF
/ADCL_CNV0
C1038
C1030 10U/1005
C1031 0.1U/1005
C1032 0.1U/1005
C1033 10U/1005
C1034 0.1U/1005
C1035 0.1U/1005
C1036 0.1U/1005
C1037 0.1U/1005
C1039
ADCL_SCK1
U146
400ps以下の精度で等長
ADCL_IN_N7
ADCL_IN_P7
ADCL_IN_N6
ADCL_IN_P6
ADCL_IN_N5
ADCL_IN_P5
ADCL_IN_N4
ADCL_IN_P4
C1040
C1041
C1042
R1005 10/1005
R1006 10/1005
R1007 10/1005
R1008 10/1005
R1009 10/1005
ADCL_OUT7
ADCL_OUT6
ADCL_CLKOUT1
ADCL_OUT5
ADCL_OUT4
/ADCL_CNV1
C1051
C1043 10U/1005
C1044 0.1U/1005
C1045 0.1U/1005
C1046 10U/1005
C1047 0.1U/1005
C1048 0.1U/1005
C1049 0.1U/1005
C1050 0.1U/1005

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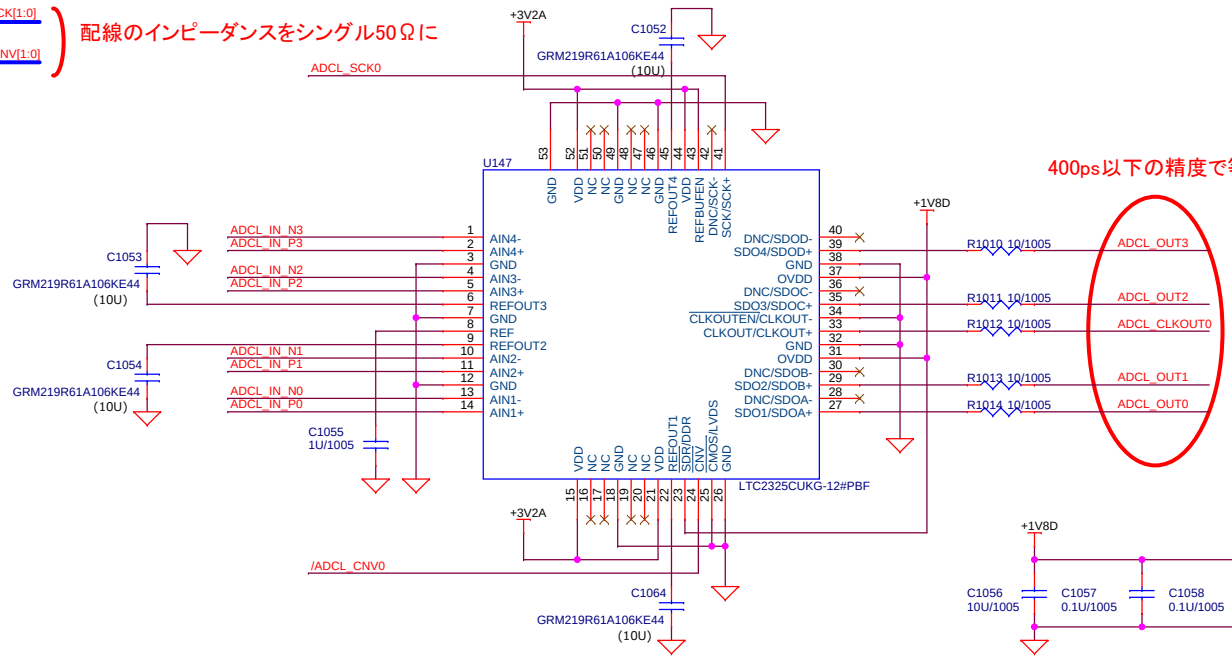
ADCL_IN_P[7:0]
ADCL_IN_N[7:0]
ADCL_SCK[1:0]
/ADCL_CNV[1:0]

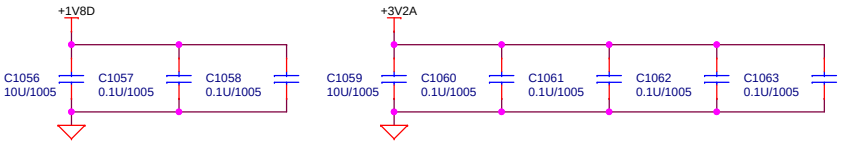
配線のインピーダンスを差動100Ωに

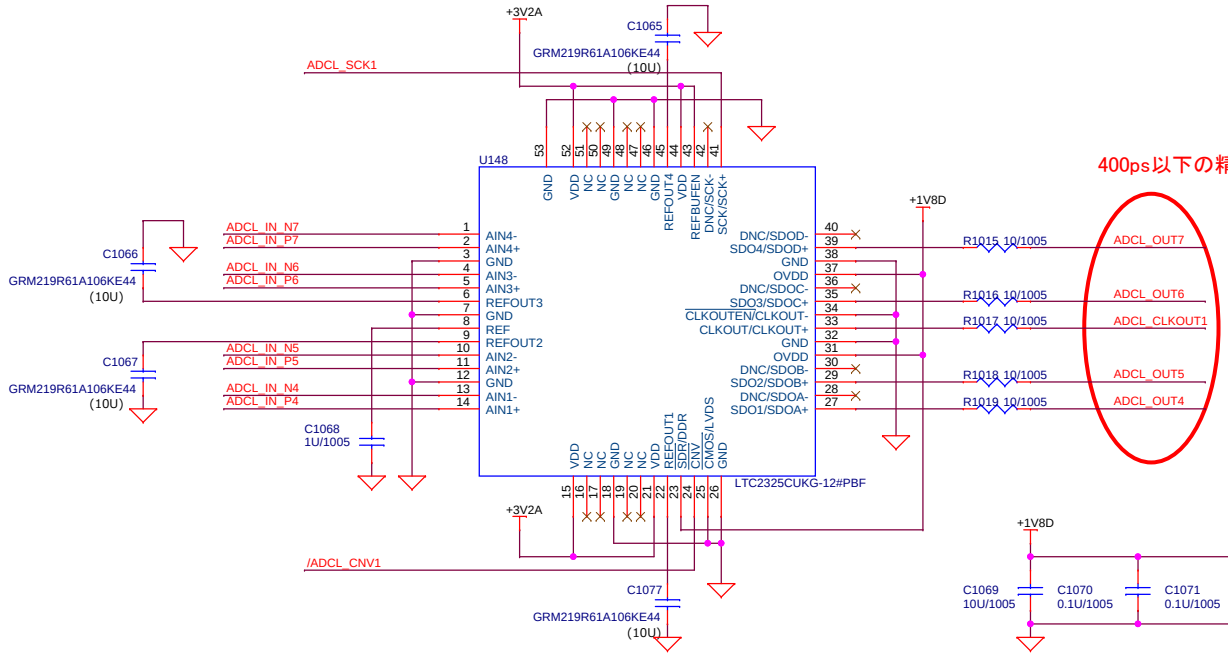
配線のインピーダンスをシングル50Ωに

ADCL_OUT[7:0]
ADCL_CLKOUT[1:0]

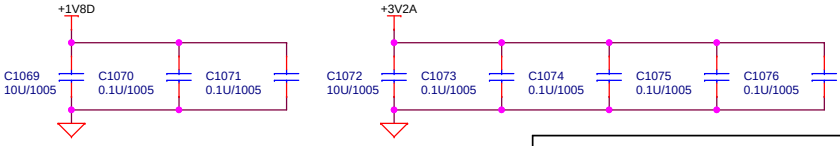


400ps以下の精度で等長配線





400ps以下の精度で等長



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ADCL_IN_P[7:0]
ADCL_IN_P[7:0]
ADCL_IN_N[7:0]
ADCL_IN_N[7:0]
配線のインピーダンスを差動100Ωに
ADCL_SCK[1:0]
ADCL_SCK[1:0]
/ADCL_CNV[1:0]
/ADCL_CNV[1:0]
配線のインピーダンスをシングル50Ωに
配線のインピーダンスをシングル50Ωに
ADCL_OUT[7:0]
ADCL_OUT[7:0]
ADCL_CLKOUT[1:0]
ADCL_CLKOUT[1:0]
+3V2A
C1078
GRM219R61A106KE44
(10U)
ADCL_SCK0
U149
400ps以下の精度で等長配線
+1V8D
ADCL_IN_N3
ADCL_IN_P3
ADCL_IN_N2
ADCL_IN_P2
ADCL_IN_N1
ADCL_IN_P1
ADCL_IN_N0
ADCL_IN_P0
C1079
C1080
C1081
1U/1005
AIN4-
AIN4+
GND
AIN3-
AIN3+
REFOUT3
GND
REF
REFOUT2
AIN2-
AIN2+
GND
AIN1-
AIN1+
DNC/SDOD-
SDO4/SDOD+
GND
OVDD
DNC/SDOC-
SDO3/SDOC+
CLKOUTEN/CLKOUT-
CLKOUT/CLKOUT+
GND
OVDD
DNC/SDOB-
SDO2/SDOB+
DNC/SDOA-
SDO1/SDOA+
VDD
NC
NC
GND
NC
NC
VDD
REFOUT1
SDR/DDR
CNV
CMOS/LVDS
GND
LTC2325CUKG-12#PBF
R1020 10/1005
R1021 10/1005
R1022 10/1005
R1023 10/1005
R1024 10/1005
ADCL_OUT3
ADCL_OUT2
ADCL_CLKOUT0
ADCL_OUT1
ADCL_OUT0
/ADCL_CNV0
C1090
C1082 10U/1005
C1083 0.1U/1005
C1084 0.1U/1005
C1085 10U/1005
C1086 0.1U/1005
C1087 0.1U/1005
C1088 0.1U/1005
C1089 0.1U/1005
C1091
ADCL_SCK1
U150
400ps以下の精度で等長
ADCL_IN_N7
ADCL_IN_P7
ADCL_IN_N6
ADCL_IN_P6
ADCL_IN_N5
ADCL_IN_P5
ADCL_IN_N4
ADCL_IN_P4
C1092
C1093
C1094
1U/1005
R1025 10/1005
R1026 10/1005
R1027 10/1005
R1028 10/1005
R1029 10/1005
ADCL_OUT7
ADCL_OUT6
ADCL_CLKOUT1
ADCL_OUT5
ADCL_OUT4
/ADCL_CNV1
C1103
C1095 10U/1005
C1096 0.1U/1005
C1097 0.1U/1005
C1098 10U/1005
C1099 0.1U/1005
C1100 0.1U/1005
C1101 0.1U/1005
C1102 0.1U/1005

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ADCL_IN_P[7:0]
ADCL_IN_P[7:0]
ADCL_IN_N[7:0]
ADCL_IN_N[7:0]
配線のインピーダンスを差動100Ωに
ADCL_SCK[1:0]
ADCL_SCK[1:0]
/ADCL_CNV[1:0]
/ADCL_CNV[1:0]
配線のインピーダンスをシングル50Ωに
配線のインピーダンスをシングル50Ωに
ADCL_OUT[7:0]
ADCL_OUT[7:0]
ADCL_CLKOUT[1:0]
ADCL_CLKOUT[1:0]
+3V2A
C1104
GRM219R61A106KE44
(10U)
ADCL_SCK0
U151
400ps以下の精度で等長配線
+1V8D
ADCL_IN_N3
ADCL_IN_P3
ADCL_IN_N2
ADCL_IN_P2
ADCL_IN_N1
ADCL_IN_P1
ADCL_IN_N0
ADCL_IN_P0
C1105
C1106
C1107
1U/1005
AIN4-
AIN4+
GND
AIN3-
AIN3+
REFOUT3
GND
REF
REFOUT2
AIN2-
AIN2+
GND
AIN1-
AIN1+
DNC/SDOD-
SDO4/SDOD+
GND
OVDD
DNC/SDOC-
SDO3/SDOC+
CLKOUTEN/CLKOUT-
CLKOUT/CLKOUT+
GND
OVDD
DNC/SDOB-
SDO2/SDOB+
DNC/SDOA-
SDO1/SDOA+
R1030 10/1005
R1031 10/1005
R1032 10/1005
R1033 10/1005
R1034 10/1005
ADCL_OUT3
ADCL_OUT2
ADCL_CLKOUT0
ADCL_OUT1
ADCL_OUT0
LTC2325CUKG-12#PBF
/ADCL_CNV0
C1116
C1108 10U/1005
C1109 0.1U/1005
C1110 0.1U/1005
C1111 10U/1005
C1112 0.1U/1005
C1113 0.1U/1005
C1114 0.1U/1005
C1115 0.1U/1005
C1117
ADCL_SCK1
U152
400ps以下の精度で等長
ADCL_IN_N7
ADCL_IN_P7
ADCL_IN_N6
ADCL_IN_P6
ADCL_IN_N5
ADCL_IN_P5
ADCL_IN_N4
ADCL_IN_P4
C1118
C1119
C1120
1U/1005
R1035 10/1005
R1036 10/1005
R1037 10/1005
R1038 10/1005
R1039 10/1005
ADCL_OUT7
ADCL_OUT6
ADCL_CLKOUT1
ADCL_OUT5
ADCL_OUT4
/ADCL_CNV1
C1129
C1121 10U/1005
C1122 0.1U/1005
C1123 0.1U/1005
C1124 10U/1005
C1125 0.1U/1005
C1126 0.1U/1005
C1127 0.1U/1005
C1128 0.1U/1005

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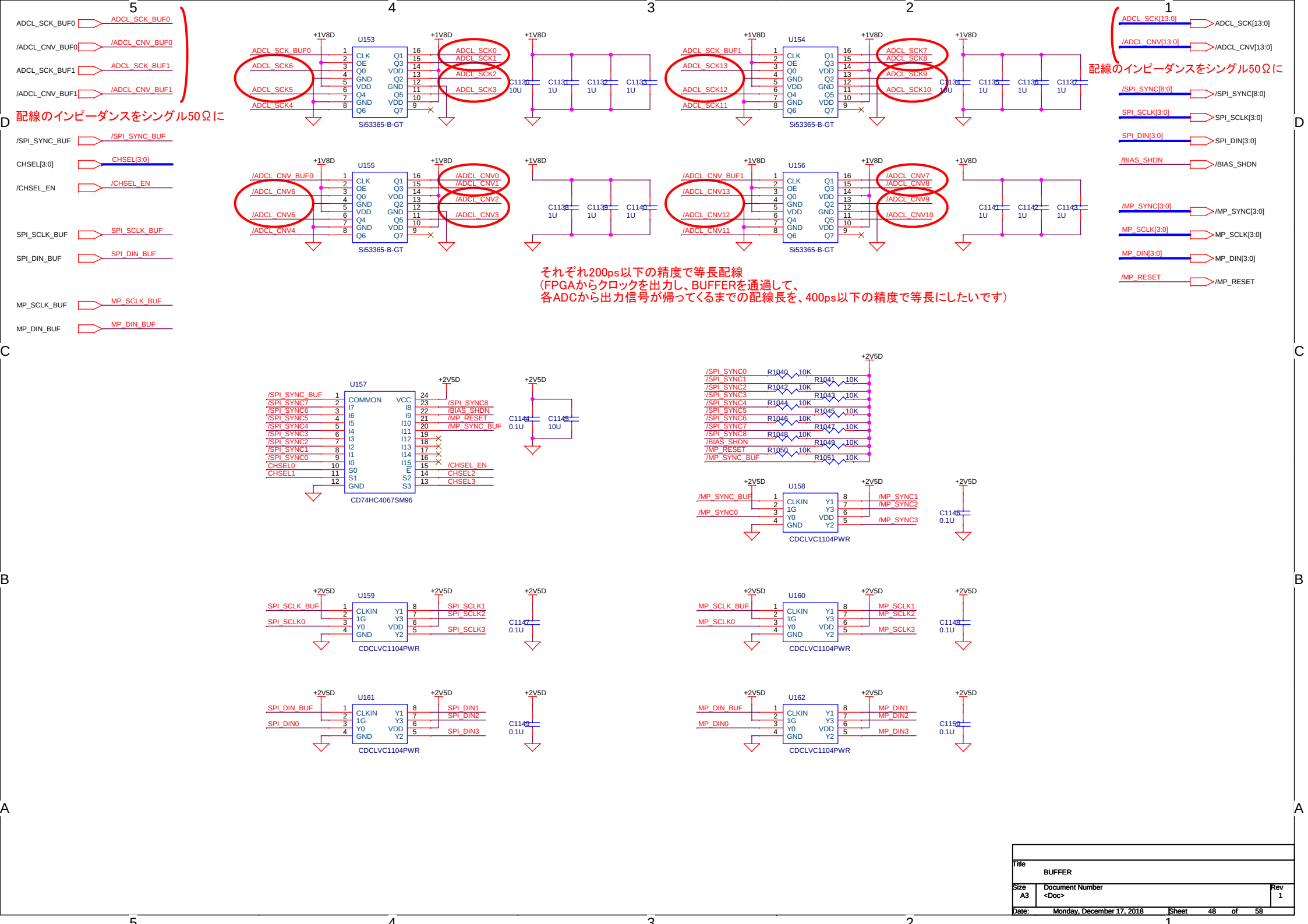
ADCL_SCK_BUF0
/ADCL_CNV_BUF0
ADCL_SCK_BUF1
/ADCL_CNV_BUF1
配線のインピーダンスをシングル50Ωに
/SPI_SYNC_BUF
CHSEL[3:0]
/CHSEL_EN
SPI_SCLK_BUF
SPI_DIN_BUF
MP_SCLK_BUF
MP_DIN_BUF
U153
U154
U155
U156
Si53365-B-GT
+1V8D
それぞれ200ps以下の精度で等長配線
(FPGAからクロックを出力し、BUFFERを通過して、
各ADCから出力信号が帰ってくるまでの配線長を、400ps以下の精度で等長にしたいです)
ADCL_SCK[13:0]
/ADCL_CNV[13:0]
/SPI_SYNC[8:0]
SPI_SCLK[3:0]
SPI_DIN[3:0]
/BIAS_SHDN
/MP_SYNC[3:0]
MP_SCLK[3:0]
MP_DIN[3:0]
/MP_RESET
U157
CD74HC4067SM96
+2V5D
U158
U159
U160
U161
U162
CDCLVC1104PWR
Title
BUFFER
Size
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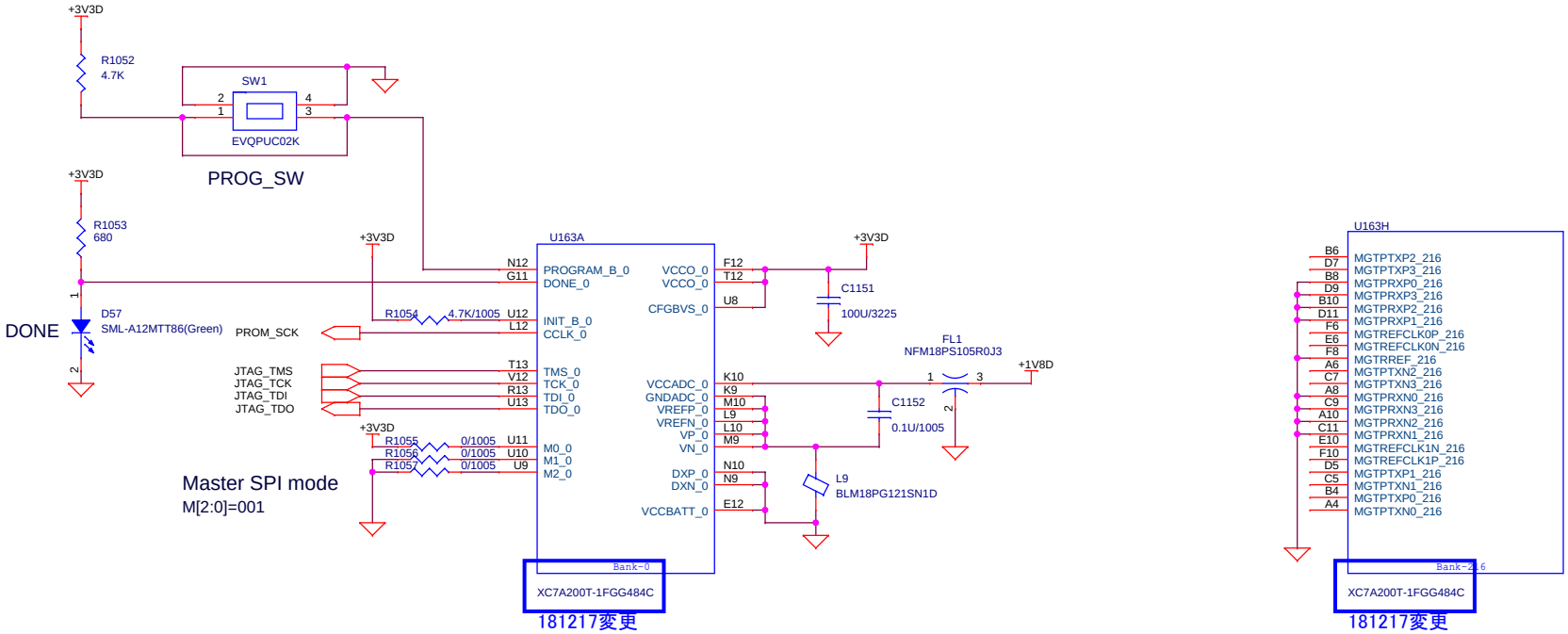

Title	FPGA_BANK_0_216	
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ETH_TXD[7:0] — ETH_TXD[7:0]
ETH_TXEN — ETH_TXEN
ETH_TXER — ETH_TXER
ETH_TXCLK — ETH_TXCLK
ETH_GTXCLK — ETH_GTXCLK

ETH_1000_LED — ETH_1000_LED
ETH_MDC — ETH_MDC
ETH_MDIO — ETH_MDIO
/ETH_RESET — /ETH_RESET
ETH_HPD — ETH_HPD

ETH_IRQ — ETH_IRQ
ETH_RXD[7:0] — ETH_RXD[7:0]
ETH_RXDV — ETH_RXDV
ETH_RXER — ETH_RXER
ETH_CRS — ETH_CRS
ETH_COL — ETH_COL
ETH_RXCLK — ETH_RXCLK

PROM_IO[3:0] — PROM_IO[3:0]
PROM_CS — PROM_CS

U163B
XC7A200T-1FGG484C
Bank-13
181217変更

U163C
XC7A200T-1FGG484C
Bank-14
181217変更

+3V3D
C1158 10U/1005
C1159 10U/1005
C1162 1U/1005
C1163 1U/1005
C1164 1U/1005
C1165 1U/1005

C1153 100U/3225
C1154 10U/1005
C1155 10U/1005
C1156 1U/1005
C1157 1U/1005
C1160 1U/1005
C1161 1U/1005

R1058 0/1005

SW2
CFP-0811MC

U164
AT93C46DN-SH
R1059 0
C1166 0.1U

40MHz CLOCK
X1
KC3225A40.0000C3GE00
(40MHz, 3.2mmx2.5mm,3.3V)
R1062 4.7K
C1179 0.01U/1005
C1180 10U
L10 BLM18PG121SN1D
R1063 22

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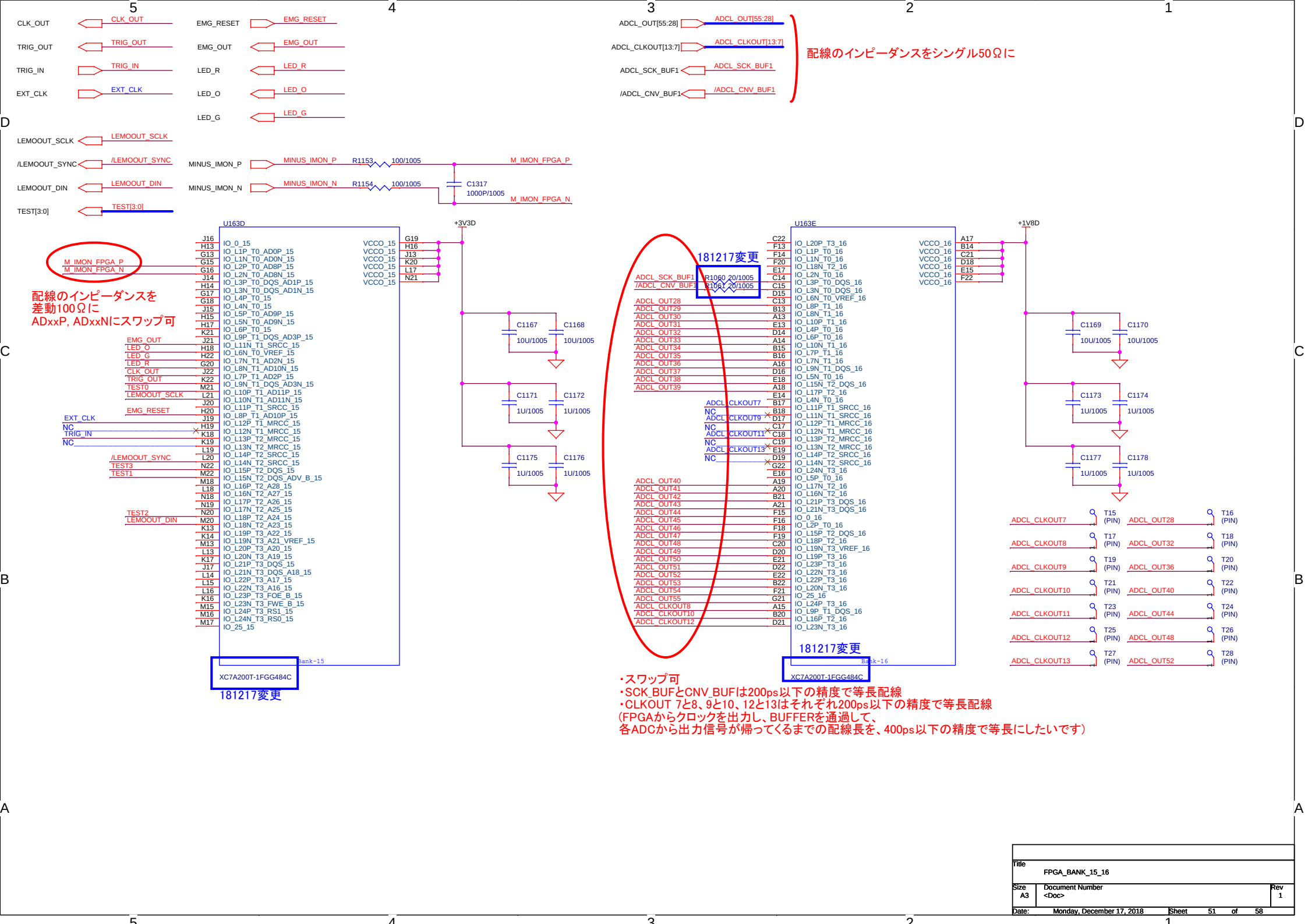

Title	FPGA_BANK_15_16
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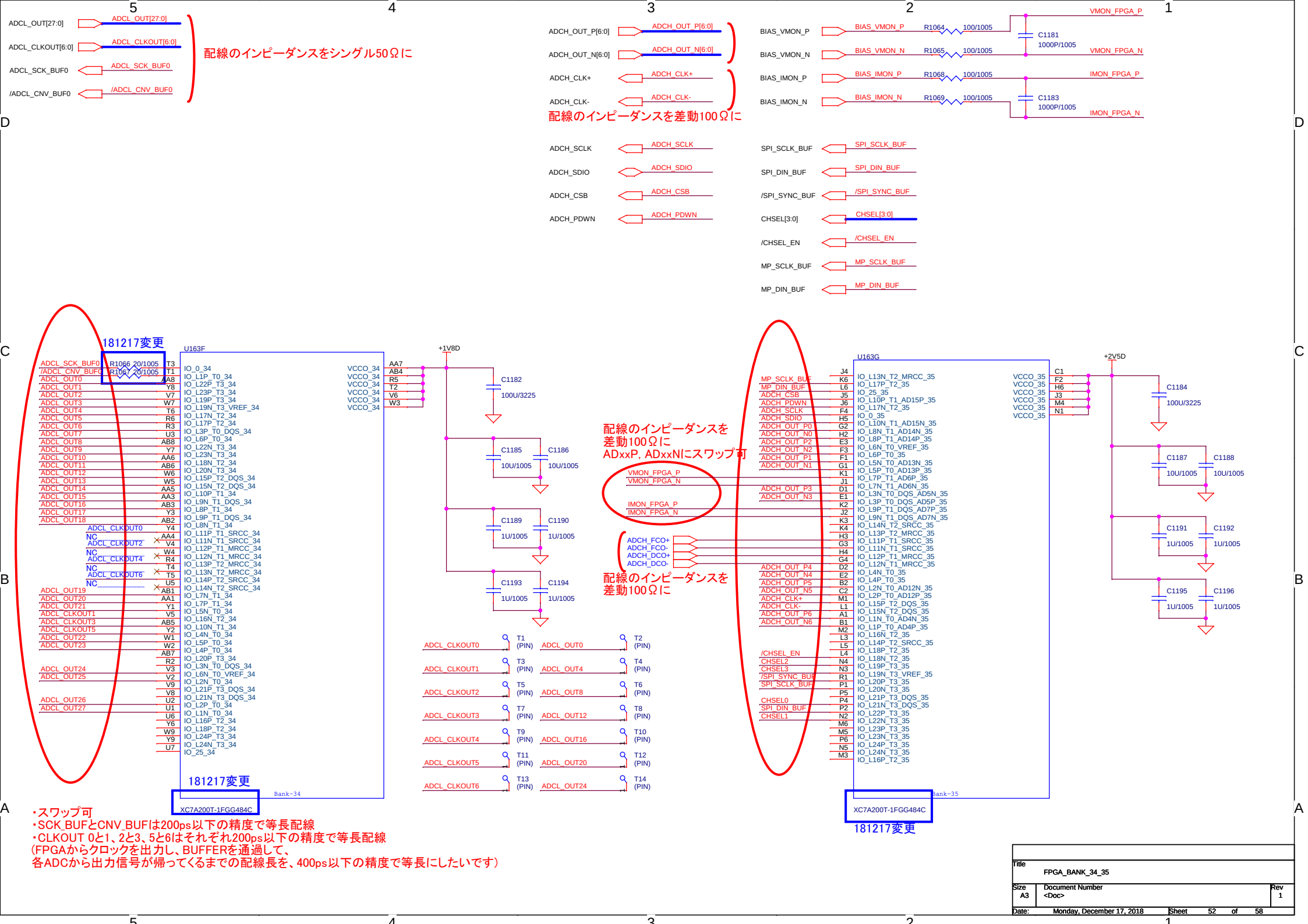
ADCL_OUT[27:0]
ADCL_CLKOUT[6:0]
ADCL_SCK_BUF0
/ADCL_CNV_BUF0
配線のインピーダンスをシングル50Ωに
ADCH_OUT_P[6:0]
ADCH_OUT_N[6:0]
ADCH_CLK+
ADCH_CLK-
配線のインピーダンスを差動100Ωに
BIAS_VMON_P
BIAS_VMON_N
BIAS_IMON_P
BIAS_IMON_N
R1064 100/1005
R1065 100/1005
R1068 100/1005
R1069 100/1005
C1181 1000P/1005
C1183 1000P/1005
VMON_FPGA_P
VMON_FPGA_N
IMON_FPGA_P
IMON_FPGA_N
ADCH_SCLK
ADCH_SDIO
ADCH_CSB
ADCH_PDWN
SPI_SCLK_BUF
SPI_DIN_BUF
/SPI_SYNC_BUF
CHSEL[3:0]
/CHSEL_EN
MP_SCLK_BUF
MP_DIN_BUF
181217変更
U163F
R1066 20/1005
R1067 20/1005
ADCL_SCK_BUF0
/ADCL_CNV_BUF0
ADCL_OUT0
ADCL_OUT1
ADCL_OUT2
ADCL_OUT3
ADCL_OUT4
ADCL_OUT5
ADCL_OUT6
ADCL_OUT7
ADCL_OUT8
ADCL_OUT9
ADCL_OUT10
ADCL_OUT11
ADCL_OUT12
ADCL_OUT13
ADCL_OUT14
ADCL_OUT15
ADCL_OUT16
ADCL_OUT17
ADCL_OUT18
ADCL_CLKOUT0
ADCL_CLKOUT2
ADCL_CLKOUT4
ADCL_CLKOUT6
NC
ADCL_OUT19
ADCL_OUT20
ADCL_OUT21
ADCL_CLKOUT1
ADCL_CLKOUT3
ADCL_CLKOUT5
ADCL_OUT22
ADCL_OUT23
ADCL_OUT24
ADCL_OUT25
ADCL_OUT26
ADCL_OUT27
IO_0_34
IO_L1P_T0_34
IO_L22P_T3_34
IO_L23P_T3_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L17N_T2_34
IO_L17P_T2_34
IO_L3P_T0_DQS_34
IO_L6P_T0_34
IO_L22N_T3_34
IO_L23N_T3_34
IO_L18N_T2_34
IO_L20N_T3_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L10P_T1_34
IO_L9N_T1_DQS_34
IO_L8P_T1_34
IO_L9P_T1_DQS_34
IO_L8N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L7N_T1_34
IO_L7P_T1_34
IO_L5N_T0_34
IO_L16N_T2_34
IO_L10N_T1_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L4P_T0_34
IO_L20P_T3_34
IO_L3N_T0_DQS_34
IO_L6N_T0_VREF_34
IO_L2N_T0_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L2P_T0_34
IO_L1N_T0_34
IO_L16P_T2_34
IO_L18P_T2_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
Bank-34
XC7A200T-1FGG484C
VCCO_34
AA7
AB4
R5
T2
V6
W3
+1V8D
C1182 100U/3225
C1185 10U/1005
C1186 10U/1005
C1189 1U/1005
C1190 1U/1005
C1193 1U/1005
C1194 1U/1005
ADCL_CLKOUT0 T1 (PIN) ADCL_OUT0 T2 (PIN)
ADCL_CLKOUT1 T3 (PIN) ADCL_OUT4 T4 (PIN)
ADCL_CLKOUT2 T5 (PIN) ADCL_OUT8 T6 (PIN)
ADCL_CLKOUT3 T7 (PIN) ADCL_OUT12 T8 (PIN)
ADCL_CLKOUT4 T9 (PIN) ADCL_OUT16 T10 (PIN)
ADCL_CLKOUT5 T11 (PIN) ADCL_OUT20 T12 (PIN)
ADCL_CLKOUT6 T13 (PIN) ADCL_OUT24 T14 (PIN)
181217変更
・スワップ可
・SCK_BUFとCNV_BUFは200ps以下の精度で等長配線
・CLKOUT 0と1、2と3、5と6はそれぞれ200ps以下の精度で等長配線
(FPGAからクロックを出力し、BUFFERを通過して、
各ADCから出力信号が帰ってくるまでの配線長を、400ps以下の精度で等長にしたいです)
配線のインピーダンスを
差動100Ωに
ADxxP, ADxxNにスワップ可
VMON_FPGA_P
VMON_FPGA_N
IMON_FPGA_P
IMON_FPGA_N
ADCH_FCO+
ADCH_FCO-
ADCH_DCO+
ADCH_DCO-
配線のインピーダンスを
差動100Ωに
U163G
MP_SCLK_BUF
MP_DIN_BUF
ADCH_CSB
ADCH_PDWN
ADCH_SCLK
ADCH_SDIO
ADCH_OUT_P0
ADCH_OUT_N0
ADCH_OUT_P2
ADCH_OUT_N2
ADCH_OUT_P1
ADCH_OUT_N1
ADCH_OUT_P3
ADCH_OUT_N3
ADCH_OUT_P4
ADCH_OUT_N4
ADCH_OUT_P5
ADCH_OUT_N5
ADCH_CLK+
ADCH_CLK-
ADCH_OUT_P6
ADCH_OUT_N6
/CHSEL_EN
CHSEL2
CHSEL3
/SPI_SYNC_BUF
SPI_SCLK_BUF
CHSEL0
SPI_DIN_BUF
CHSEL1
IO_L13N_T2_MRCC_35
IO_L17P_T2_35
IO_25_35
IO_L10P_T1_AD15P_35
IO_L17N_T2_35
IO_0_35
IO_L10N_T1_AD15N_35
IO_L8N_T1_AD14N_35
IO_L8P_T1_AD14P_35
IO_L6N_T0_VREF_35
IO_L6P_T0_35
IO_L5N_T0_AD13N_35
IO_L5P_T0_AD13P_35
IO_L7P_T1_AD6P_35
IO_L7N_T1_AD6N_35
IO_L3N_T0_DQS_AD5N_35
IO_L3P_T0_DQS_AD5P_35
IO_L9P_T1_DQS_AD7P_35
IO_L9N_T1_DQS_AD7N_35
IO_L14N_T2_SRCC_35
IO_L13P_T2_MRCC_35
IO_L11P_T1_SRCC_35
IO_L11N_T1_SRCC_35
IO_L12P_T1_MRCC_35
IO_L12N_T1_MRCC_35
IO_L4N_T0_35
IO_L4P_T0_35
IO_L2N_T0_AD12N_35
IO_L2P_T0_AD12P_35
IO_L15P_T2_DQS_35
IO_L15N_T2_DQS_35
IO_L1N_T0_AD4N_35
IO_L1P_T0_AD4P_35
IO_L16N_T2_35
IO_L14P_T2_SRCC_35
IO_L18P_T2_35
IO_L18N_T2_35
IO_L19P_T3_35
IO_L19N_T3_VREF_35
IO_L20P_T3_35
IO_L20N_T3_35
IO_L21P_T3_DQS_35
IO_L21N_T3_DQS_35
IO_L22P_T3_35
IO_L22N_T3_35
IO_L23P_T3_35
IO_L23N_T3_35
IO_L24P_T3_35
IO_L24N_T3_35
IO_L16P_T2_35
Bank-35
XC7A200T-1FGG484C
181217変更
VCCO_35
C1
F2
H6
J3
M4
N1
+2V5D
C1184 100U/3225
C1187 10U/1005
C1188 10U/1005
C1191 1U/1005
C1192 1U/1005
C1195 1U/1005
C1196 1U/1005
Title
FPGA_BANK_34_35
Size
A3
Document Number
<Doc>
Rev
1
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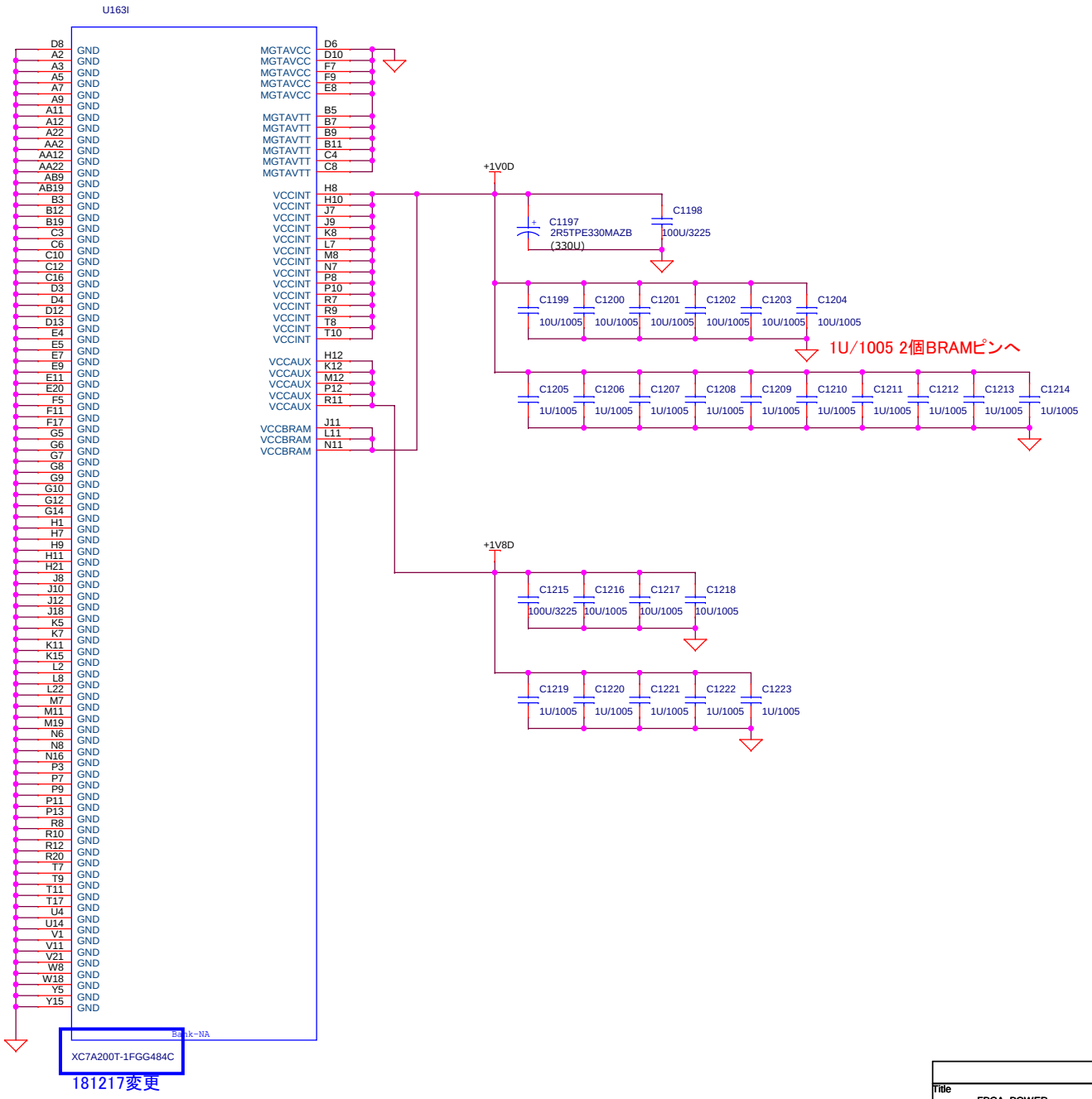

Title	FPGA_POWER	
Size A3	Document Number <Doc>	Rev 1
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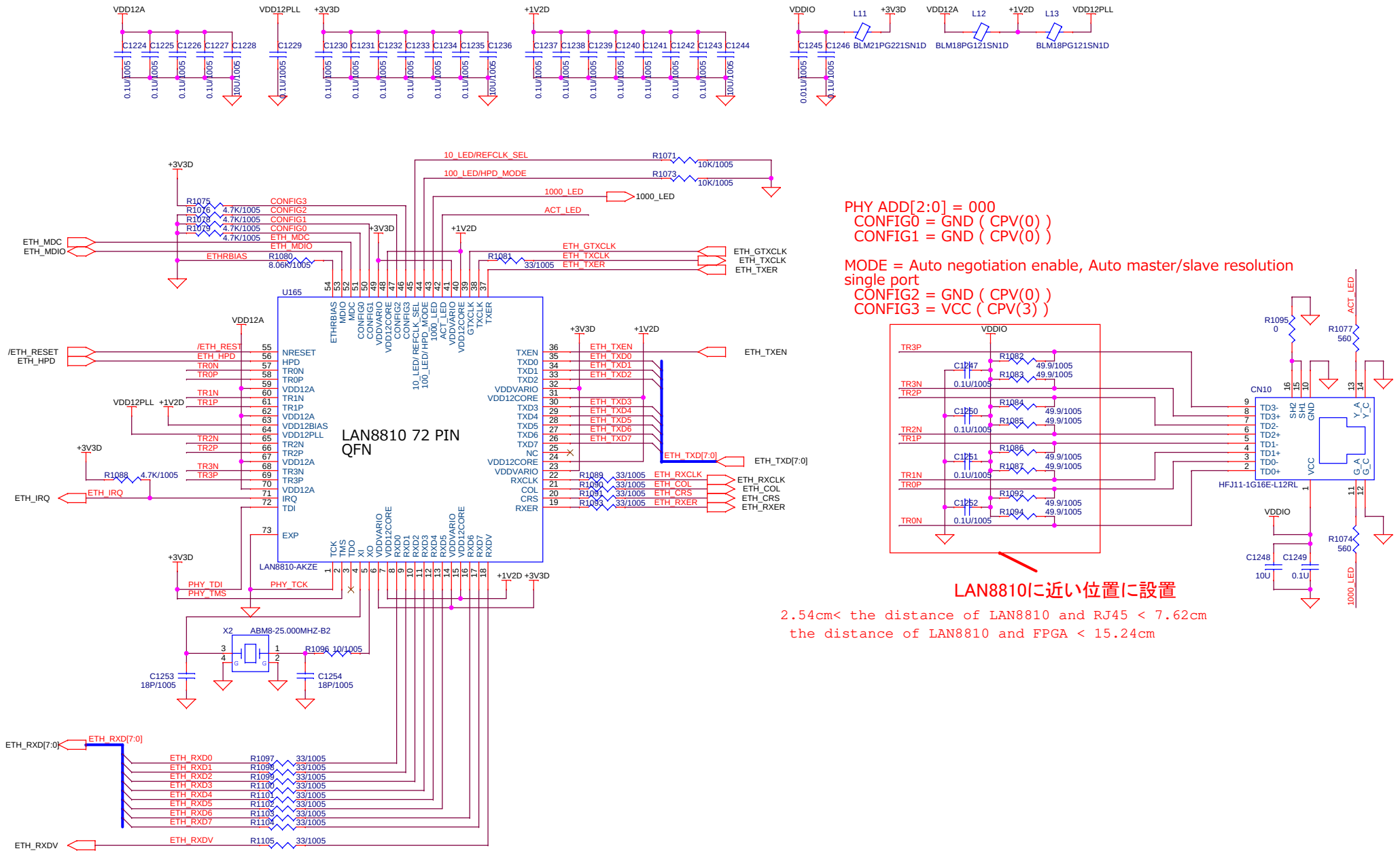

PHY ADD[2:0] = 000
CONFIG0 = GND (CPV(0))
CONFIG1 = GND (CPV(0))

MODE = Auto negotiation enable, Auto master/slave resolution single port
CONFIG2 = GND (CPV(0))
CONFIG3 = VCC (CPV(3))

LAN8810に近い位置に設置

2.54cm< the distance of LAN8810 and RJ45 < 7.62cm
the distance of LAN8810 and FPGA < 15.24cm

HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION, KEK		
Title: ETHPHY		
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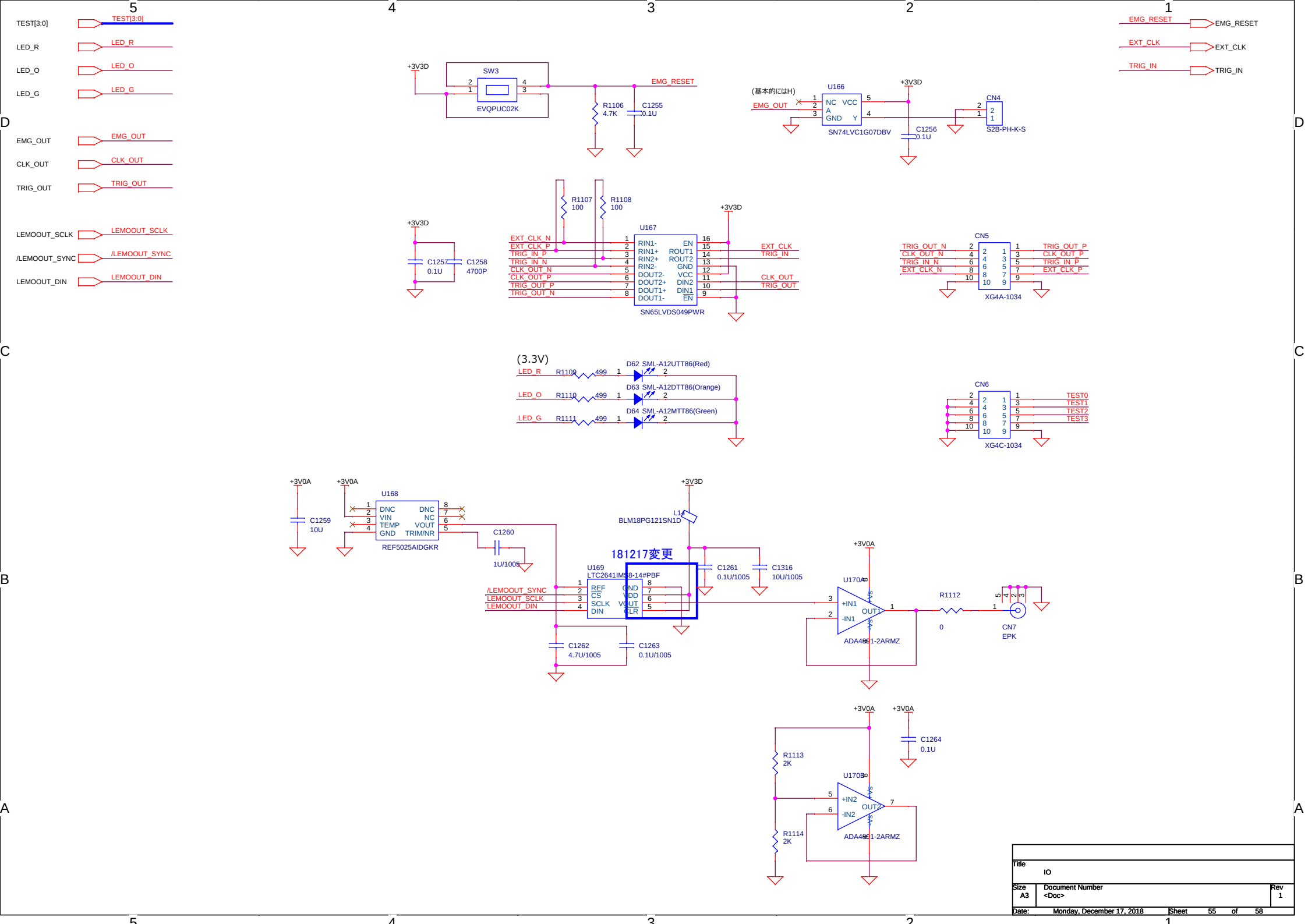
TEST[3:0]
LED_R
LED_O
LED_G
EMG_OUT
CLK_OUT
TRIG_OUT
LEMOOUT_SCLK
/LEMOOUT_SYNC
LEMOOUT_DIN
EMG_RESET
EXT_CLK
TRIG_IN
SW3
EVQPUC02K
R1106 4.7K
C1255 0.1U
U166
SN74LVC1G07DBV
C1256 0.1U
CN4
S2B-PH-K-S
R1107 100
R1108 100
U167
SN65LVDS049PWR
C1257 0.1U
C1258 4700P
CN5
XG4A-1034
(3.3V)
D62 SML-A12UTT86(Red)
D63 SML-A12DTT86(Orange)
D64 SML-A12MTT86(Green)
CN6
XG4C-1034
U168
REF5025AIDGKR
C1259 10U
C1260 1U/1005
L1 BLM18PG121SN1D
181217変更
U169
LTC2641IMS8-14#PBF
C1261 0.1U/1005
C1316 10U/1005
C1262 4.7U/1005
C1263 0.1U/1005
U170A
ADA4891-2ARMZ
R1112 0
CN7 EPK
U170B
R1113 2K
R1114 2K
C1264 0.1U
Title IO
Size A3
Document Number <Doc>
Rev 1
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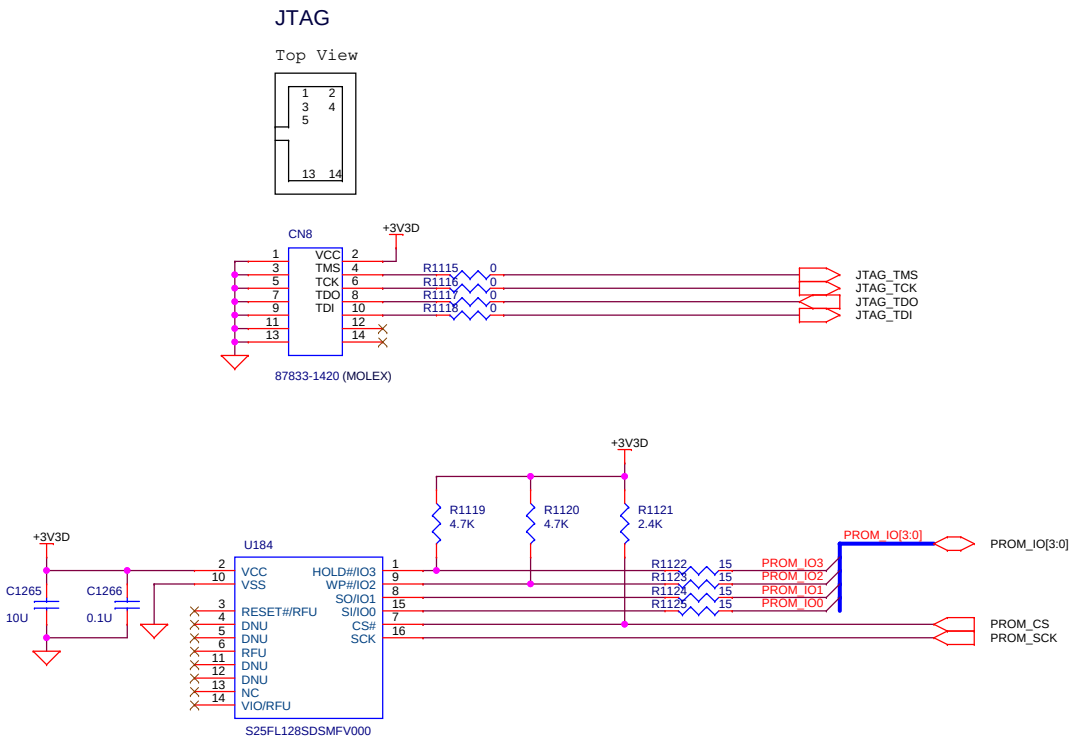

Title	PROM	
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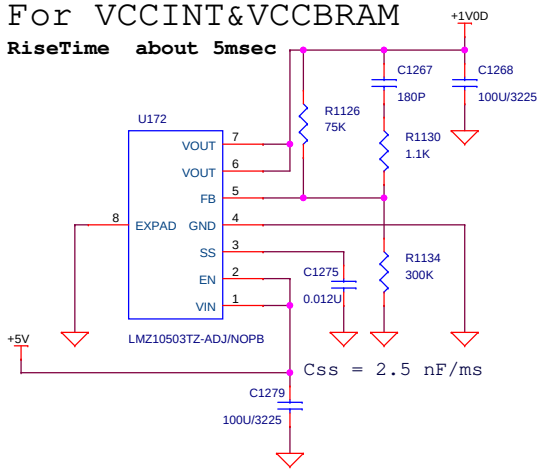
For VCCINT&VCCBRAM

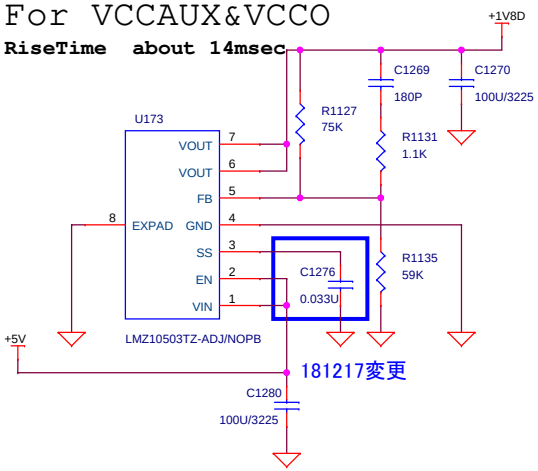
RiseTime about 5msec



(+5.0V -> +1.0V) (3.0A)

For VCCAUX&VCCO

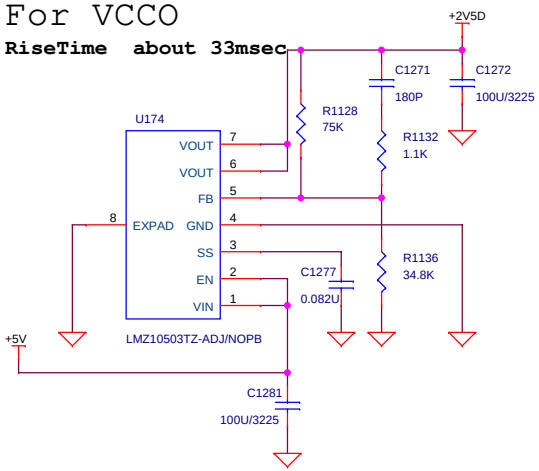
RiseTime about 14msec



(+5.0V -> +1.8V) (3.0A)

For VCCO

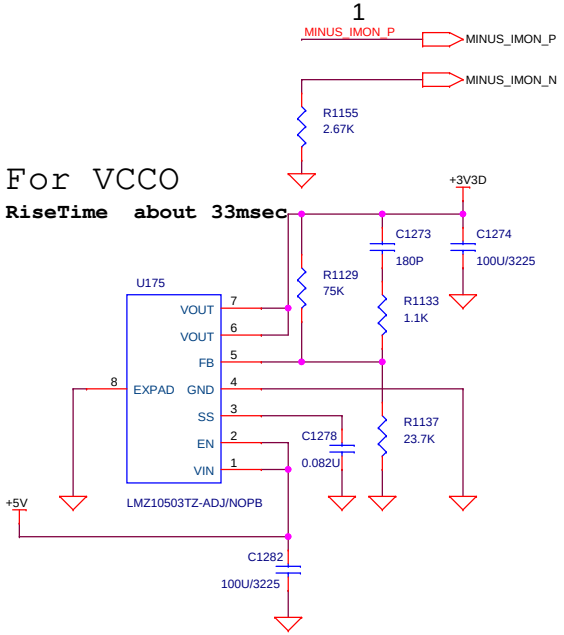
RiseTime about 33msec



(+5.0V -> +2.5V) (3.0A)

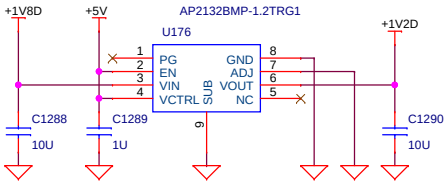
For VCCO

RiseTime about 33msec

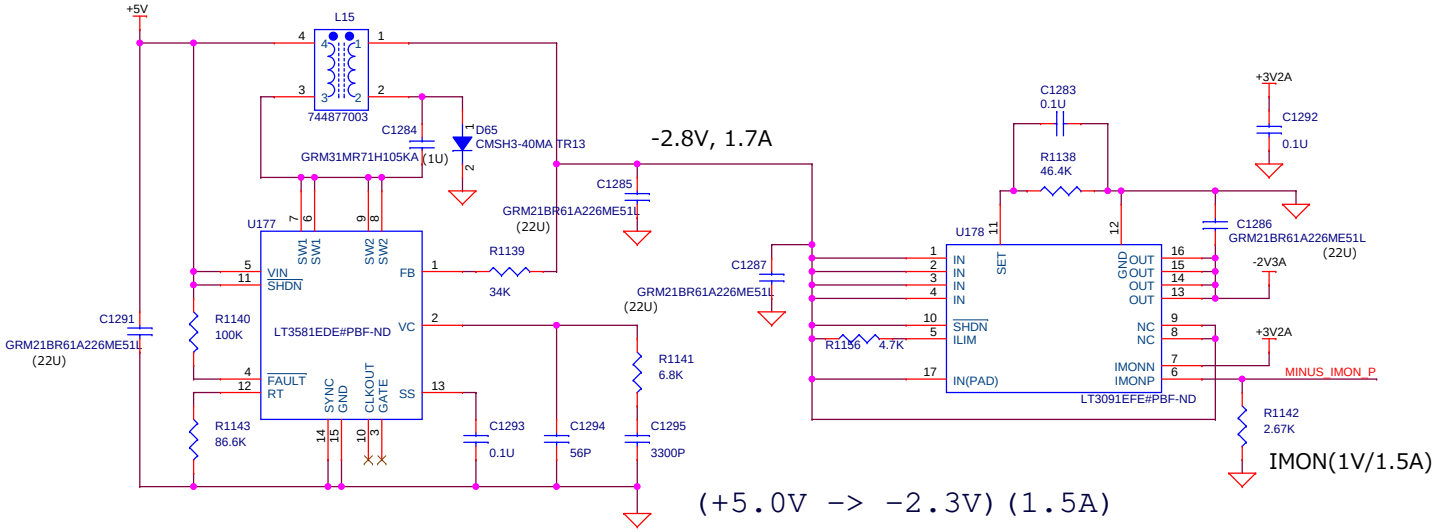


(+5.0V -> +3.3V) (3.0A)

For ETHERNET



(+1.8V -> +1.2V) (2.0A)



(+5.0V -> -2.3V) (1.5A)

Title	REG1	
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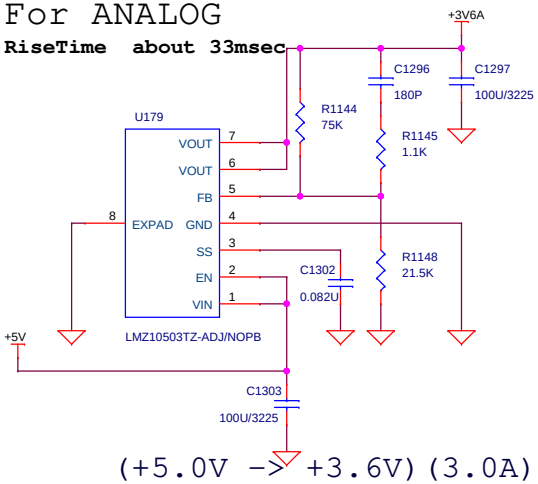
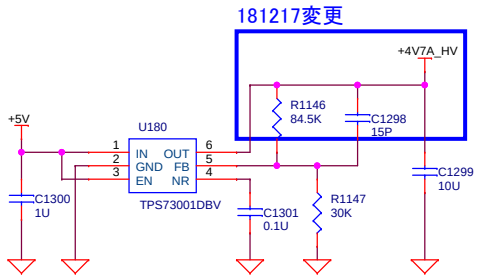
For ANALOG

RiseTime about 33msec

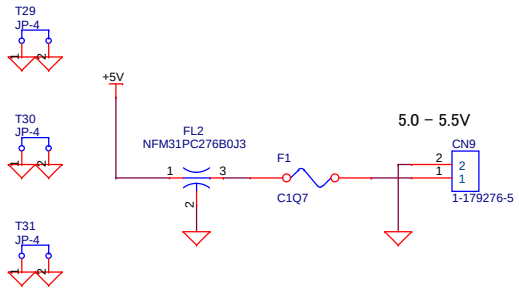


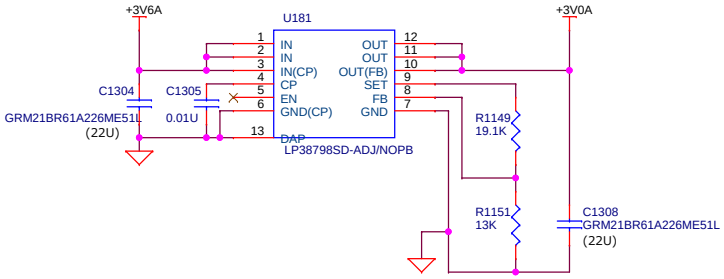
(+5.0V -> +3.6V)(3.0A)

181217変更

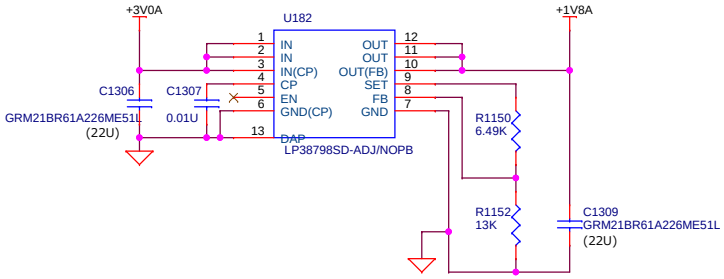


(+5.0V -> +4.7V_HV)(0.2A)

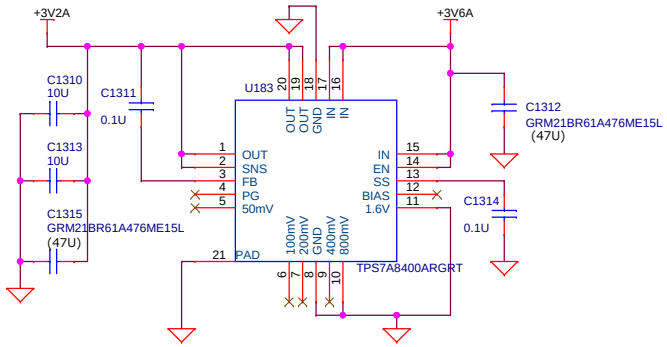




(+3.6V -> +3.0V)(0.8A)



(+3.0V -> +1.8V)(0.8A)



(+3.6V -> +3.2V)(3A)

Title	REG2	
Size A3	Document Number <Doc>	Rev 1
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