

# 印刷用資料

- OPEN-IT FPGA トレーニングコース -

第 1.1 版

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1 日目 : 4.1.節で入力する HDL コード

**TEST.v**

```
1 `timescale 1ns / 1ps
2 ////////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date:    17:52:09 08/07/2014
7 // Design Name:
8 // Module Name:    TEST
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ////////////////////////////////////////////////////////////////////
21 module TEST(
22     input SW_A,
23     input SW_B,
24     output LED0
25 );
26
27     assign LED0 = SW_A & SW_B;
28
29 endmodule
```

1 日目：4.2.節で入力する HDL コード

TEST\_TB.v

```
1 `timescale 1ns / 1ps
2
3 ///////////////////////////////////////////////////////////////////
4 // Company:
5 // Engineer:
6 //
7 // Create Date: 17:54:06 08/07/2014
8 // Design Name: TEST
9 // Module Name: C:/Temp/FPGA_Seminar/ISE/TEST_TB.v
10 // Project Name: ISE
11 // Target Device:
12 // Tool versions:
13 // Description:
14 //
15 // Verilog Test Fixture created by ISE for module: TEST
16 //
17 // Dependencies:
18 //
19 // Revision:
20 // Revision 0.01 - File Created
21 // Additional Comments:
22 //
23 ///////////////////////////////////////////////////////////////////
24
25 module TEST_TB;
26
27     // Inputs
28     reg SW_A;
29     reg SW_B;
30
31     // Outputs
32     wire LED0;
33
34     // Instantiate the Unit Under Test (UUT)
35     TEST uut (
36         .SW_A(SW_A),
37         .SW_B(SW_B),
38         .LED0(LED0)
39     );
40
41     initial begin
42         // Initialize Inputs
43         SW_A = 0;
44         SW_B = 0;
45
46         // Wait 100 ns for global reset to finish
47         #100 SW_A = 1'b1;
48         #300 SW_B = 1'b1;
49         #200 SW_A = 1'b0;
50
51         // Add stimulus here
52
53     end
54
55 endmodule
56
```

1 日目 4.3.節、2 日目 7.2 節  
で入力するピンアサイン

# ピンリスト

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昨日行った事を思い出しながら  
Plan Aheadを使用してピン設定を行ってください

Name	Site	I/O Std.	Drive Str.	Pull type	Slew
CLK50M	P57	LVCMOS33			
RST_SW	P72	LVCMOS33			
SW_A	P70	LVCMOS33			
SW_B	P71	LVCMOS33			
LED7	P130	LVCMOS33	12		Slow
LED2	P139	LVCMOS33	12		Slow
LED1	P141	LVCMOS33	12		Slow
LED0	P142	LVCMOS33	12		Slow

記載が無い項目はdefaultを設定



1 日目 : 4.3.節で作成する UCF ファイル

TEST.ucf

```
1 |
2 | # PlanAhead Generated physical constraints
3 |
4 | NET "LEDO" LOC = P142;
5 |
6 | # PlanAhead Generated IO constraints
7 |
8 | NET "LEDO" IOSTANDARD = LVCMOS33;
9 |
10 | # PlanAhead Generated physical constraints
11 |
12 | NET "SW_A" LOC = P70;
13 |
14 | # PlanAhead Generated IO constraints
15 |
16 | NET "SW_A" IOSTANDARD = LVCMOS33;
17 |
18 | # PlanAhead Generated physical constraints
19 |
20 | NET "SW_B" LOC = P71;
21 |
22 | # PlanAhead Generated IO constraints
23 |
24 | NET "SW_B" IOSTANDARD = LVCMOS33;
```

2 日目 : 7.1.節で入力する HDL コード

TEST.v

```
1 `timescale 1ns / 1ps
2 ////////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date:    17:52:09 08/07/2014
7 // Design Name:
8 // Module Name:    TEST
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ////////////////////////////////////////////////////////////////////
21 module TEST(
22     input CLK50M,
23     input RST_SW,
24     input SW_A,
25     input SW_B,
26     output LED0,
27     output LED7
28 );
29
30     assign LED0 = SW_A & SW_B;
31
32     reg [31:0] syn_counter;
33
34     always @(posedge CLK50M or negedge RST_SW)begin
35         if(!RST_SW)begin
36             syn_counter[31:0] <= 32'd0;
37         end else begin
38             syn_counter[31:0] <= syn_counter[31:0] + 32'd1;
39         end
40     end
41
42     assign LED7 = syn_counter[28];
43
44 endmodule
```

2 日目 : 7.2.節で入力する HDL コード

TEST\_TB.v

```

1 `timescale 1ns / 1ps
2
3 ///////////////////////////////////////////////////////////////////
4 // Company:
5 // Engineer:
6 //
7 // Create Date: 17:54:06 08/07/2014
8 // Design Name: TEST
9 // Module Name: C:/Temp/FPGA_Seminar/ISE/TEST_TB.v
10 // Project Name: ISE
11 // Target Device:
12 // Tool versions:
13 // Description:
14 //
15 // Verilog Test Fixture created by ISE for module: TEST
16 //
17 // Dependencies:
18 //
19 // Revision:
20 // Revision 0.01 - File Created
21 // Additional Comments:
22 //
23 ///////////////////////////////////////////////////////////////////
24
25 module TEST_TB;
26
27     // Inputs
28     reg CLK50M;
29     reg RST_SW;
30     reg SW_A;
31     reg SW_B;
32
33     // Outputs
34     wire LED0;
35     wire LED7;
36
37     // Instantiate the Unit Under Test (UUT)
38     TEST uut (
39         .CLK50M(CLK50M),
40         .RST_SW(RST_SW),
41         .SW_A(SW_A),
42         .SW_B(SW_B),
43         .LED0(LED0),
44         .LED7(LED7)
45     );
46
47     initial begin
48         // Initialize Inputs
49         SW_A = 0;
50         SW_B = 0;
51
52         // Wait 100 ns for global reset to finish
53         #100 SW_A = 1'b1;
54         #300 SW_B = 1'b1;
55         #200 SW_A = 1'b0;
56
57         // Add stimulus here
58
59     end
60
61     /* Clock */
62     parameter PERIOD = 20;
63
64     always begin
65         CLK50M = 1'b0;
66         #(PERIOD/2) CLK50M = 1'b1;
67         #(PERIOD/2);
68     end
69
70     /* Reset */
71     initial begin
72         RST_SW = 1'b0;
73         #700 RST_SW = 1'b1;
74     end
75
76 endmodule
77

```

2日目：7.2.節で作成する UCF ファイル

TEST.ucf

```
1 |
2 | # PlanAhead Generated physical constraints
3 |
4 | NET "LEDO" LOC = P142;
5 |
6 | # PlanAhead Generated IO constraints
7 |
8 | NET "LEDO" IOSTANDARD = LVCMOS33;
9 |
10 | # PlanAhead Generated physical constraints
11 |
12 | NET "SW_A" LOC = P70;
13 |
14 | # PlanAhead Generated IO constraints
15 |
16 | NET "SW_A" IOSTANDARD = LVCMOS33;
17 |
18 | # PlanAhead Generated physical constraints
19 |
20 | NET "SW_B" LOC = P71;
21 |
22 | # PlanAhead Generated IO constraints
23 |
24 | NET "SW_B" IOSTANDARD = LVCMOS33;
25 |
26 | # PlanAhead Generated physical constraints
27 |
28 | NET "CLK50M" LOC = P57;
29 |
30 | # PlanAhead Generated IO constraints
31 |
32 | NET "CLK50M" IOSTANDARD = LVCMOS33;
33 |
34 | # PlanAhead Generated physical constraints
35 |
36 | NET "LED7" LOC = P130;
37 |
38 | # PlanAhead Generated IO constraints
39 |
40 | NET "LED7" IOSTANDARD = LVCMOS33;
41 |
42 | # PlanAhead Generated physical constraints
43 |
44 | NET "RST_SW" LOC = P72;
45 |
46 | # PlanAhead Generated IO constraints
47 |
48 | NET "RST_SW" IOSTANDARD = LVCMOS33;
```



2 日目 : 10.節で入力する HDL コード

TEST.v

```

1 `timescale 1ns / 1ps
2 ////////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date:    17:52:09 08/07/2014
7 // Design Name:
8 // Module Name:    TEST
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ////////////////////////////////////////////////////////////////////
21 module TEST(
22     input CLK50M,
23     input RST_SW,
24     input SW_A,
25     input SW_B,
26     output LED0,
27     output LED7
28 );
29
30 wire CLK100M;
31 wire sysRstN;
32
33 sys_dcm SYS_DCM (
34     .CLKIN_IN      ( CLK50M ),
35     .RST_IN        ( ^RST_SW ),
36     .CLKFX_OUT     (),
37     .CLKIN_IBUFG_OUT (),
38     .CLKO_OUT      (),
39     .CLK2X_OUT     ( CLK100M ),
40     .LOCKED_OUT    ( sysRstN )
41 );
42
43 assign LED0 = SW_A & SW_B;
44
45 reg [31:0] syn_counter;
46
47 always @(posedge CLK100M or negedge sysRstN)begin
48     if(!sysRstN)begin
49         syn_counter[31:0] <= 32'd0;
50     end else begin
51         syn_counter[31:0] <= syn_counter[31:0] + 32'd1;
52     end
53 end
54
55 assign LED7 = syn_counter[28];
56
57 endmodule

```

2 日目 : 10 節で作成する UCF ファイル

TEST.ucf

```
1 |
2 | # PlanAhead Generated physical constraints
3 |
4 | NET "LEDO" LOC = P142;
5 |
6 | # PlanAhead Generated IO constraints
7 |
8 | NET "LEDO" IOSTANDARD = LVCMOS33;
9 |
10 | # PlanAhead Generated physical constraints
11 |
12 | NET "SW_A" LOC = P70;
13 |
14 | # PlanAhead Generated IO constraints
15 |
16 | NET "SW_A" IOSTANDARD = LVCMOS33;
17 |
18 | # PlanAhead Generated physical constraints
19 |
20 | NET "SW_B" LOC = P71;
21 |
22 | # PlanAhead Generated IO constraints
23 |
24 | NET "SW_B" IOSTANDARD = LVCMOS33;
25 |
26 | # PlanAhead Generated physical constraints
27 |
28 | NET "CLK50M" LOC = P57;
29 |
30 | # PlanAhead Generated IO constraints
31 |
32 | NET "CLK50M" IOSTANDARD = LVCMOS33;
33 |
34 | # PlanAhead Generated physical constraints
35 |
36 | NET "LED7" LOC = P130;
37 |
38 | # PlanAhead Generated IO constraints
39 |
40 | NET "LED7" IOSTANDARD = LVCMOS33;
41 |
42 | # PlanAhead Generated physical constraints
43 |
44 | NET "RST_SW" LOC = P72;
45 |
46 | # PlanAhead Generated IO constraints
47 |
48 | NET "RST_SW" IOSTANDARD = LVCMOS33;
49 |
50 | NET "CLK50M" CLOCK_DEDICATED_ROUTE = FALSE;
```