印刷用資料

- OPEN-IT FPGA トレーニングコース -

第 1.1 版

2014 年 8 月 25 日

高エネルギー加速器研究機構

素粒子原子核研究所

エレクトロニクスシステムグループ

内田 智久

1 日目：4.1.節で入力する HDL コード

TEST.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    17:52:09 08/07/2014
// Design Name:
// Module Name:    TEST
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module TEST(
    input SW_A,
    input SW_B,
    output LED0
    );

    assign LED0 = SW_A & SW_B;

endmodule
```

1 日目：4.2.節で入力する HDL コード

TEST_TB.v

```
`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:   17:54:06 08/07/2014
// Design Name:   TEST
// Module Name:   C:/Temp/FPGA_Seminar/ISE/TEST_TB.v
// Project Name:  ISE
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: TEST
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////

module TEST_TB;

    // Inputs
    reg SW_A;
    reg SW_B;

    // Outputs
    wire LED0;

    // Instantiate the Unit Under Test (UUT)
    TEST uut (
        .SW_A(SW_A),
        .SW_B(SW_B),
        .LED0(LED0)
    );

    initial begin
        // Initialize Inputs
        SW_A = 0;
        SW_B = 0;

        // Wait 100 ns for global reset to finish
        #100 SW_A = 1'b1;
        #300 SW_B = 1'b1;
        #200 SW_A = 1'b0;

        // Add stimulus here

    end

endmodule

```

1 日目 4.3.節、2 日目 7.2 節
で入力するピンアサイン

ピンリスト

昨日行った事を思い出しながら
Plan Aheadを使用してピン設定を行ってください

Name	Site	I/O Std.	Drive Str.	Pull type	Slew
CLK50M	P57	LVCMOS33			
RST_SW	P72	LVCMOS33			
SW_A	P70	LVCMOS33			
SW_B	P71	LVCMOS33			
LED7	P130	LVCMOS33	12		Slow
LED2	P139	LVCMOS33	12		Slow
LED1	P141	LVCMOS33	12		Slow
LED0	P142	LVCMOS33	12		Slow

記載が無き項目はdefaultを設定

1 日目：4.3.節で作成する UCF ファイル

TEST.ucf

```
1
2  # PlanAhead Generated physical constraints
3
4  NET "LED0" LOC = P142;
5
6  # PlanAhead Generated IO constraints
7
8  NET "LED0" IOSTANDARD = LVCMOS33;
9
10 # PlanAhead Generated physical constraints
11
12 NET "SW_A" LOC = P70;
13
14 # PlanAhead Generated IO constraints
15
16 NET "SW_A" IOSTANDARD = LVCMOS33;
17
18 # PlanAhead Generated physical constraints
19
20 NET "SW_B" LOC = P71;
21
22 # PlanAhead Generated IO constraints
23
24 NET "SW_B" IOSTANDARD = LVCMOS33;
```

2 日目：7.1.節で入力する HDL コード

TEST.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    17:52:09 08/07/2014
// Design Name:
// Module Name:    TEST
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module TEST(
    input CLK50M,
     input RST_SW,
    input SW_A,
    input SW_B,
    output LED0,
    output LED7
    );

    assign LED0 = SW_A & SW_B;

   reg [31:0] syn_counter;

   always @(posedge CLK50M or negedge RST_SW)begin
       if(!RST_SW)begin
           syn_counter[31:0] <= 32'd0;
         end else begin
           syn_counter[31:0] <= syn_counter[31:0] + 32'd1;
         end
    end

    assign LED7 = syn_counter[28];

endmodule
```

2 日目：7.2.節で入力する HDL コード

TEST_TB.v

```
`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:   17:54:06 08/07/2014
// Design Name:   TEST
// Module Name:   C:/Temp/FPGA_Seminar/ISE/TEST_TB.v
// Project Name:  ISE
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: TEST
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////

module TEST_TB;

    // Inputs
   reg CLK50M;
   reg RST_SW;
    reg SW_A;
    reg SW_B;

    // Outputs
    wire LED0;
   wire LED7;

    // Instantiate the Unit Under Test (UUT)
    TEST uut (
      .CLK50M(CLK50M),
        .RST_SW(RST_SW),
        .SW_A(SW_A),
        .SW_B(SW_B),
        .LED0(LED0),
      .LED7(LED7)
    );

    initial begin
        // Initialize Inputs
        SW_A = 0;
        SW_B = 0;

        // Wait 100 ns for global reset to finish
        #100 SW_A = 1'b1;
        #300 SW_B = 1'b1;
        #200 SW_A = 1'b0;

        // Add stimulus here

    end

   /* Clock */
   parameter PERIOD = 20;

   always begin
      CLK50M = 1'b0;
        #(PERIOD/2) CLK50M = 1'b1;
        #(PERIOD/2);
    end

   /* Reset */
   initial begin
      RST_SW = 1'b0;
      #700 RST_SW = 1'b1;
    end

endmodule

```

２日目：7.2.節で作成する UCF ファイル

TEST.ucf

```
# PlanAhead Generated physical constraints

NET "LED0" LOC = P142;

# PlanAhead Generated IO constraints

NET "LED0" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "SW_A" LOC = P70;

# PlanAhead Generated IO constraints

NET "SW_A" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "SW_B" LOC = P71;

# PlanAhead Generated IO constraints

NET "SW_B" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "CLK50M" LOC = P57;

# PlanAhead Generated IO constraints

NET "CLK50M" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "LED7" LOC = P130;

# PlanAhead Generated IO constraints

NET "LED7" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "RST_SW" LOC = P72;

# PlanAhead Generated IO constraints

NET "RST_SW" IOSTANDARD = LVCMOS33;
```

2 日目：10.節で入力する HDL コード

TEST.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    17:52:09 08/07/2014
// Design Name:
// Module Name:    TEST
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module TEST(
    input CLK50M,
     input RST_SW,
    input SW_A,
    input SW_B,
    output LED0,
    output LED7
    );

    wire CLK100M;
    wire sysRstN;

    sys_dcm    SYS_DCM (
        .CLKIN_IN        ( CLK50M  ),
        .RST_IN          (~RST_SW  ),
        .CLKFX_OUT       (),
        .CLKIN_IBUFG_OUT (),
        .CLK0_OUT        (),
        .CLK2X_OUT       ( CLK100M ),
        .LOCKED_OUT      ( sysRstN )
    );

    assign LED0 = SW_A & SW_B;

   reg [31:0] syn_counter;

   always @(posedge CLK100M or negedge sysRstN)begin
       if(!sysRstN)begin
           syn_counter[31:0] <= 32'd0;
         end else begin
           syn_counter[31:0] <= syn_counter[31:0] + 32'd1;
         end
    end

    assign LED7 = syn_counter[28];

endmodule
```

2 日目：10 節で作成する UCF ファイル

TEST.ucf

```
# PlanAhead Generated physical constraints

NET "LED0" LOC = P142;

# PlanAhead Generated IO constraints

NET "LED0" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "SW_A" LOC = P70;

# PlanAhead Generated IO constraints

NET "SW_A" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "SW_B" LOC = P71;

# PlanAhead Generated IO constraints

NET "SW_B" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "CLK50M" LOC = P57;

# PlanAhead Generated IO constraints

NET "CLK50M" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "LED7" LOC = P130;

# PlanAhead Generated IO constraints

NET "LED7" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "RST_SW" LOC = P72;

# PlanAhead Generated IO constraints

NET "RST_SW" IOSTANDARD = LVCMOS33;

NET "CLK50M" CLOCK_DEDICATED_ROUTE = FALSE;
```