Super-Kamiokandeでの新エレキ開発とHV入れ替え

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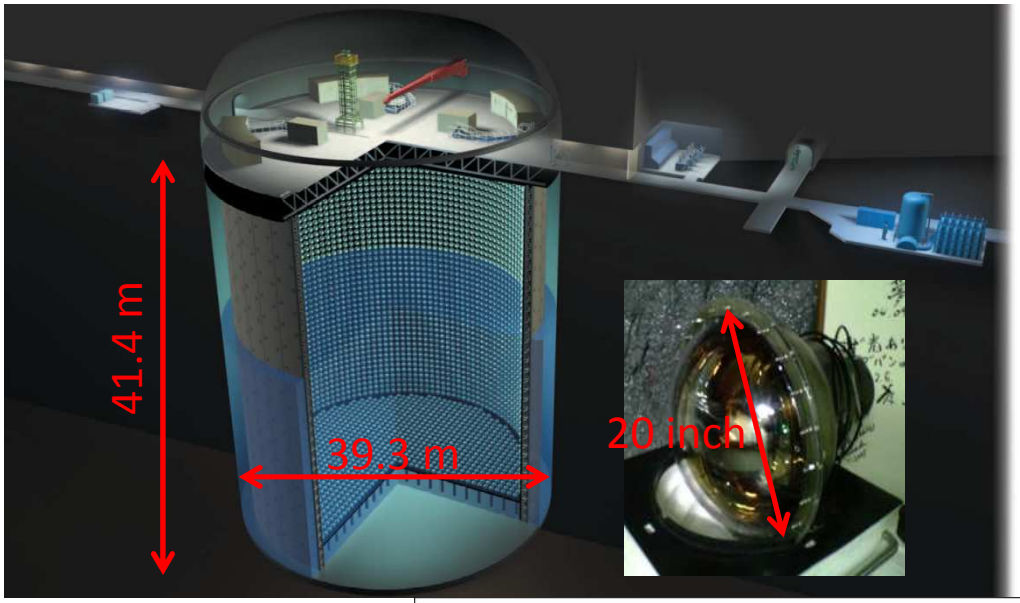
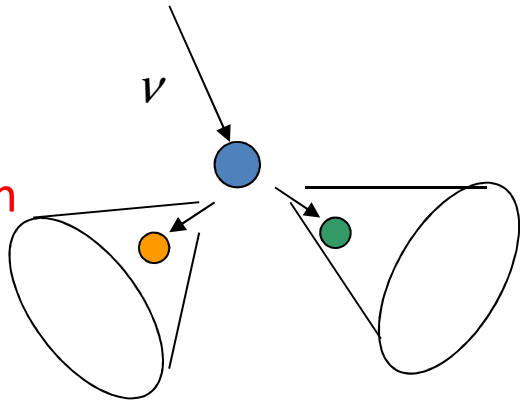
Introduction

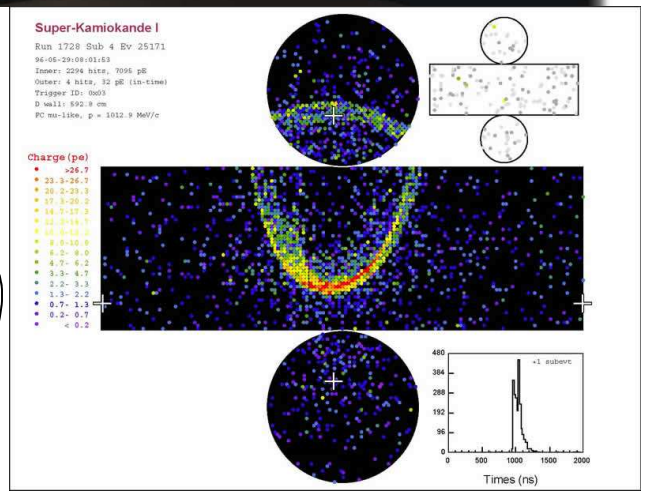
- Currently, we have two electronics upgrade plans at Super-Kamiokande.
  1. New data acquisition (DAQ) system for nearby supernova burst
     - Just add new system parallel to the current system
  2. Replace high voltage (HV) system for inner detector (ID) PMTs
     - Completely replace the old HV system for ID with new one in summer 2013.

Super-Kamiokande Detector

- Super-Kamiokande (SK) is a ring imaging water Cherenkov detector
  - 13,000 photomultiplier tubes (PMTs) equipped in 50,000 tons of water tank
- Physics Topics of SK
  - Atmospheric neutrino oscillation: Δm_{23}, θ_{23}
  - Solar neutrino oscillation: Δm_{12}, θ_{12}
  - Neutrino beam from accelerator (T2K): search for θ_{13}
  - Search for neutrinos from supernovae (burst or diffused)
  - Search for proton decay



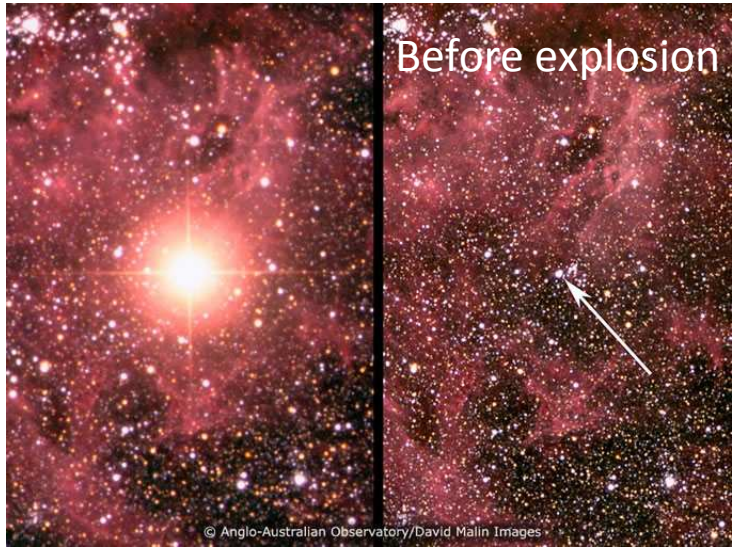


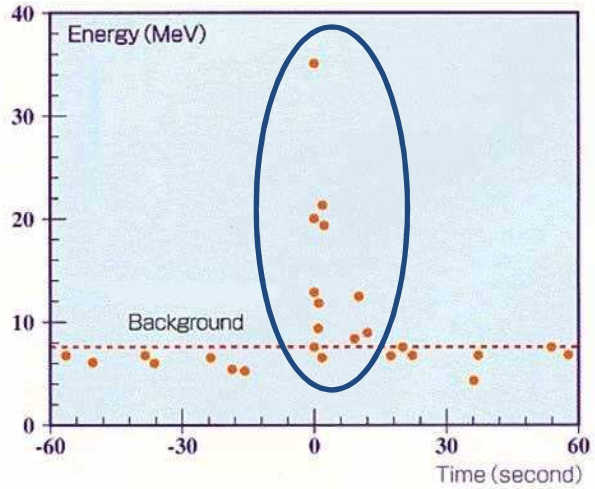


NEW DAQ SYSTEM FOR NEARBY SUPERNOVA BURST

Neutrino Astronomy

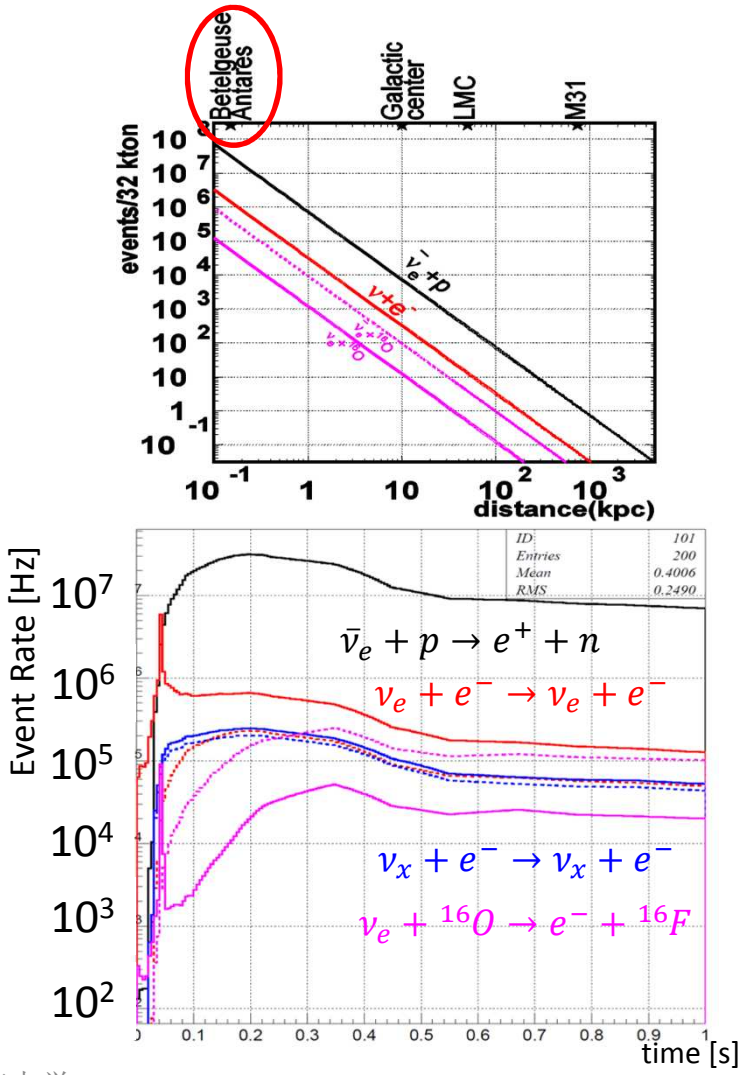
- Supernova Explosion (SN)
  - Collapse of a massive star
  - Release enormous amount of energy
    - Primarily (> 99%) in the form of neutrino
    - In just 10 seconds
- SN1987A
  - On February 23, 1987, SN occurred in Large Magellanic Clouds.
  - Kamiokande observed 11 events of neutrinos from SN.
- SN is expected to occur inside the Galaxy once every 10 to 50 years.
  - If a SN occurs at the center of the Galaxy, SK expects to detect about 10k neutrino events.





Nearby Supernova

- In June 2009, it was reported that the size of Betelgeuse (α Orionis) decreased by 15% over past 15 years.
  - C. H. Townes *et al.* 2009, *ApJ*, **697**, L127
- If a SN burst occurs at 500 ly from the earth, the total number of events in 10 s at SK reaches 30M and the maximum event rate exceeds 30 MHz.
  - Candidates
    - Betelgeuse: 640 ly
    - Antares: 550 ly

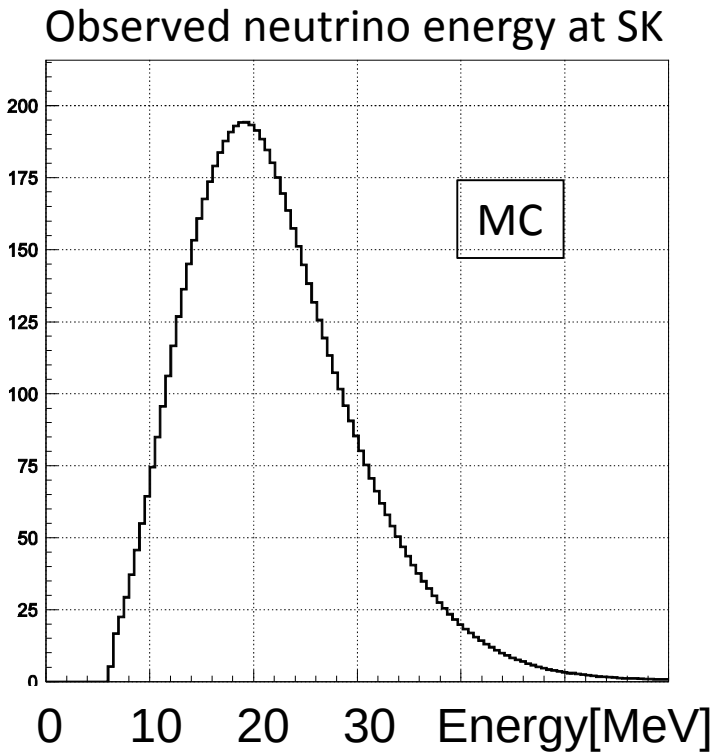


Current DAQ Capability

- SK DAQ system was renewed in 2008.
  - Larger charge dynamic range
  - Lower power consumption
  - High speed data transfer
- Current DAQ can process up to 6M events/10 s without losing data.
  - Bottleneck is mainly disk access.
  - Corresponds to ~1300 ly SN.
  - For 500-ly SN, only first 20% of data can be recorded.
- Implemented prescale (= 100) for such high event rate.
  - Inputting veto trigger into frontend electronics board to reduce data size for main DAQ system
  - Can avoid large dead time
  - Not enough to understand SN structure.

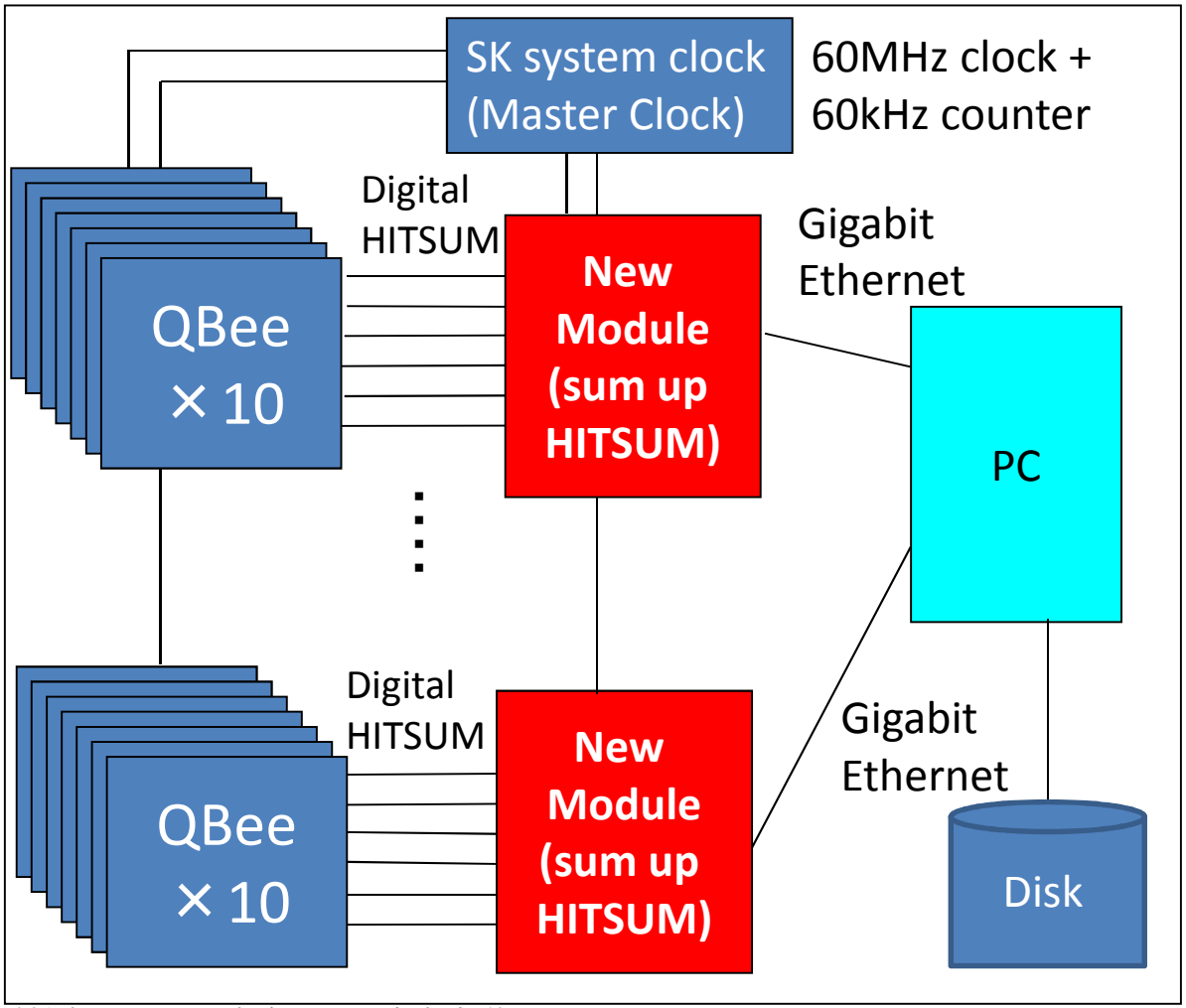
New DAQ System

- Need new DAQ system in parallel to the current system for the SN burst study.
- Requirements for new system:
  - Independent from current online DAQ system
  - Stable against event rate
- Utilize number of hit PMTs
  - Since energy distribution of SN neutrino is narrow, we can estimate the number of neutrinos from number of hits.



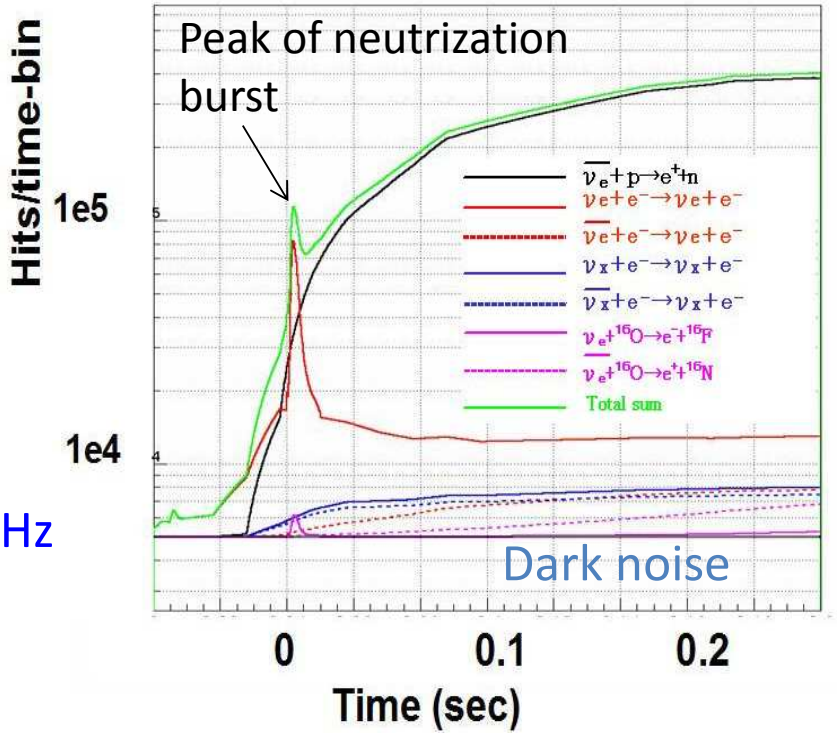
Schematic View of New DAQ System

- Digital HITSUM
  - Frontend electronics board (QBee) has an output of number of hit PMTs.
  - Provided in 60 MHz
- New module
  - Sums up HITSUMs from 10 boards.
  - Average over 1000 clocks. (Next slide.)
  - Summed-up numbers are read out by PC through Gigabit Ethernet and written to disk.



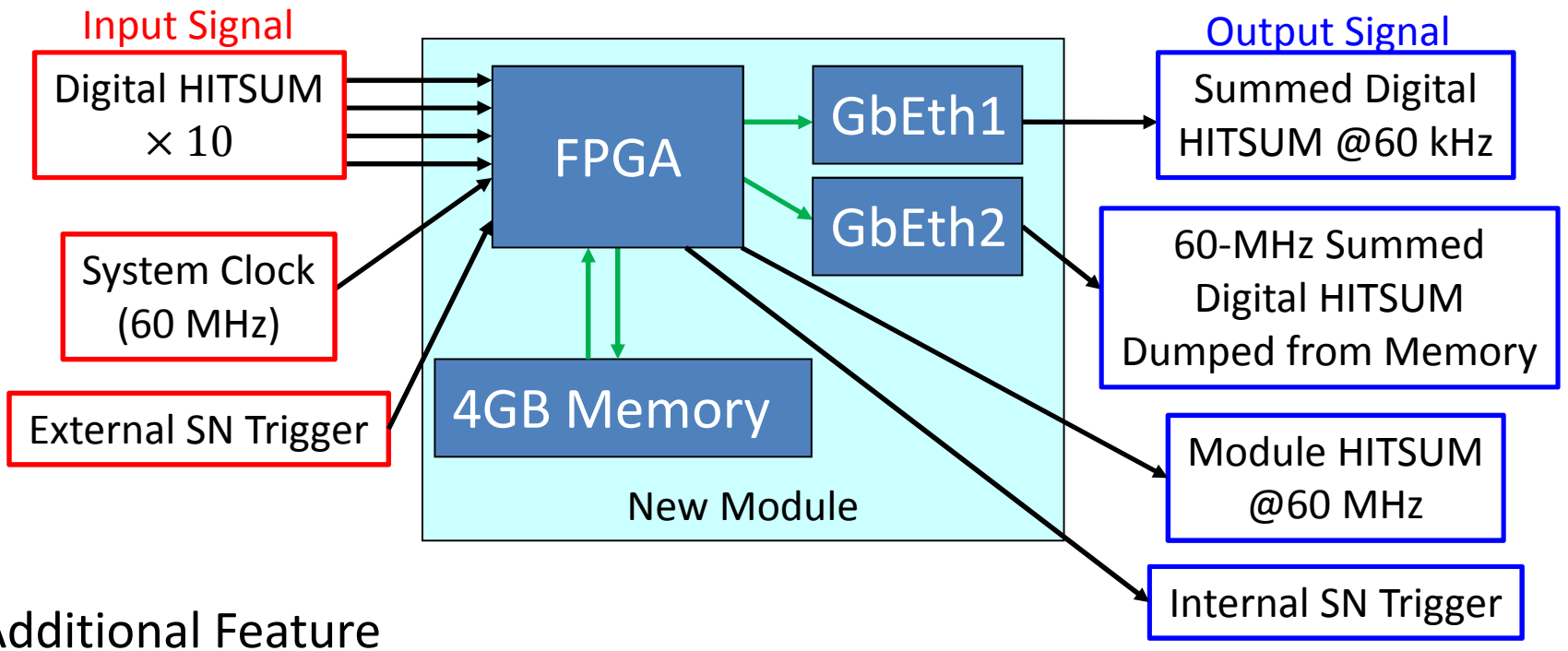
Time Resolution

Time resolution [MHz]	Fluctuation of dark noise [hit/time bin]
60	±0.83
0.1	±22
0.06	±26
0.01	±71



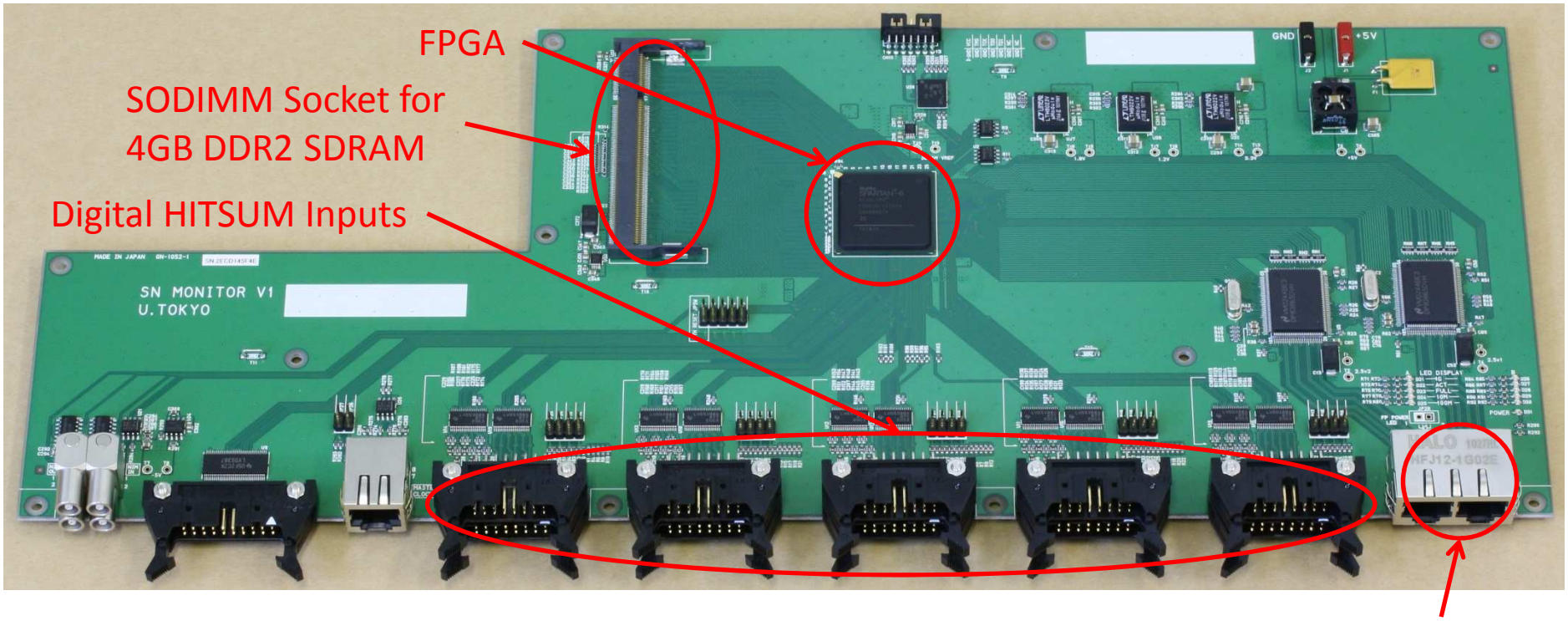
- Data size problem
  - Recording sum of HITSUMs at 60 MHz corresponds to ~500 TB/day.
    - Cf. Current SK DAQ: ~720 GB/day
  - Need reduction of data size
- Lower the time resolution to reduce data size
  - Sensitivity to the peak of neutrization burst should be kept.
  - Keep good significance for ~120 hits/event signal.
  - We chose 60 kHz.
    - $S/\sigma_{\mathrm{BG}} \gtrsim 4$, data size ~ 500 GB/day.

Block Diagram of New Module



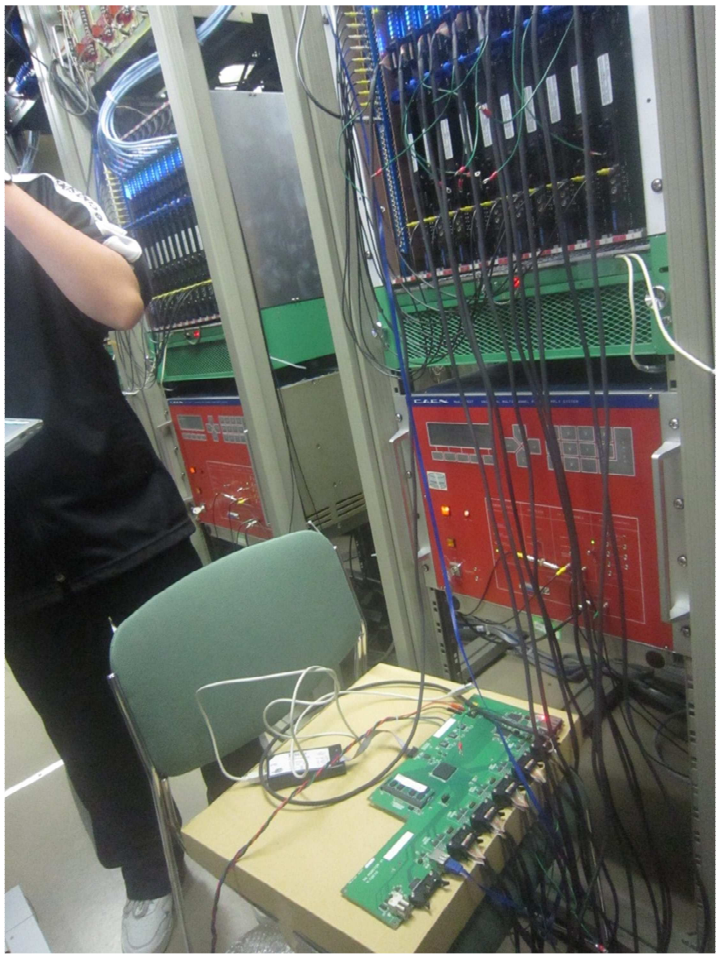
- Additional Feature
  - 4 GB RAM to store 60-MHz summed HITSUM information for 1 min
    - Obtain maximal time resolution around supernova trigger
    - Dump data on memory through another Gigabit Ethernet port
  - Supernova trigger can be generated inside the module, or input from the other system.

First Prototype of New Module



- A prototype of the new DAQ module was made.
  - Test with prototype module at test bench was done.
    - Basic test for the module functionality
    - Debug of the FPGA program (firmware)

Connection Test with Current DAQ



- Test of the prototype module connected with the current DAQ system was done in Aug., 2011.
  - No DAQ error occurred.
  - New module was functioning correctly.
- Effect of the module (especially, noise) was investigated.
  - Pedestals
  - Charge and timing distributions
  - Dark noise rate
  - Etc.

Revision of Module

- Revision of the module was necessary.
  - Correction for the malfunctioning part
    - Wrong wiring
      - Fixed by adding jumper cables for current prototype.
    - Signal termination for DRAM wiring is incompatible with DDR2 specification.
      - Due to the resource limitation of Spartan-6 FPGA
      - Plan to change FPGA (to bigger Spartan-6)
  - Addition of functionalities that we overlooked
    - Dip switch for more configurable options and ease of access.
    - On-board clock source used as internal clock for stand-alone debugging.

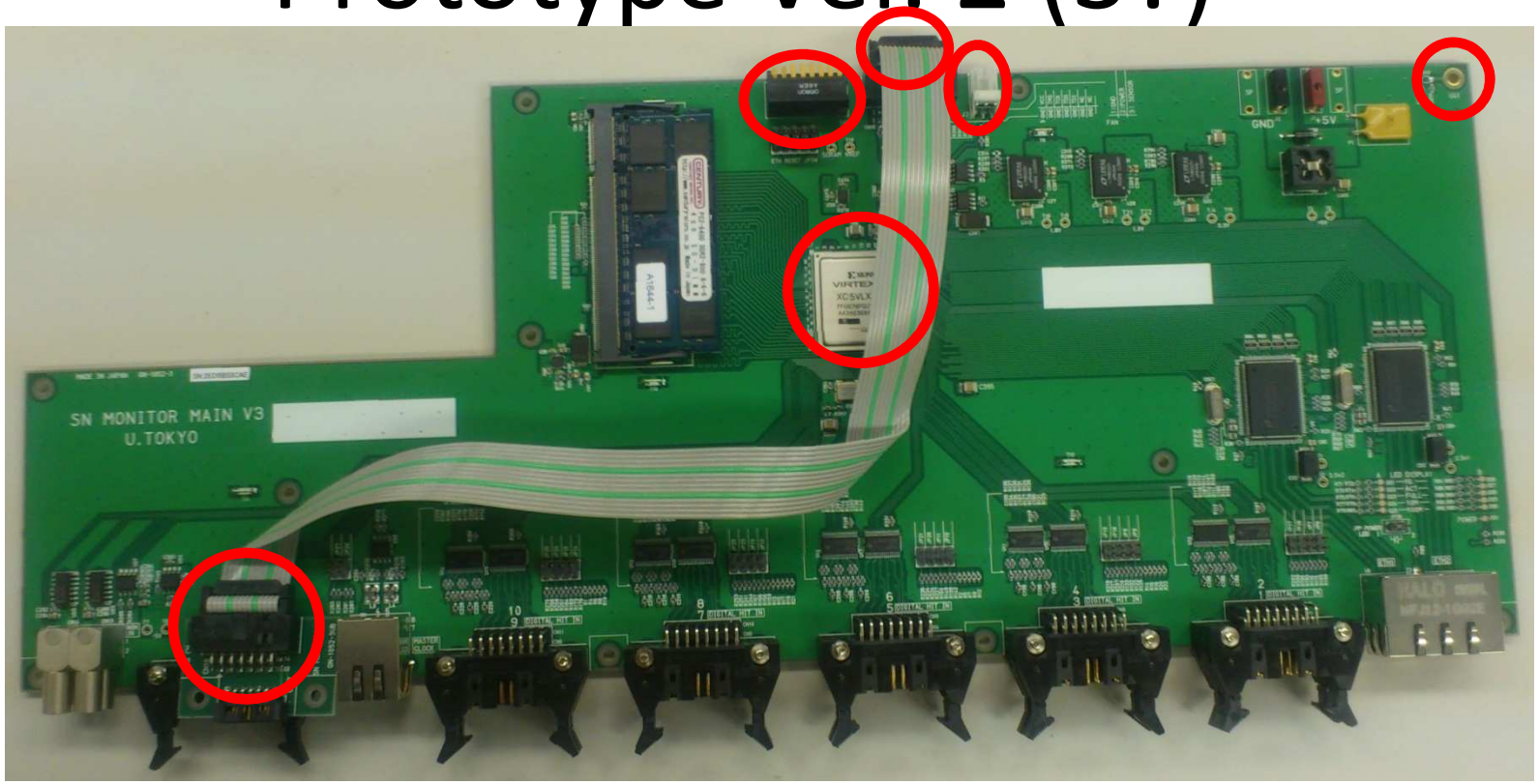
DDR2 Data Signal

- DDR2 signal standard is SSTL18.
  - SSTL18 Class II bidirectional termination is required for DDR2 data lines (DQ signals).
- Spartan-6 FPGA supports SSTL18_II, but only in restricted banks.
  - 28 out of 64 DQ pins are not SSTL18_II compatible.
    - Need re-assignment
  - Spartan-6 LX45 → LX100
    - More I/O pins are available and should be easy for re-arrangement
    - Did not choose LX75 due to late delivery date.

Re-Revision of Circuit

- Revision (Ver. 2) was almost done and we were about to order test production…
- However, we found it still does not meet the DDR2 specification.
  - Data strobe (DQS) pins must be SSTL_II clock-capable ones according to the DDR2 specification.
    - Spartan-6 has 4 differential pairs of such pins in left and right side banks, respectively. But we need 8 pairs in one side.
      - Changing the grade would not solve this problem.
  - We decided to change FPGA from low-end one (Spartan-6) to high-end one (Virtex-5).
    - Need to redo pin assignments and circuit design

Prototype Ver. 2 (3?)



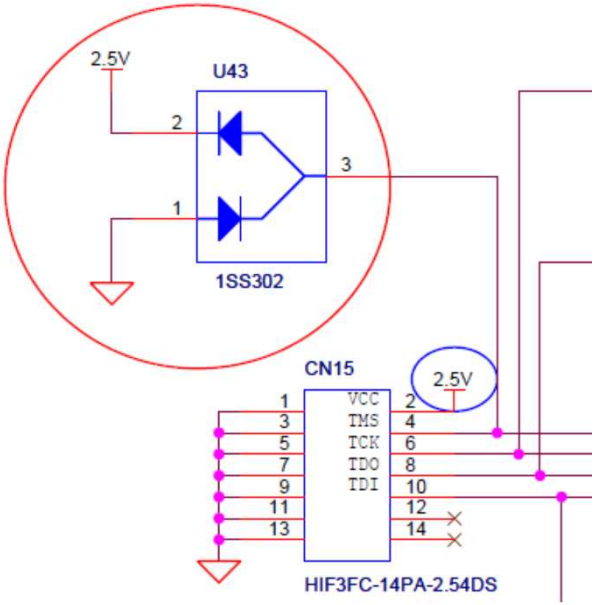
- Two new prototype boards were delivered in Apr., 2012.
  - Several corrections had been made in past few months.
    - Mainly due to the change of series of FPGA.

Changes from the Previous Prototype

- Change the FPGA (Spartan-6 → Virtex-5)
- Optimized power lines
  - New power line for new FPGA
  - One regulator chip for DDR reference and termination (sink/source)
- GND is connected to the chassis through screw hole.
- Optimize terminations, filters, and decoupling capacitors
- Add JTAG connector in the front panel
- Add protection diodes for JTAG lines
- Chassis fan monitor (and power)

Check of the New Prototype

- One problem in the new circuit
  - When powered on, it consumes ~2.2A and 2.5V power line for JTAG provide ~2.0V.
  - Due to the flip of protection diode.
    - These diodes are placed on reverse side.
  - These protection diodes were removed for a moment.
- Connection of I/O ports were checked
  - Clocks (Master Clock / Internal Debug Clock)
  - LEDs
  - dip/jumper switches
  - NIM outputs/inputs
  - LVDS output (Module HITSUM)
  - LVDS inputs (QBEE HITSUMs)
  - Ethernet port (x2)
  - DDR2 Memory I/O



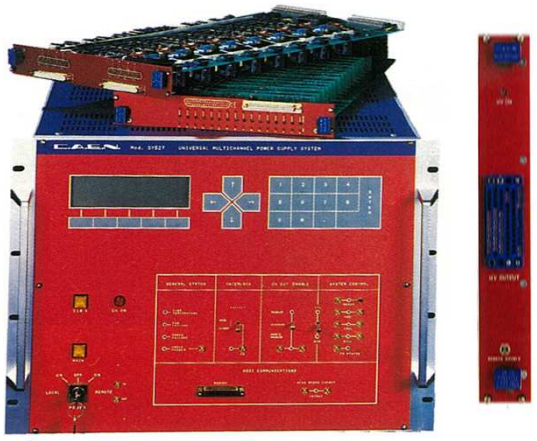
Plan

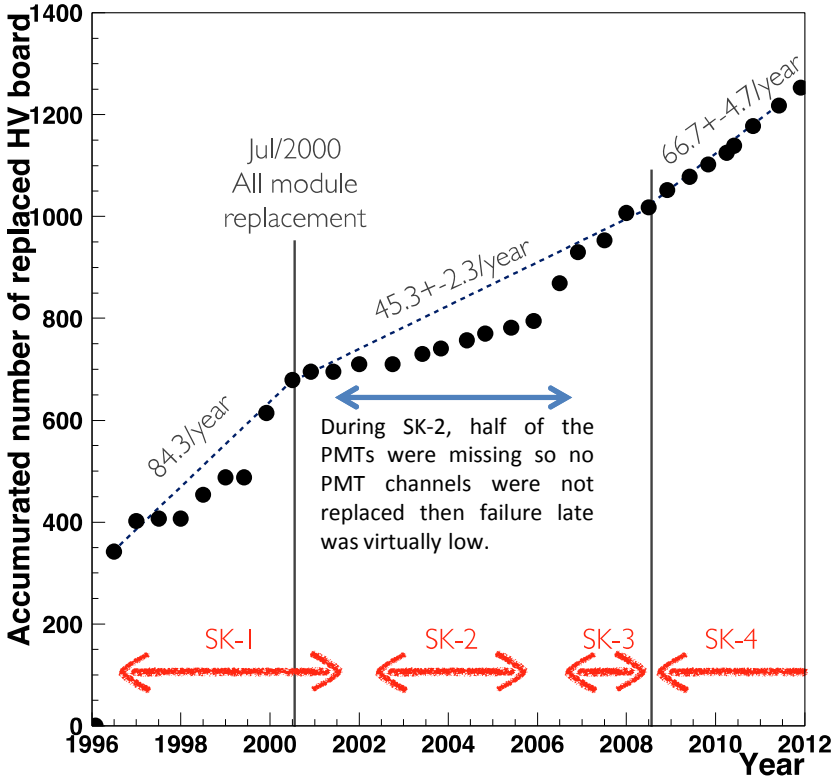
- Start mass production soon after the cooling power of the fans attached to the box is confirmed to be enough.
  - If cooling is not enough, change fans to more faster ones and/or add heat sink to FPGA and Ethernet PHY.
- Redo the connection test with the current DAQ using the new prototype.
- Check the boards in mass production one by one.
- Install the modules to SK when there is no T2K beam.
- Finalize the FPGA firmware before the operation starts.

ID HV REPLACEMENT

Current ID HV System

- CAEN SY527 + A933K
  - Installed in 1995
  - 24 channels/board, 10 boards/crate
  - H.V. Distributor
    - primary voltage 0 to 2550V
    - Voltage drop for each distributed output up to 900V
  - Voltage Set/Monitor Resolution: 0.2V
  - Max Current: 0.5mA / channel
  - Voltage Ripple: <5mV$_{P-P}$
  - Control from sparc PC via caenet - vme





- Good performance but problem is high failure rate…
  - Recently increasing???
  - 86 boards shipped, 60 received in FY2011

Schedule

- Current schedule for the procurement process
  - Feb. 16(Thu), 2012: Public announcement on the opinions for specification draft
  - Feb. 23(Thu), 2012: Briefing for specification draft
  - Mar. 8(Thu), 2012: Deadline for the opinion
  - Mar. 15(Thu), 2012: Specification settlement committee
  - Apr. 26(Thu), 2012: Public announcement on the national gazette for tender
  - May. 7(Mon), 2012: Briefing for tender
  - Jun. 18(Mon), 2012: Deadline for tender
  - Jun. 21(Thu), 2012: Technical assessment committee
  - Jul. 2(Mon), 2012: Open tender
  - Mar. 29(Fri), 2013: Deadline for delivery
- Test with 1 crate connected to SK will be performed before mass production.
  - During no T2K beam period, of course.
- In this fiscal year, only delivery of HV system into the mine SK area will be done.
  - Installation will be carried out in summer 2013, while there is no T2K beam.
    - Need another contract in next fiscal year.

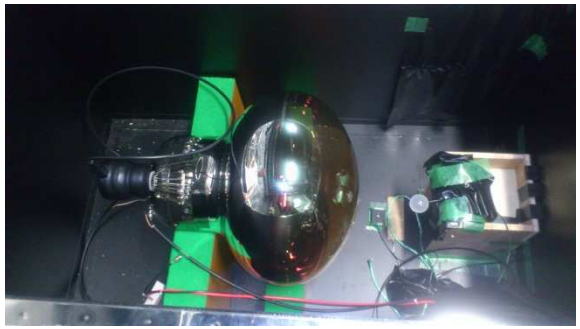
New ID HV System

- Winner of the tender is REPIC.
  - Actual manufacturer is iseg Spezialelektronik GmbH.
- Specifications: Basically same as the current one
  - 240ch/crate(mainframe) x 48 crates + 3 spare crates
    - 24ch/board x 10 boards in one crate, 30 spare boards
  - Compatible connector with the current one
  - Max. voltage: 2500V, positive polarity
    - Max. voltage difference among 24ch: 2500V
      - Can turn HV off channel by channel.
  - Max. current: 0.5mA/ch
  - Voltage set/monitor resolution: 0.2% or 3V
  - Ripple and noise: <10mVp-p
  - Failure rate: < 0.1%/year in channel base
    - This means < 11 failures/year.
  - 5-year warranty
  - Etc.

The photos are for illustrative purposes only.
Actual crate/board is different from the one in the photo.

Test with Test Crate

- Checked all 240 channels one by one.
  - Turn on/off, monitor values, control software
- Installed the test crate to SK and took data for ~1 day.
  - Checking data if there is any difference.
- Moved test crate to another lab. and started long term stability test w/ dummy loads and a spare PMT
  - Planning to test for ~1 month.



Summary

- New DAQ system for nearby supernova burst is under development and mass production will start soon.
  - 2^{nd} (3^{rd}?) prototype was made and tested.
  - Mass production starts soon.
  - Installation will be done in no-T2K-beam time.
- ID HV system will be replaced in summer 2013.
  - Manufacturer was decided.
  - Test crate and modules were delivered and are now being tested.
  - Whole system will be delivered by the end of Mar. 2013 and installed in Summer 2013.