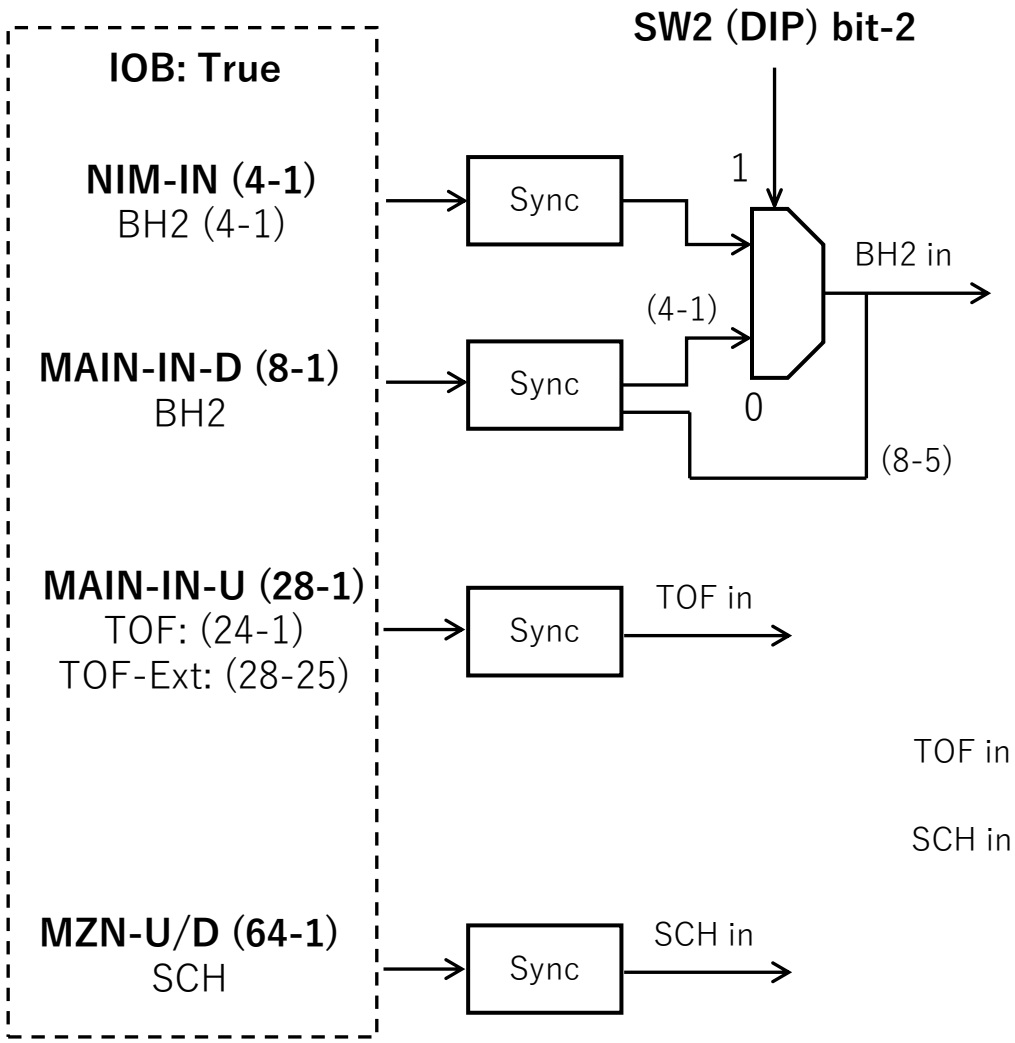
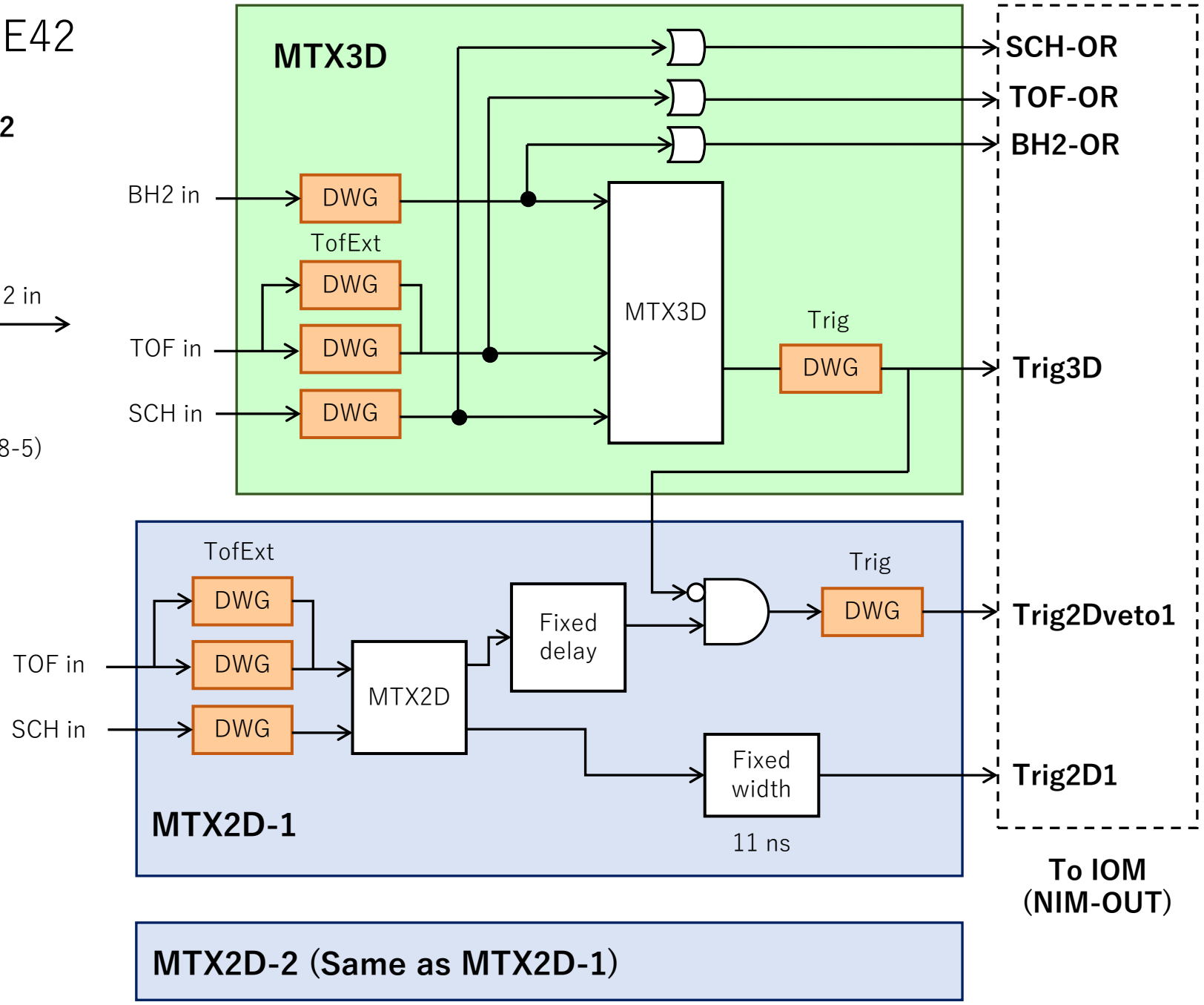
MTX3D-E03E42

Version 1.1

Configuration of MTX3D-E03E42





DWG: Delay Width Generator
Sync: Double-FF

HUL MTX3D_E03E42 software

Control software is included in hul-software.git as Mtx3D_E03E42.
To build executable files from sources, gcc version 7 (or more) is necessary.
If your OS is CentOS 8, no problem. But, if you are using CentOS 7, devtoolset must be enabled (or gcc compiled by yourself).

Executable files.

- load_nimo: Select ouput signals from NIM-OUT ports.
- load_register: Set DWG registers.
- load_matrix3d: Set matrix pattern to the matrix3d module.
- load_matrix2d: Set matrix pattern to the matrix2d-1 (or -2) modules.

Example registers for these exec files are in Mtx3D_E03E42/example_register.

In the fe_hul02 computer, devtoolset-7 and executable files compiled by gcc 7.3 are installed.
But, devtoolset-7 is not enabled usually. When you use it, run this command.
scl enable devtoolset-7 bash

NIMO (IOM) register

Example register file is in example_register/nimo.
How to use:

- load_nimo [IP] [register file]

```
1  ##########################################################
2  # Example IOM register file of MTX3D-E03E42
3  ##########################################################
4  # #: Indicates comment line
5  #
6  # Command list
7  #  Trig3D:      0
8  #  Trig2Dveto1: 1
9  #  Trig2Dveto2: 2
10 #  Trig2D1:     3
11 #  Trig2D2:     4
12 #  tofOR:       5
13 #  schOR:       6
14 #  bh2OR:       7
15
16 #################
17 #### NIM-OUT ####
18 #################
19 OUT1  5
20 OUT2  6
21 OUT3  7
22 OUT4  0
```

These commands are set to NIM-OUT 1-4 ports.

DWG register

Example register file is in example_register/dwg.
How to use:

- load_register [IP] [register file]

```
1  ##################################################
2  # Example register file of MTX3D-E03E42
3  ##################################################
4  # #: Indicates comment line
5  #
6  # DWG: Delay & Width generator
7  #      Delay range : 0-31
8  #      Width range : 1-32
9  #
10 # Clock frequency: 350 MHz
11 # LSB of DWG bit:  2.857... ns
12
13 #################
14 #### MTX2D-1 ####
15 #################
16 MTX2D1::Tof::Delay     0
17 MTX2D1::TofExt::Delay  0
18 MTX2D1::Sch::Delay     0
19 MTX2D1::Trig::Delay    0
20
21 MTX2D1::Tof::Width     10
22 MTX2D1::TofExt::Width  10
23 MTX2D1::Sch::Width     10
24 MTX2D1::Trig::Width    10
```

Do NOT exceed these range.

LSB of DWG register corresponds to 2.85... ns

```
39 #################
40 ####  MTX3D  ####
41 #################
42 MTX3D::Tof::Delay     0
43 MTX3D::TofExt::Delay  0
44 MTX3D::Sch::Delay     0
45 MTX3D::Bh2::Delay     0
46 MTX3D::Trig::Delay    0
47
48 MTX3D::Tof::Width     10
49 MTX3D::TofExt::Width  10
50 MTX3D::Sch::Width     10
51 MTX3D::Bh2::Width     10
52 MTX3D::Trig::Width    10
```

Width of TOF, SCH, and BH2-OR signals are determined by registers in MTX3D.

Veto timing.
Should be 0 in usual.

Veto window.
Should be adjusted.

Matrix3D register

Example register file is in example_register/mtx.
How to use:

- load_matrix3d [IP] [register file]

```
### Bit pattern of BH2 for each TOF x SCH element
### 0 : off, 1 : on
# BH2-0 <====> BH2-7
# TOF segment 0
SCH00 00000000
SCH01 00000000
SCH02 00000000
SCH03 00000000
SCH04 00000000
SCH05 00000000
SCH06 00000000
SCH07 00000000
SCH08 00000000
SCH09 00000000
SCH10 00000000
SCH11 00000000
SCH12 00000000
SCH13 00000000
SCH14 00000000
SCH15 00000000
SCH16 00000000
```

E.g. register for TOF-0 x SCH-2 x BH2-(0-7) segments.
Most left bit is BH2-0, Most right bit is BH2-7.
If you want to enable a target matrix element, set 1.

Software doesn't check this label. This is just for user convenience.
Do NOT change the register order.

Matrix2D register

Example register file is in example_register/mtx.
How to use:

- load_matrix2d [IP] [register file] [index (1 or 2)]

As there are two matrix2d modules in FPGA, index (1 or 2) is necessary to indicate which one is selected. Only 1 or 2 are meaningful numbers.

```
### Bit pattern of BH2 for each TOF x SCH element
### 0 : off, 1 : on
# TOF segment 0
SCH00 0
SCH01 0
SCH02 0
SCH03 0
SCH04 0
SCH05 0
SCH06 0
SCH07 0
SCH08 0
```

TOF x SCH matrix pattern.
Important points are the same as that of MTX3D.

Comments

Shell scripts and log system are not prepared.

Latest firmware files are in
https://wwwkm.phys.sci.osaka-u.ac.jp/nextcloud/index.php/s/LGNfPbNgsJmFq2E