J-PARCハドロン実験における連続読み出しDAQ用主回路, AMANEQの開発

Outline

- Introduction
- Design of AMANEQ
- Result of performance evaluation
- Firmware development status
- Summary

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Introduction

Introduction, J-PARC E50 experiment

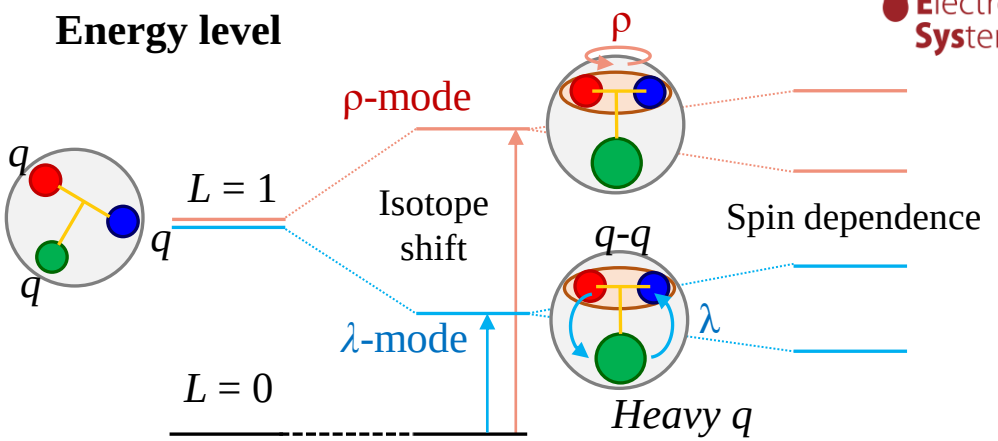
Motivation

- Reveal the effective degree of free of the baryon internal structure, the di-quark correlation, by introducing heavy (c) quark.

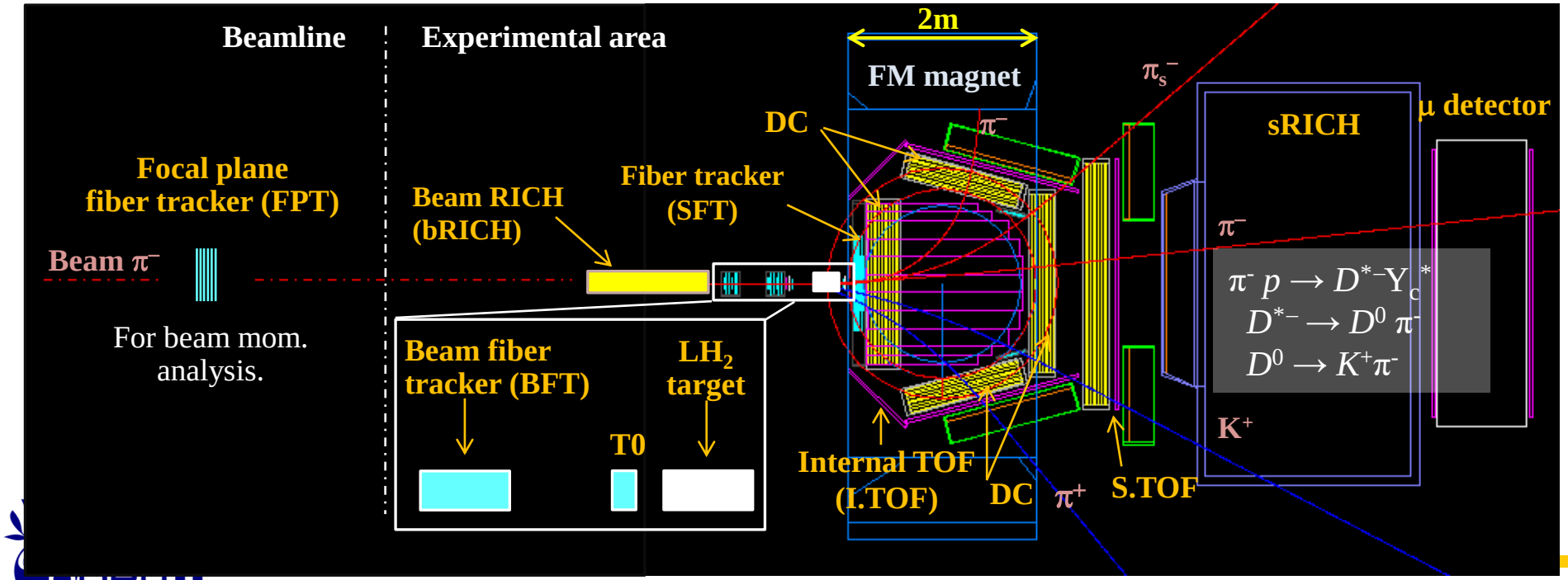
Strategy

- Missing spectroscopy via the $\pi^- p \rightarrow D^{*-} Y_c^*$ reaction.
- Measure production cross and decay branching ratio simultaneously.

Energy level



The experimental setup at J-PARC high-p beamline



Secondary π^- beam

- 20 GeV/c
- 30 MHz (60 M/spill)
  - (2s duration)

Target

- Liquid H_2, 4-g/cm^2

Reaction

Charmed-baryon production
- ~1 nb/sr

Background reaction
- 2.4 mb/sr

Total reaction rate
- 1.5 MHz

Charged-particle multiplicity
- 4

Requirement for the DAQ system

Requirement from E50

Momentum analysis is essential to reduce the trigger rate to the acceptable (~10kHz) rate.

+

Other physics program at this beam line

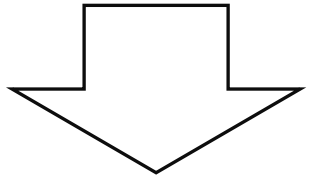
Λp scattering

Ξ* spectroscopy

Pion-induced Drell-Yan

I=3 dibaryon search

The required trigger condition are different.



The DAQ system must be flexible and scalable.

Omit the hardware (FPGA) based trigger,

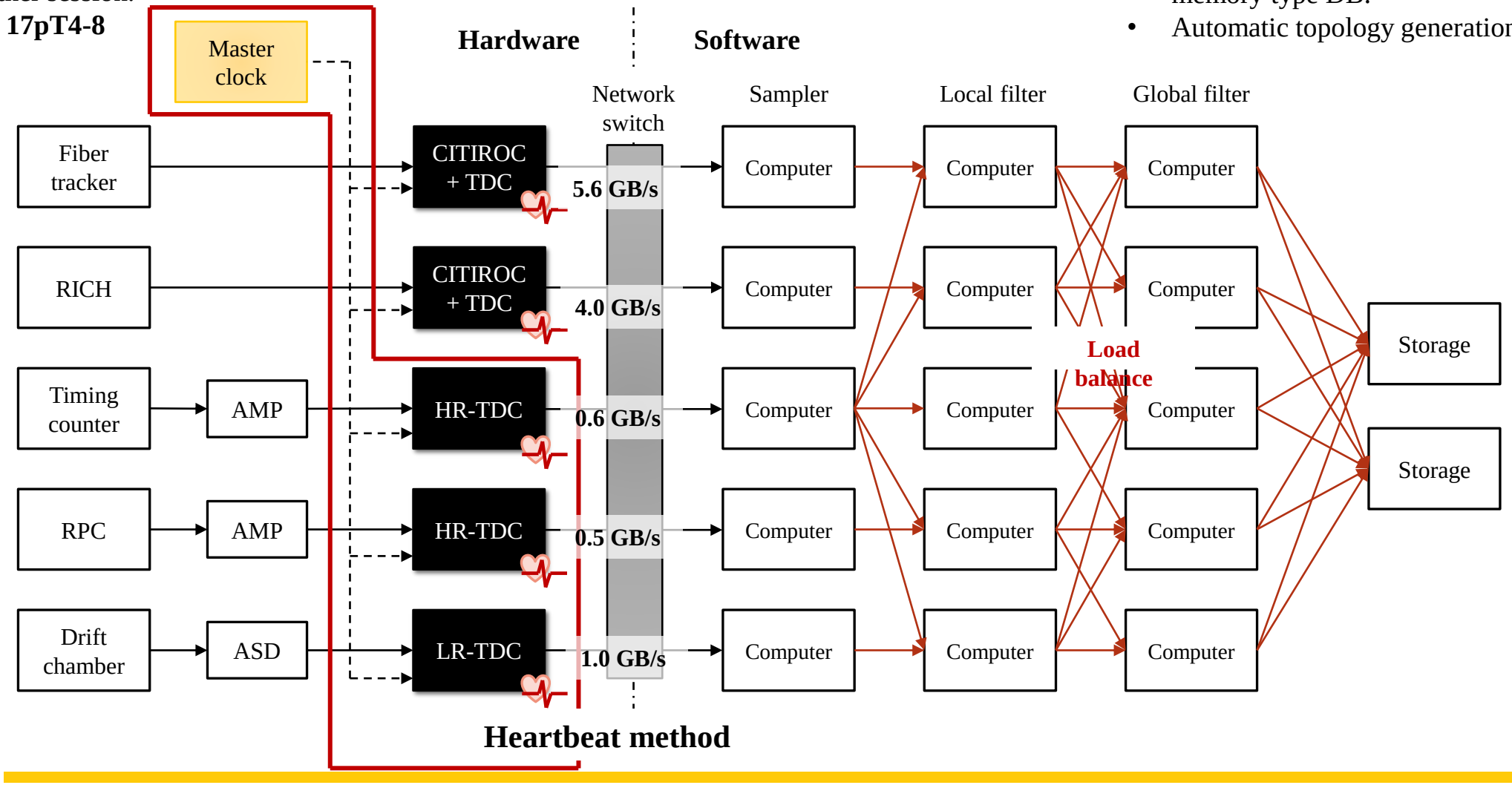
and introduce the trigger-less data-streaming-type DAQ system.

Schema of the DAQ system at the high-p beam line

FairMQ + redis

The clock/timing distribution will be reported in other session.
R. Honda 17pT4-8

- Process monitor and control via in-memory type DB.
- Automatic topology generation



Total data rate: ~12 GB/s (E50 case)

Design of AMANEQ

Requirement for the front-end electronics

It plays several roles.
- High-resolution TDC (30 ps)
- Low-resolution TDC (1 ns)
- Clock/timing distribution

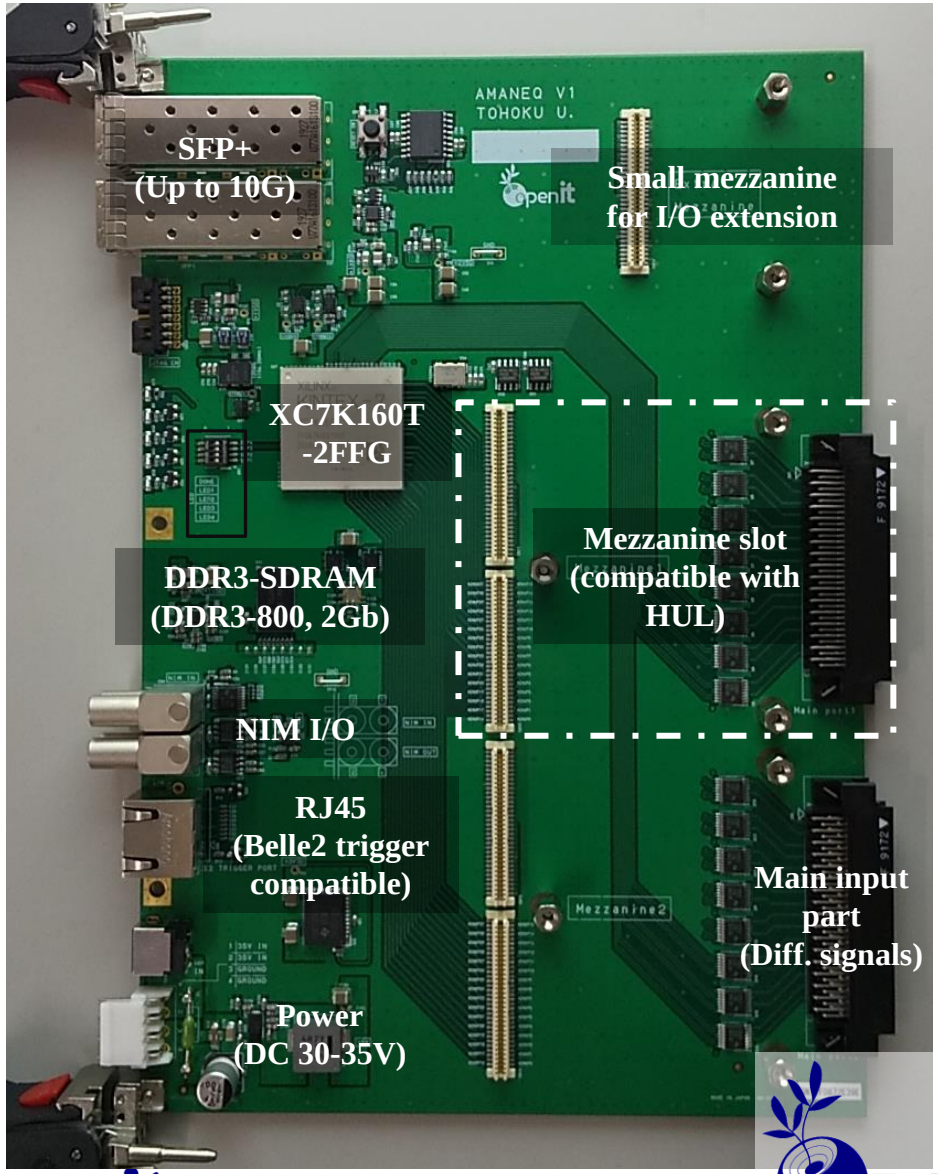
Function extendibility by mezzanine card
- Being compatible with that of the hadron universal logic (HUL) module.
  - Open-It project: https://openit.kek.jp/project/HUL/HUL
- High-resolution timing measurement is outsourced to the mezzanine card.

High speed data link
- Maximum data rate will be 4 Gbps/board

Use speed grade -2 FPGA and adopt SiTCP-XG

Large buffer
- Prevent from data drop due to the TCP re-transmission.

Use DDR3-SDRAM



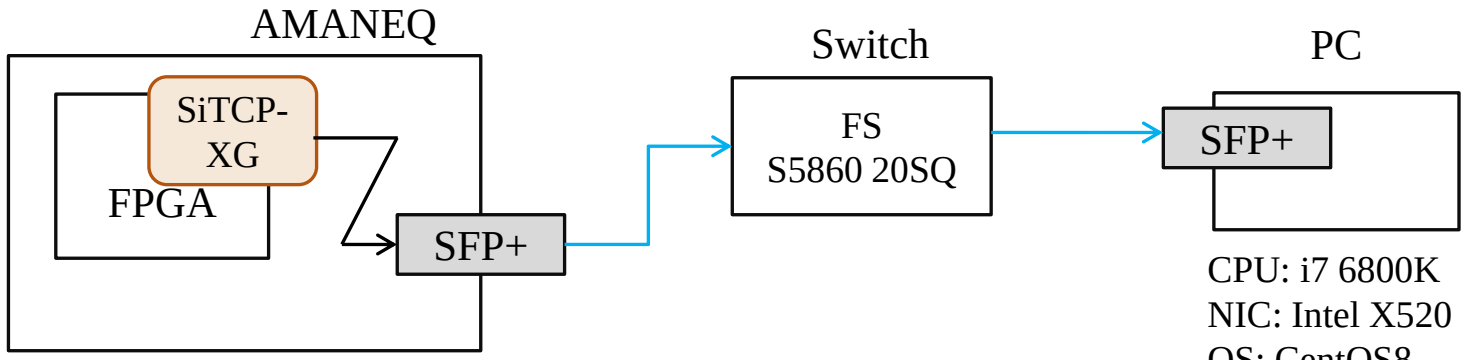
A main electronics for network oriented trigger-less data acquisition system (AMANEQ)

- VME 6U size but it doesn't have VME bus
  - VME crate without the power is used as a housing box
- Kintex7 with speed grade -2
  - Transceiver bandwidth up to 10Gbps
  - Can implement SiTCP-XG
- Main input ports compatible with HUL
- Has two mezzanine slot
  - Compatible with HUL
  - Mount HUL mezzanine HR-TDC
  - Mount DCR mezzanine for DC readout
- Belle2 trigger port (master clock)
  - Has a jitter cleaner to clean up the master clock
- DDR3-SDRAM as a de-randomizer
  - DDR3-800 with 16-bit bus width.
  - 2 Gb
  - It allows us to use spill off time for data transfer
- Powered by the external power supply with DC 30-35V

Result of performance evaluation

Data transfer speed via SiTCP-XG

Test setup

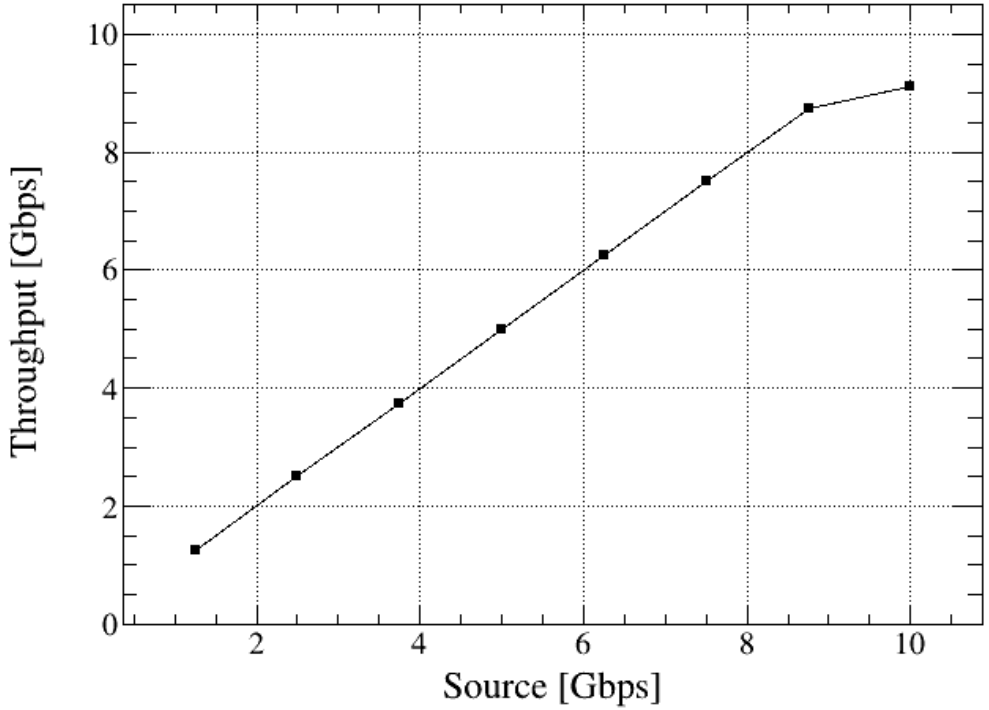


Read data using C++ software.

CPU: i7 6800K
NIC: Intel X520
OS: CentOS8

Tested by H. Sendai (KEK E-sys)

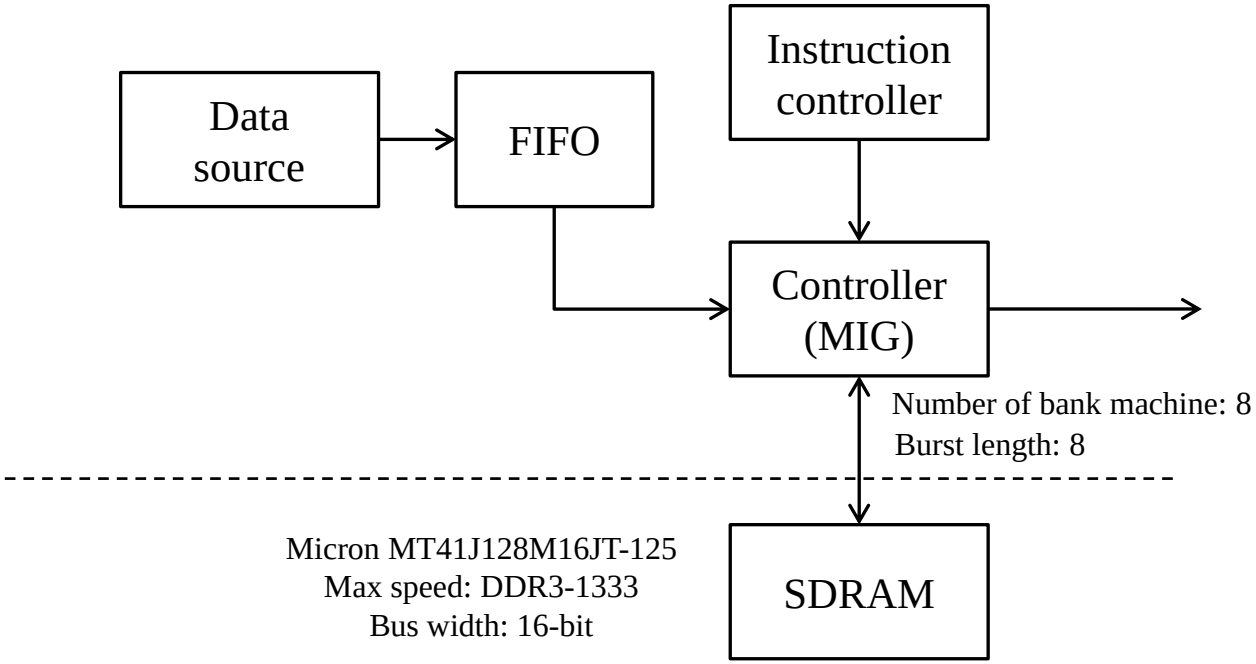
Measured throughput

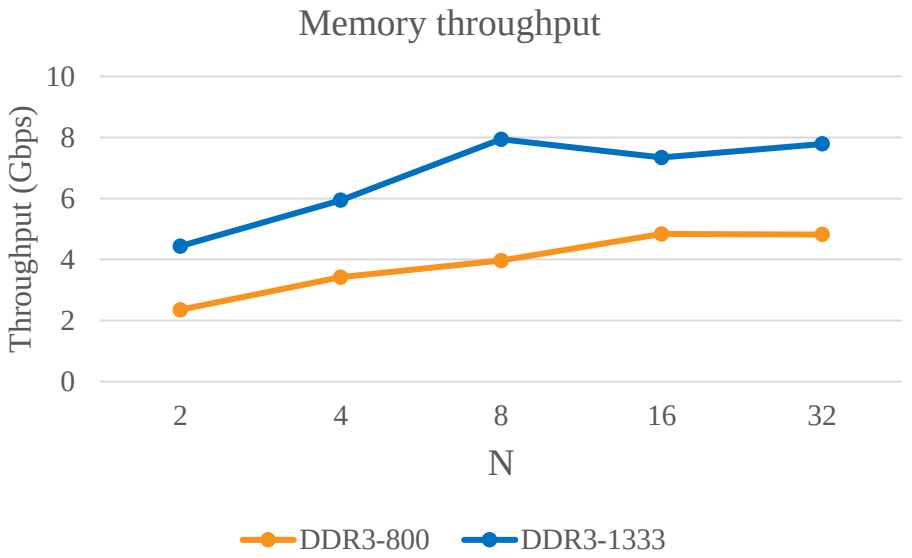


Obtained throughput: 9.12 Gbps
~96% of TCP payload limit (MTU 1500)

Throughput of DDR3-SDRAM

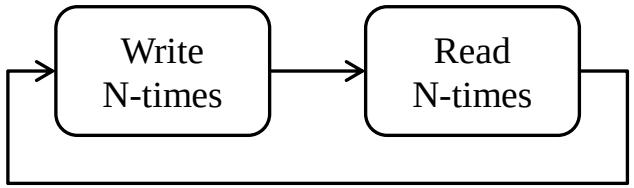
Firmware configuration





Data bus of SDRAM is bi-directional.
Memory operation is determined by command.

Tested write/read pattern.



Obtained throughput (reference value)

DDR3-800

- ~4.8 Gbps (6.4 Gbps)

DDR3-1333

- ~7.9 Gbps (10.66 Gbps)

***Access to the same memory bank.
Larger over head when changing the bank address.

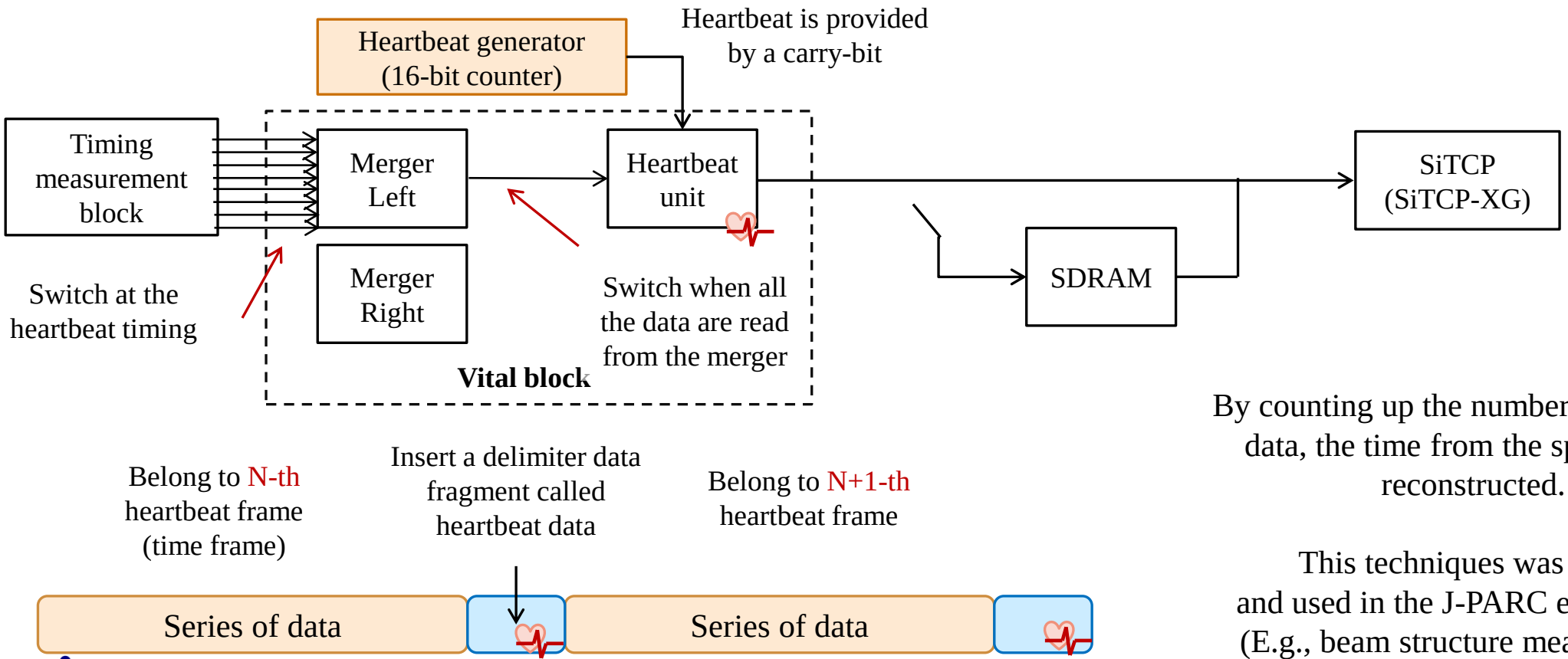
Firmware development status

Heartbeat method for the continuous timing measurement

We need the continuous timing measurement over 2 s (spill duration of J-PARC slow extraction)

- Required dynamic range: ~10^{10} (1 ns TDC case)

Introduce **heartbeat method**: a technique to reconstruct the time without a long-length time stamp.

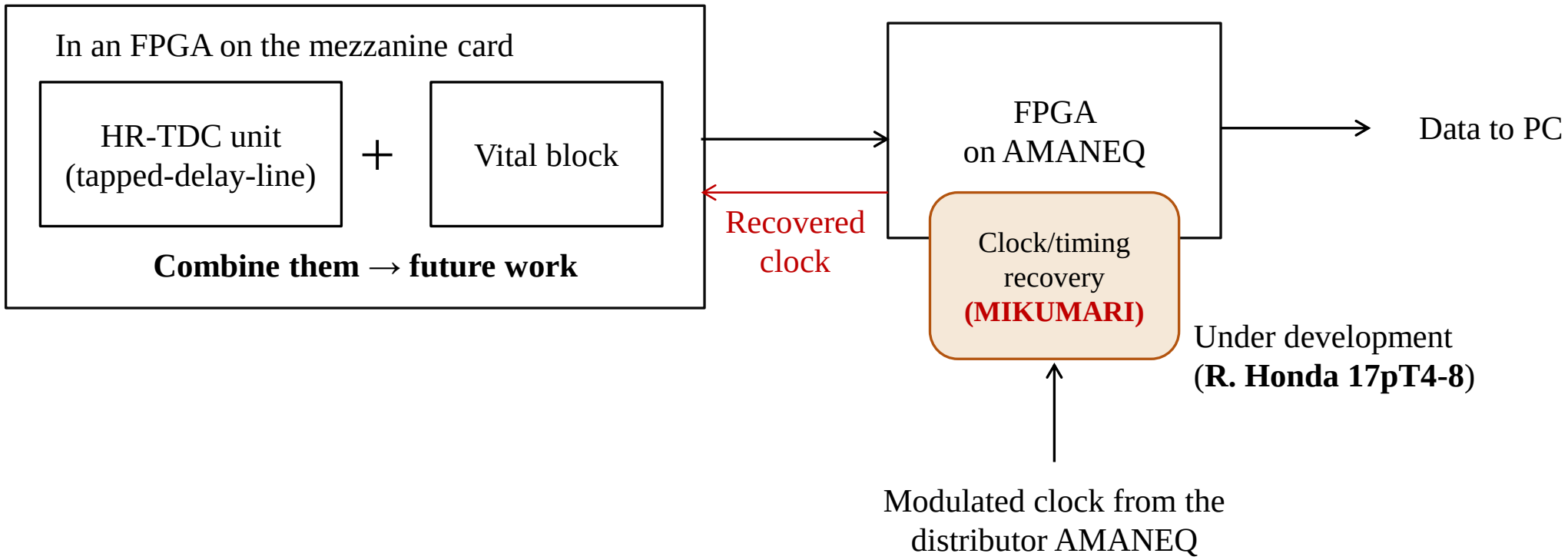


By counting up the number of heartbeat data, the time from the spill start is reconstructed.

This techniques was tested and used in the J-PARC experiment. (E.g., beam structure measurement)

Future prospect

For high-resolution timing measurement



Development of key technologies, HR-TDC, heartbeat method, clock/timing distribution, and high-speed data transmission are almost finished.
In future, combine them and test it.

Summary

- The trigger-less data-streaming-type DAQ system is introduced in the J-PARC E50 experiment and is shared among the other experiments in the high-p beam line.
  - The total expected data is 12 GB/s for the E50 case.

- A main electronics for network oriented trigger-less data acquisition system (AMANEQ) was developed.
  - Two mezzanine slots, which is compatible with HUL, for the function extension.
  - Two data link with the speed up to 10 Gbps. Realized 10 Gbps TCP communication by SiTCP-XG.
  - 2 Gb DDR3-SDRAM.

- The obtained throughput of SiTCP-XG was 9.12 Gbps. 96% of the TCP payload limit.
- SDRAM throughput was ~7.9 Gbps with DDR3-1333.
- These performance are sufficient for the required data rate of 4 Gbps.

- The heartbeat technique was developed for the continuous timing measurement with a 16-bit time stamp length. It enables us to measure the time over 2s corresponds to the J-PARC spill duration.

- Development of the key technologies are almost finished. Combining them is the future work.

Resource utilization of SiTCP-XG and transceiver

Target FPGA: XC7K160-2 (Kintex-7)

SiTCP-XG

Name	Slice LUTs (101400)	Slice Registers (202800)	F7 Muxes (50700)	F8 Muxes (25350)	Slice (25350)	LUT as Logic (101400)	LUT as Memory (35000)	Block RAM Tile (325)
u_LED_Inst (LEDModule)	<0.01%	<0.01%	0.00%	0.00%	0.02%	<0.01%	0.00%	0.00%
u_PCSPMA_Inst (ten_gig_eth_pcs_pma)	2.37%	1.60%	<0.01%	0.00%	4.33%	2.28%	0.27%	0.00%
u_RST_Inst (SystemReset)	<0.01%	<0.01%	0.00%	0.00%	0.01%	<0.01%	0.00%	0.00%
u_SDS_Inst (SelfDiagnosisSystem)	0.38%	0.39%	0.02%	0.00%	0.97%	0.35%	0.07%	0.46%
u_SiTCPXG_Inst (WRAP_SiTCPXG_XC7K_128K)	4.81%	4.47%	0.43%	0.13%	9.97%	4.52%	0.82%	21.69%
u_TSD_Inst (TCPsenderXG)	<0.01%	<0.01%	0.00%	0.00%	0.01%	<0.01%	0.00%	0.00%

SiTCP

Name	Slice LUTs (101400)	Slice Registers (202800)	F7 Muxes (50700)	F8 Muxes (25350)	Slice (25350)	LUT as Logic (101400)	LUT as Memory (35000)	Block RAM Tile (325)
toplevel	8.27%	5.97%	0.36%	0.25%	14.63%	8.08%	0.53%	7.85%
gen_pcspma[0].u_pcspma_Inst (GbEPcsPma__xdcDup__1)	0.54%	0.54%	0.00%	0.00%	1.33%	0.52%	0.06%	0.00%
gen_pcspma[1].u_pcspma_Inst (GbEPcsPma)	0.54%	0.54%	0.00%	0.00%	1.29%	0.52%	0.06%	0.00%
gen_SiTCP[0].u_gTCP_inst (global_sitcp_manager)	0.00%	<0.01%	0.00%	0.00%	<0.01%	0.00%	0.00%	0.00%
gen_SiTCP[0].u_SiTCP_Inst (WRAP_SiTCP_GMII_XC7K_32K)	3.16%	2.03%	0.16%	0.13%	5.03%	3.11%	0.16%	3.54%
gen_SiTCP[1].u_gTCP_inst (global_sitcp_manager_1)	0.00%	<0.01%	0.00%	0.00%	<0.01%	0.00%	0.00%	0.00%

Power consumption of SiTCP-XG + GTX transceiver

SiTCP-XG

Utilization	Name	Clocks (W)	Signals (W)	Data (W)	Clock Enable (W)	Set/Reset (W)	Logic (W)	BRAM (W)	Clock Manager (W)	MMCM (W)	I/O (W)	GTX (W)	GTX (W)
1.158 W (84% of total)	N toplevel												
0.571 W (42% of total)	u_SiTCPXG_Inst (WRAP_SiTCPXG_XC7K_128K)	0.065	0.064	0.063	<0.001	0.001	0.045	0.397	<0.001	<0.001	<0.001	<0.001	<0.001
0.447 W (33% of total)	u_PCSPMA_Inst (ten_gig_eth_pcs_pma)	0.032	0.011	0.01	<0.001	0.001	0.01	<0.001	<0.001	<0.001	<0.001	0.394	0.394
0.107 W (8% of total)	u_ClkMan_Inst (clk_wiz_sys)	0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.101	0.101	0.005	<0.001	<0.001
0.02 W (1% of total)	u_SDS_Inst (SelfDiagnosisSystem)	0.005	0.005	0.004	<0.001	<0.001	0.003	0.004	<0.001	<0.001	<0.001	<0.001	<0.001
0.008 W (1% of total)	u_FMP_Inst (FlashMemoryProgrammer)	0.005	0.001	0.001	<0.001	<0.001	0.001	0.002	<0.001	<0.001	<0.001	<0.001	<0.001

SiTCP

Utilization	Name	Clocks (W)	Signals (W)	Data (W)	Clock Enable (W)	Set/Reset (W)	Logic (W)	BRAM (W)	Clock Manager (W)	MMCM (W)	I/O (W)	GTX (W)
0.891 W (82% of total)	N toplevel											
0.263 W (24% of total)	gen_pcspma[0].u_pcspma_Inst (GbEPcsPma__xdcDup__1)	0.01	0.002	0.002	<0.001	<0.001	0.002	<0.001	<0.001	<0.001	<0.001	0.249
0.263 W (24% of total)	gen_pcspma[1].u_pcspma_Inst (GbEPcsPma)	0.01	0.002	0.002	<0.001	<0.001	0.002	<0.001	<0.001	<0.001	<0.001	0.249
0.124 W (11% of total)	u_ClkMan_Inst (clk_wiz_sys)	0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.118	0.118	0.005	<0.001
0.095 W (9% of total)	u_GtClockDist_Inst (GtClockDistributer2)	0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.095	0.095	<0.001	<0.001
0.055 W (5% of total)	gen_SiTCP[1].u_SiTCP_Inst (WRAP_SiTCP_GMII_XC7K_32K_0)	0.026	0.01	0.009	<0.001	<0.001	0.009	0.01	<0.001	<0.001	<0.001	<0.001
0.054 W (5% of total)	gen_SiTCP[0].u_SiTCP_Inst (WRAP_SiTCP_GMII_XC7K_32K)	0.026	0.01	0.01	<0.001	<0.001	0.009	0.01	<0.001	<0.001	<0.001	<0.001