Clock-duty-cycle-modulation (CDCM)を用いたクロック・データ伝送システムの開発

Outline

- Introduction
- CDCM based transceiver
- SPDT protocol
- Results
- Summary

2021.09.17

KEK IPNS E-sys
Ryotaro Honda

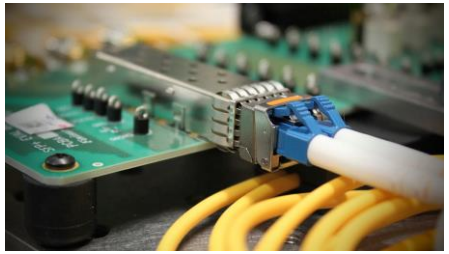
Background

Precise clock distribution is a key issue for many particle and nuclear experiments.

Typical requirements

- Low jitter (a few tenth ps)
- Synchronous data with predictable latency (trigger in typical)
- Controllable phase of the recovered clock
- Distribute a clock over meters to kilo-meters
- As few transmission lines as possible

Usual solution



\+ 8b10b modulation +

FPGA
high-speed serial transceiver
(e.g. Xilinx GT transceivers)

It actually works well, but

- Strongly depends on FPGA built-in blocks.
  - CDR circuit is not an user primitive.
  - Some of them are black boxes.
- Need a special electronics dedicated for distributing clock/data via serial transceivers.

Develop a serial transceiver independent clock/data distribution system.
Develop a protocol to send a data and synchronous pulse over.

Expected users

J-PARC E50 experiment (charmed-baryon spectroscopy)

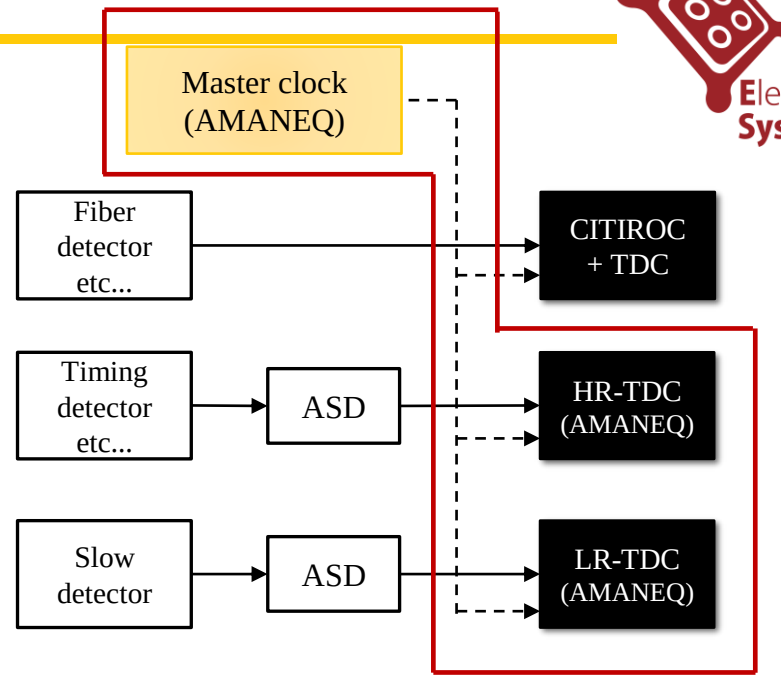
- DAQ system: trigger-less data-streaming-type DAQ
- Synchronization of FEE with the 125 MHz master clock.
- Synchronous timing, e.g., spill start/end and global time stamp distribution.

J-PARC g-2/EDM experiment

- DAQ system: conventional trigger-type DAQ
- Synchronization of FEE with the 100 MHz master clock.
- Trigger and tag distribution.

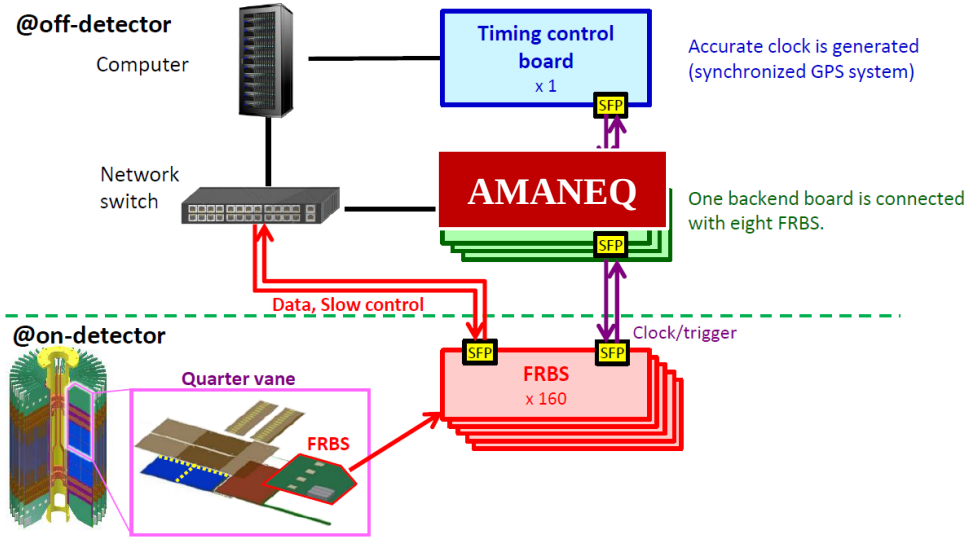
J-PARC Neutrino beam line is also interested.

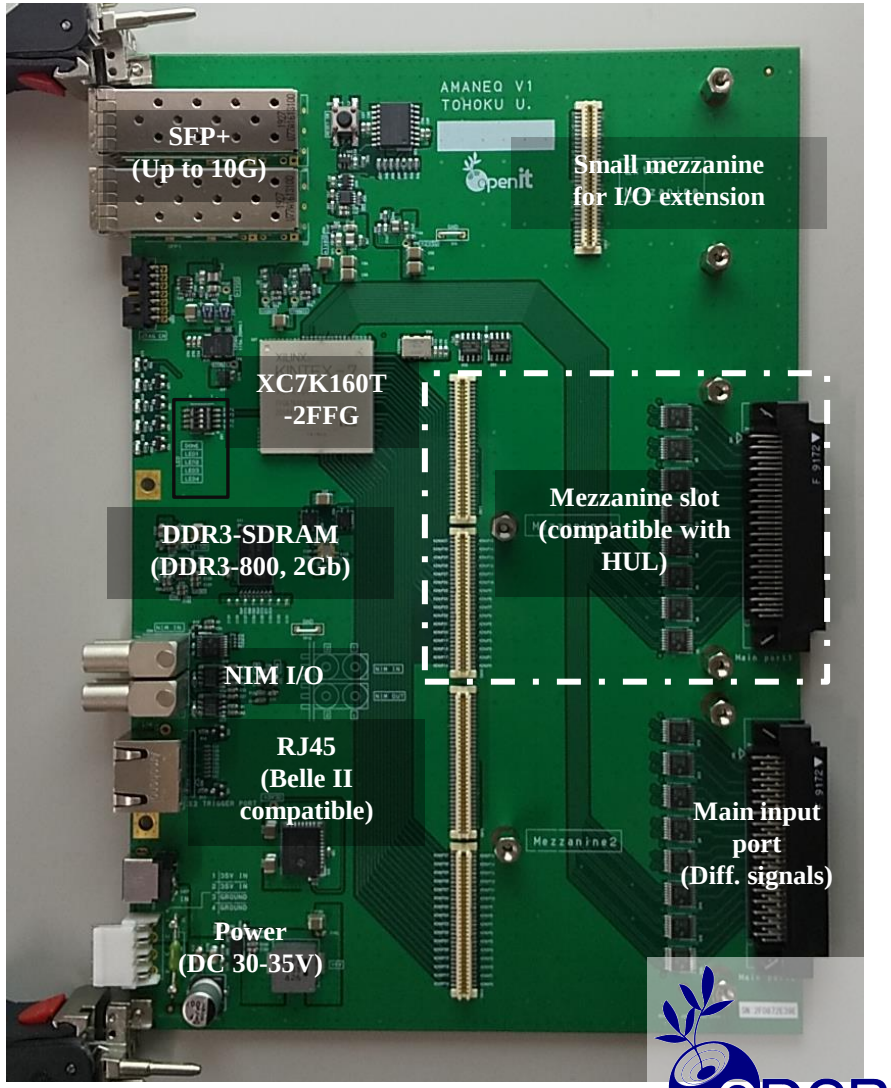
E50 case



R. Honda et al., 16pV1-10

g-2/EDM case





A main electronics for network oriented trigger-less data acquisition system (AMANEQ)

- VME 6U size but it doesn't have VME bus
- Kintex7 with speed grade -2
  - Can implement 10G SiTCP (SiTCP-XG)
- Main input ports compatible with HUL
- Has two mezzanine slots
  - Compatible with HUL
- Belle II link port
- Has a jitter cleaner (CDCE62002)
- DDR3-SDRAM as a de-randomizer
  - DDR3-1333 with 16-bit bus width.
  - 2 Gb
- Powered by the external power supply with DC 30-35V

General purpose logic module for J-PARC experiments.
Clock/timing distribution is one of its tasks.

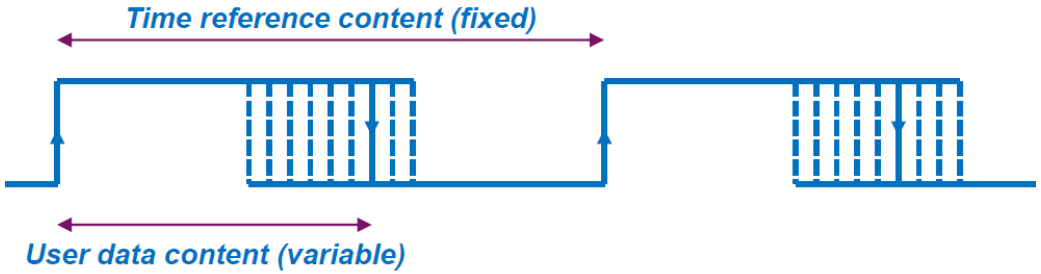
R. Honda et al., 16pV1-10

Clock-duty-cycle-modulation (CMCM) based transceiver

Principle of CDCM

Adopting clock-duty-cycle-modulation (CDCM) as a core technology

- CDCM is a data-on-clock type modulation. (8b10b is a clock-on-data type)
- Data bits are embedded to the trailing edges of the clock signal.



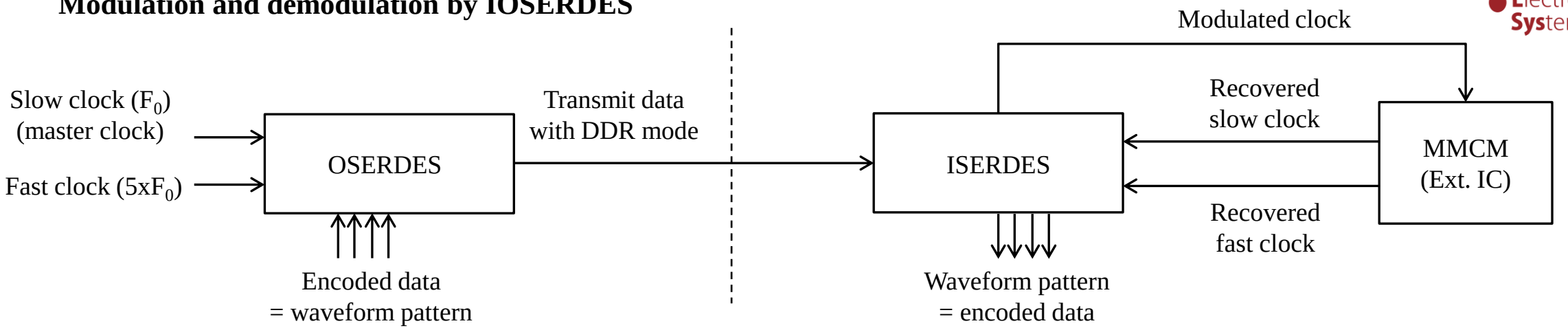
Denis Calvet,
IEEE TNS (Volume: 67, Issue: 8, Aug. 2020)

Advantages

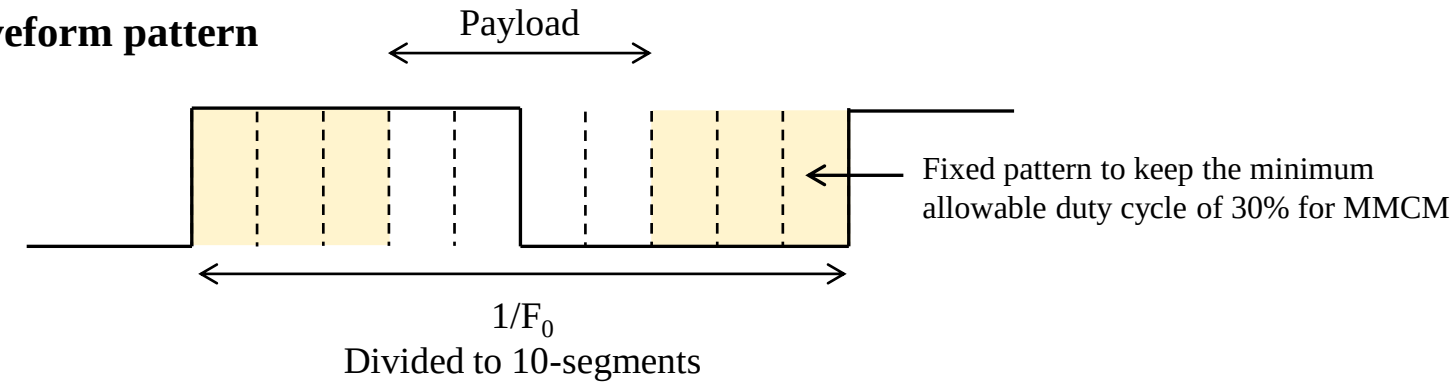
- This modulated clock can be directly input to PLLs and MMCMs in FPGA and external jitter cleaner ICs.
  - Because the leading edge is used by the phase detector to control VCO, but the trailing edge is not.
- Output clock skews from MMCMs respect to the input modulated clock are automatically adjusted by using the global clock network in FPGA.
  - Automatic phase alignment among front-end electronics.
  - Recovered clock by MMCM can give a phase reference for a clock from the external PLL, which does not have a zero-delay mode.

Principle of CDCM

Modulation and demodulation by IOSERDES



Waveform pattern



*0.5 means idle pattern
Naming rule is defined in Ref. [1]

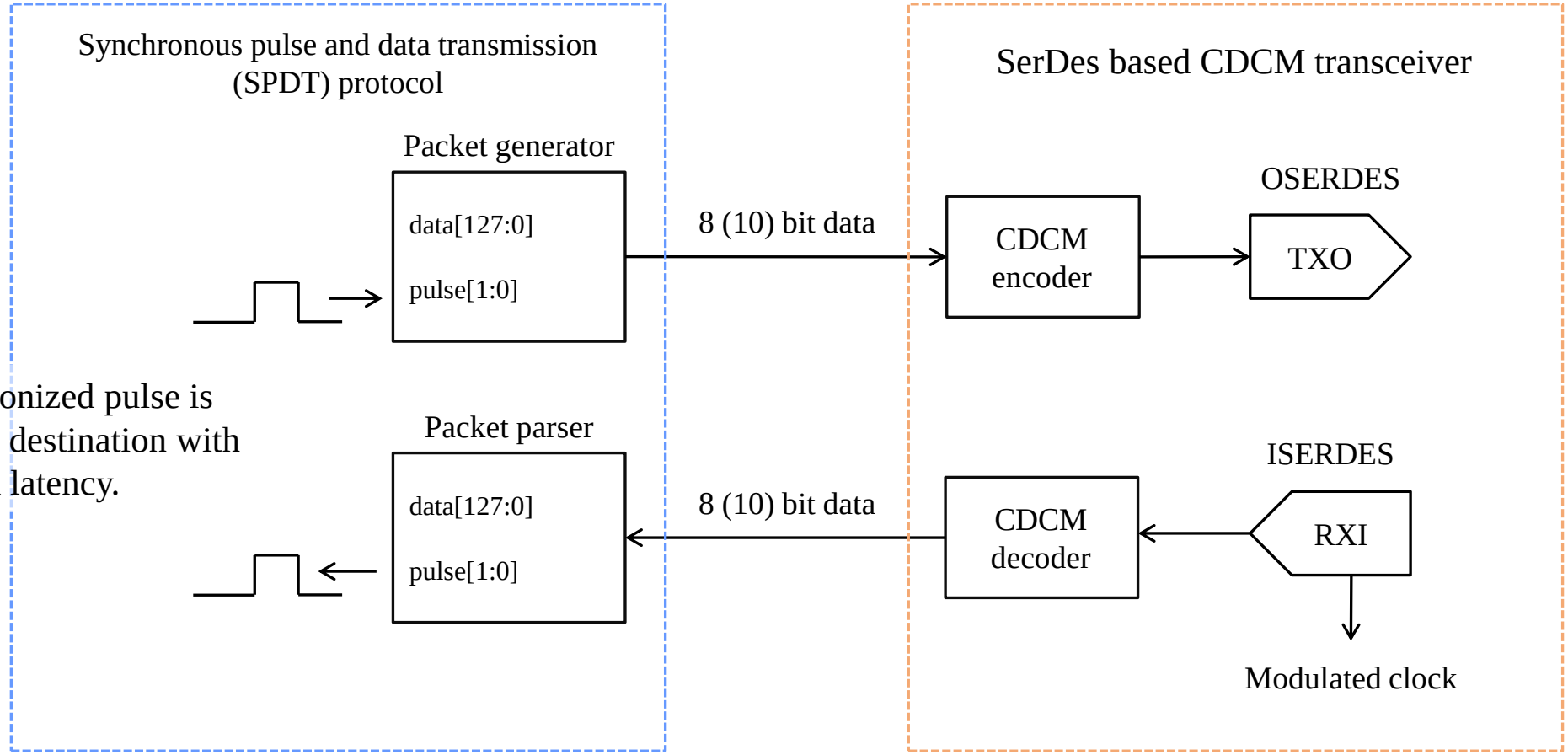
CDCM-10-2.5
CDCM-10-1.5
are realized by IOSERDES

For skew adjustment between slow and fast clocks, the global clock buffer is necessary.

- Maximum transferrable frequency: 125 (142) MHz due to the limitation of the BUFG performance.

[1]. D. Calvet, IEEE TNS (Vol67, Issue8, Aug. 2020)

Developed FPGA firmware components

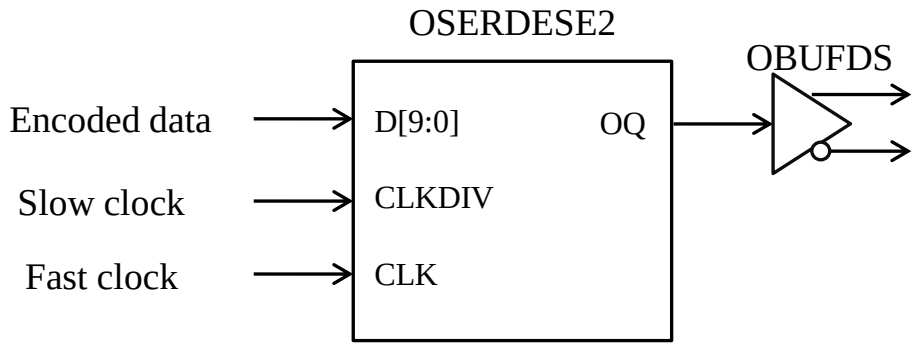


Clock synchronized pulse is transferred to a destination with a fixed latency.

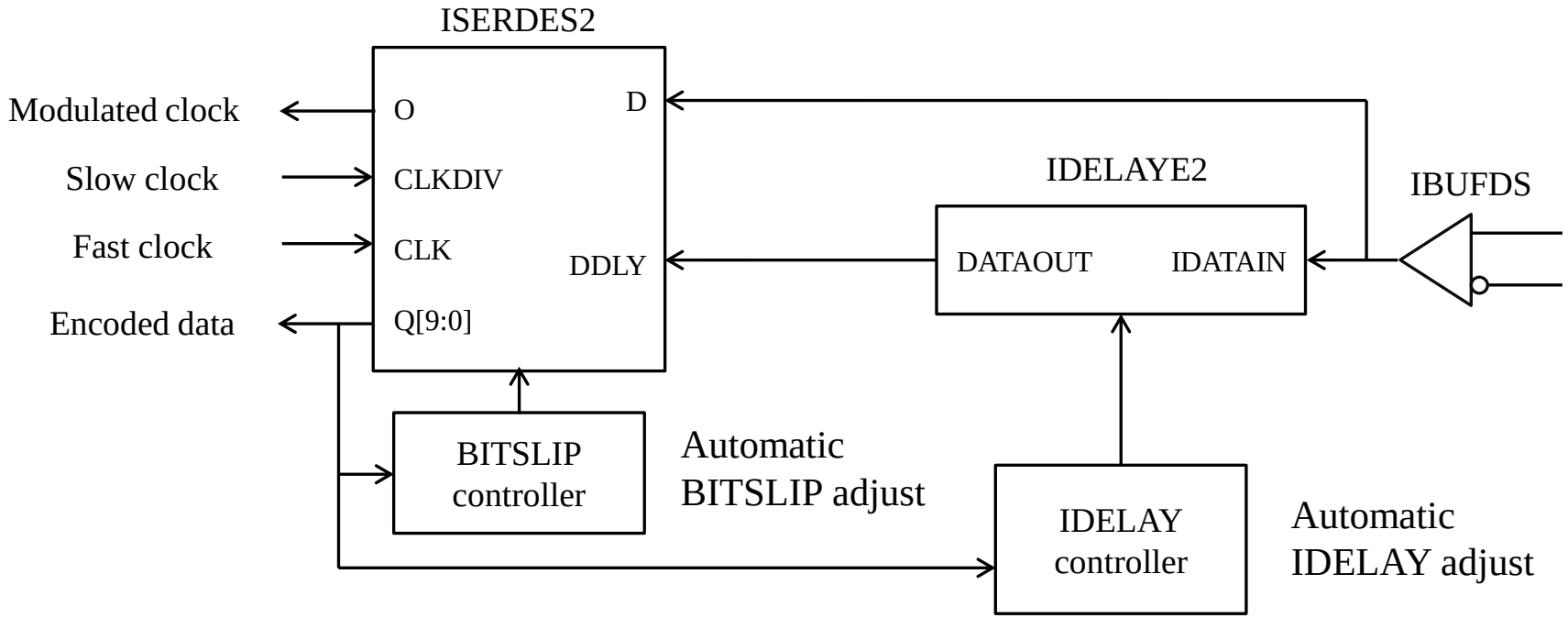
MIKUMARI
水分神（みくまりのかみ）：水の分配をつかさどる神

SerDes based CDCM transceiver

TXO



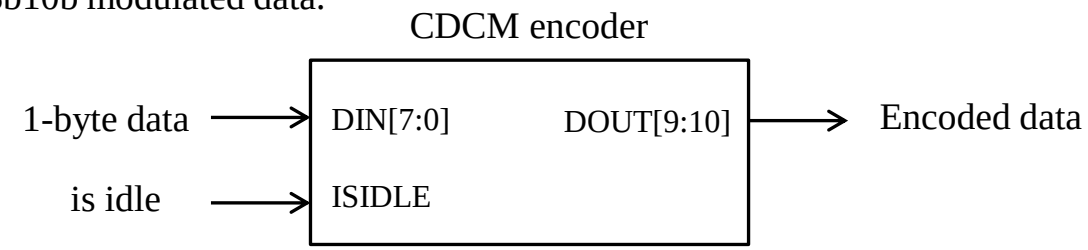
RXI



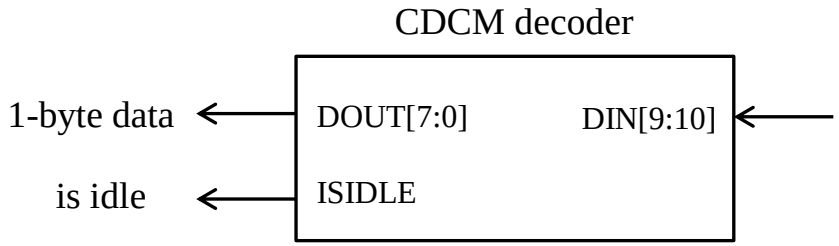
SerDes based CDCM transceiver

Encoder

*10-bit length data input
is also supported for
8b10b modulated data.



Decoder



CDCM-10-2.5 encode table

Binary	Encoded
00	0000
01	0001
IDLE	0011
10	0111
11	1111

Synchronous pulse and data transmission (SPDT) protocol

SPDT protocol

SPDTP packet structure

Magic (0xFD)	Data length + Instruction	Pulse timing	Reserve	User data	Check sum	IDLE
1 byte	1 byte	2 byte	1 byte	0-16 byte	2 byte	1 byte

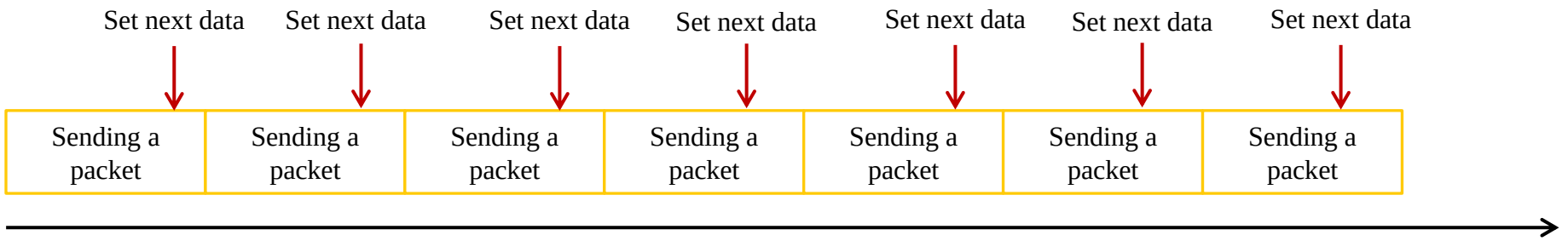
***IDLE: duty 50% pattern.

- CDCM data rate: 2-bit per clock-cycle (CDCM-10-2.5)
- Encoder/decoder need 4 clock-cycles to encode/decode 1-byte data.
- SPDTP packet size: 8-bytes + user data (0-16 bytes)
  - 32-96 clock-cycles are necessary to send/receive a packet.

Expect to periodically transfer a fixed size packet.
Currently, interrupt at any timing is not considered.

⇨ Pulse timing is included in a packet.

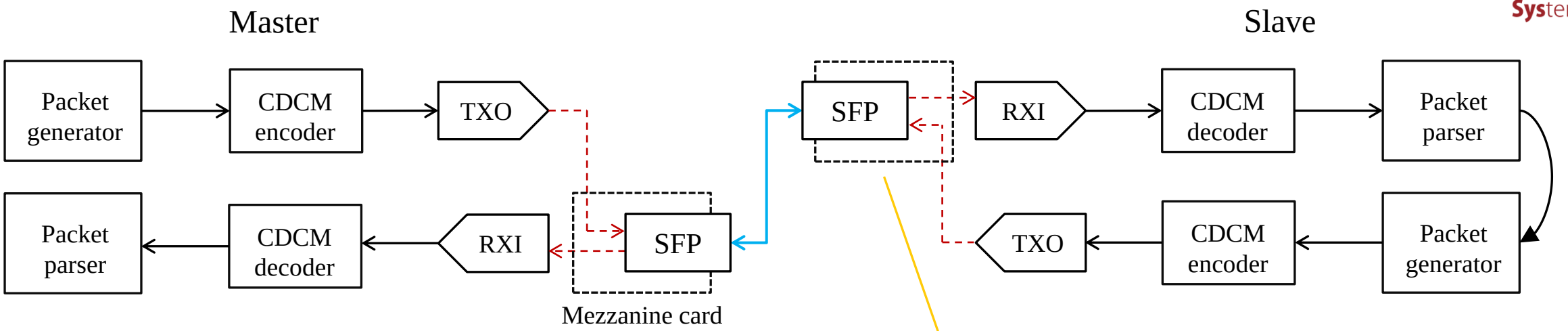
Send packet always

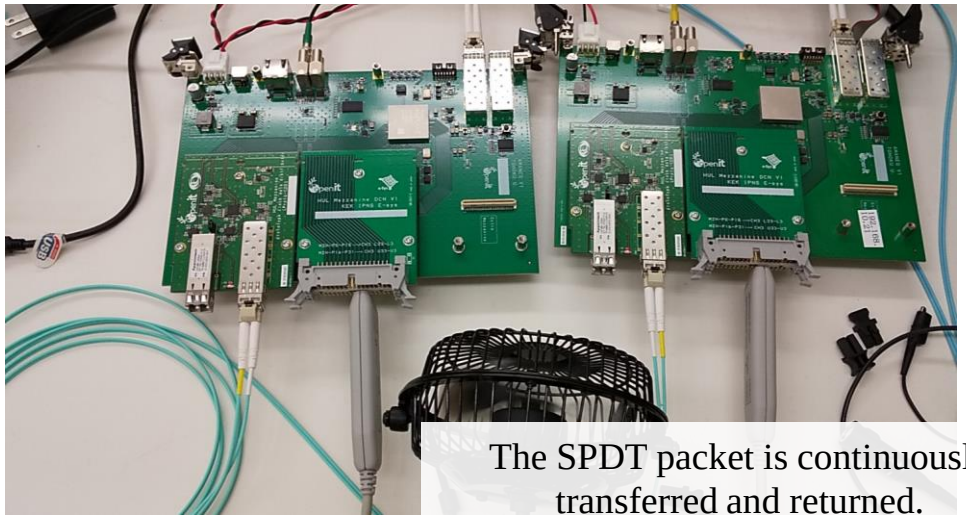


Sometimes send packet

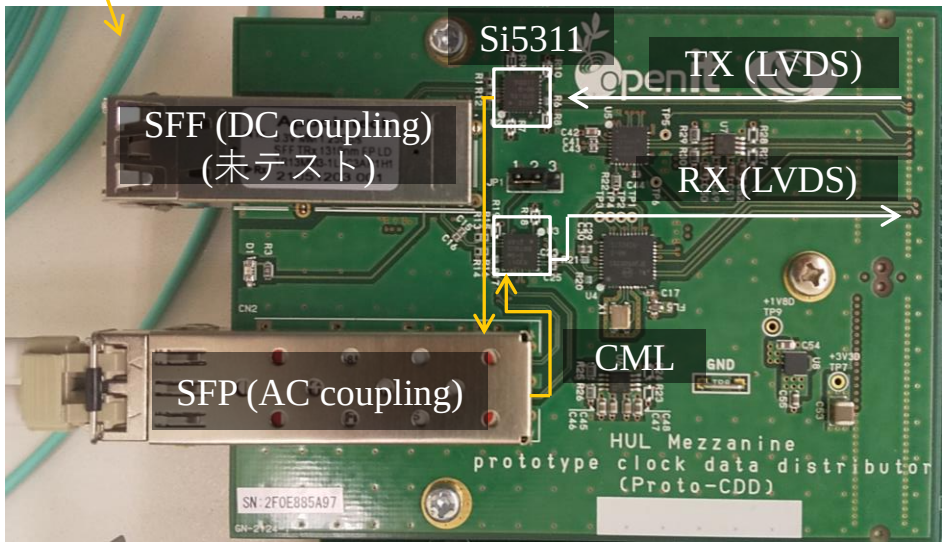
Test results

Test configuration

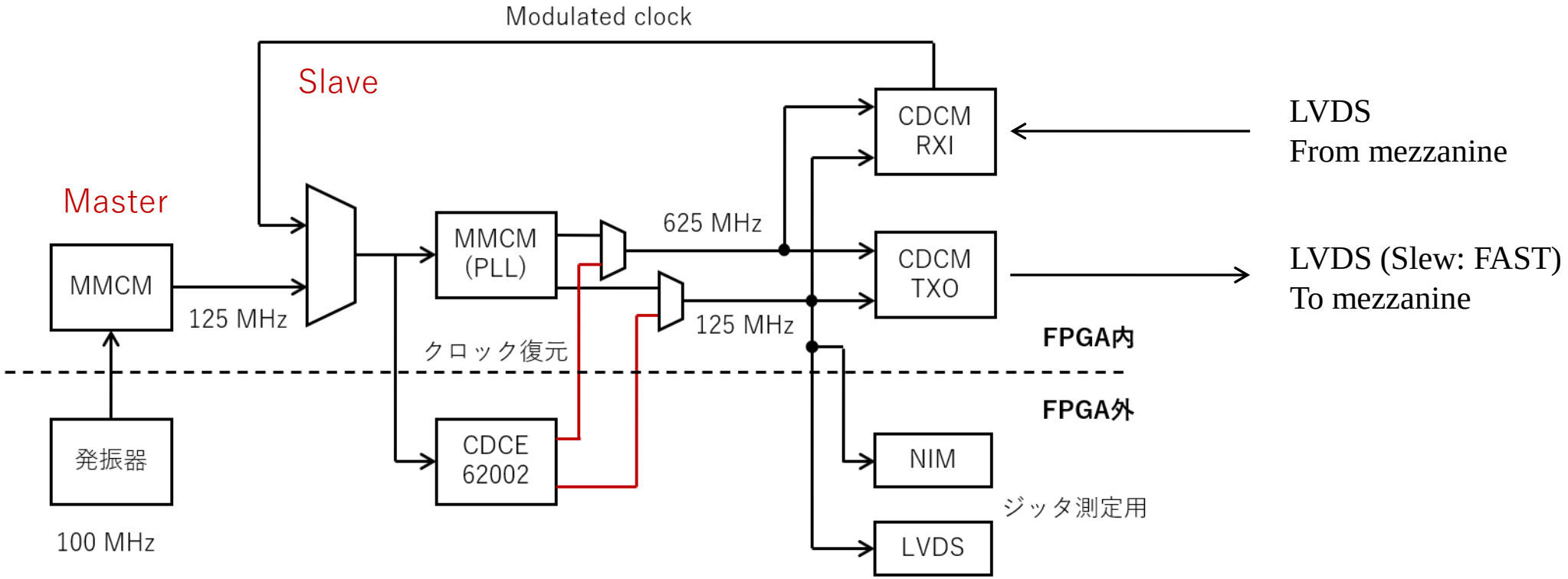




The SPDT packet is continuously transferred and returned.
User data: incremental data.



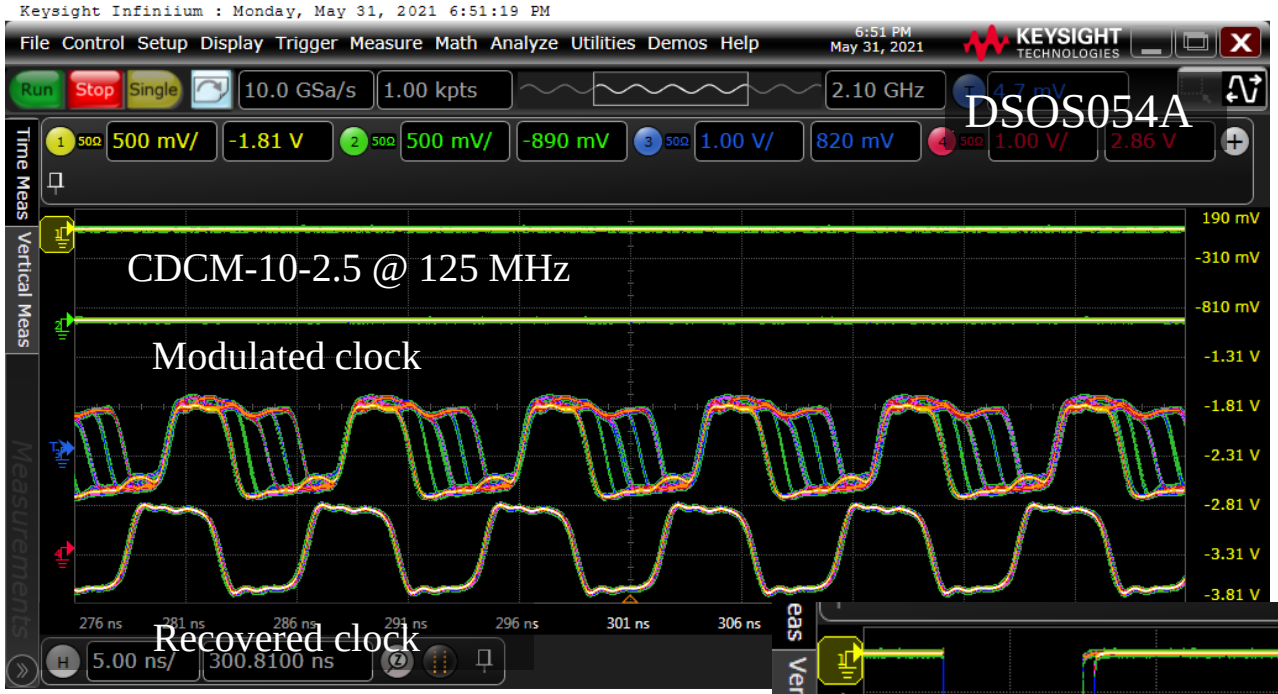
Test configuration (clock path)



Used oscilloscope

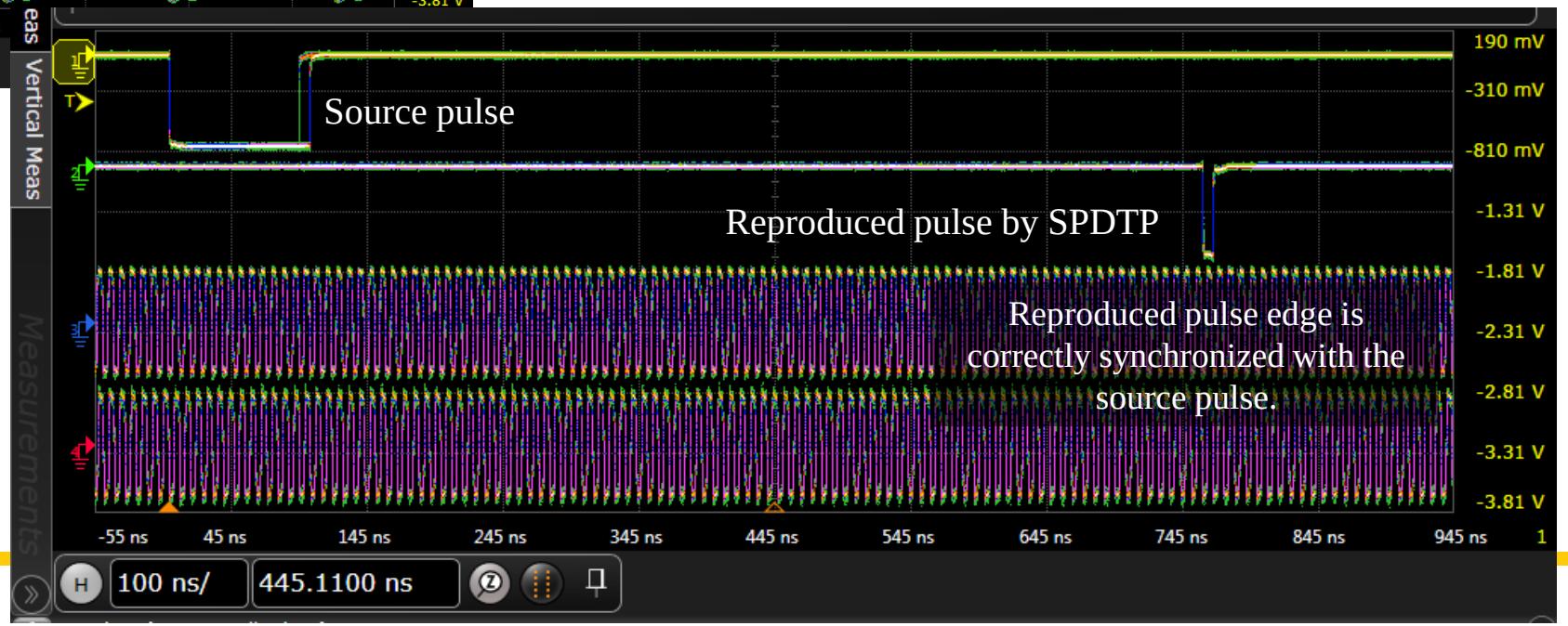
- Keysight DSOS054A (Analog BW: 2.1 GHz, 20 GSPS)
  - For NIM signal measurement
- Tektronix DPO 7254 (Analog BW: 2.5 GHz, 40 GSPS)
  - For LVDS measurement

Demonstration



40T packets were transferred in this demo.
No packet drop and checksum mismatch were happened.

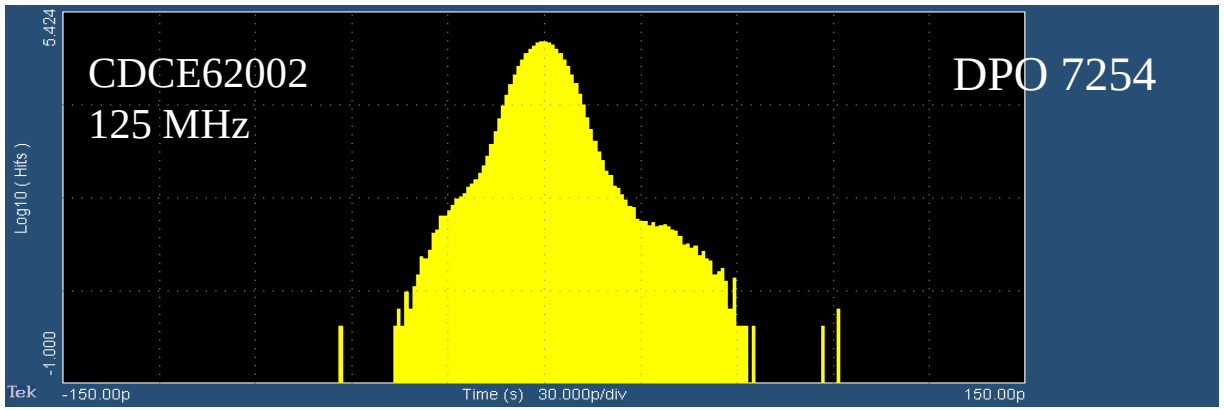
Pulse transfer by SPDT protocol

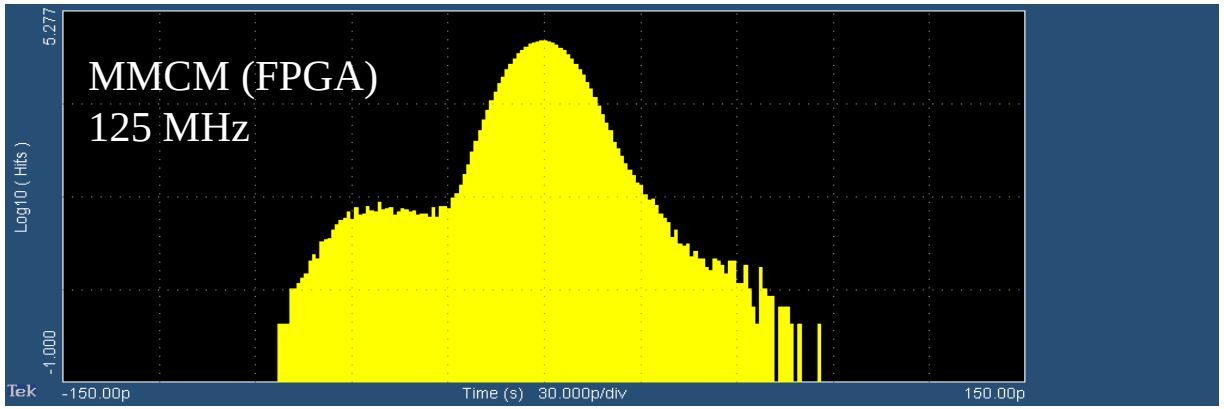


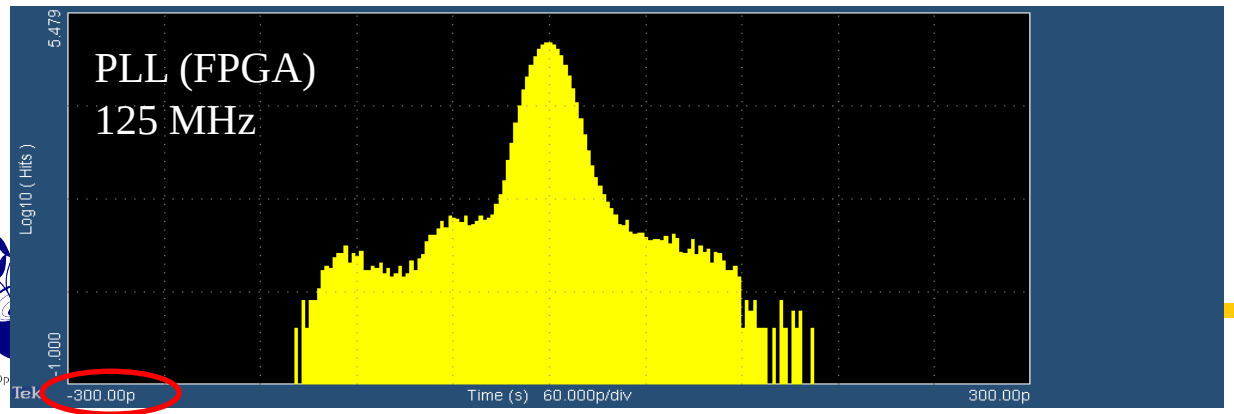
Jitter performance of master clock

Electronics System Group

Jitter distribution of master clock







	Std. div.	Total jitter (Tj) @ BER 1e-12
CDCE6200	5.0	110 77
MMCM	7.9	190 106
PLL	8.8	297 114

DPO7254
DSOS054A

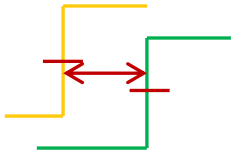
Unit: ps

	CDCM linkup	SPDT data transmission
CDCE62002	Succeed	Succeed
MMCM (FPGA)	Succeed	Succeed
PLL (FPGA)	Succeed	**Fail**

Linkup: Completing IDELAY adjust and bit slip for SERDES and encoder/decoder.

FW with PLL detects the broken modulated pattern soon after the communication start.
Modulated pattern transfer and/or receive don't work well due to the large clock jitter.

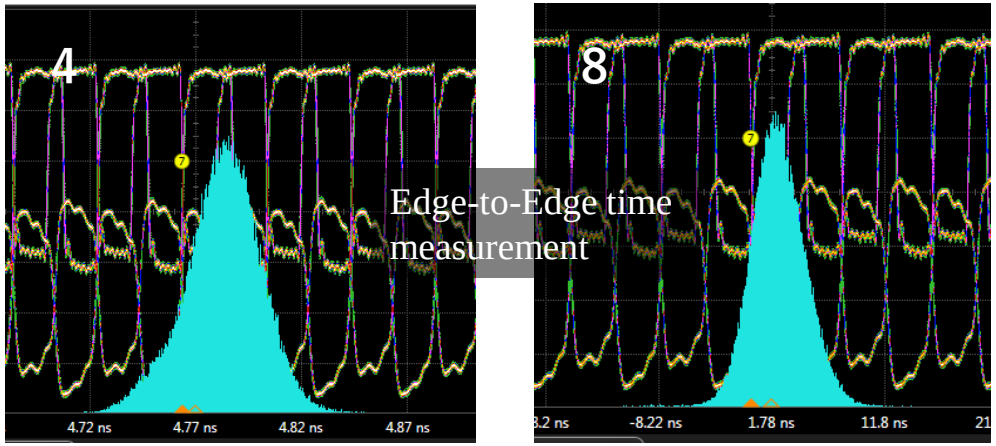
Jitter performance of recovered clock



Edge-to-Edge time measurement
between master and recovered clock

Condition	Master	Slave	データ送信	Edge-Edge Std. div.	Recovered clock jitter Std. div.	Tj @ BER 1E-12
1	CDCE	CDCE	SPDTP	12.5	8.9	158 70
4	MMCM	MMCM	SPDTP	17.7	15.5	240 168
5	CDCE	CDCE	アイドル	11.4	8.8	162 71
8	MMCM	MMCM	アイドル	11.9	7.6	213 121

Unit: ps

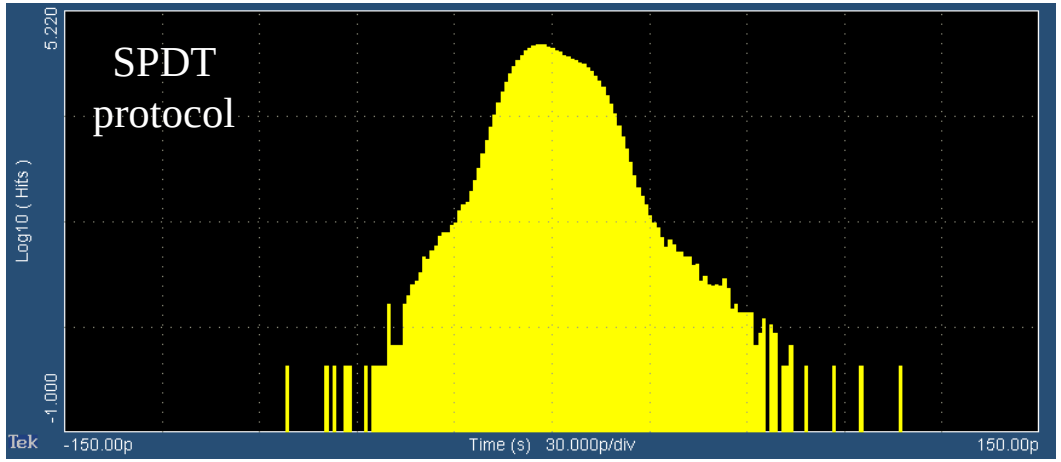


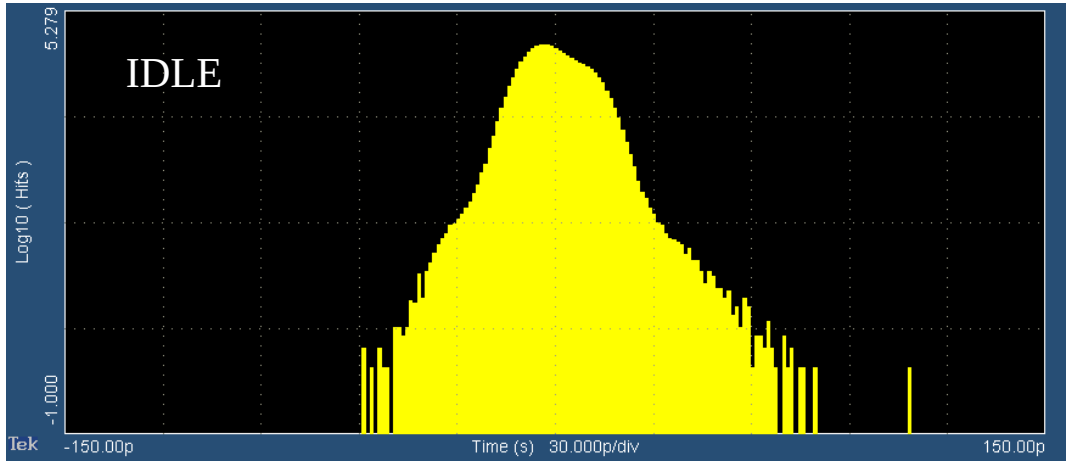
Edge-to-Edge measurement reflects the structure of the main peak of the jitter distribution.

In order to take into account the long tail structure, additional jitter measurement using the spectrum fitting is necessary.

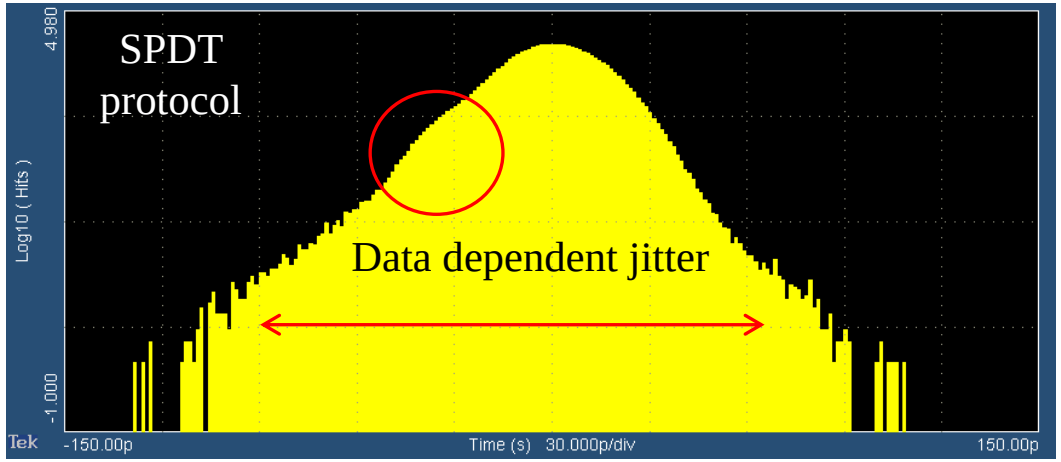
Jitter performance of recovered clock

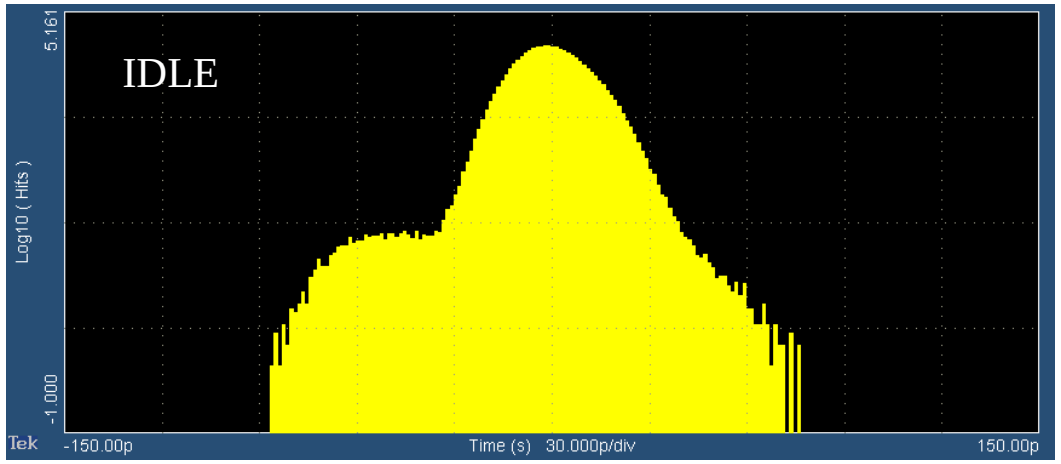
Jitter distribution of recovered clock
(CDCE62002 - CDCE62002)





Jitter distribution of recovered clock
(MMCM - MMCM)





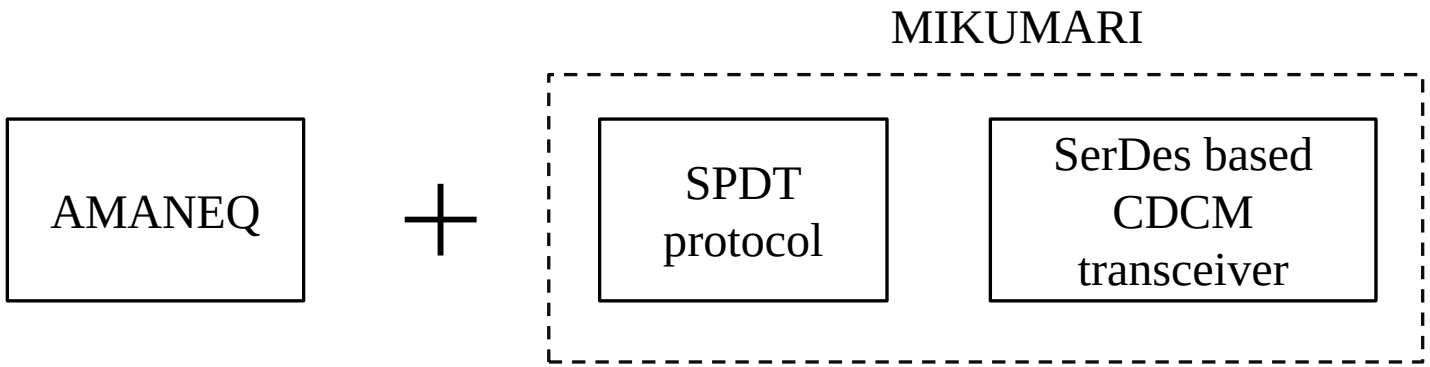
Data dependent jitter is suppressed in the case of CDCE62002.
If you use MMCM, sending IDLE pattern provides a better jitter performance.

Future prospect

Performance evaluation

- Develop a protocol to recovery CDCM link when a link is down.
- Use spectrum analyzer to evaluate jitter in the frequency domain.
- Measure the actual TOF distribution using HR-TDC synchronized by MIKUMARI.

Promotion



Each part is independent from other.
If you are interested in any parts, please contact with me.

Summary

- AMANEQ will be used for the clock/timing distribution in the J-PARC experiments.
- In order to transmit the clock and data using a full-duplex optical transceiver, clock-duty-cycle-modulation was adopted.
  - The modulated clock can be directly fed into PLL.

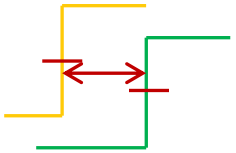
- SerDes based CDCM transceiver and the synchronous pulse and data transmission (SPDT) protocol were developed and implemented in FPGA on AMANEQ.
  - The maximum clock frequency can be transferred by this transceiver is 125 and 142 MHz for the speed grade -1 and -2 FPGA, respectively.

- The jitter performance of CDCE62002 is better than that of MMCM in FPGA.
  - 5.0 ps in std. div., ~110 ps peak-to-peak (eye measurement.)
- PLL in FPGA accompanies a long tail in the jitter distribution. And the clock from PLL can not drive the CDCM transceiver correctly.

- The two AMANEQs are synchronized within 12-13 ps in std. div..
- Basically, sending IDLE patter except when the trigger is transmitted provides the better jitter permeance.

Backup

Jitter performance of recovered clock



Edge-to-Edge time measurement
between master and recovered clock

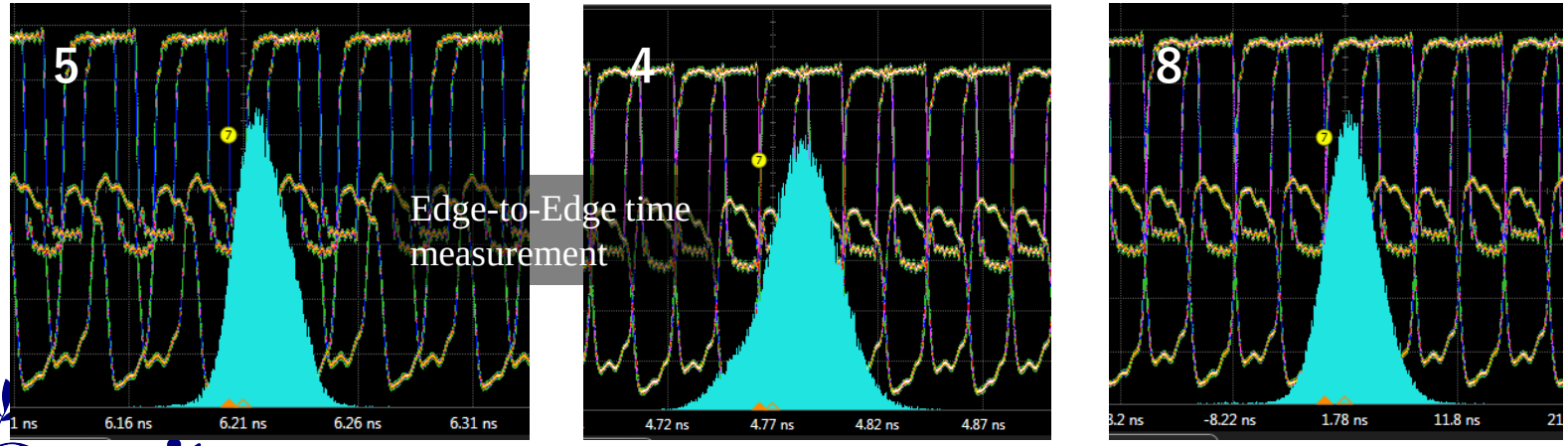
Recovered clock jitter

Condition	Master	Slave	データ送信	Edge-Edge Std. div.	Std. div.	Peak-to-peak
1	CDCE	CDCE	SPDTP	12.5	8.9	~140
2	MMCM	CDCE	SPDTP	13.2	9.0	~140
3	CDCE	MMCM	SPDTP	17.0	9.6	~160
4	MMCM	MMCM	SPDTP	17.7	15.5	~230
5	CDCE	CDCE	アイドル	11.4	8.8	~120
6	MMCM	CDCE	アイドル	13.2	8.6	~140
7	CDCE	MMCM	アイドル	10.3	9.2	~150
8	MMCM	MMCM	アイドル	11.9	7.6	~160

Unit: ps

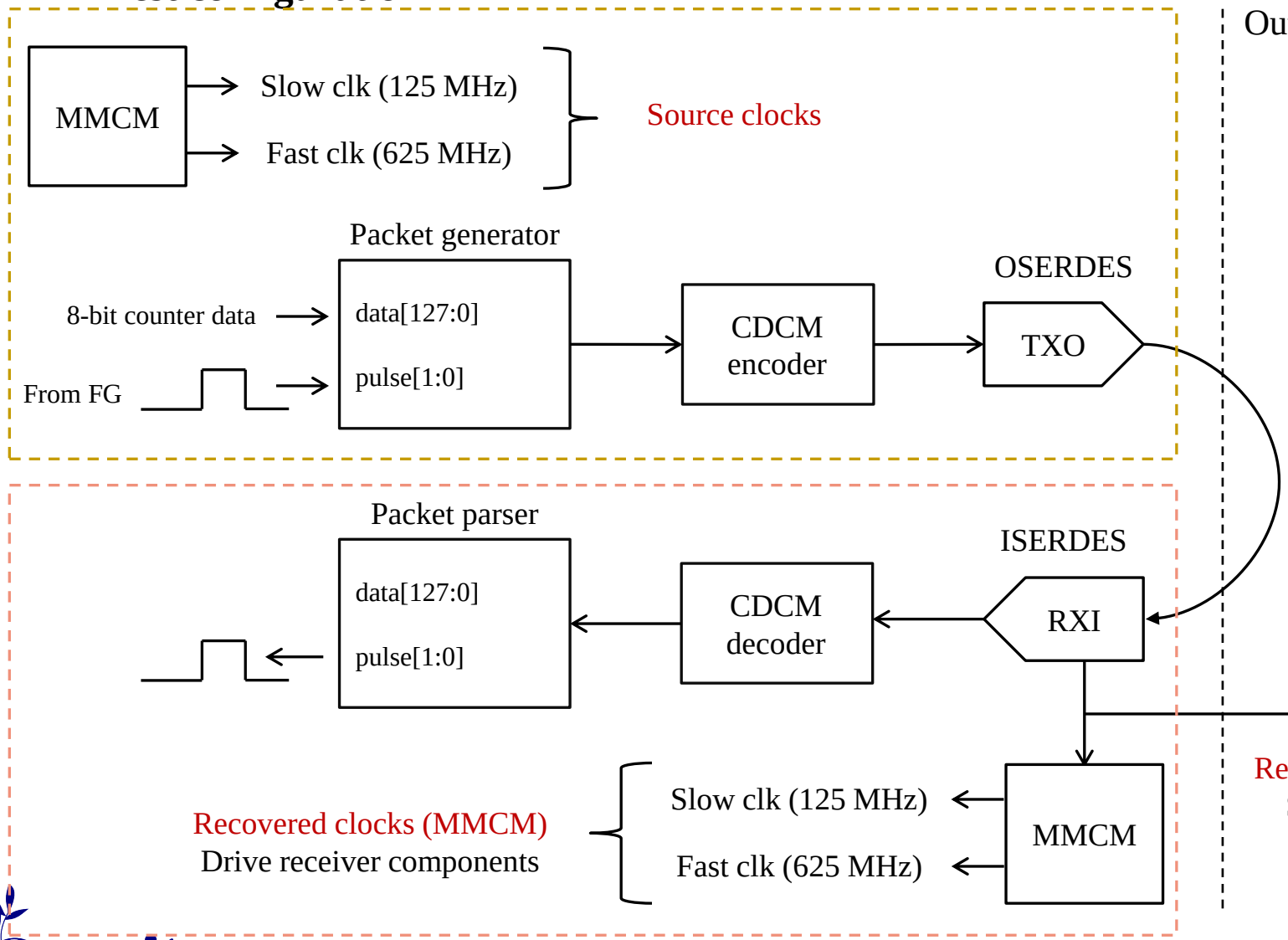
Measured by DPO 7254

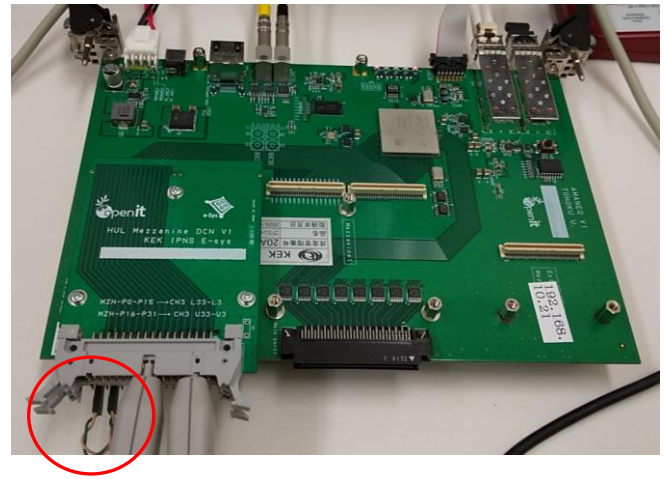
Idle: duty 50% clock



Edge-to-Edge measurement reflects the structure of the main peak of the jitter distribution.
In order to take into account the long tail structure, additional jitter measurement using the spectrum fitting is necessary.

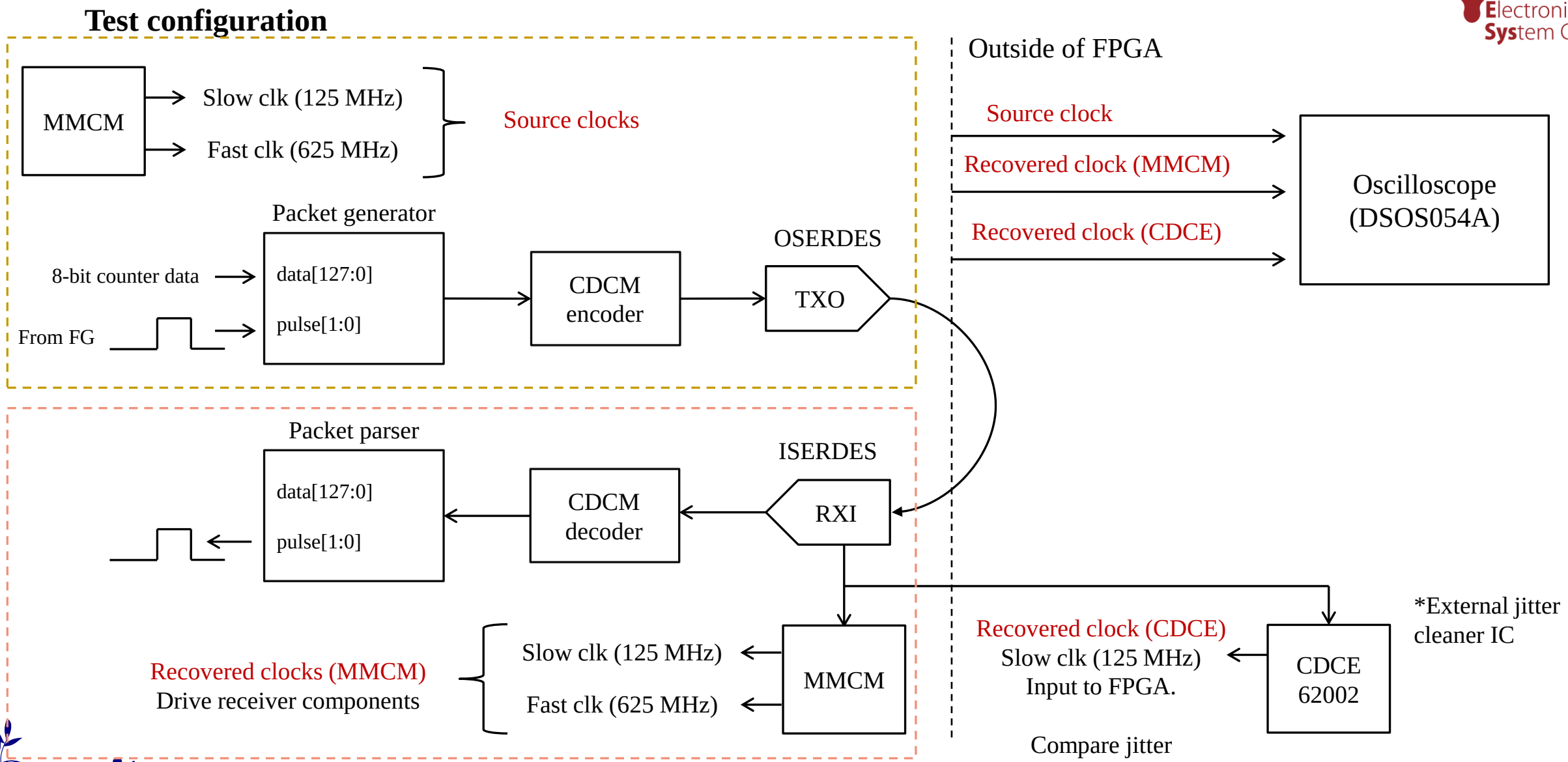
Test configuration





At preset, I don't have two AMANEQs.
I tested them by making loop-back.

*External jitter cleaner IC


Test configuration
MMCM
Slow clk (125 MHz)
Fast clk (625 MHz)
Source clocks
Outside of FPGA
Source clock
Recovered clock (MMCM)
Recovered clock (CDCE)
Oscilloscope
(DSOS054A)
Packet generator
8-bit counter data
From FG
data[127:0]
pulse[1:0]
CDCM
encoder
OSERDES
TXO
Packet parser
data[127:0]
pulse[1:0]
CDCM
decoder
ISERDES
RXI
Recovered clocks (MMCM)
Drive receiver components
Slow clk (125 MHz)
Fast clk (625 MHz)
MMCM
Recovered clock (CDCE)
Slow clk (125 MHz)
Input to FPGA.
CDCE
62002
*External jitter
cleaner IC
Compare jitter
performance with MMCM

Test configuration

Test configuration

MMCM

Slow clk (125 MHz)

Fast clk (625 MHz)

Source clocks

Packet generator

8-bit counter data

From FG

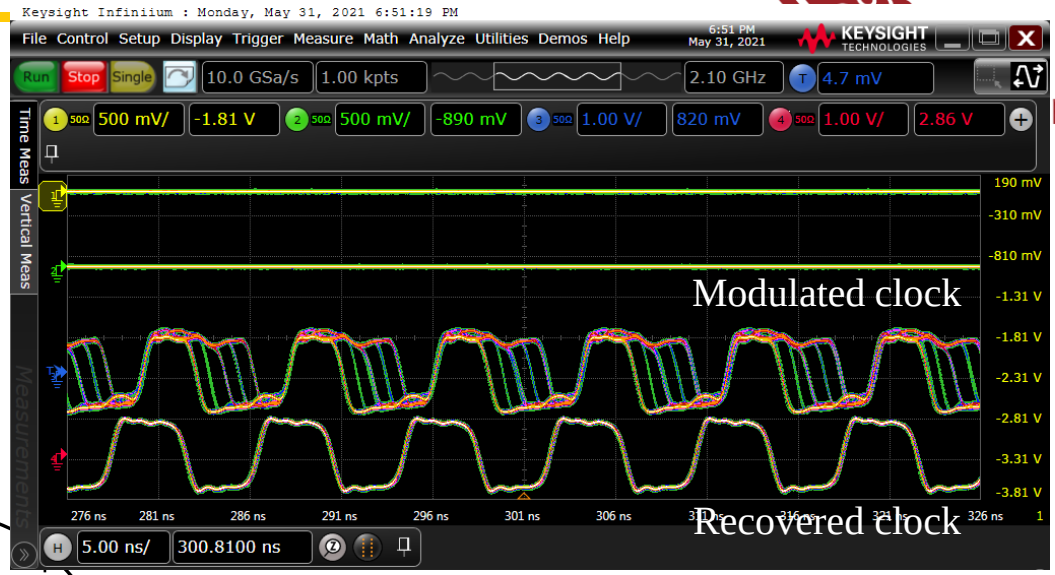
data[127:0]

pulse[1:0]

CDCM encoder

OSERDES

TXO



Packet parser

data[127:0]

pulse[1:0]

CDCM decoder

ISERDES

RXI

Recovered clocks (MMCM)
Drive receiver components

Slow clk (125 MHz)

Fast clk (625 MHz)

MMCM

Recovered clock (CDCE)
Slow clk (125 MHz)
Input to FPGA.

CDCE 62002

*External jitter cleaner IC

Compare jitter performance with MMCM