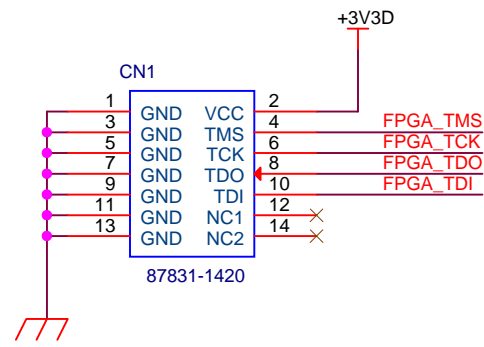
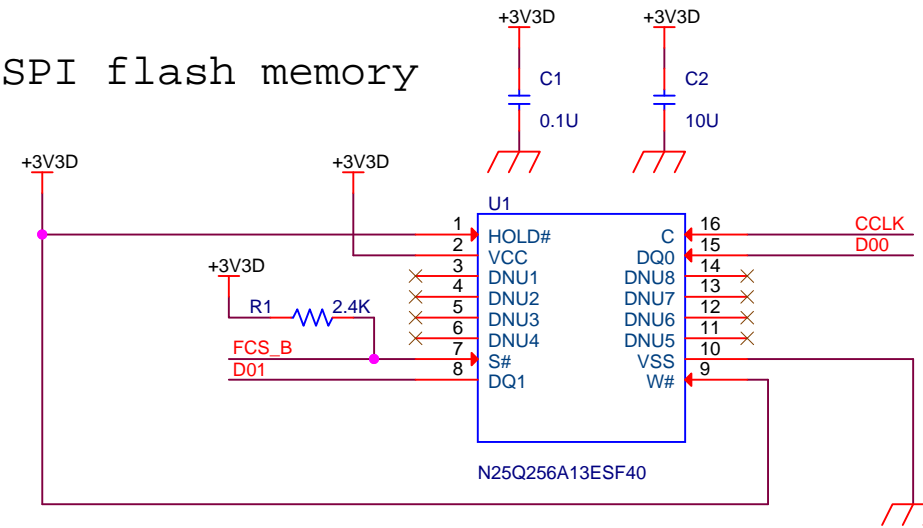


Title		
MicroPOD Testboard (temp)		
Size	Document Number	Rev
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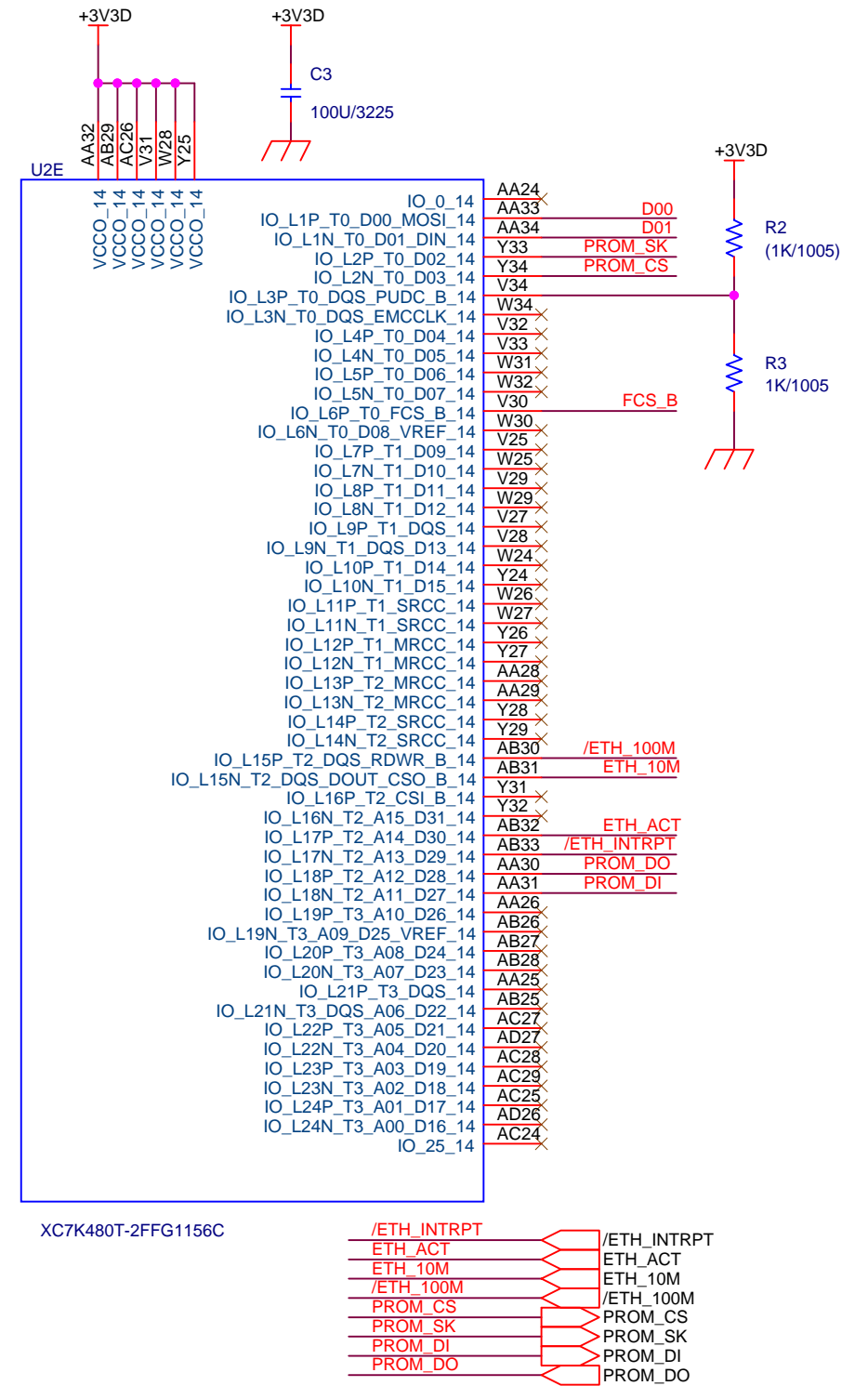
JTAG for FPGA



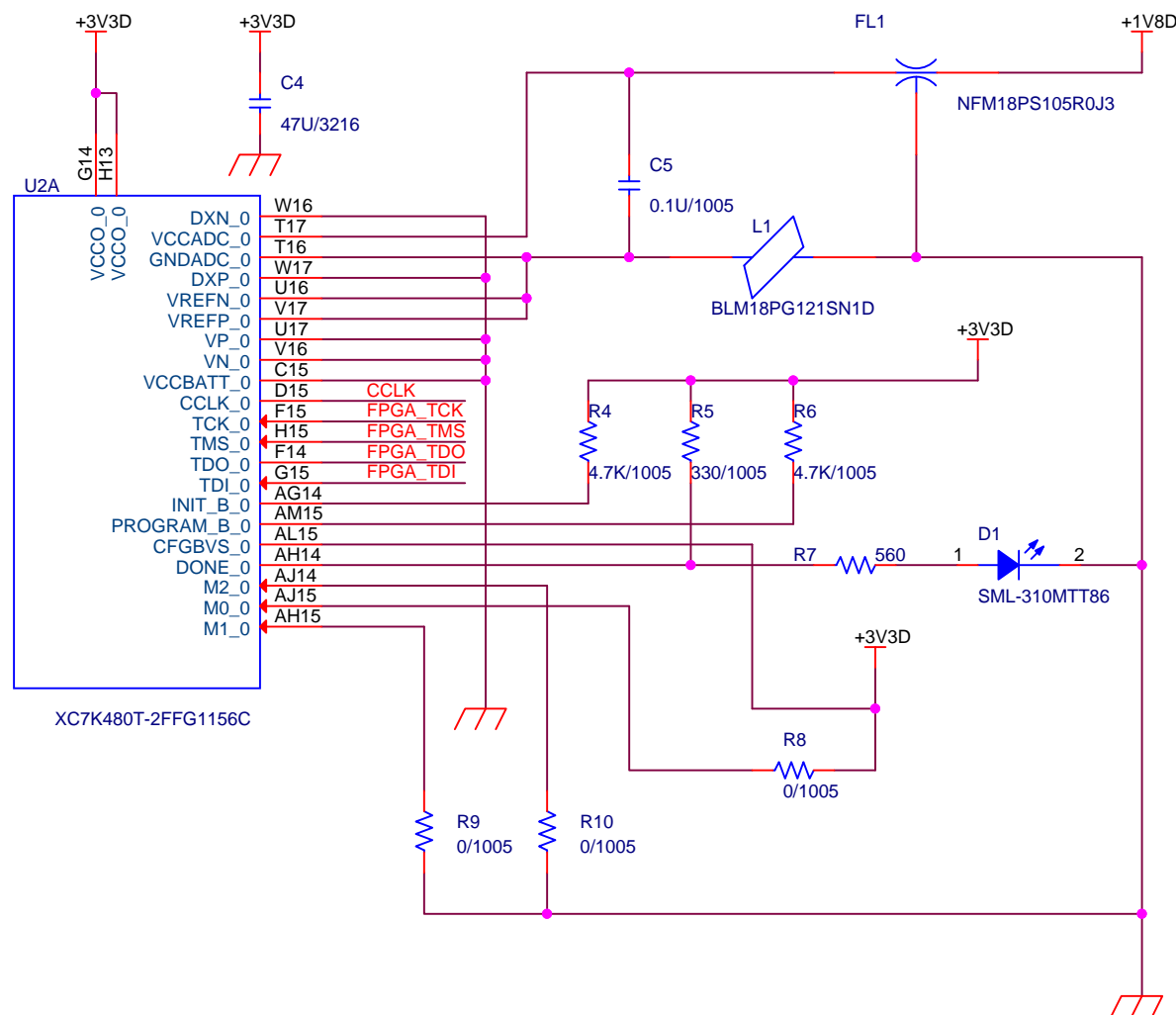
SPI flash memory



FPGA BANK14

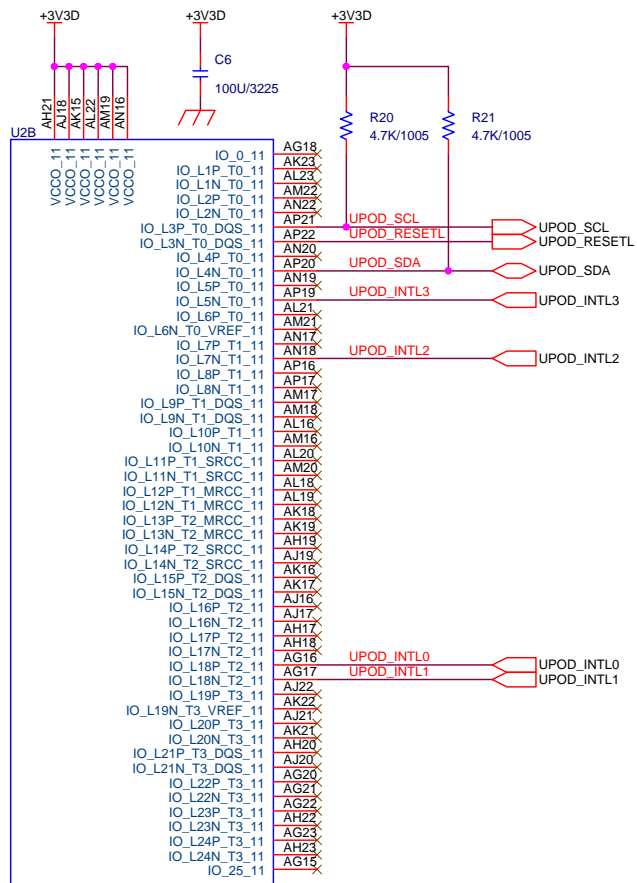


FPGA BANK0



Title		
FPGA_CONFIG		
Size	Document Number	Rev
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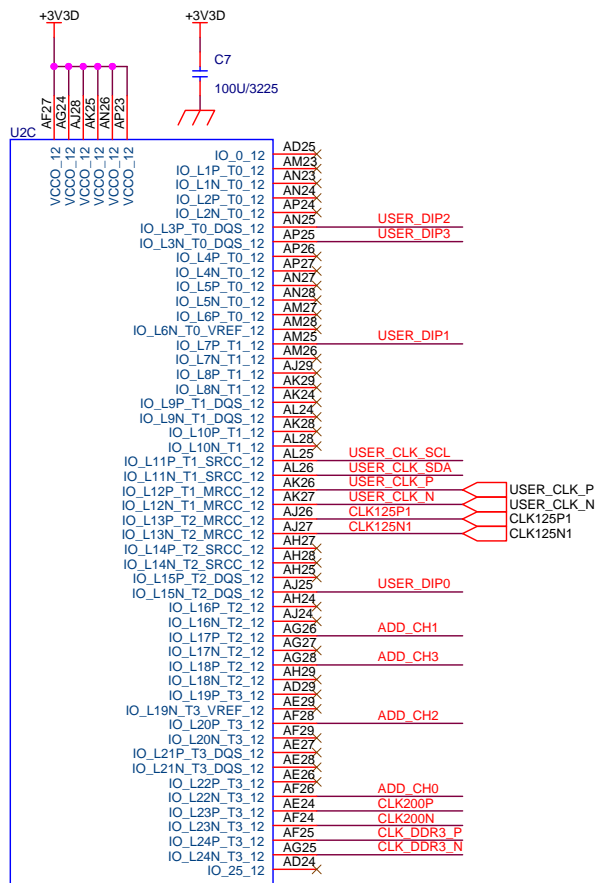
FPGA BANK11



全ての線がスワップ可能

XC7K480T-2FFG1156C

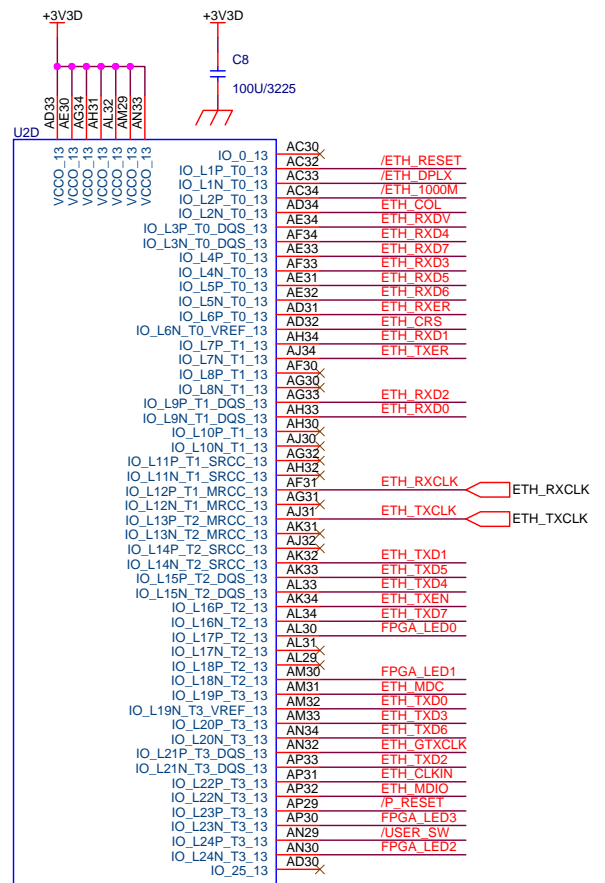
FPGA BANK12



CLK125とUSER_CLKはスワップ不可
それ以外は可

XC7K480T-2FFG1156C

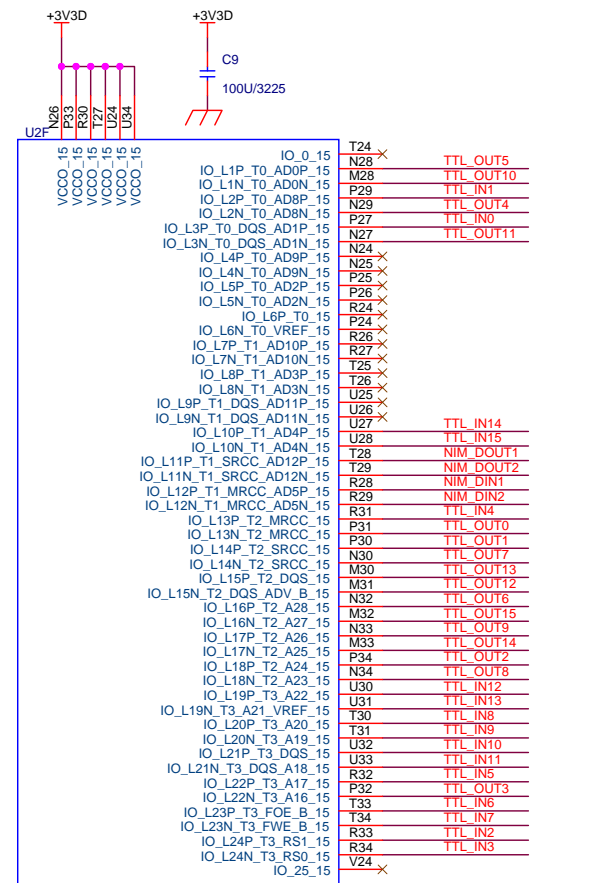
FPGA BANK13



ETH_TXCLKとETH_RXCLKはスワップ不可
それ以外は可

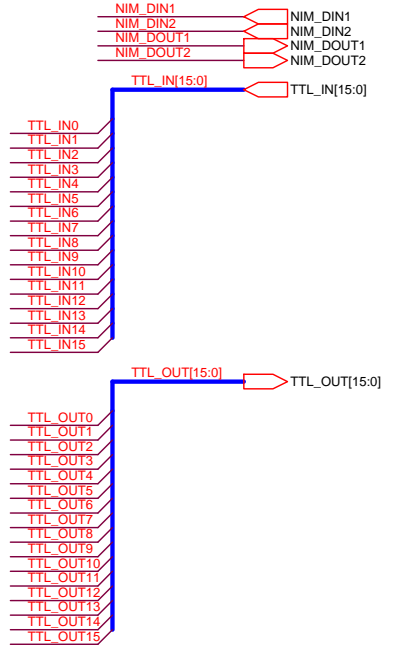
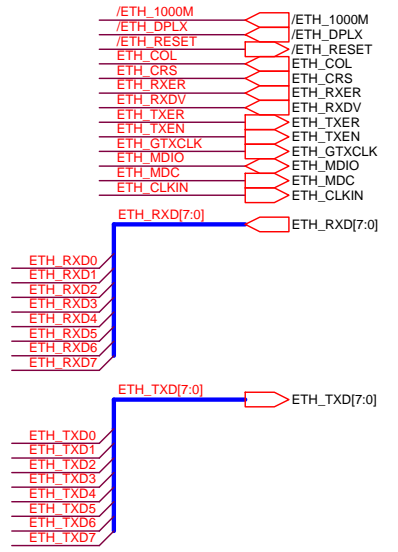
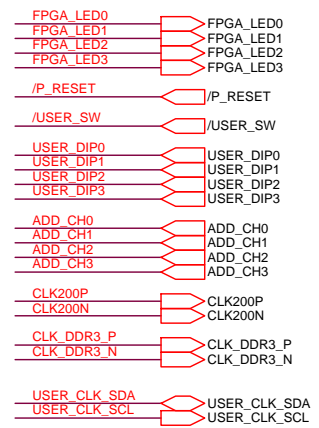
XC7K480T-2FFG1156C

FPGA BANK15

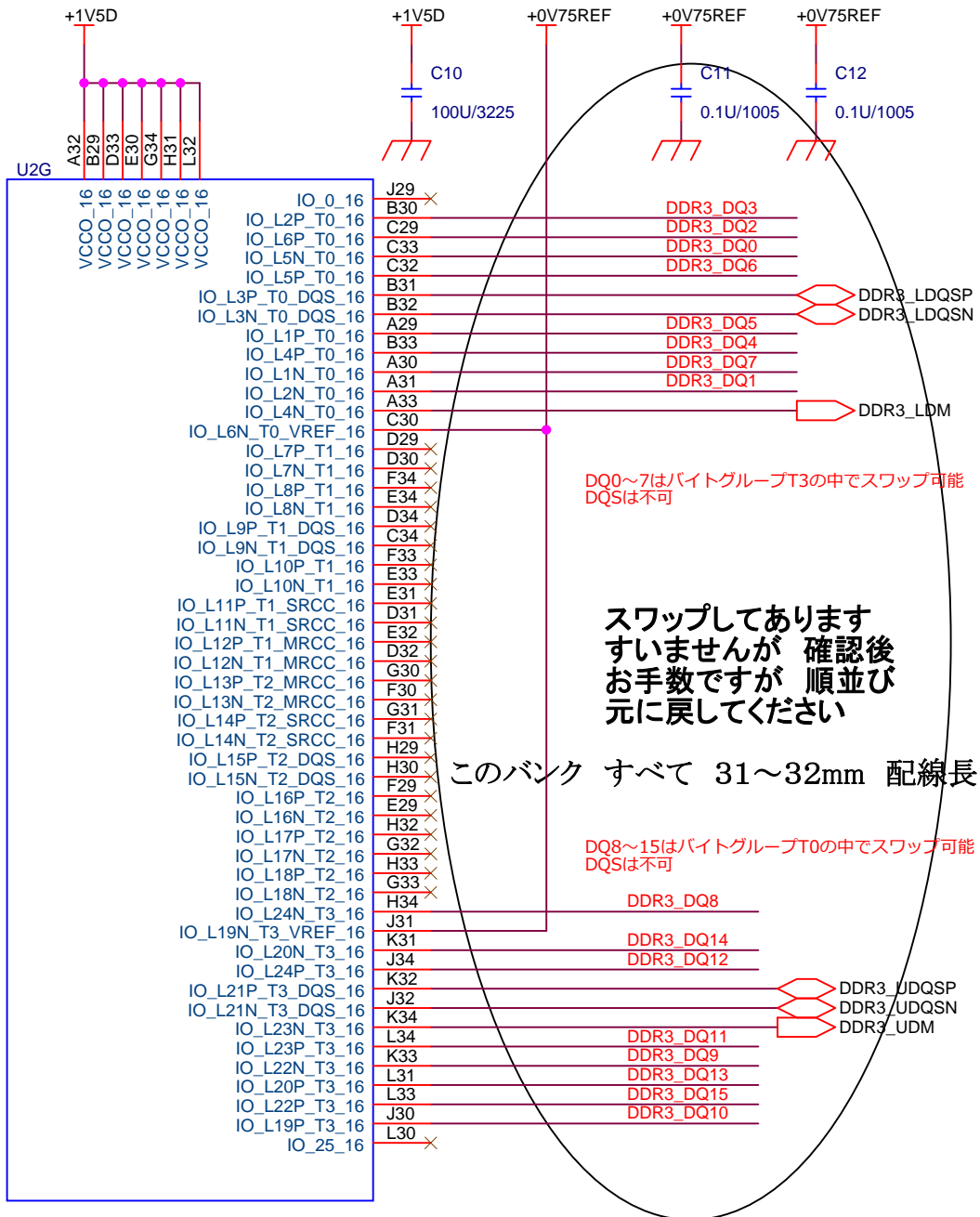


NIM_DIN1,2はスワップ不可
他の線は全てスワップ可能

XC7K480T-2FFG1156C

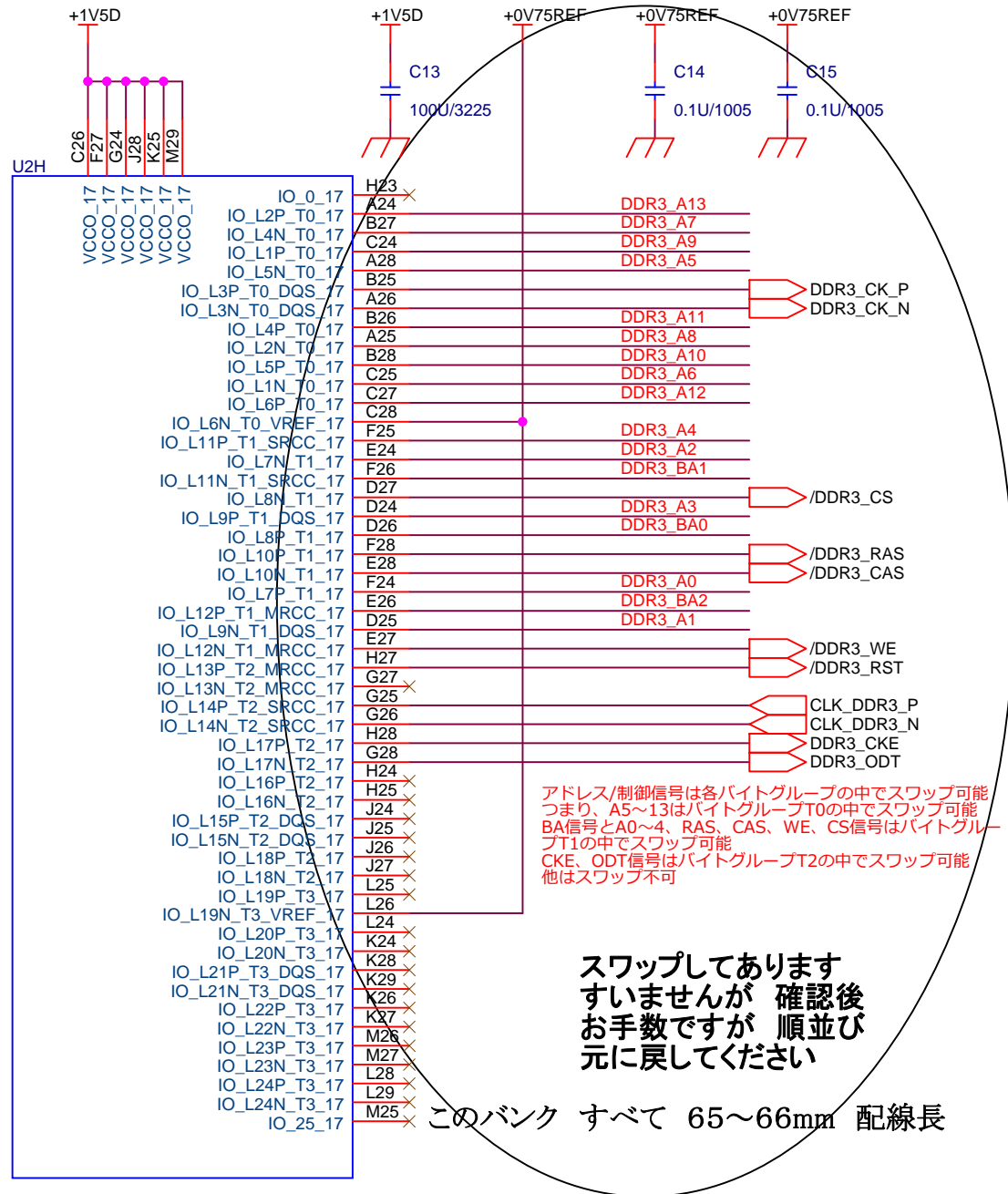


FPGA BANK16



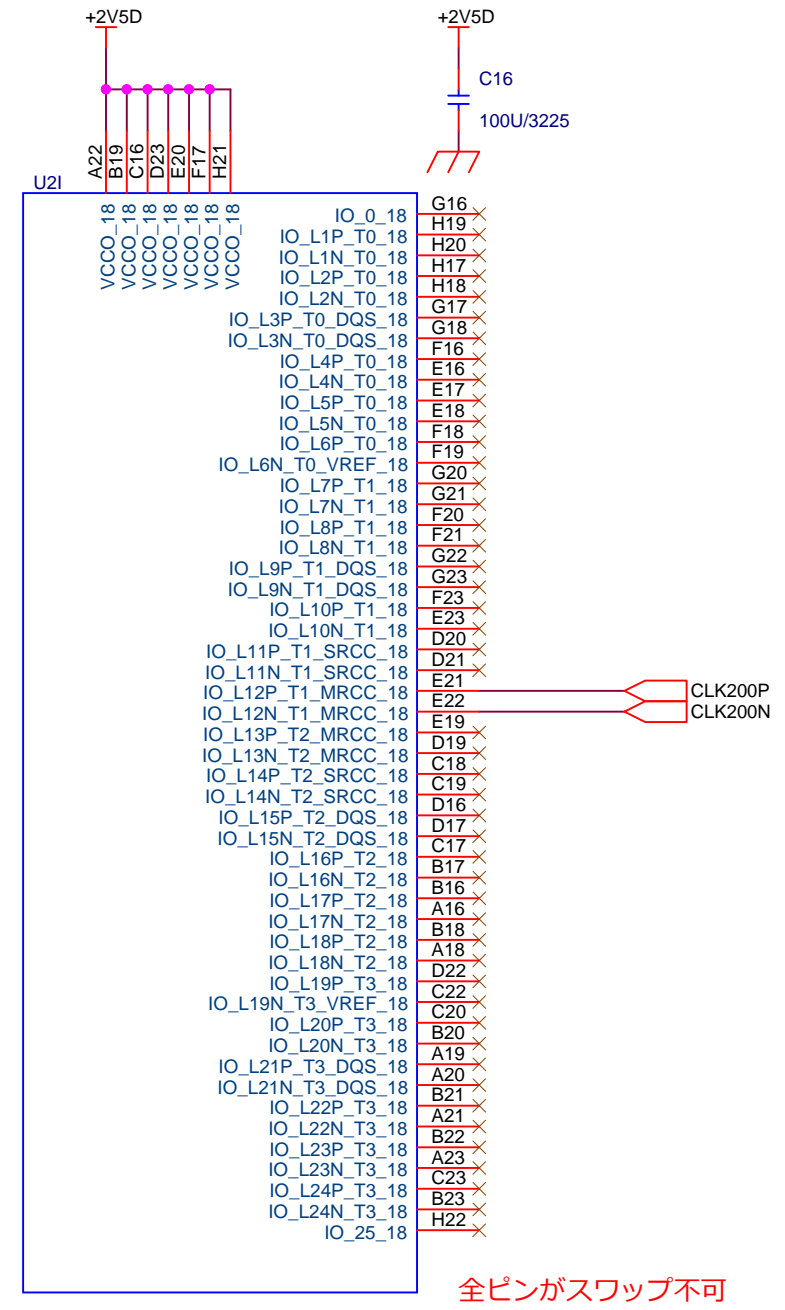
XC7K480T-2FFG1156C

FPGA BANK17

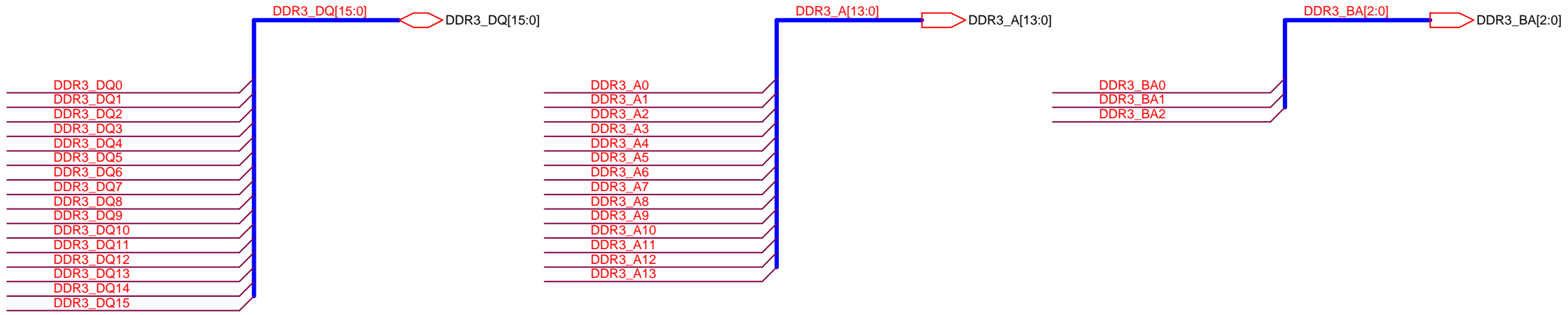


XC7K480T-2FFG1156C

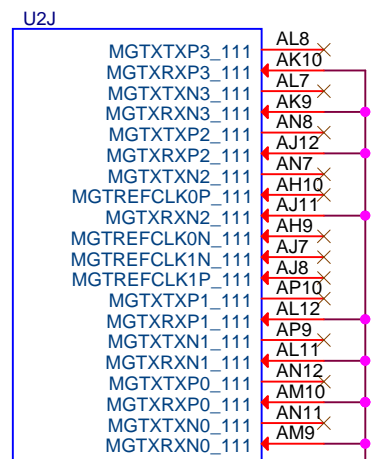
FPGA BANK18



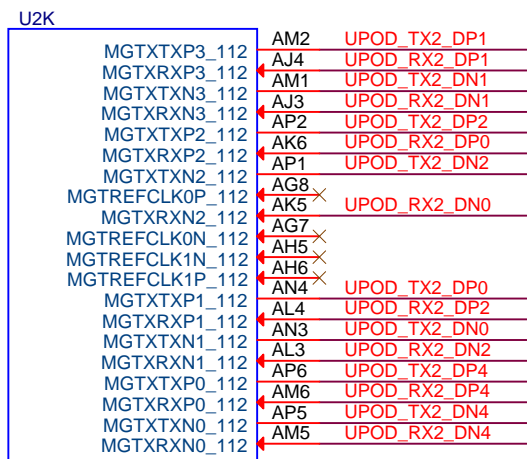
XC7K480T-2FFG1156C



Title		
FPGA_IO2		
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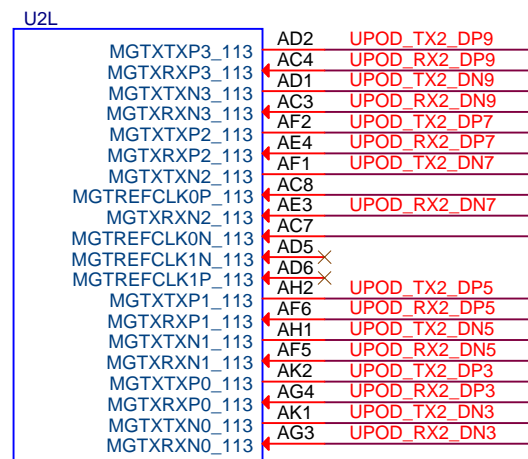


XC7K480T-2FFG1156C



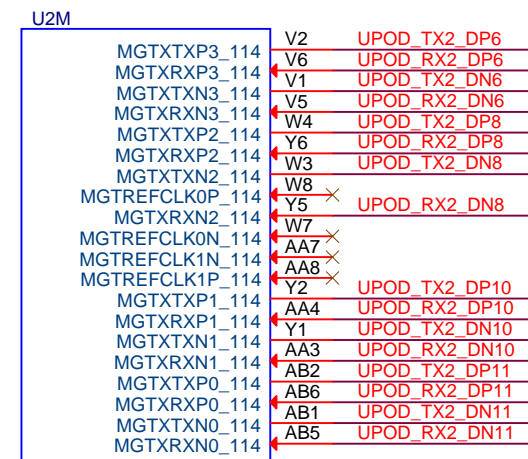
XC7K480T-2FFG1156C

0~3のチャンネル単位で
スワップ可能
PとNもスワップ可能



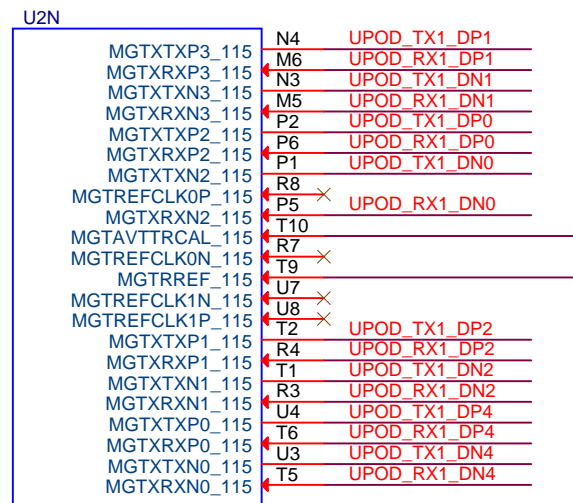
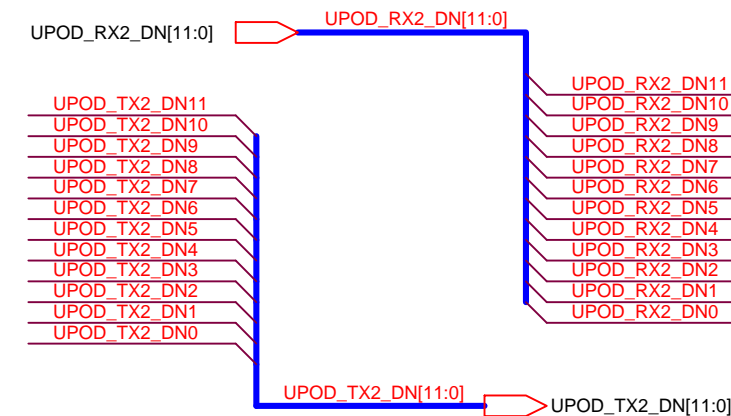
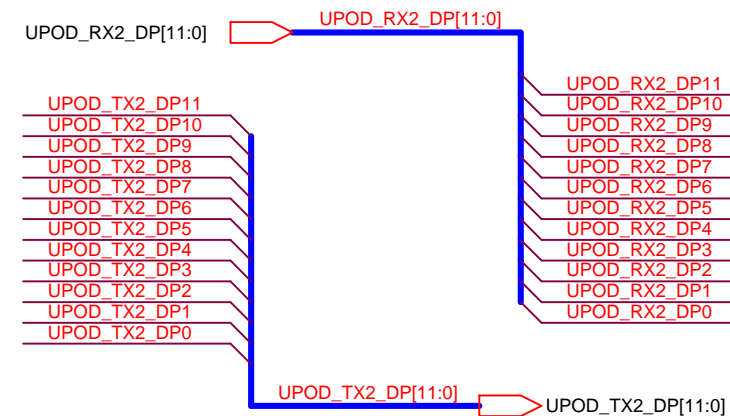
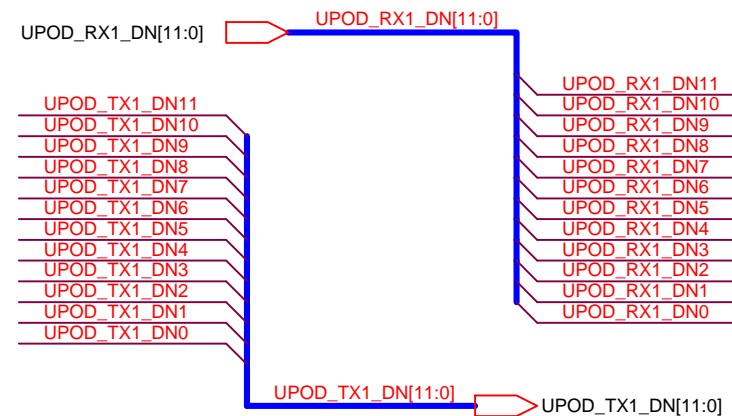
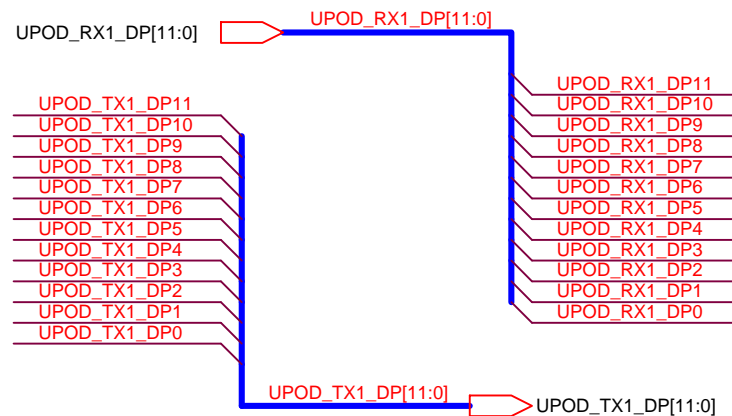
XC7K480T-2FFG1156C

CLK125はスワップ不可
0~3のチャンネル単位で
スワップ可能
PとNもスワップ可能



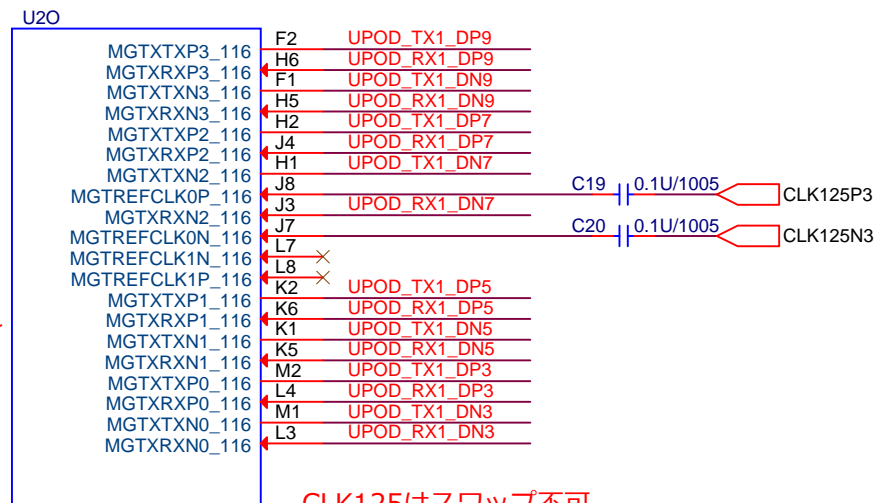
XC7K480T-2FFG1156C

0~3のチャンネル単位で
スワップ可能
PとNもスワップ可能



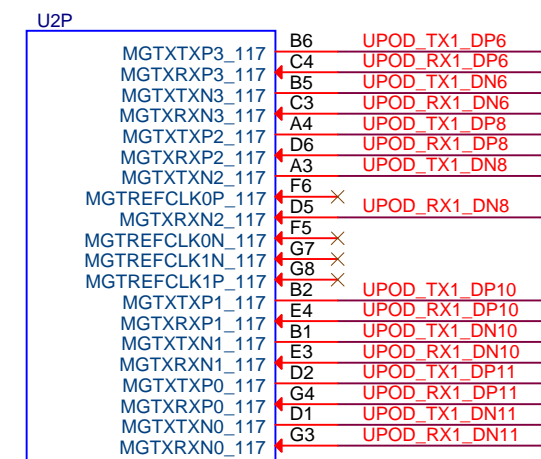
XC7K480T-2FFG1156C

0~3のチャンネル単位で
スワップ可能
PとNもスワップ可能



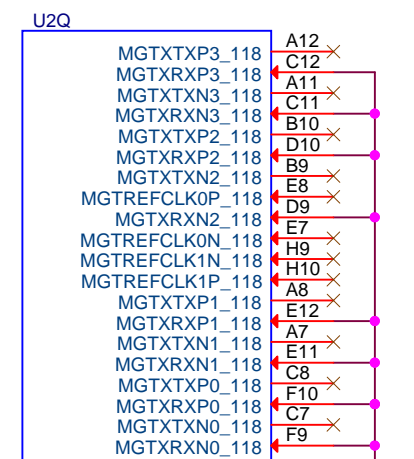
XC7K480T-2FFG1156C

CLK125はスワップ不可
0~3のチャンネル単位で
スワップ可能
PとNもスワップ可能



XC7K480T-2FFG1156C

0~3のチャンネル単位で
スワップ可能
PとNもスワップ可能

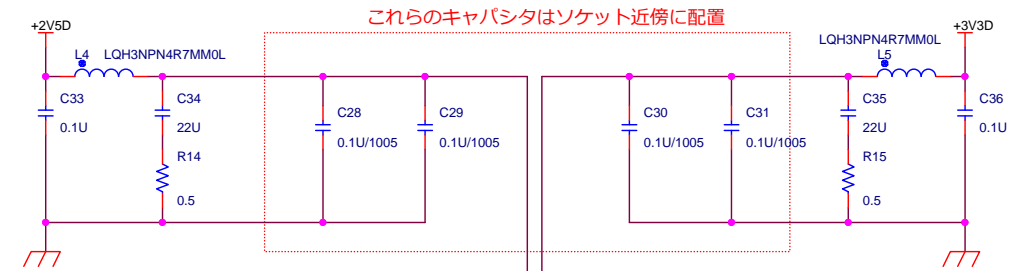
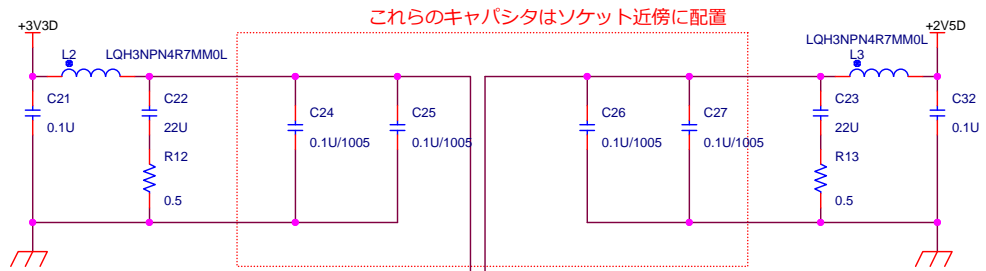


XC7K480T-2FFG1156C

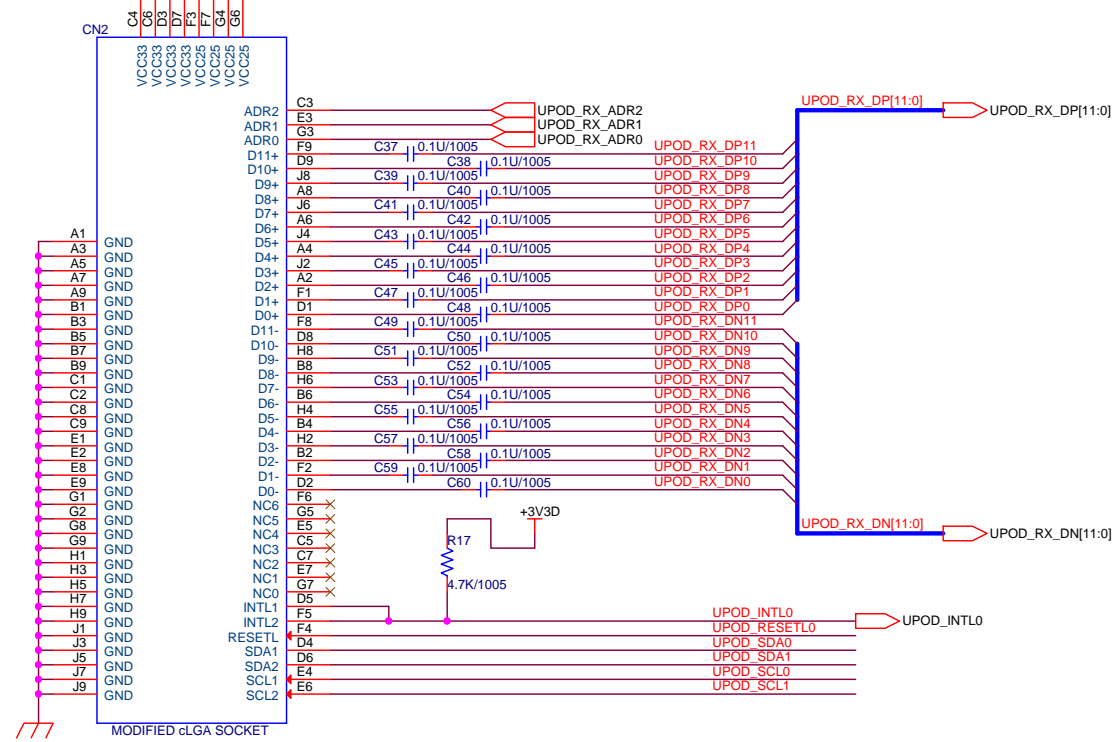
各ピンから抵抗のそれぞれのピンまで互いに等長

全て差動100Ω配線です

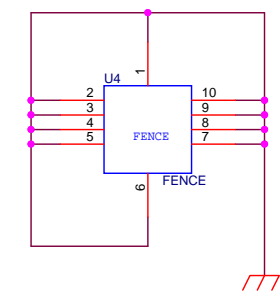
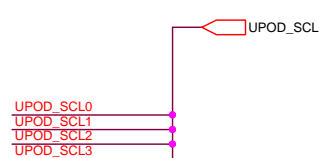
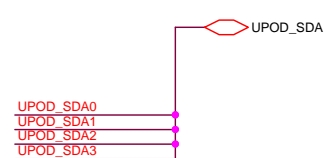
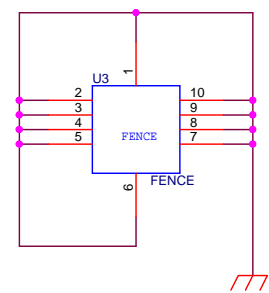
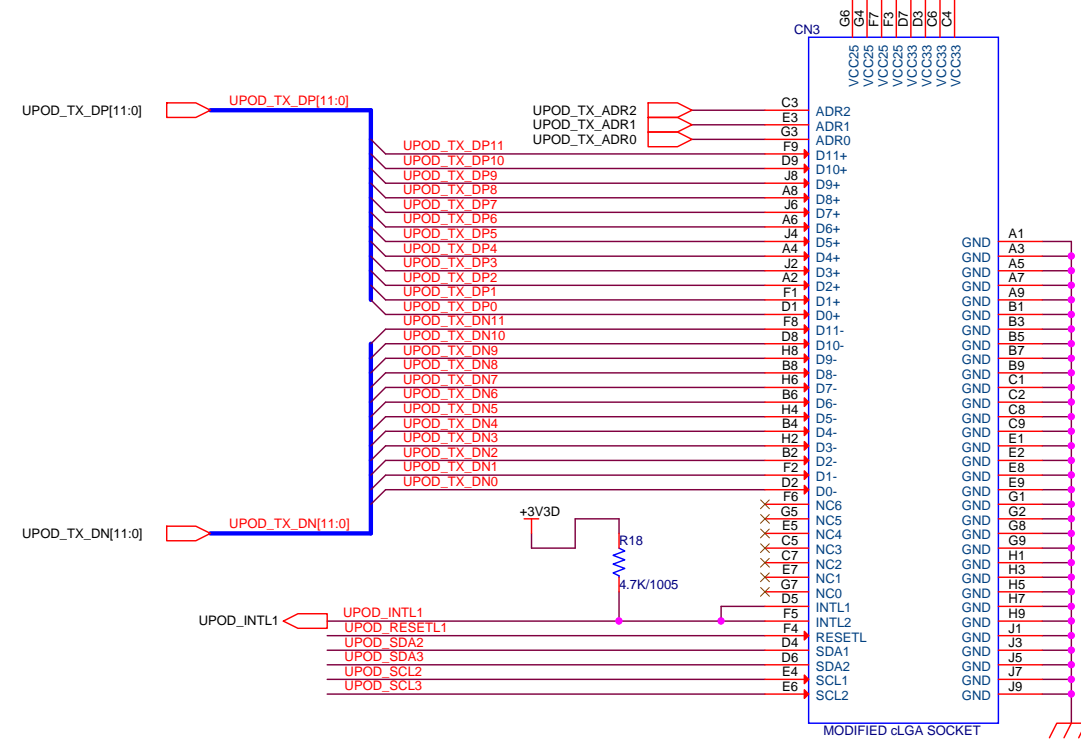
Title		
FPGA_GTX		
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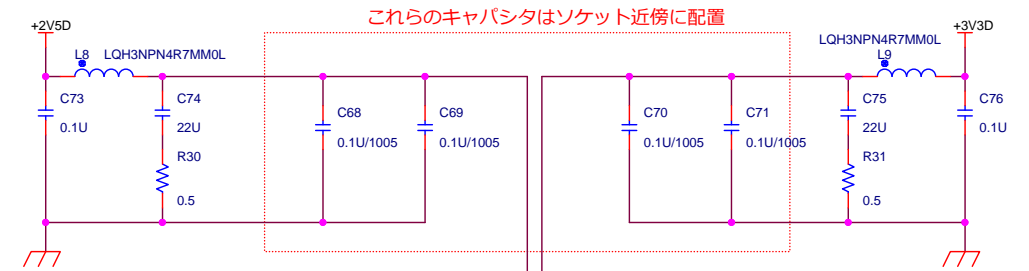
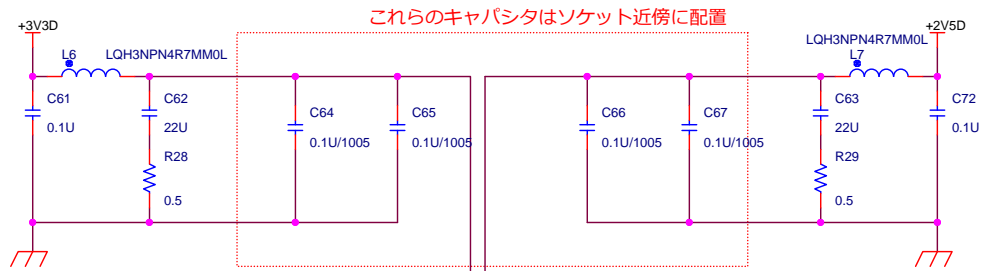
MicroPOD Receiver



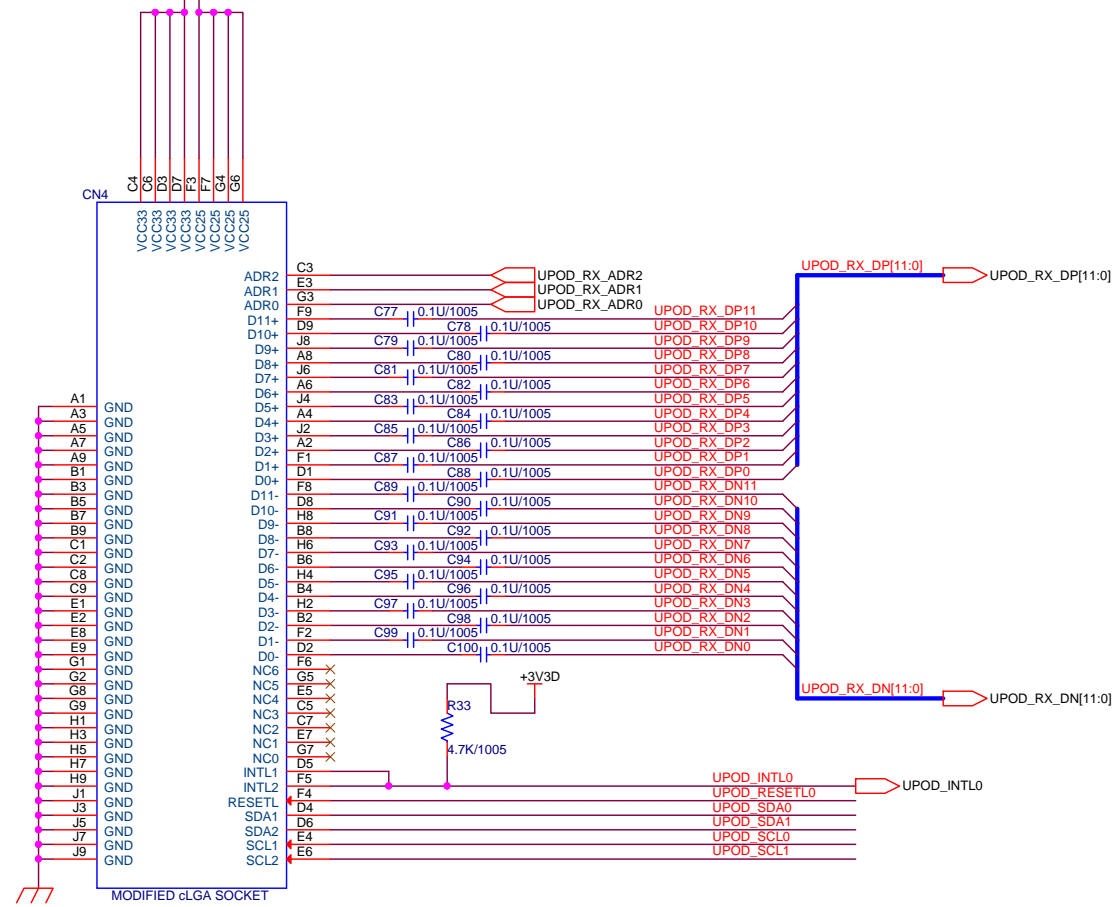
MicroPOD Transmitter



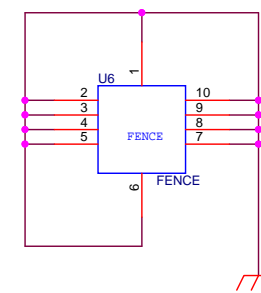
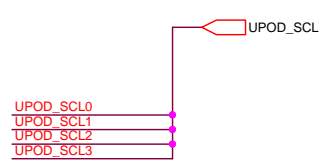
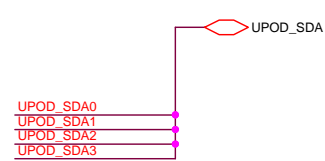
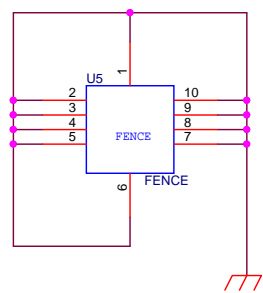
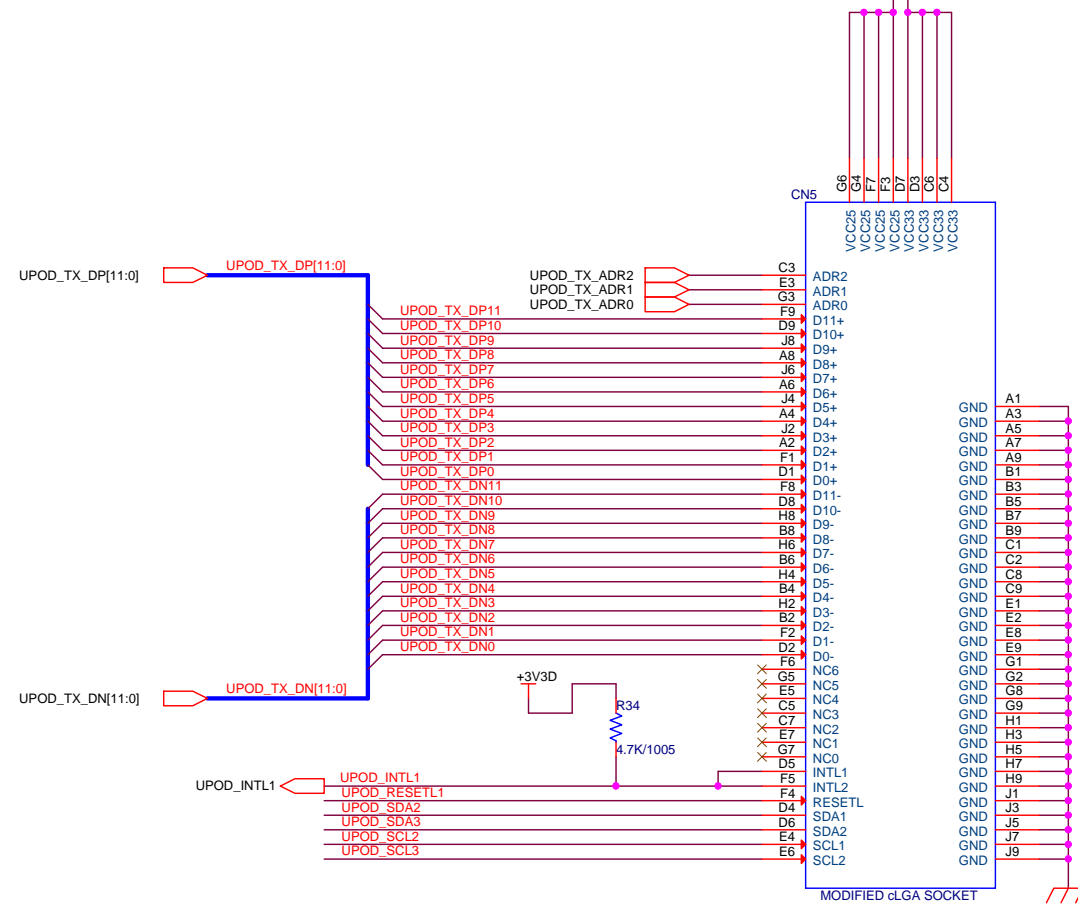
Title		
MicroPOD1		
Size	Document Number	Rev
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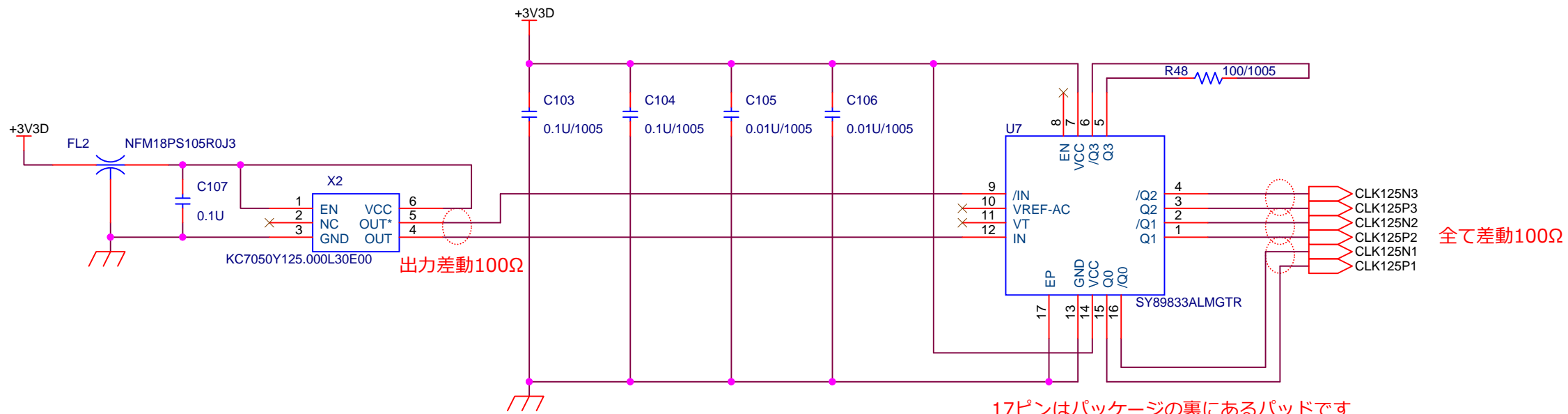
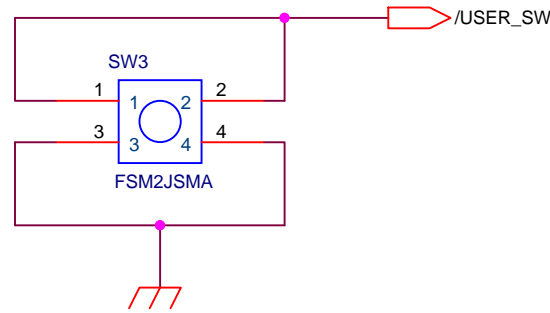
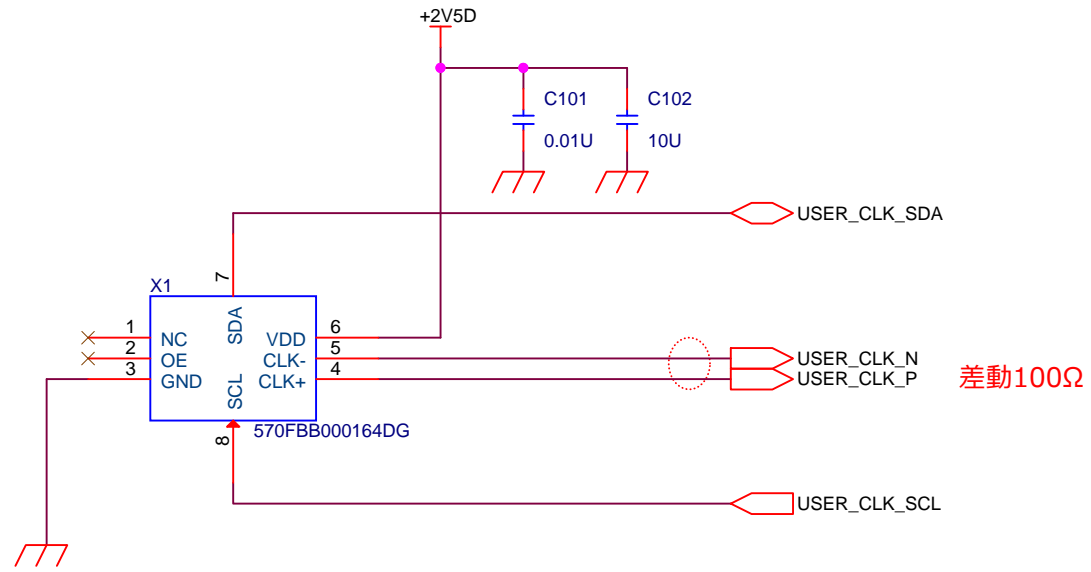
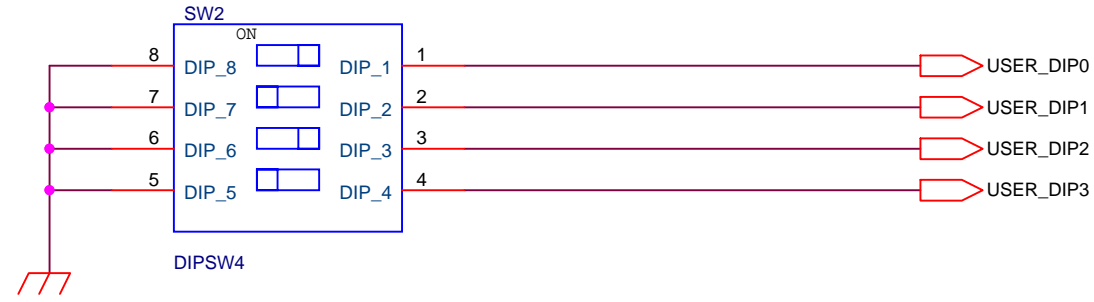
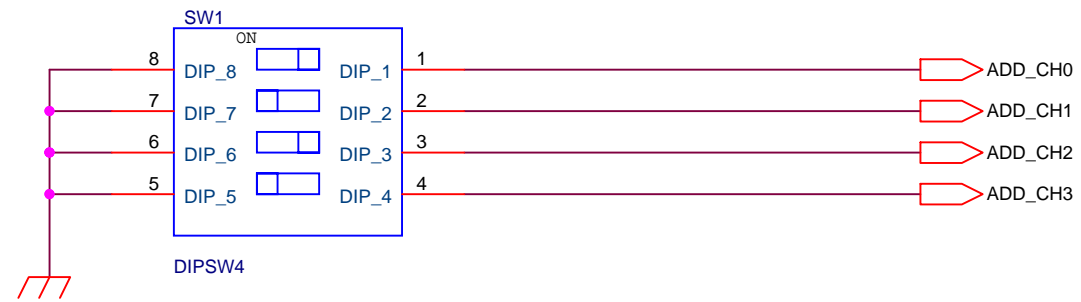
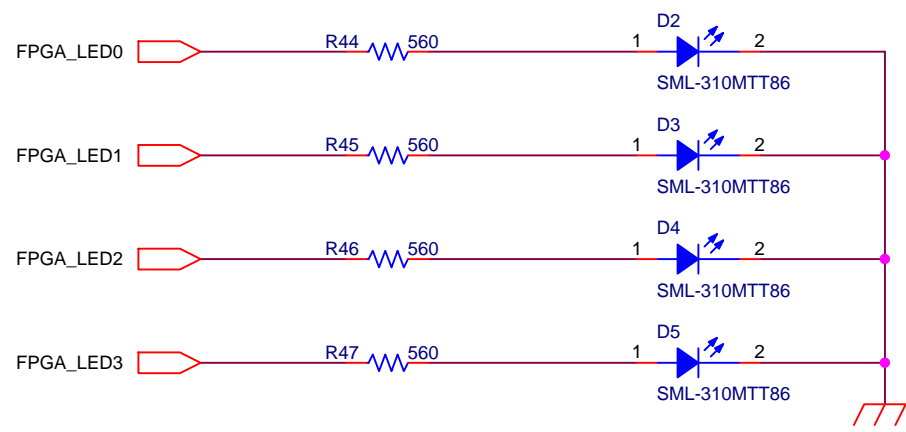
MicroPOD Receiver



MicroPOD Transmitter

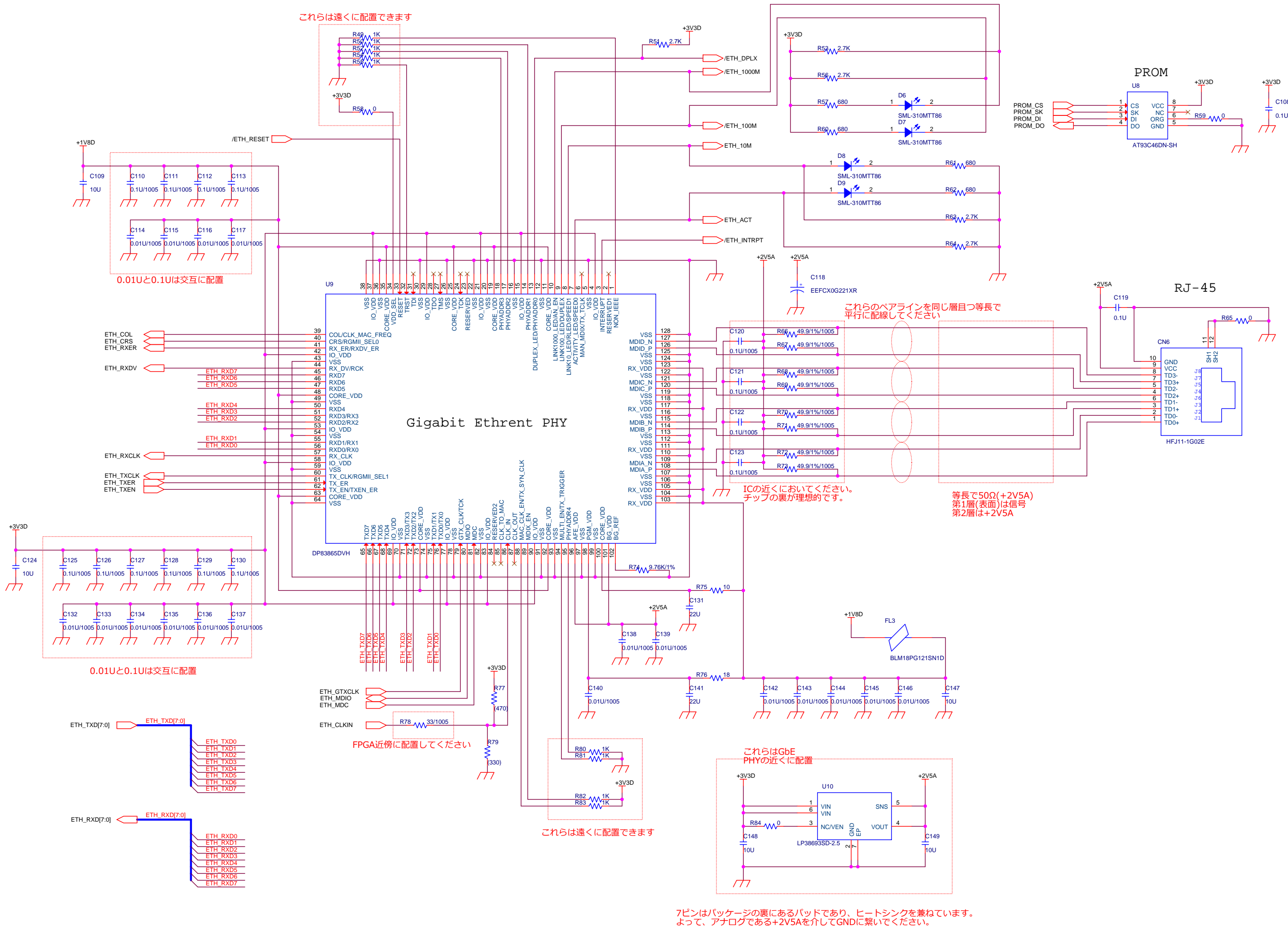


Title		
MicroPOD1		
Size	Document Number	Rev
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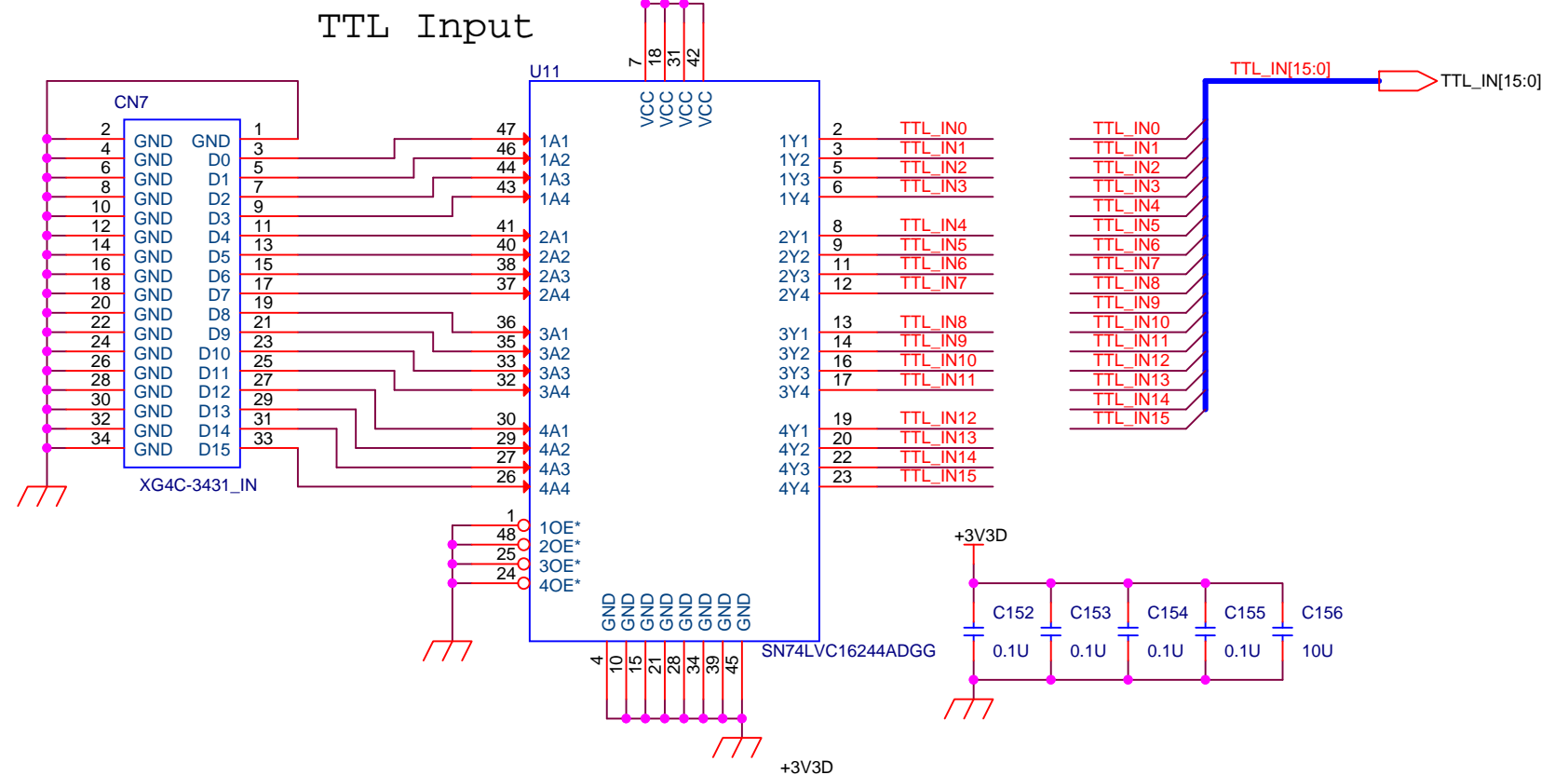
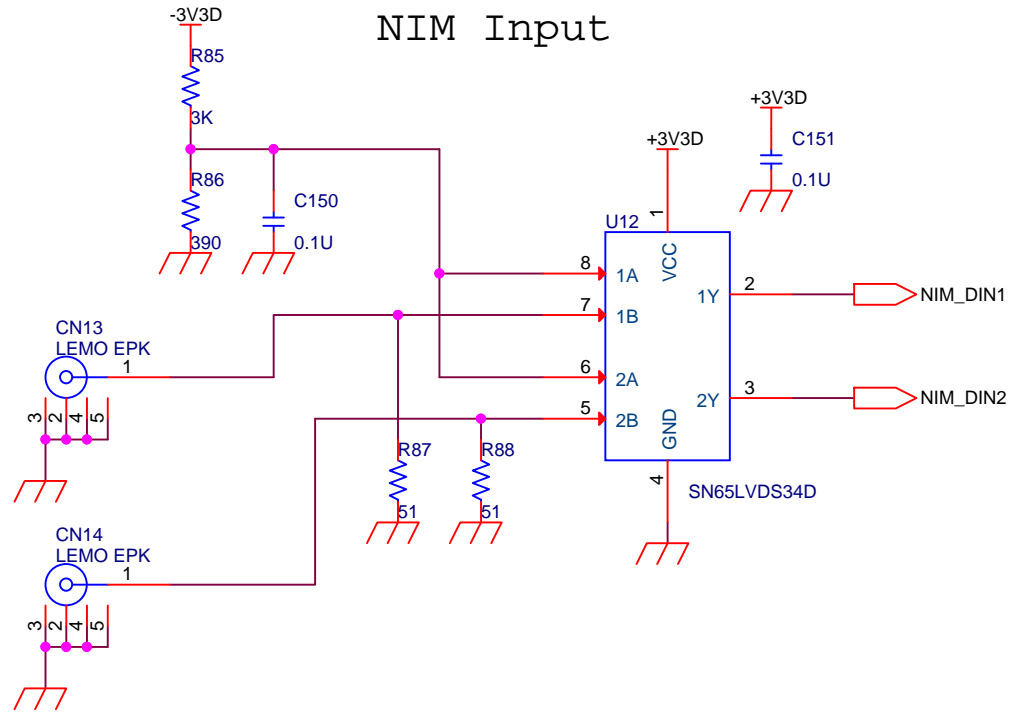
17ピンはパッケージの裏にあるパッドです

Title		
Clock and Switch		
Size B	Document Number <Doc>	Rev <Rev Code>
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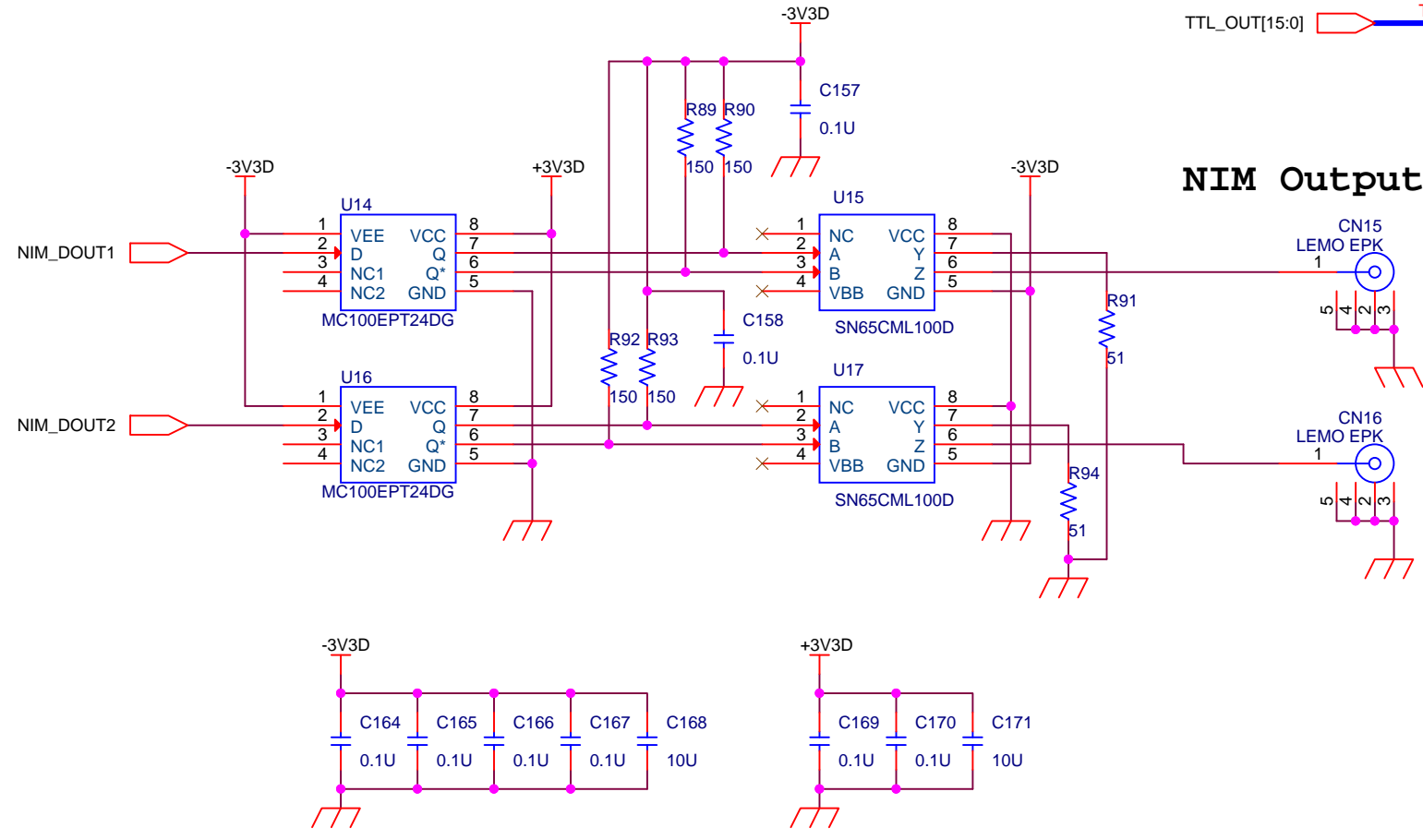
7ピンはパッケージの裏にあるパッドであり、ヒートシンクを兼ねています。よって、アナログである+2V5Aを介してGNDに繋いでください。

Title			Gigabit Ethernet
Size	Document Number	Rev	
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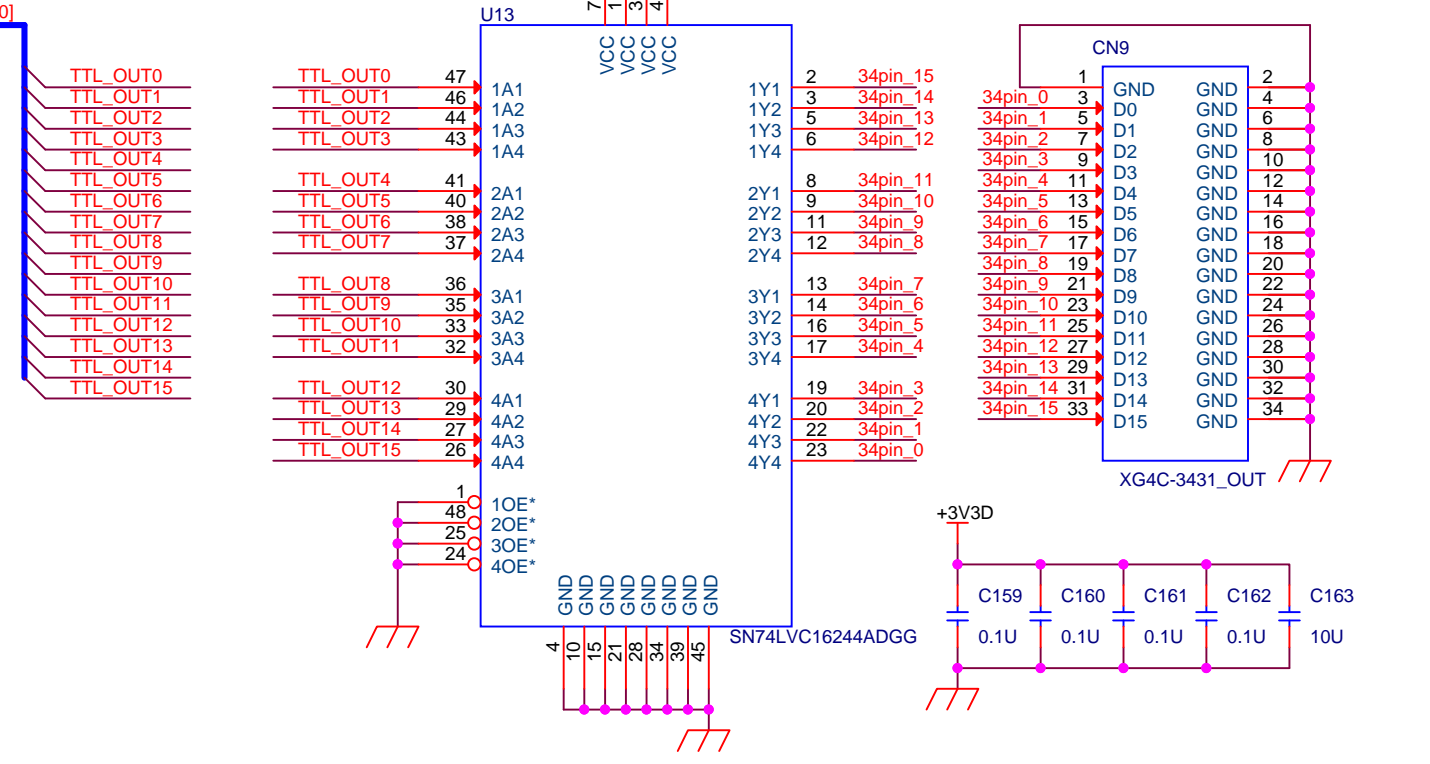


NIM Input

NIM Output

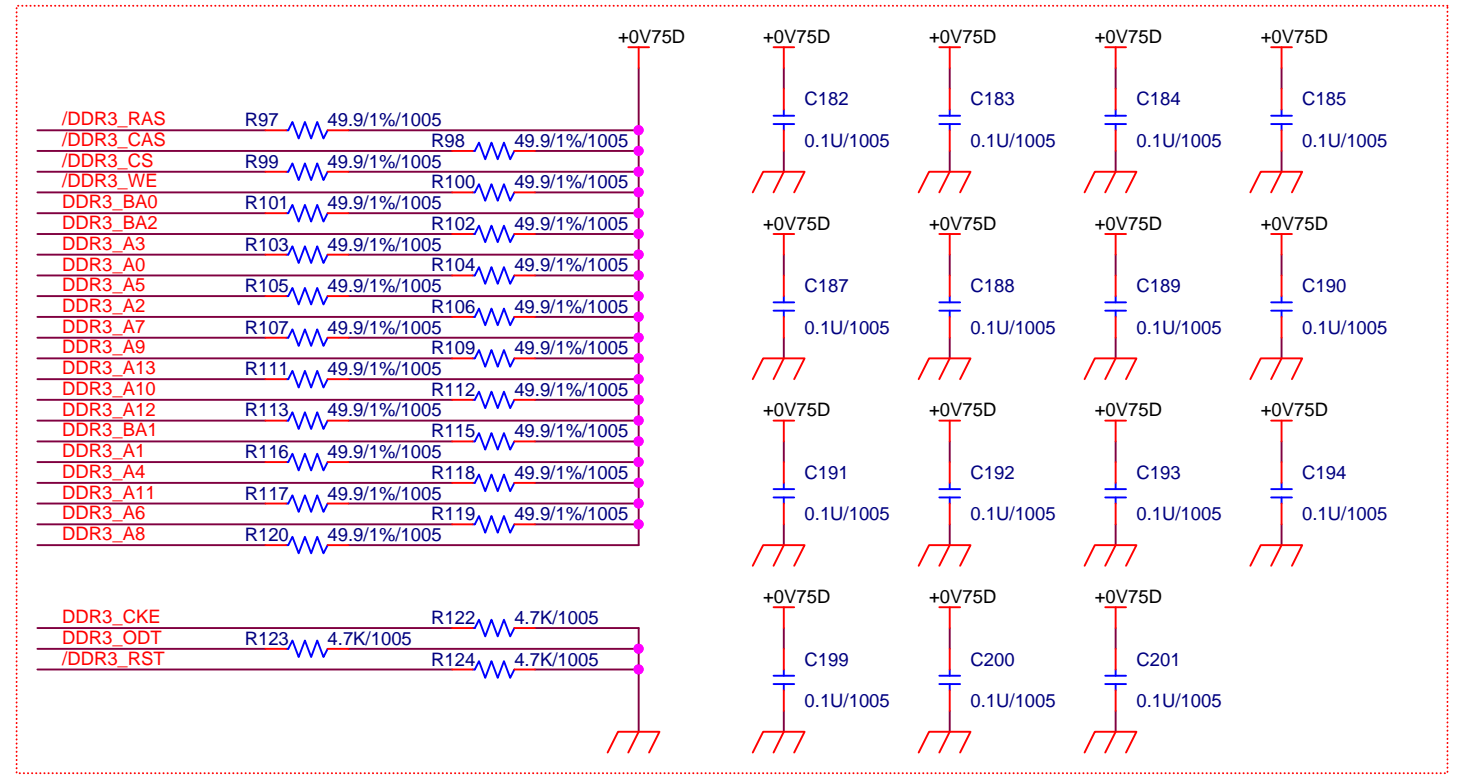
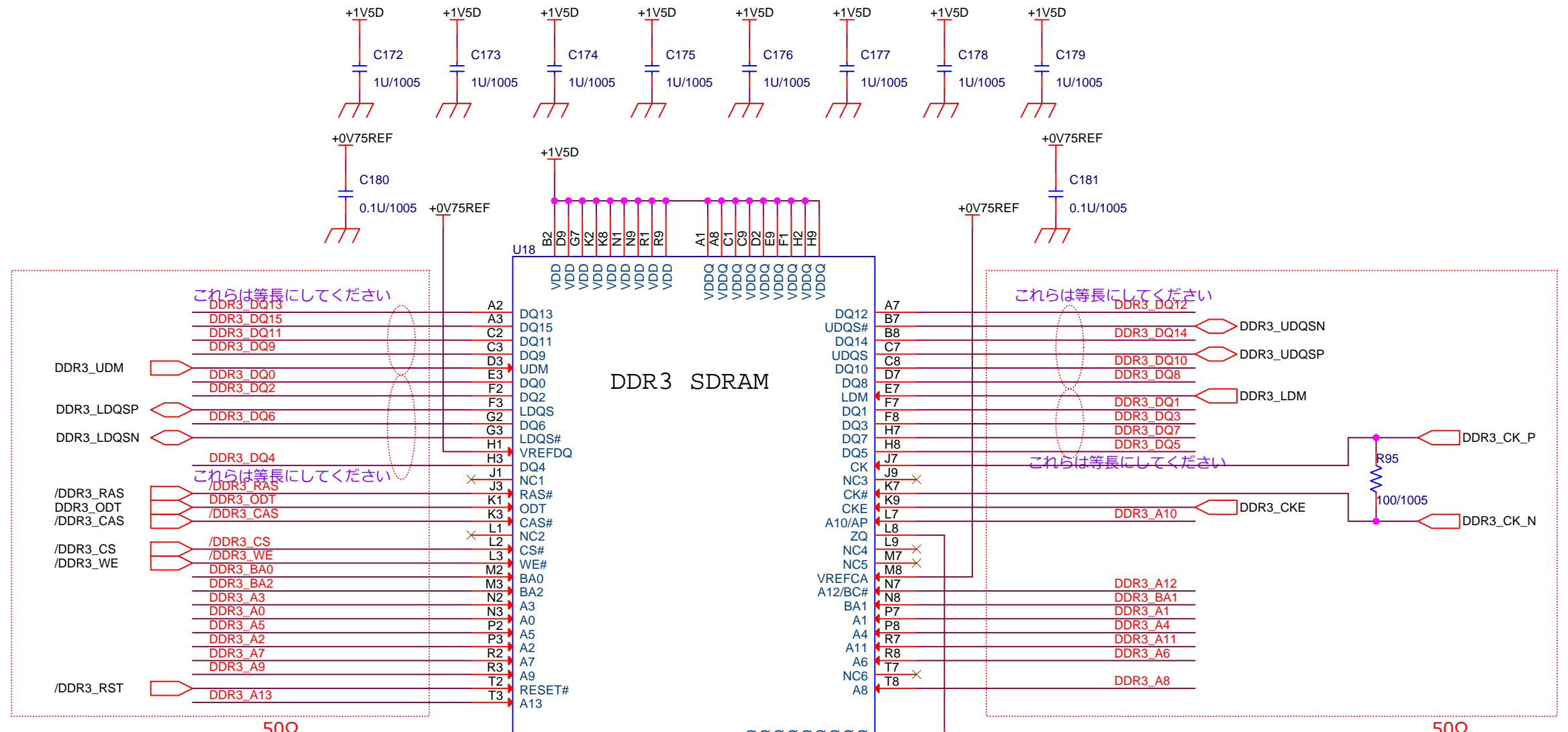
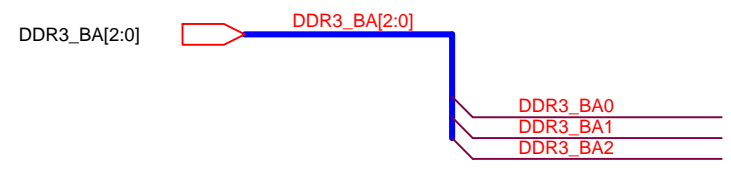
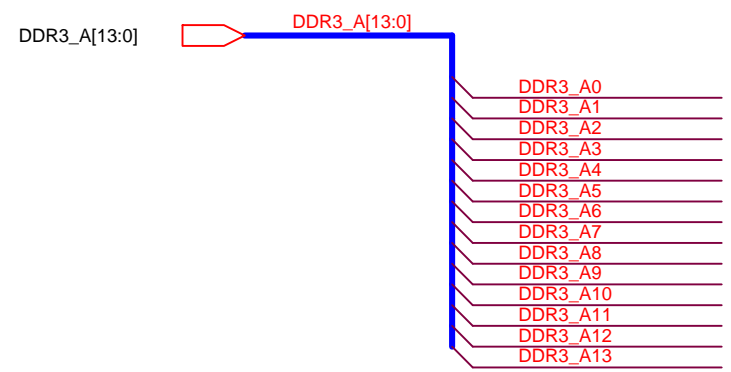
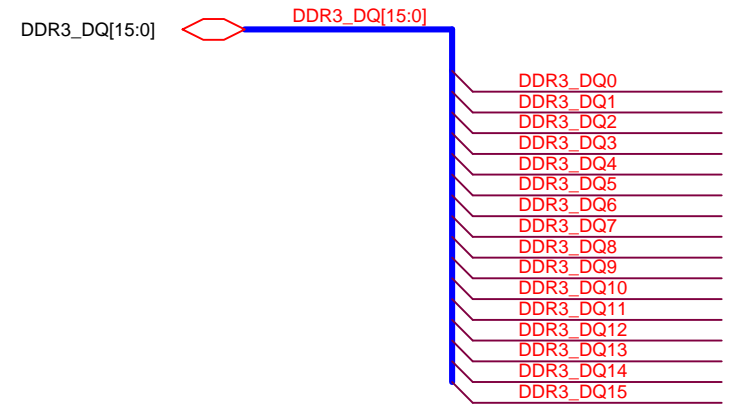


TTL Output

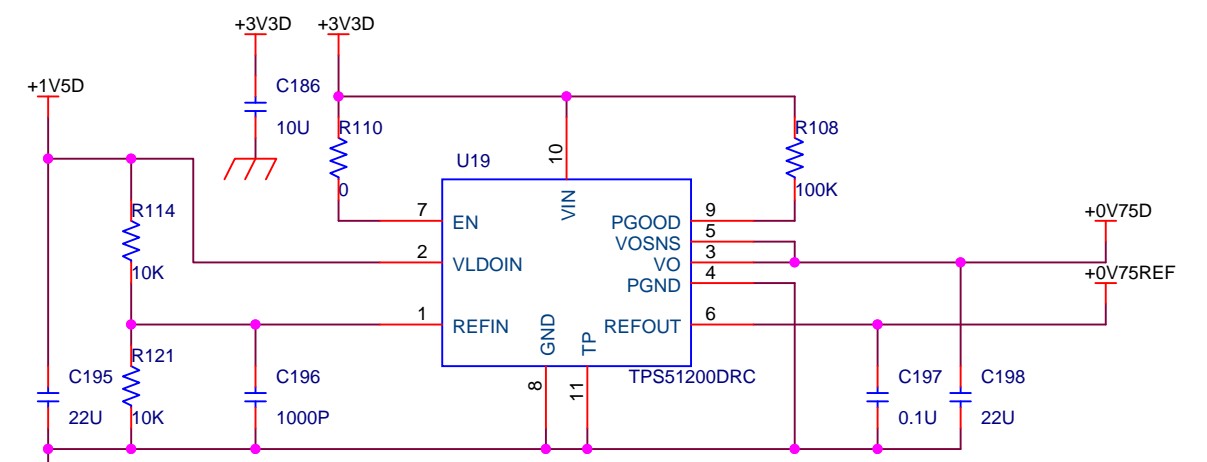


NIM Output

Title		
NIM and TTL		
Size	Document Number	Rev
B	<Doc>	<RevCode>
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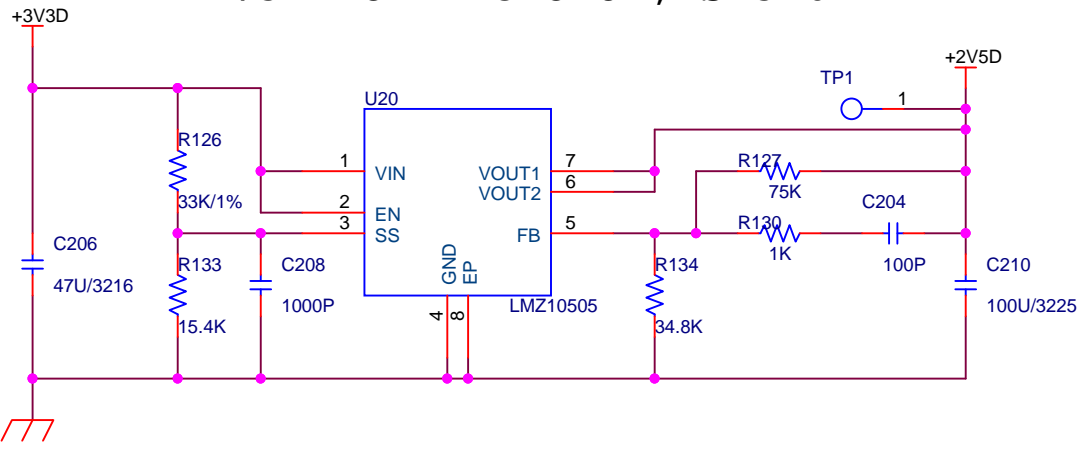


FPGAとDDR3の延長線上に配置してください

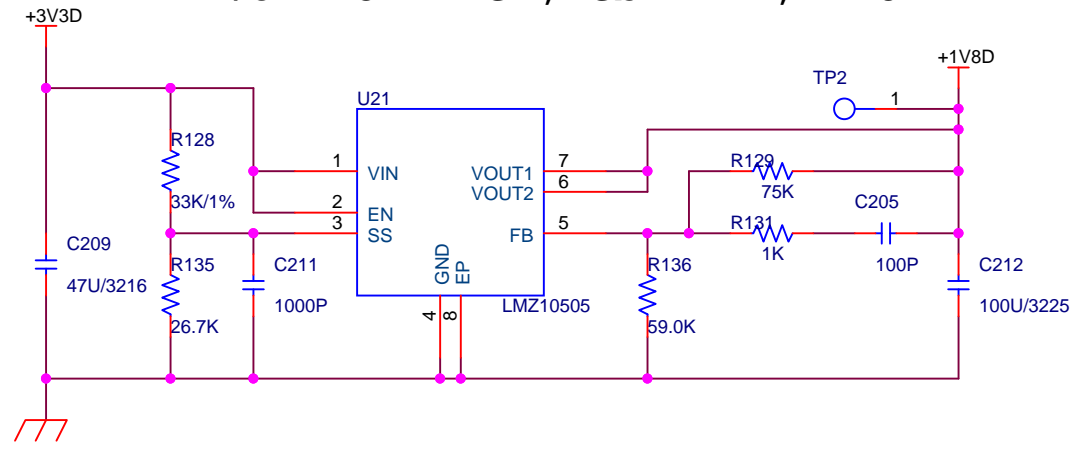


Title		
DDR3		
Size	Document Number	Rev
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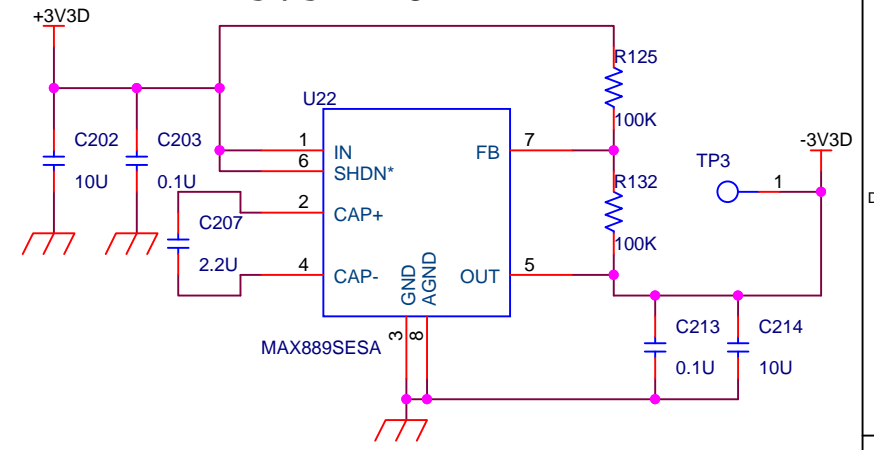
+2V5D for MicroPOD, Si570



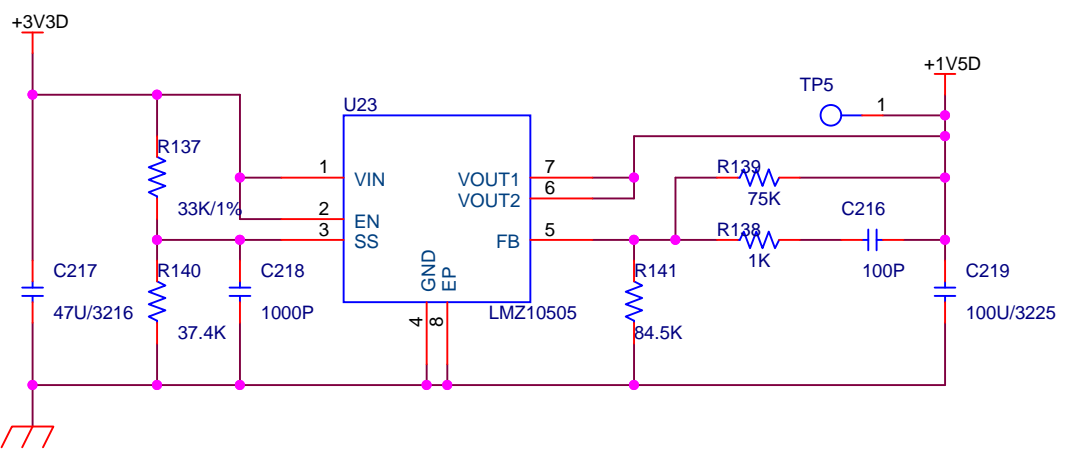
+1V8D for FPGA, GbE PHY, PROM



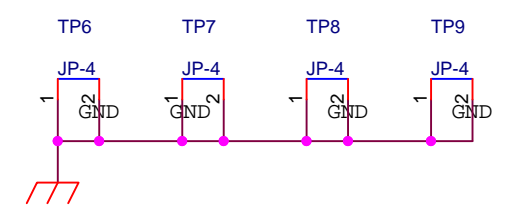
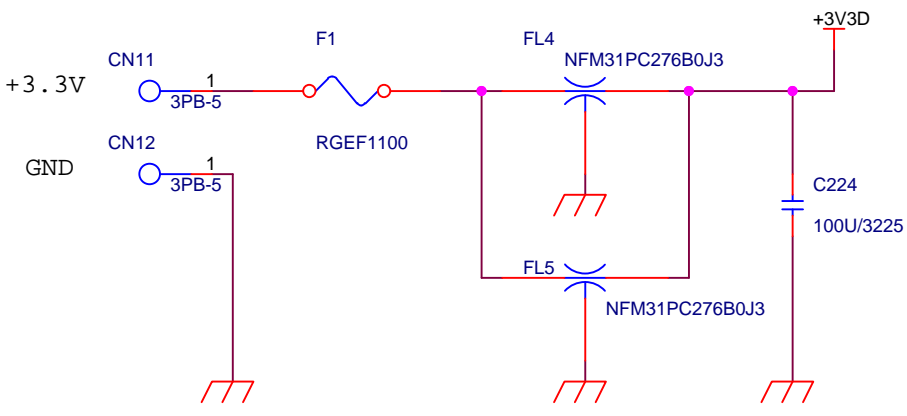
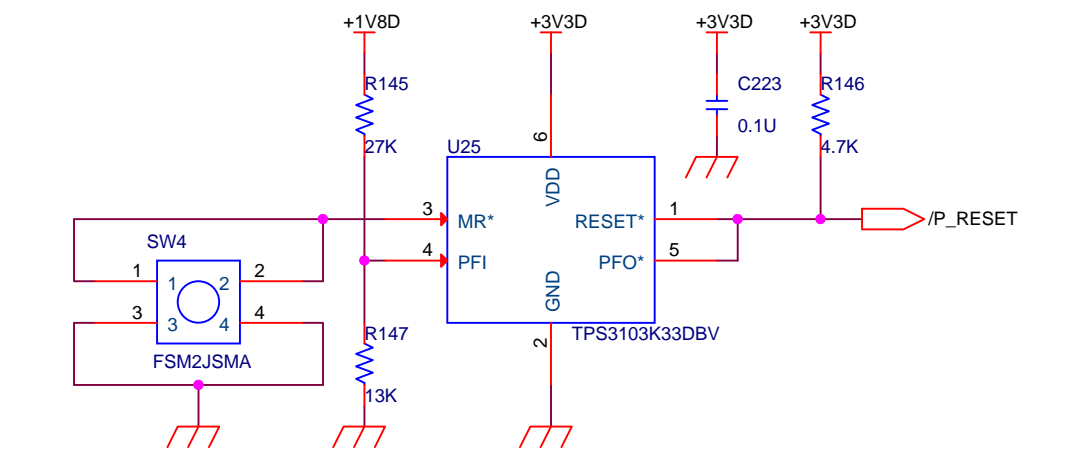
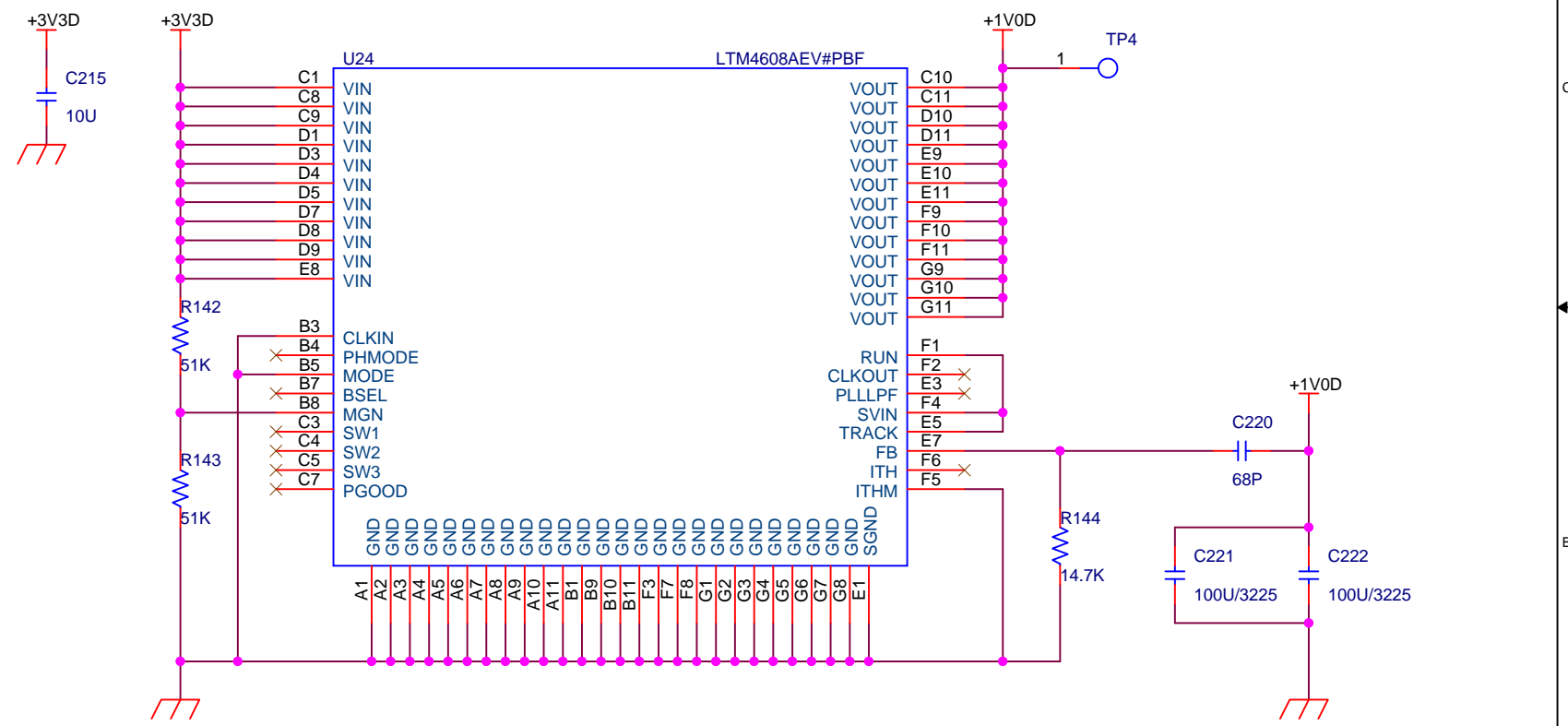
-3V3D for NIM



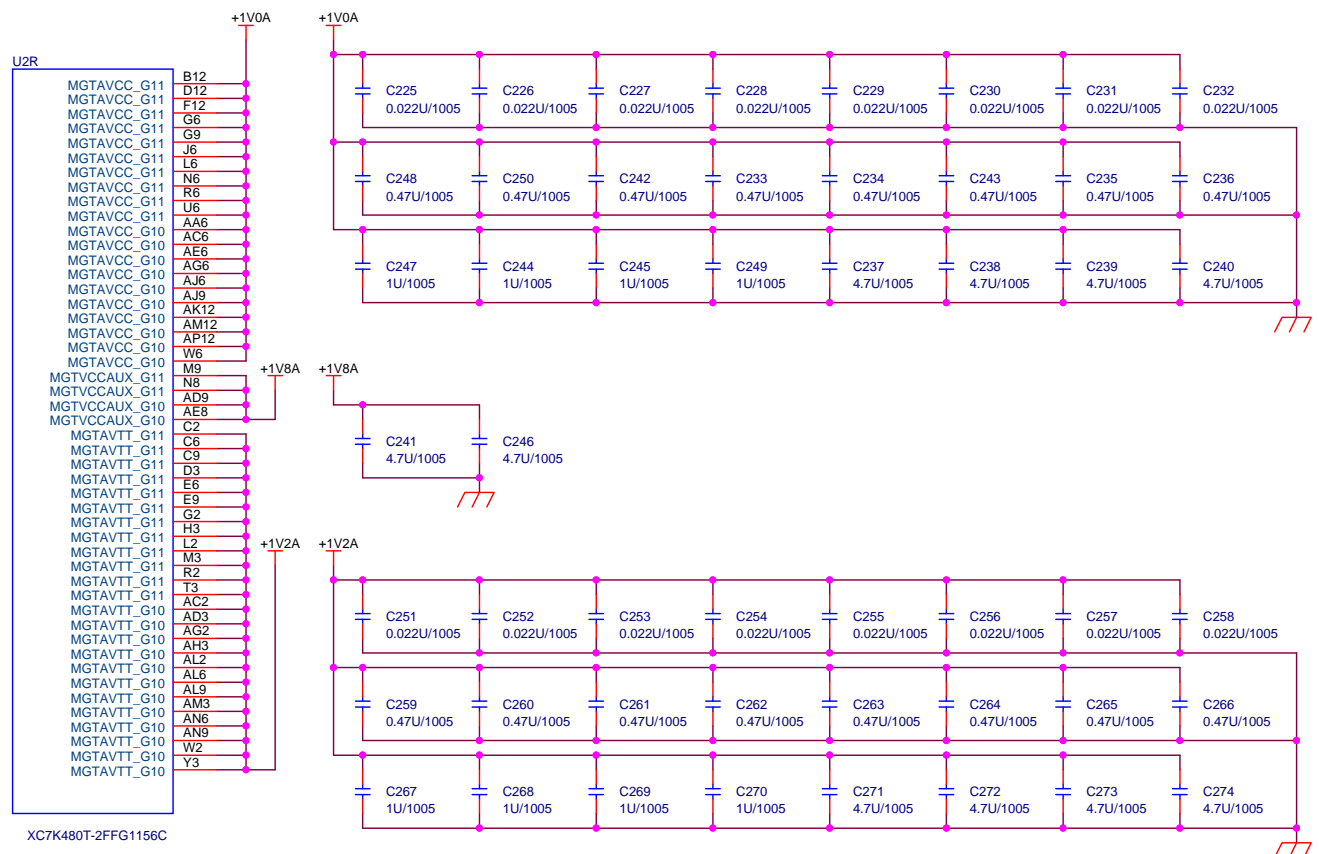
+1V5D for DDR3



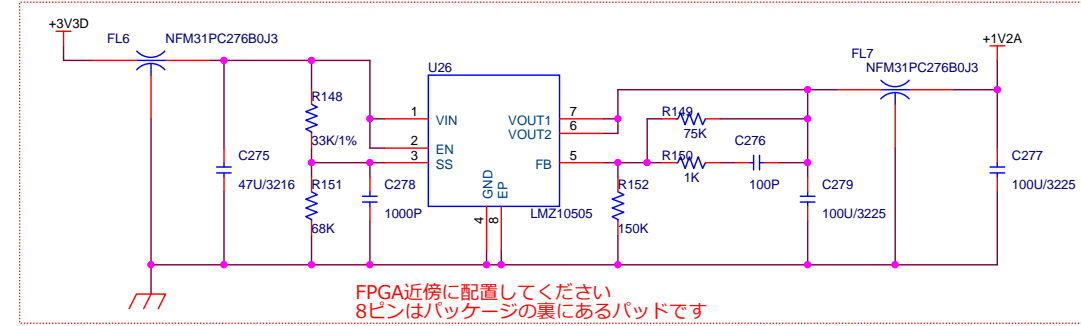
+1V0D for FPGA



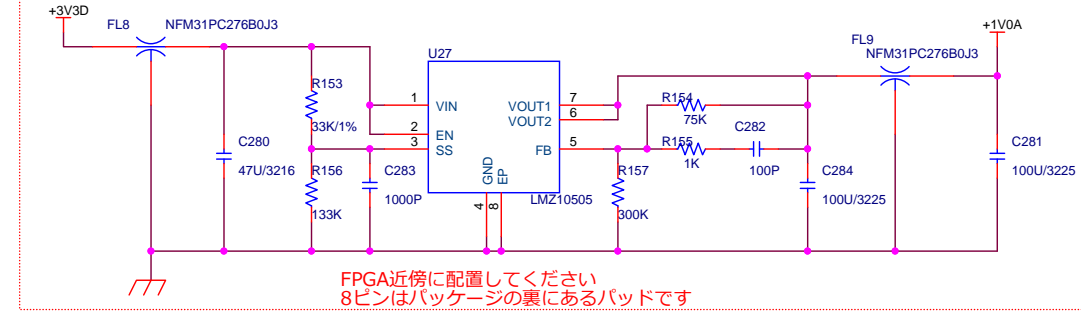
Title		
POWER		
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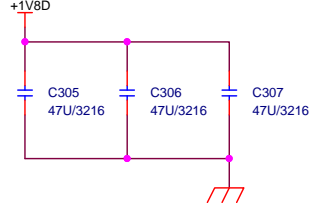
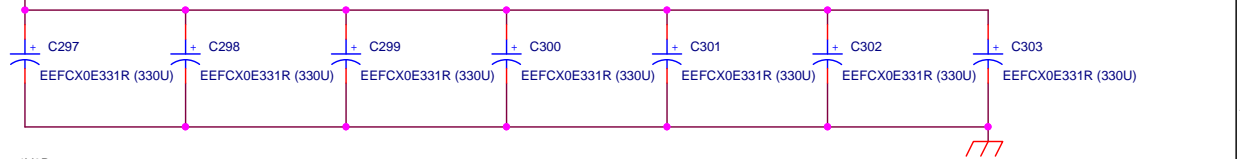
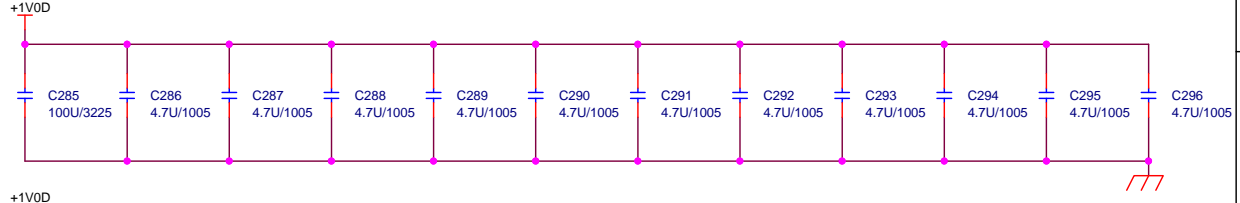
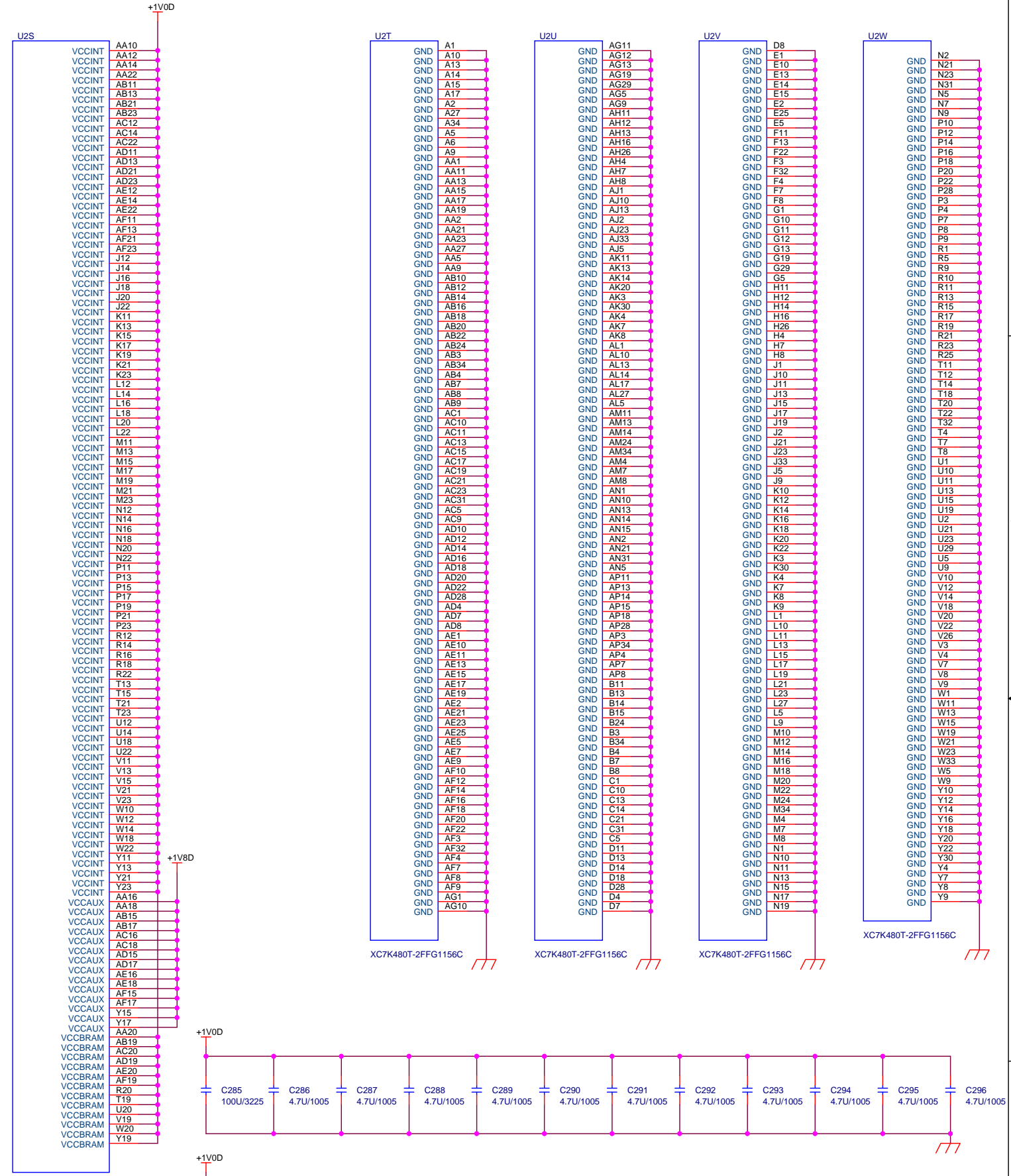
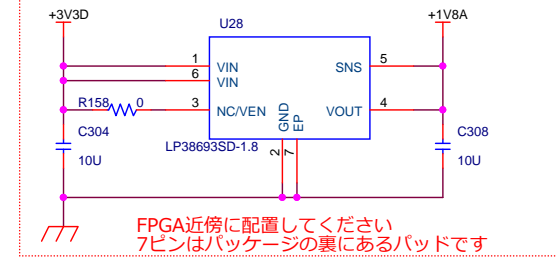
+1V2A for FPGA (U1N, U1R)



+1V0A for FPGA (U1R)



+1V8A for FPGA (U1R)



Title			FPGA_POWER
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