PP ASIC

Overview and Prototype Test Results

Shuichi Ito and the TGC Electronics Group

Final Design Review

6 Dec. 2018

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  - PLL and variable delay
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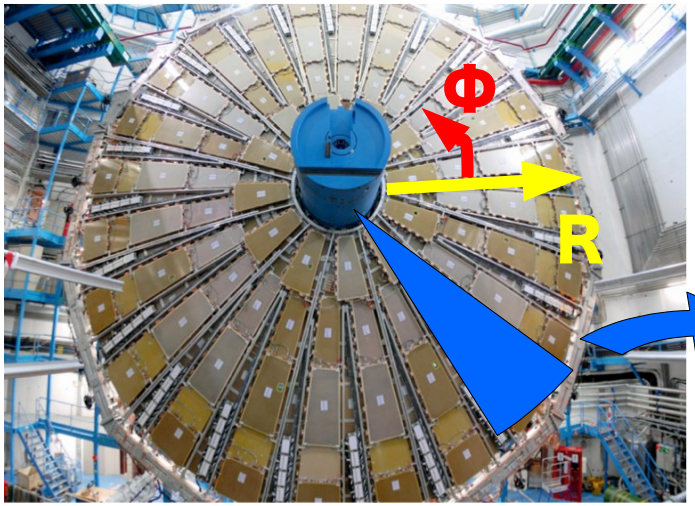
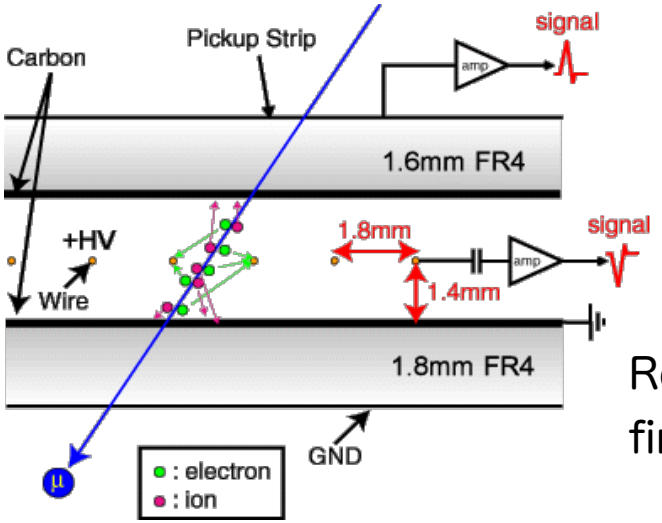
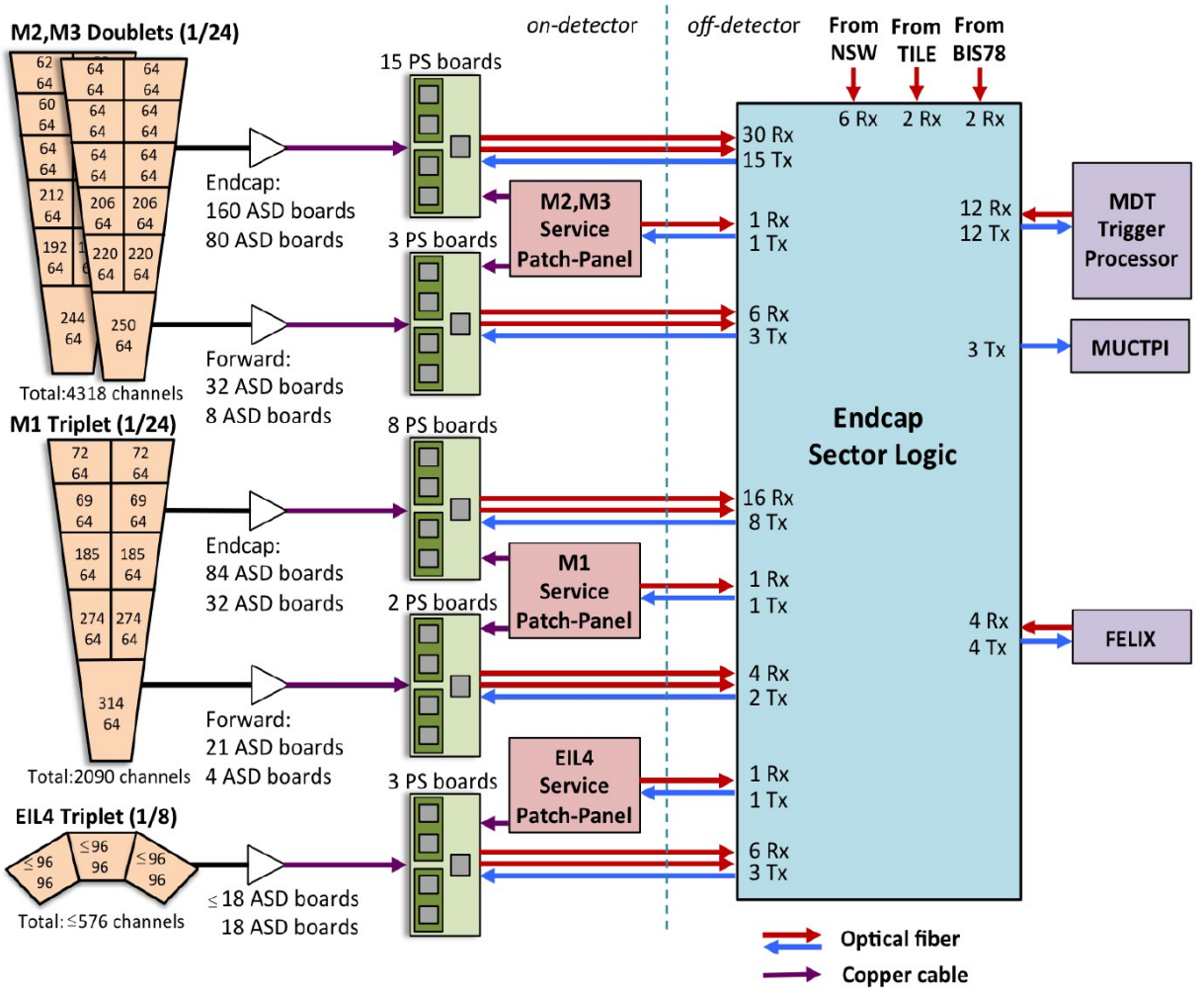
Phase II TGC Trigger and Readout System

Thin Gap Chamber (TGC)



Two-dimensional measurements by the wires and the strips



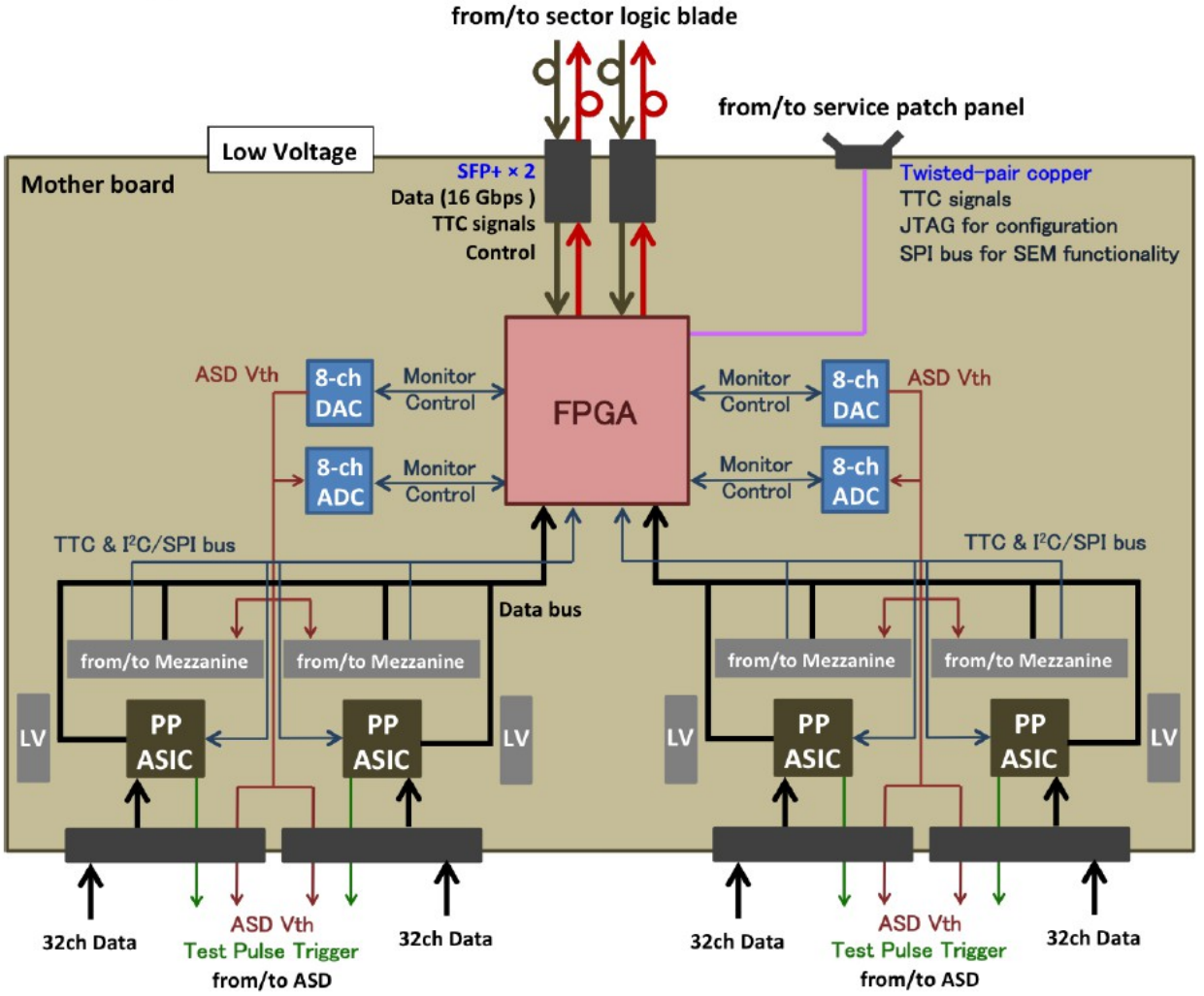


Replace all boards except for ASDs for an extension of the first-level trigger rate (1 MHz) and latency (10 μs).

All hit signals will be transferred to the off-detector boards.

Phase II TGC PS Board Overview

Phase II TGC PS board contains PP ASICs, FPGAs, etc.

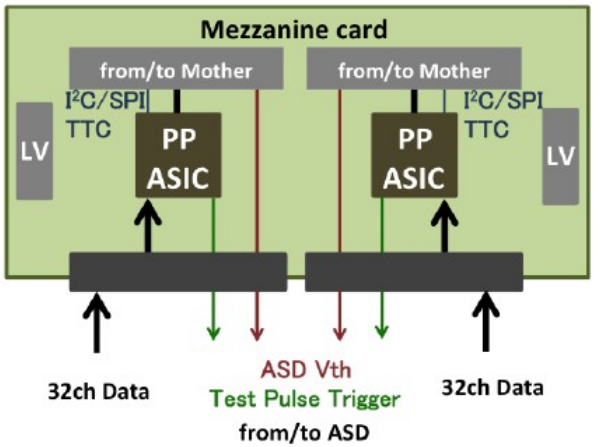


PP ASIC

- Receive LVDS signals from ASDs, and align the timing.
  Send the aligned signals to FPGA.
- Send test pulse to ASDs.

FPGA

- Collect signals from PP ASICs and transfer to off-detector (8 Gbps × 2 = 16 Gbps)
- Control threshold voltage of the discriminators of ASDs.



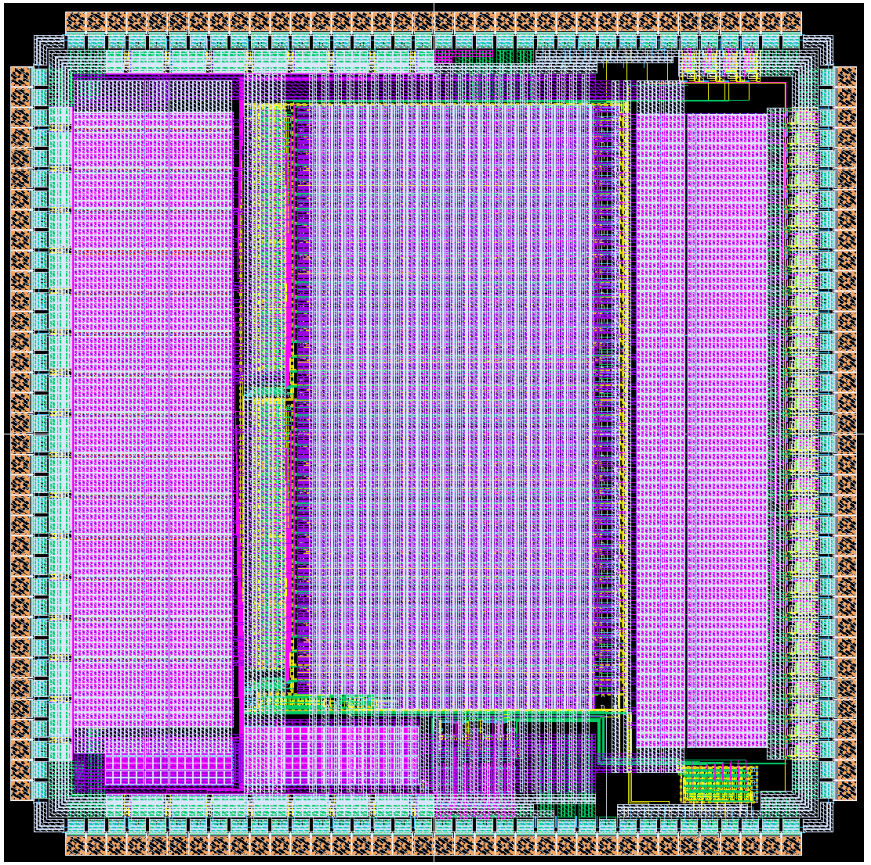
Phase II TGC PP ASIC Timeline

Preliminary Design Review (PDR) was held on 6 Mar. 2018.

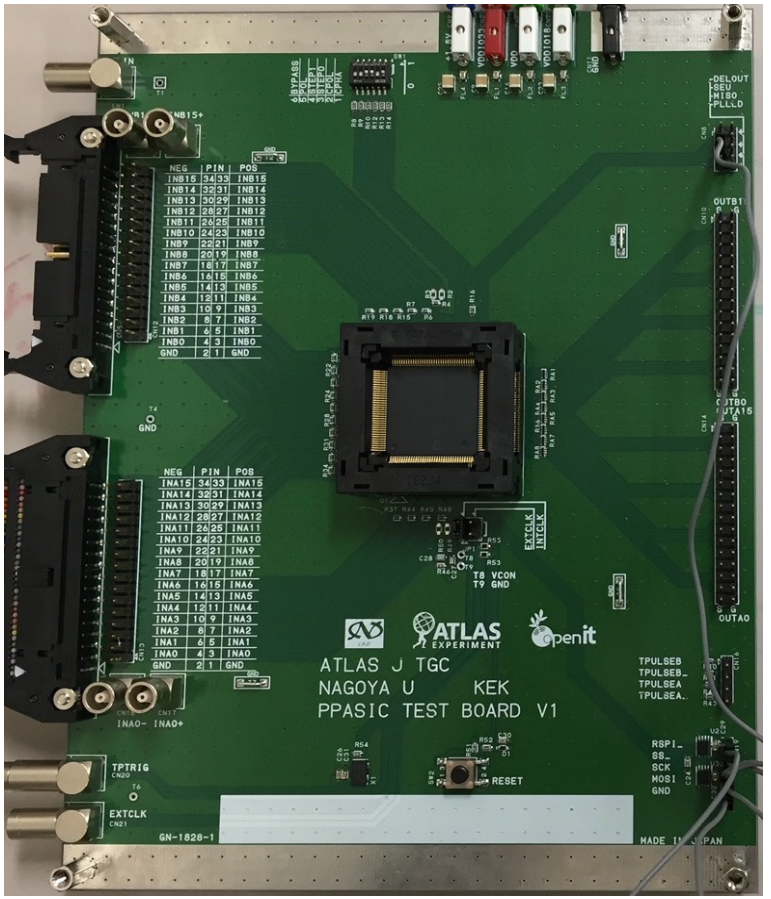
The tapeout of the prototype finished in Jun. 2018.

Twenty packaged chips were delivered on 3 Oct. 2018.

Prototype layout



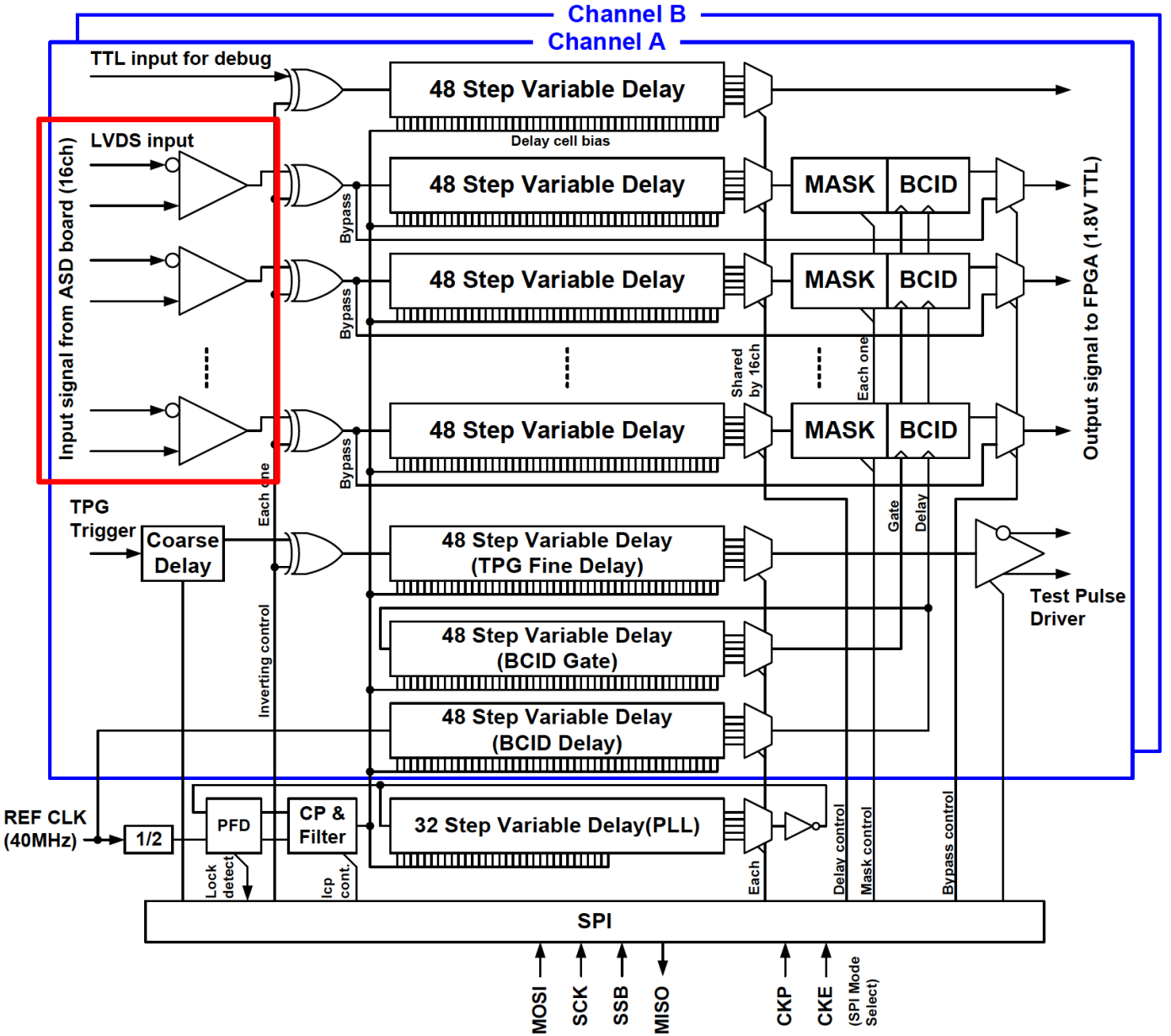
Test board with the PP ASIC prototype



Target Specification

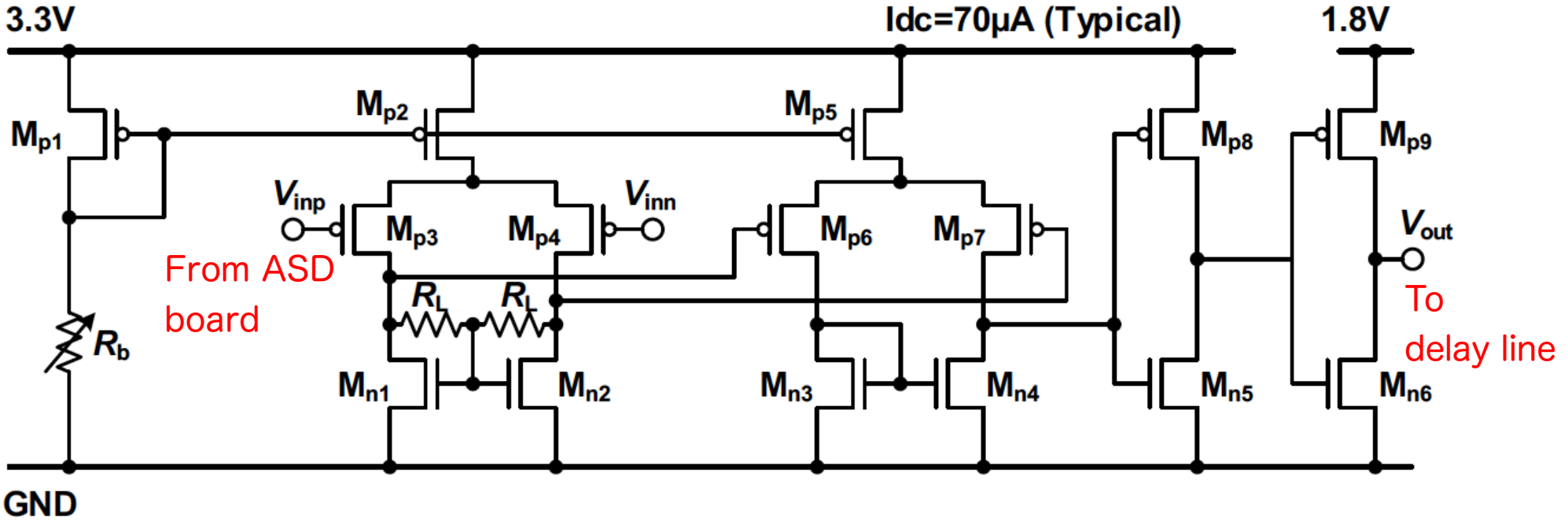
Design process	Silterra 0.18 μm CMOS 6M1P
Supply voltage	3.3 V (LVDS Rx, TPG Driver) 1.8 V (PLL, Delay line, CMOS input and output) Voltage tolerance : ± 10 %
# of channels	Group A (16 ch), Group B (16 ch)
Timing control resolution	< 1 ns
Timing control range	> 40 ns
Timing jitter	< 0.1 ns (RMS)
Temperature range	10 ~ 70 ℃
Power consumption	130 mW (previous design) or less

LVDS Receiver



Schematic of LVDS Receiver

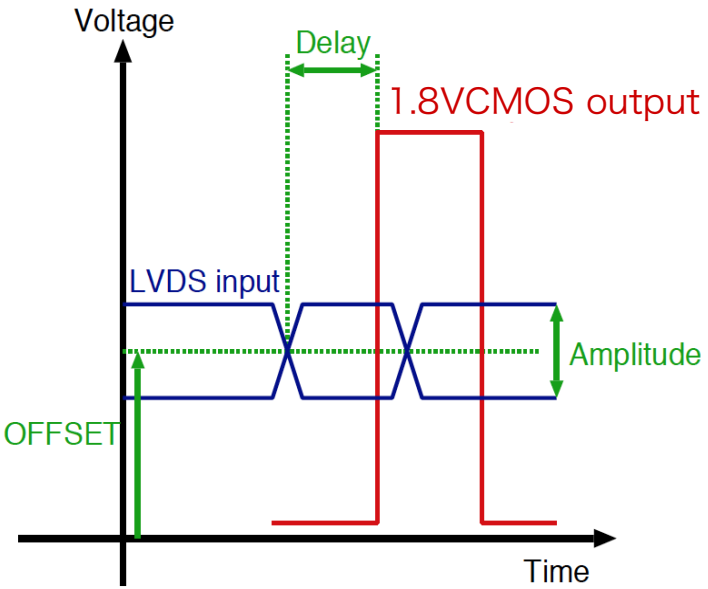
- LVDS Rx consists of two differential amplifiers and two stages of inverter.
- Level shifter is implemented in LVDS Rx. (3.3 V → 1.8 V)
- DC power consumption is 0.23 mW from 3.3 V.(70 μA × 3.3 V)
- LVDS Rx is not fully compatible with the LVDS Rx standard specificaition (IEEE 1596.3).

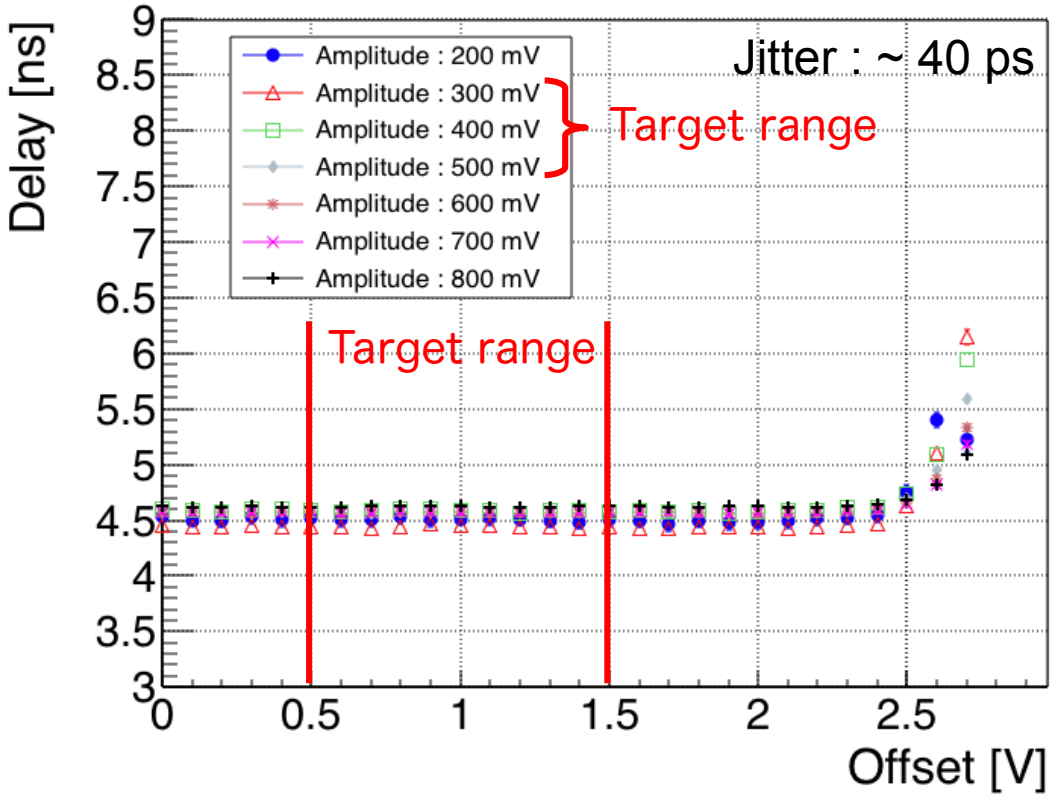


Delay Dependence on Offset and Amplitude

Delay of the LVDS reciever was measured depending on amplitude and offset.

Offset voltage is defined to be the central voltage of the input differential signals.





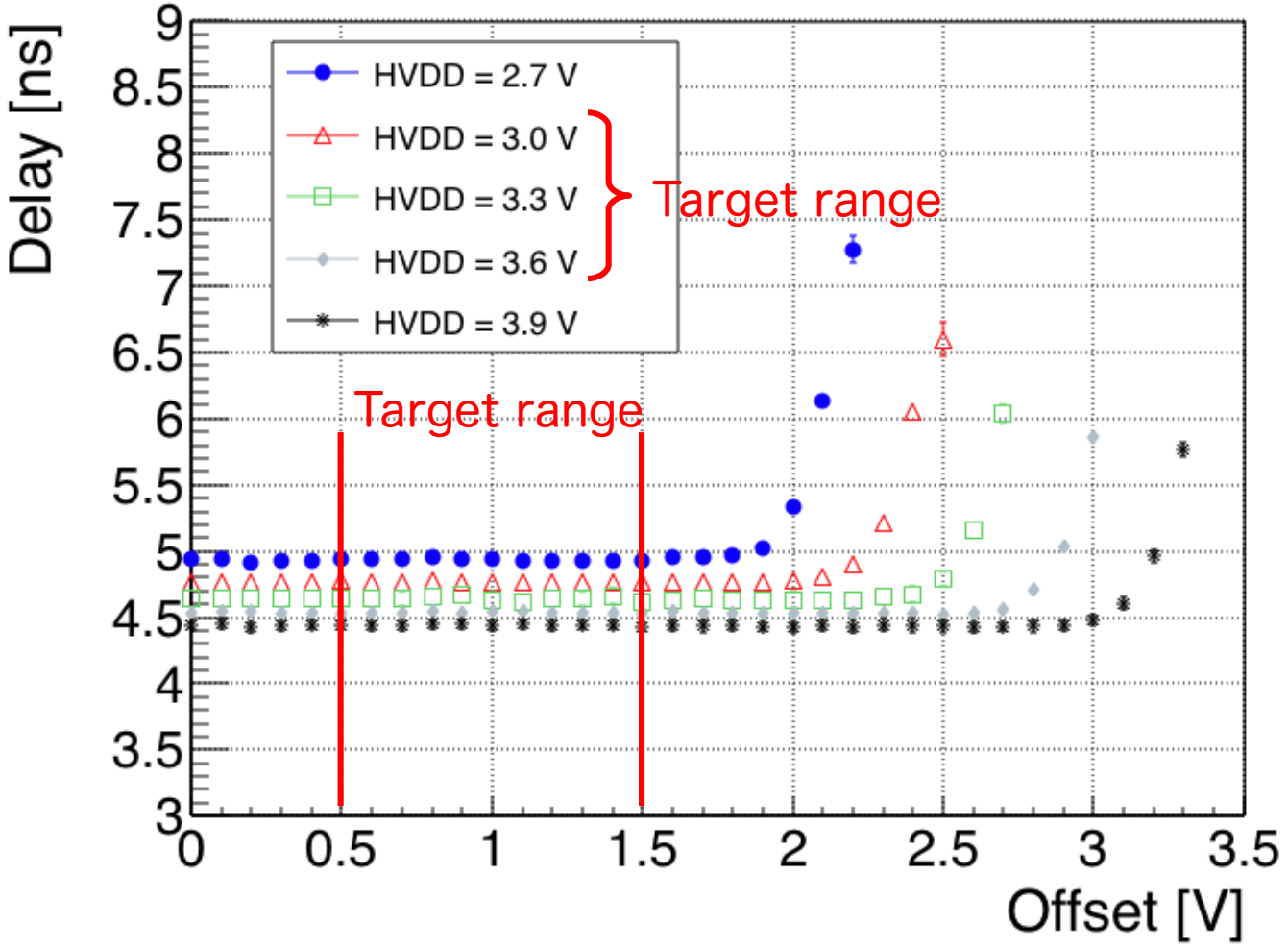
The measured delay is the sum of the propagation delay of the receiver, the multiplexer, and the output buffer.

The dalay is 4.6 ± 0.1 ns for target ranges of amplitude and offset.

satisfies the requirement of timing control resolution < 1 ns.

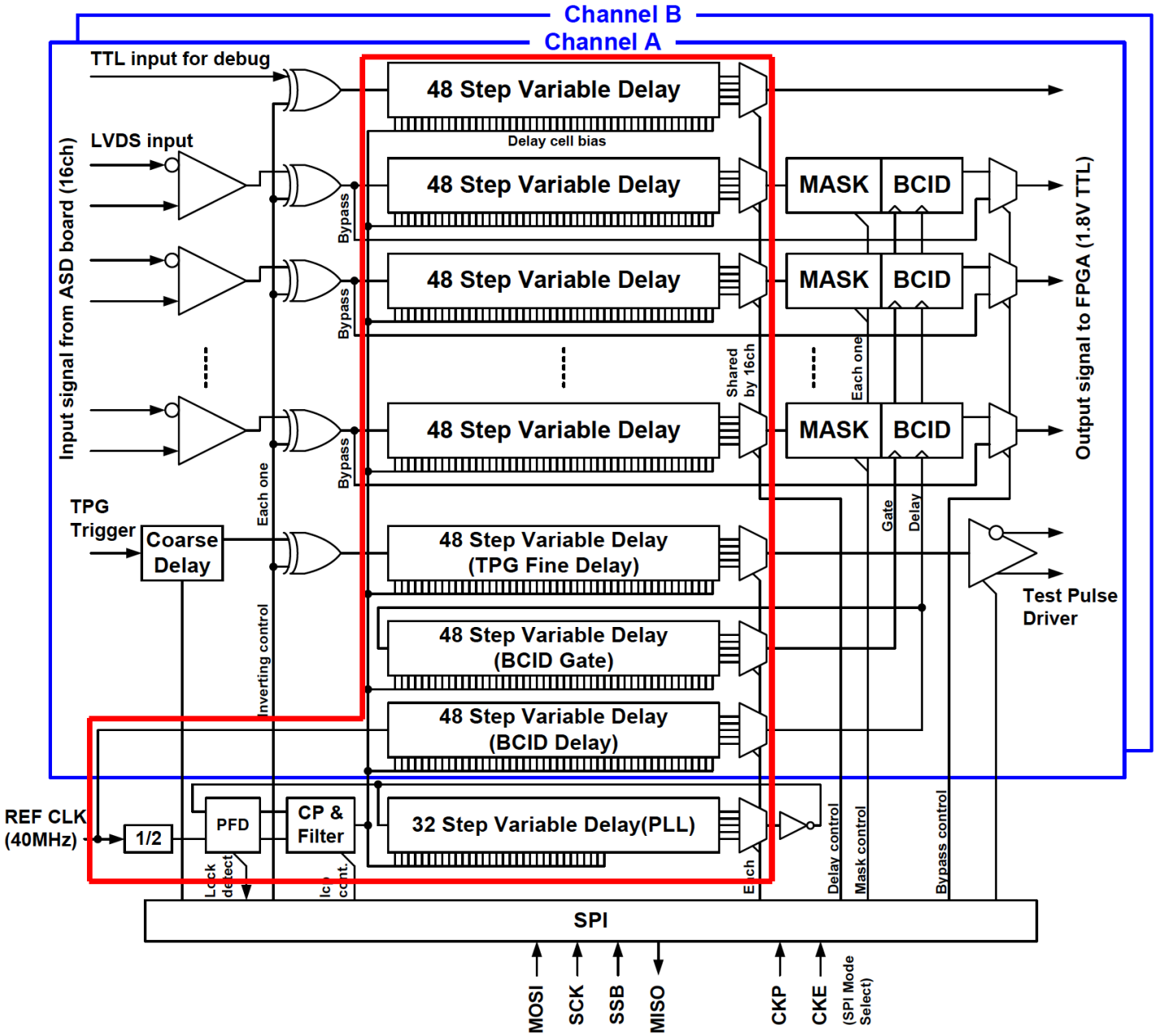
Delay Dependence on VDD and Offset

Delay of the LVDS receiver was measured depending on VDD and offset.



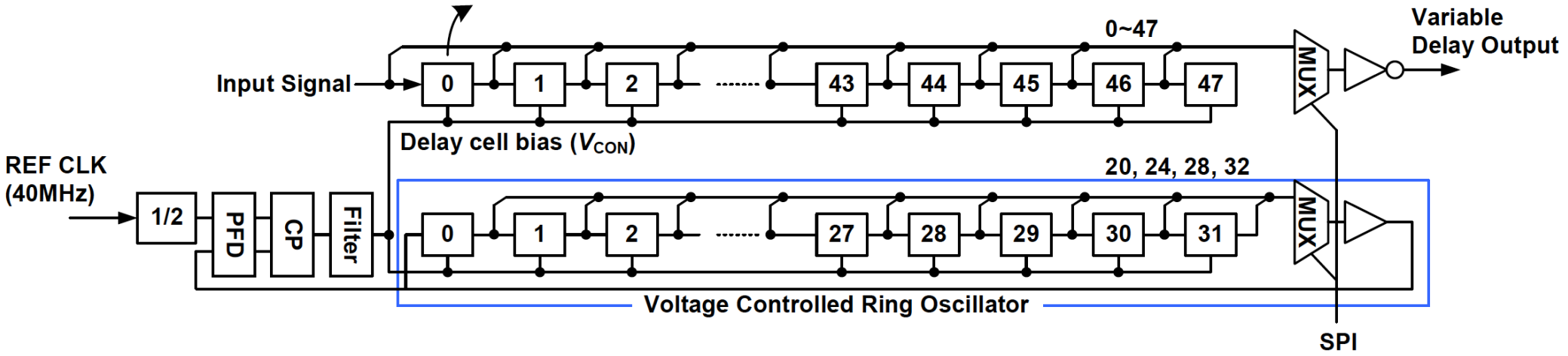
The delay is 4.6 ± 0.1 ns for target ranges of VDD and offset satisfies the requirement of timing control resolution < 1 ns.

PLL and Variable Delay



PLL and Variable Delay Line

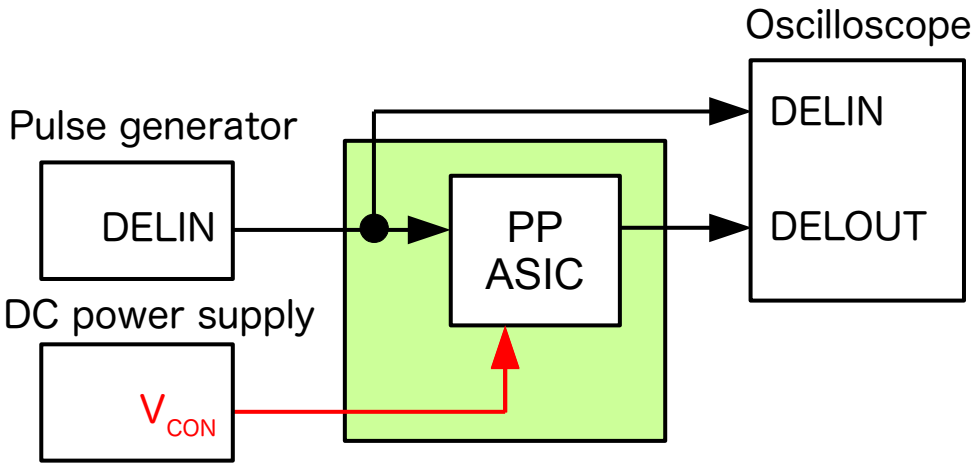
- A common delay cell design is used in both PLL and variable delay lines. They are controlled by a common bias voltage which is generated from charge pump circuit in PLL.
- PLL keeps the signal propagation delay of the ring at 25 ns. The number of delay cells in PLL can be changed from 20 to 32 via SPI control signal.
- The propagation delay of the variable delay will be kept constant against the changes of oparation conditions.

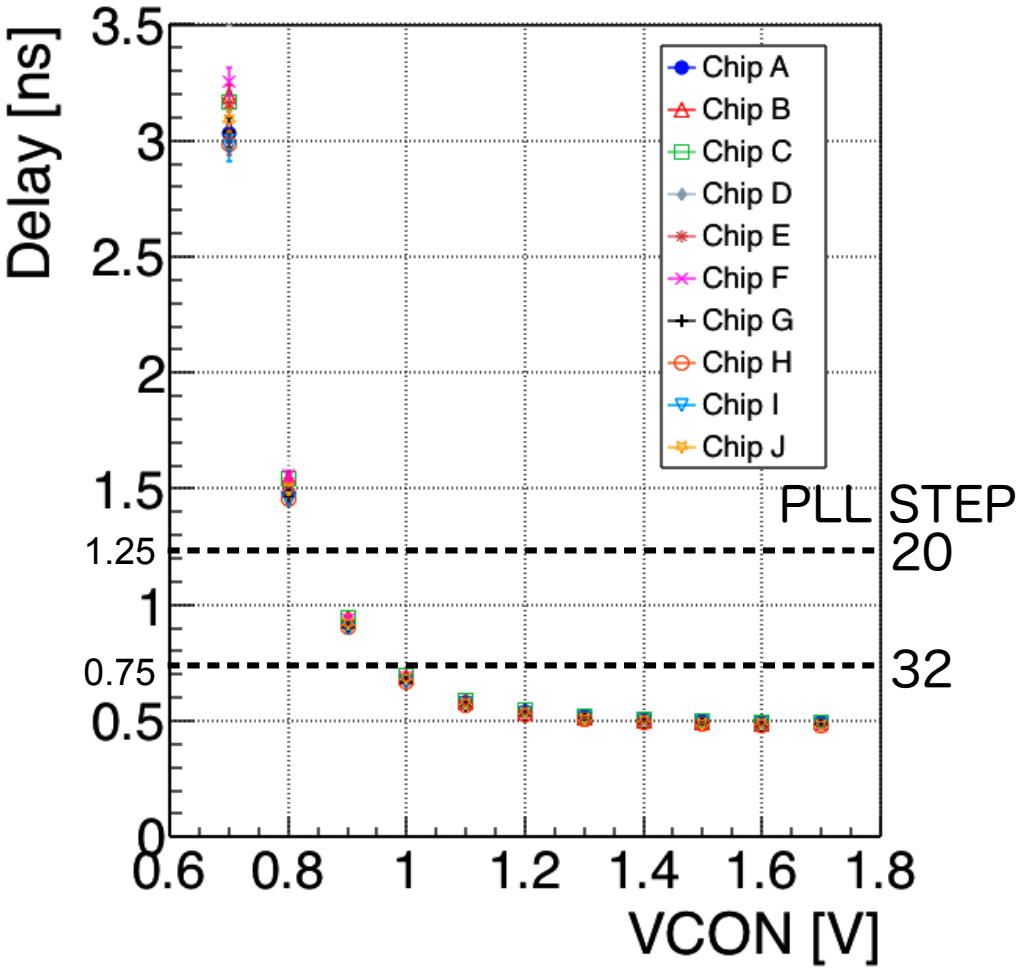


Relation between Delay and Control Voltage (V_{CON})

Delay of a delay cell of 10 chips was measured depending on V_{CON}.

V_{CON} was supplied by DC power supply.

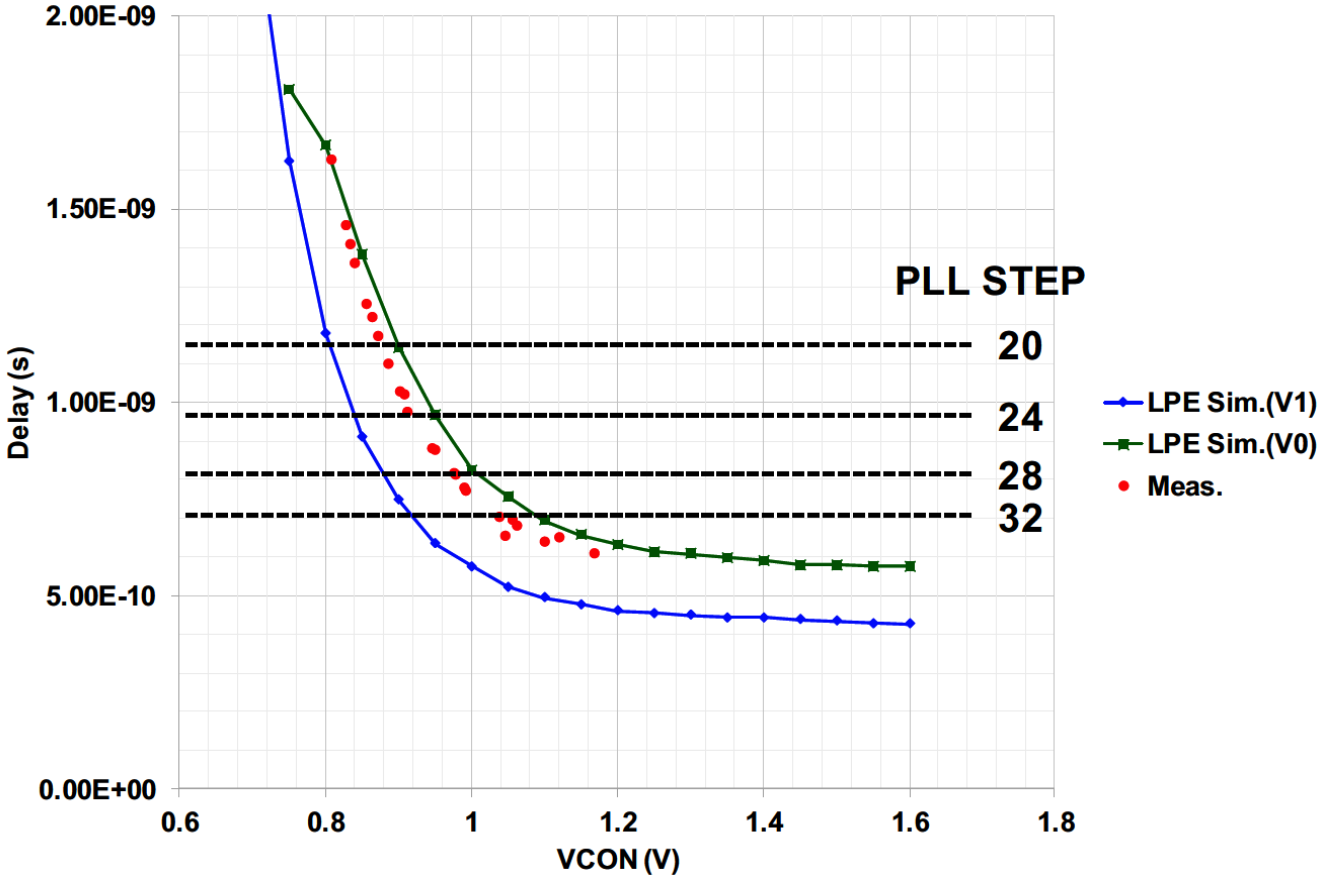




The delay can be changed from 0.5 ns to 3 ns.

The requirement of timing control resolution < 1 ns is satisfied with margin.

Comparison with the Simulation

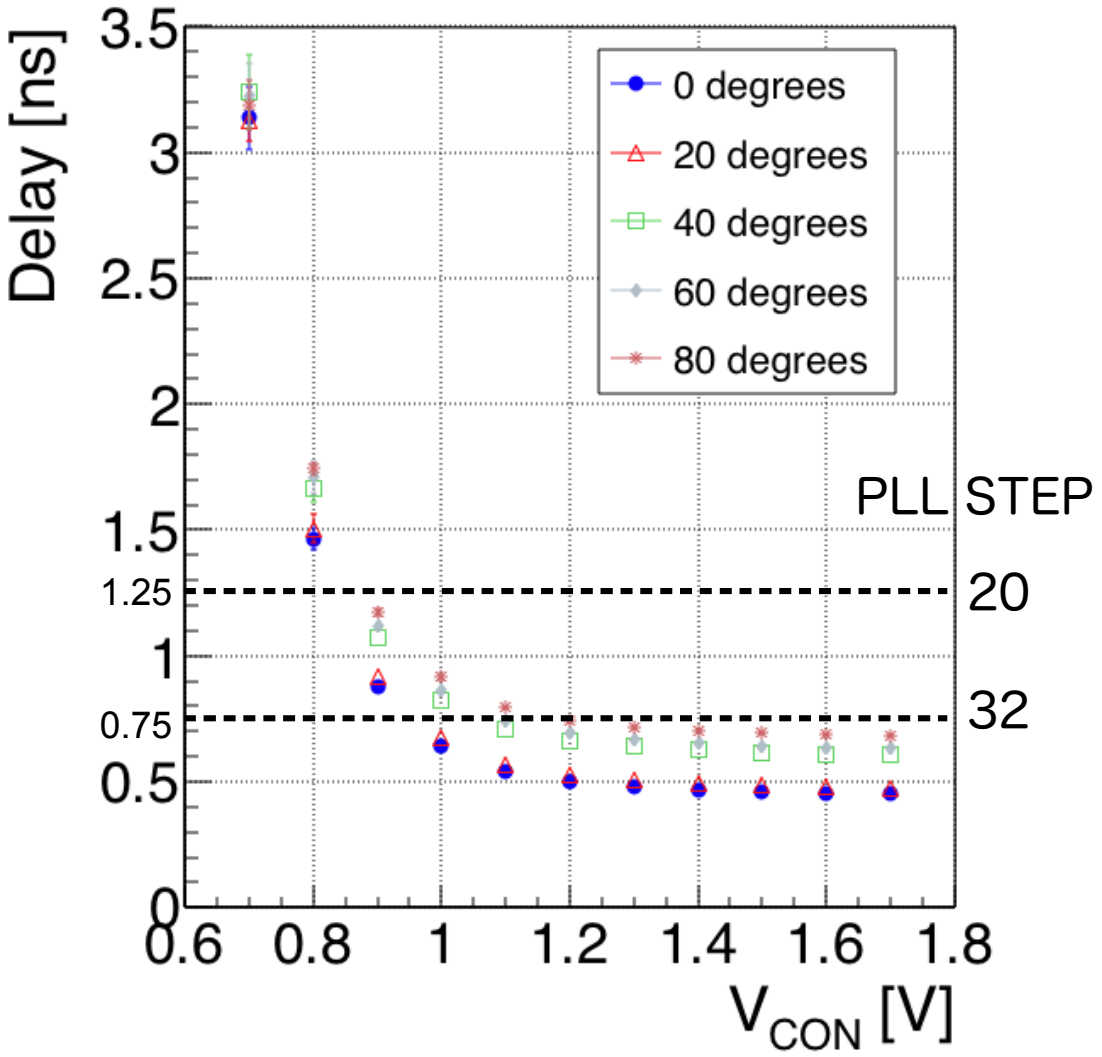


The measured delay for prototype v.0 is similar to the Layout Parasitic Extraction (LPE) simulation with typical condition.

The prototype v.0 may not have enough margin in case of PLL STEP = 32.

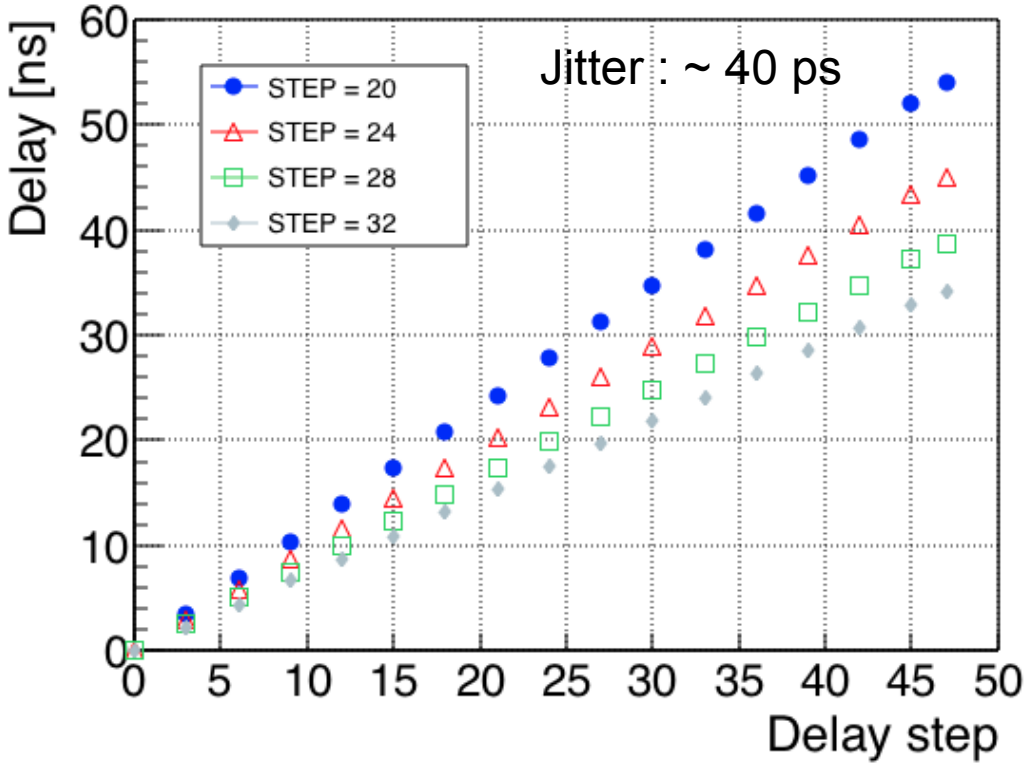
For next version (v.1), the delay is reduced by changing the gate length of transistor in the delay units.

Delay Dependence on Temperature



The delay < 1 ns is covered for 0-80 degrees.

Linearity of the Variable Delay



PLL STEP	Delay per step	Control range
20	1.15 ns	54.1 ns
24	0.96 ns	45.0 ns
28	0.82 ns	38.1 ns
32	0.73 ns	34.2 ns

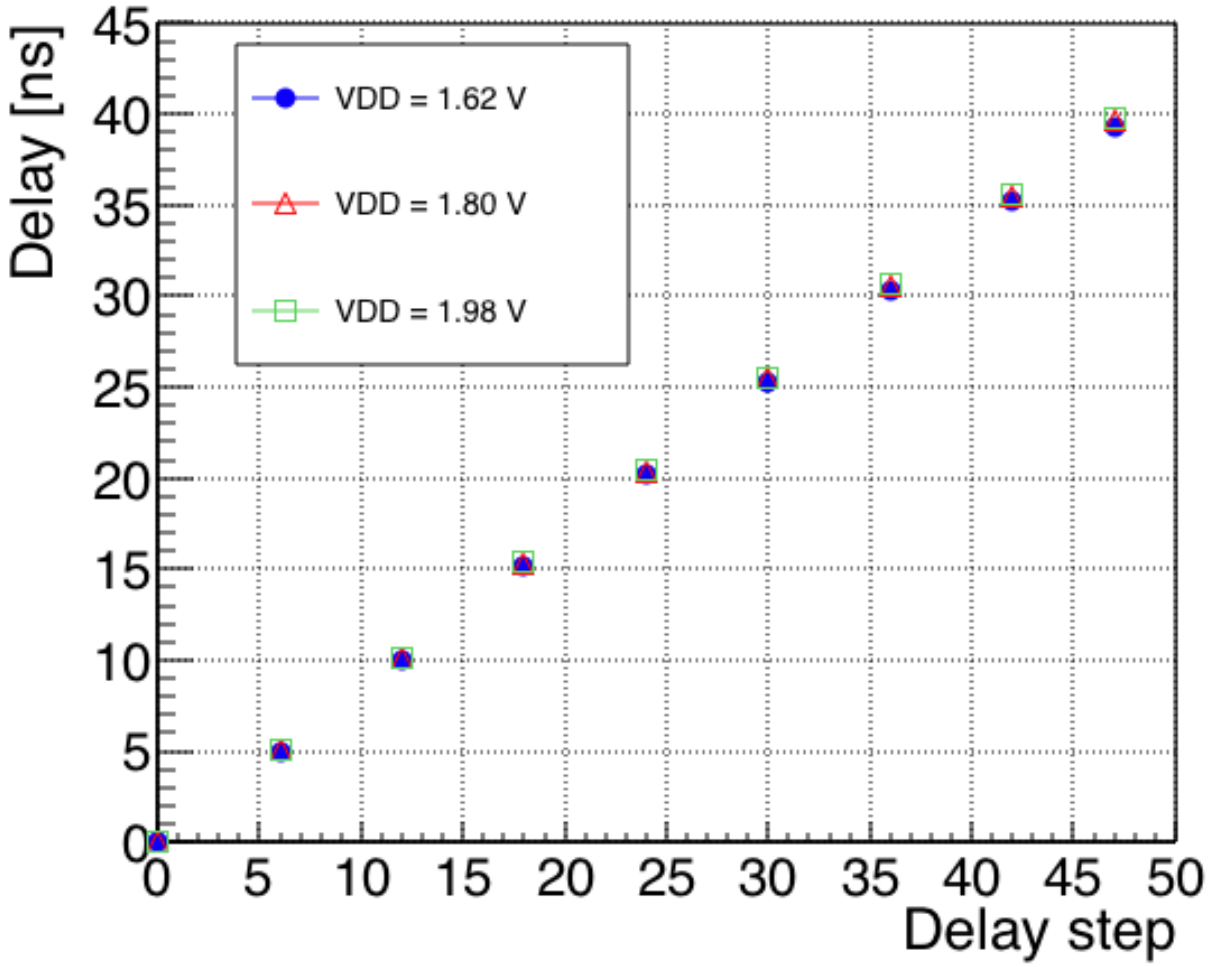
The linearity has been confirmed for all STEP configurations.

The delay of single step is < 1 ns (target specification) for STEP ≧ 24.

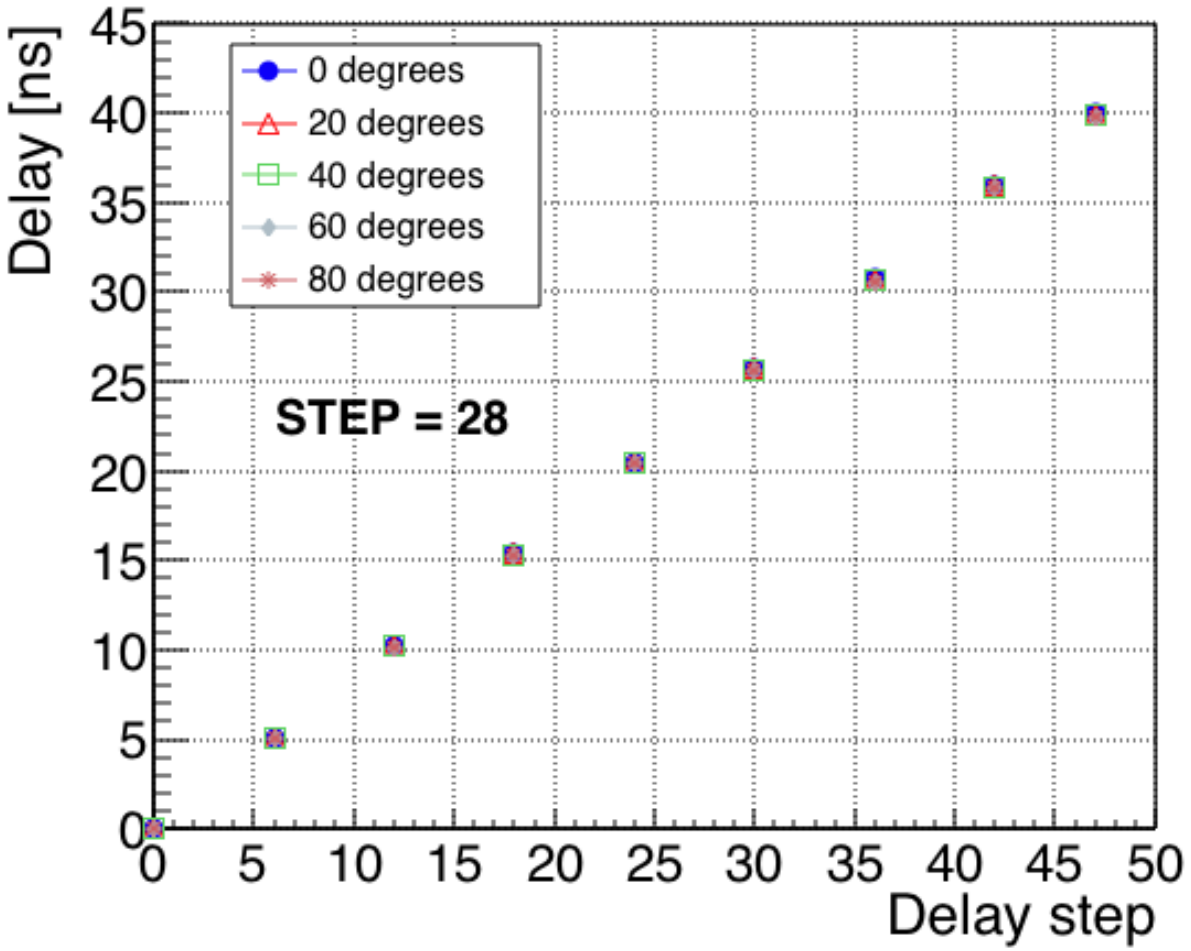
The dynamic range is greater than the target specification.

Performance of the Variable Delay Depending on VDD

The linearity of variable delay was confirmed for VDD = 1.62-1.98 V.

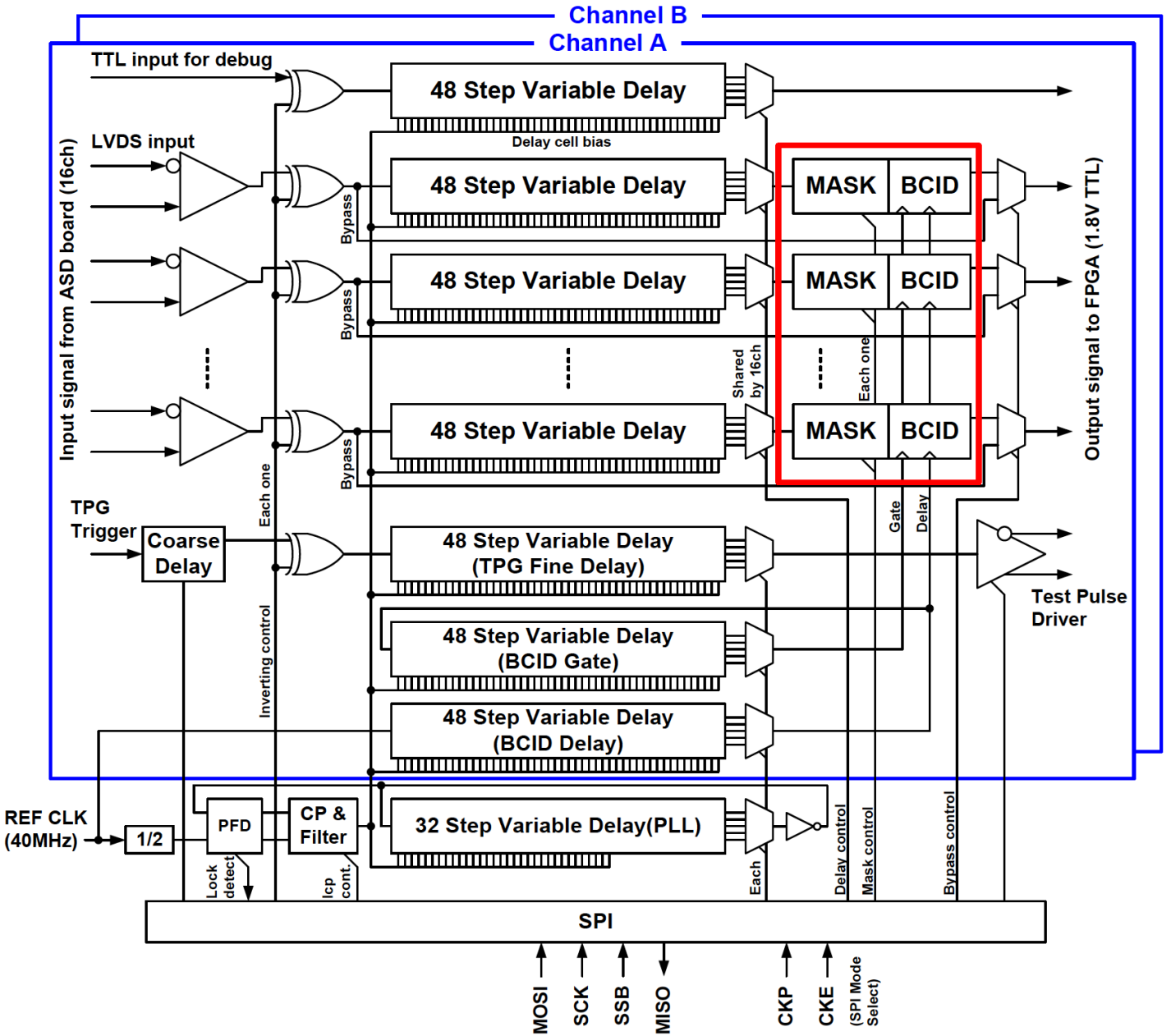


Performance of the Variable Delay Depending on Temperature

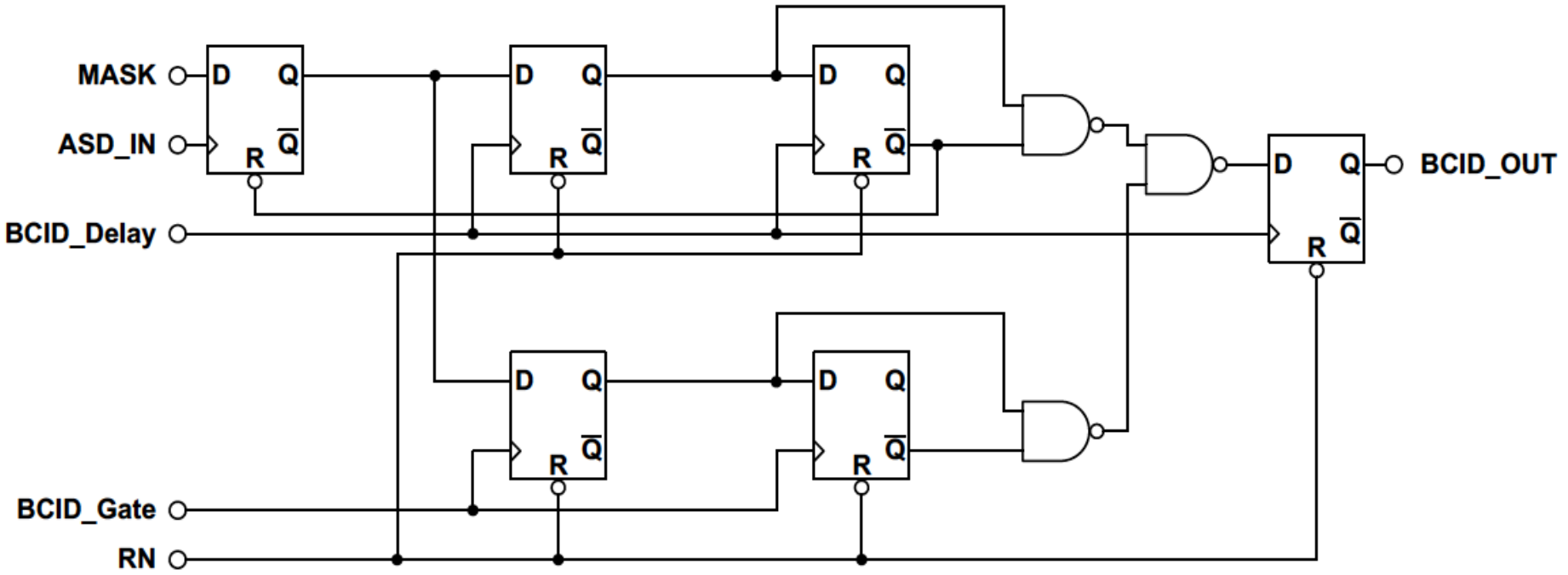


The linearity of variable delay was confirmed for 0-80 degrees.

BCID


Channel B
Channel A
TTL input for debug
LVDS input
Input signal from ASD board (16ch)
48 Step Variable Delay
Delay cell bias
48 Step Variable Delay
48 Step Variable Delay
48 Step Variable Delay
MASK
BCID
MASK
BCID
MASK
BCID
Bypass
Bypass
Bypass
Shared by 16ch
Each one
Output signal to FPGA (1.8V TTL)
TPG Trigger
Coarse Delay
Each one
48 Step Variable Delay (TPG Fine Delay)
48 Step Variable Delay (BCID Gate)
48 Step Variable Delay (BCID Delay)
Gate
Delay
Test Pulse Driver
Inverting control
REF CLK (40MHz)
1/2
PFD
CP & Filter
32 Step Variable Delay(PLL)
Lock detect
Icp cont.
Each
Delay control
Mask control
Bypass control
SPI
MOSI
SCK
SSB
MISO
CKP
CKE
(SPI Mode Select)

BCID



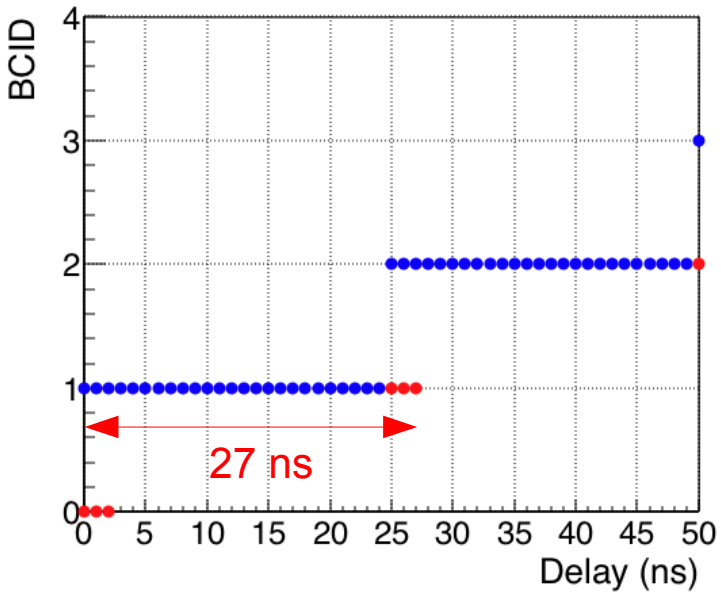
The BCID circuit synchronises the signals with 40 MHz clock.
Each rising edge of the 40 MHz clock corresponds to a bunch crossing.

BCID_Delay is used to adjust for the phase difference between the 40 MHz clock and the earliest arrival times of signals from ASDs.

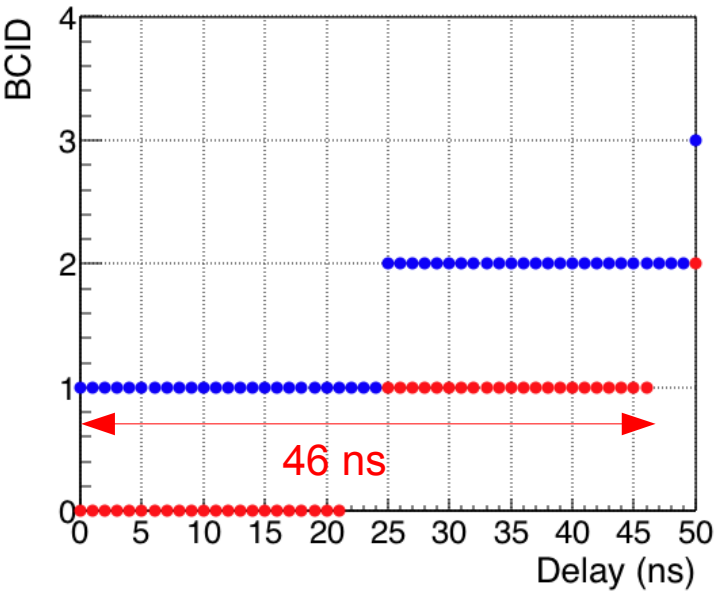
BCID_Gate is used to adjust the effective gate width. Each signal is assigned to either one or two bunch crossings depending on the timing.

BCID Test Results

- BCID GATE = 1

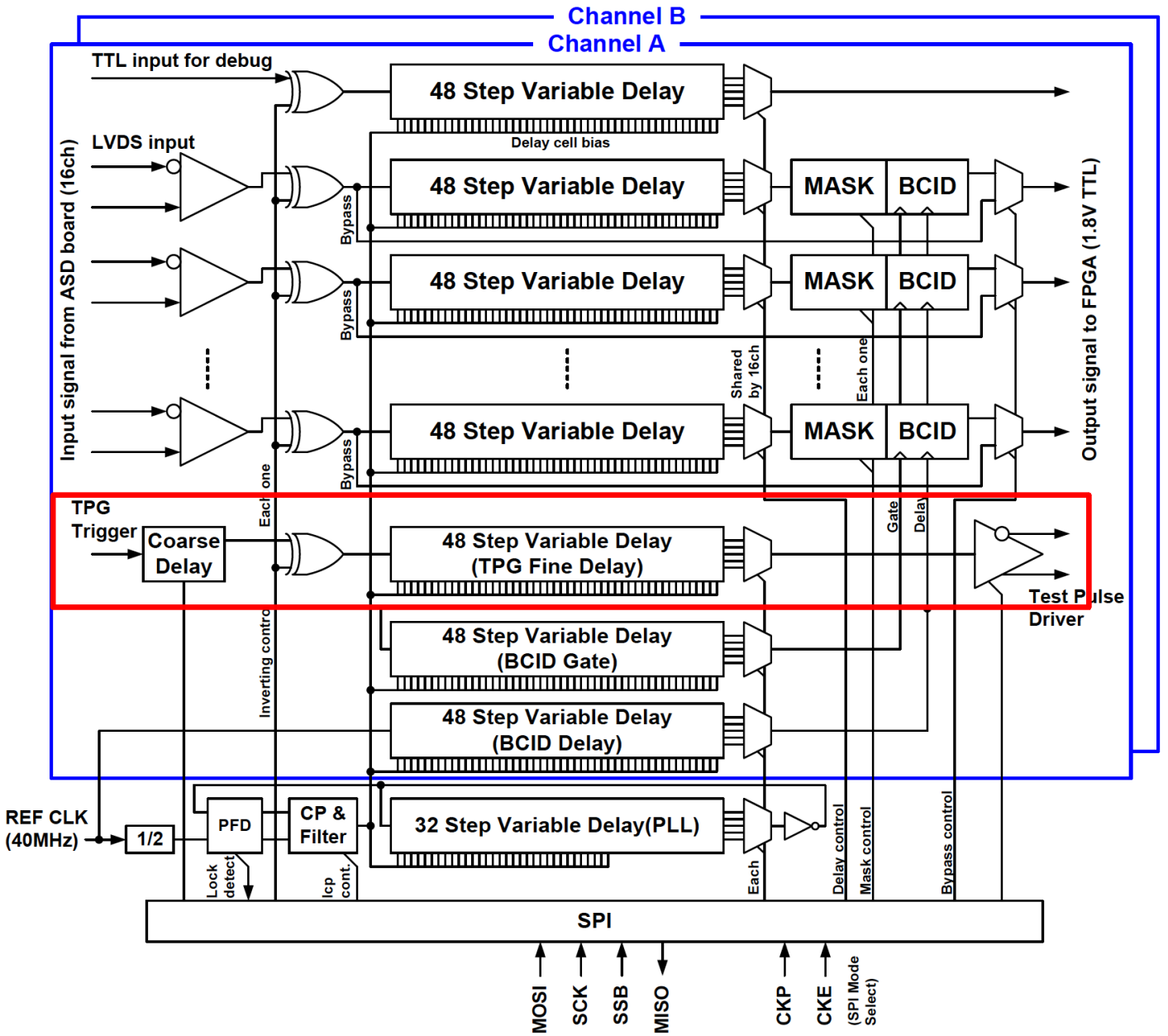


- BCID GATE = 26

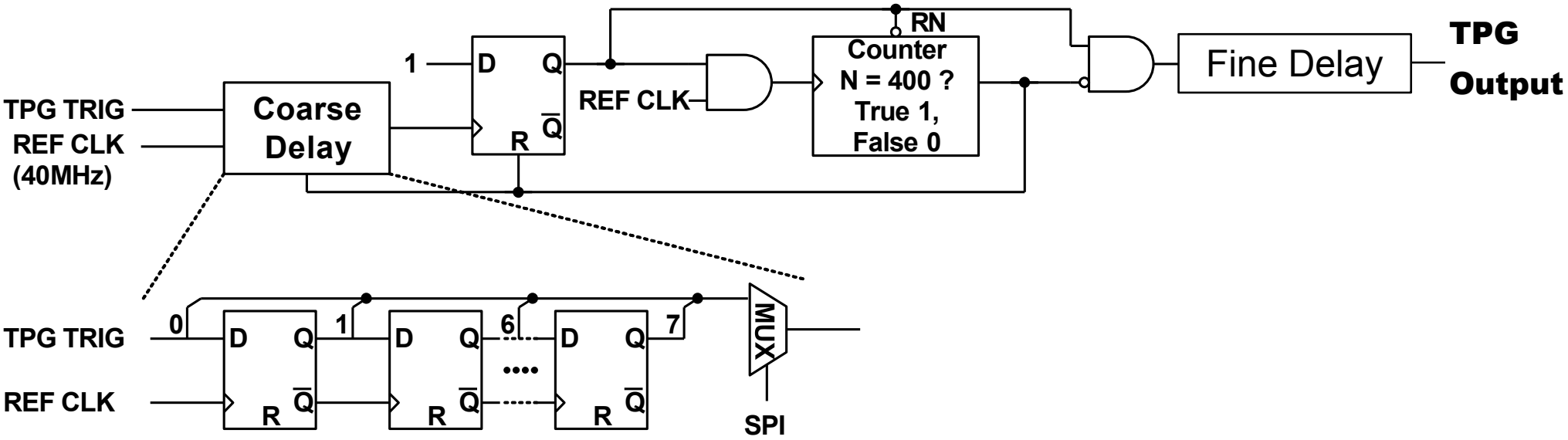


The functions of BCID circuit have been confirmed.

Test Pulse Generator (TPG)



Test Pulse Generator (TPG)



TPG generates the pulse with coarse delay (0-7 CLK).

The pulse is set via SPI in a range from 25 ns to 102.4 μs.

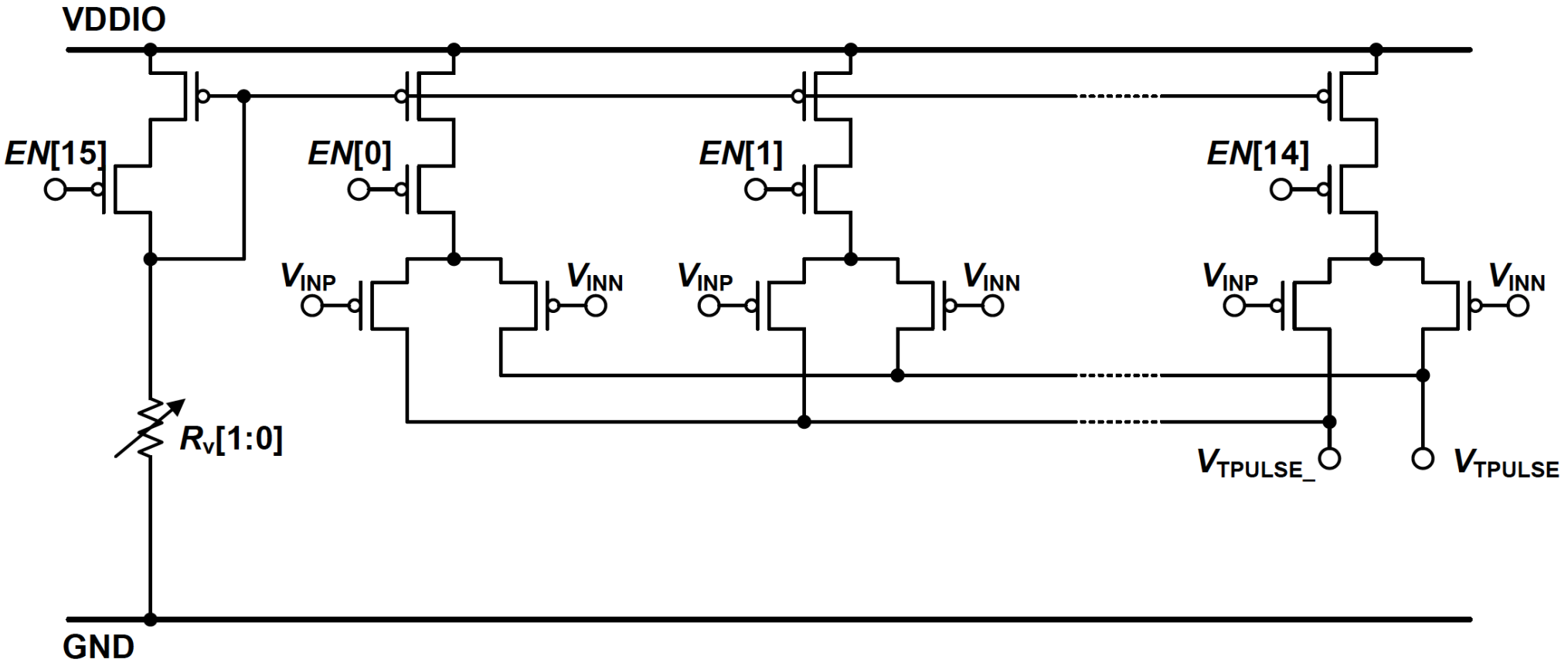
TPG output delay time is controlled by another fine delay (0-40 ns, < 1 ns resolution).

TPG Driver

Drivability of TPG driver can be controlled by

- Changing the number of current sources (EN[0-14])
- Changing the bias current using variable resistor.

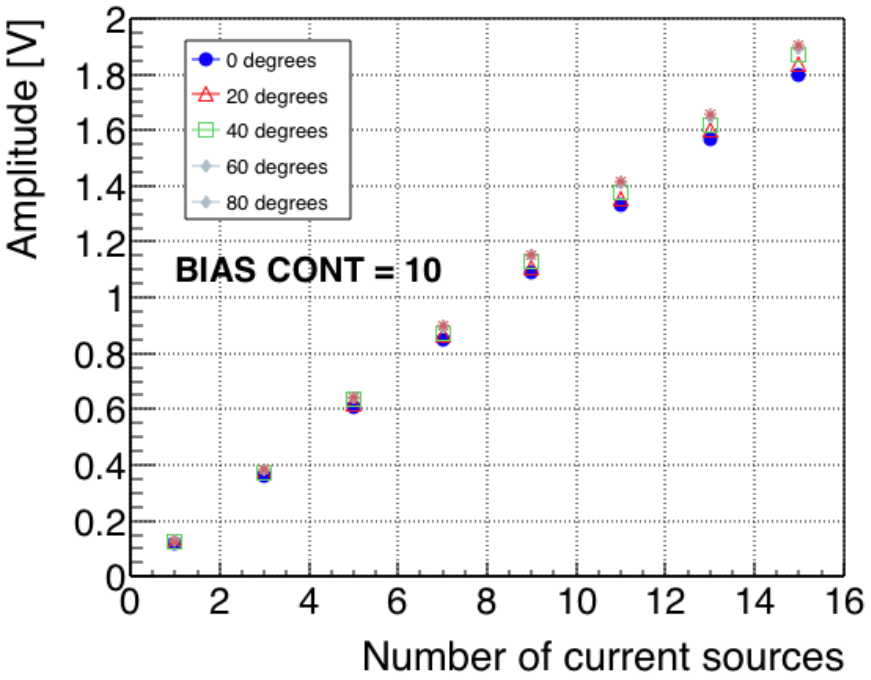
Load condition in measurements: 100 Ω/20 pF



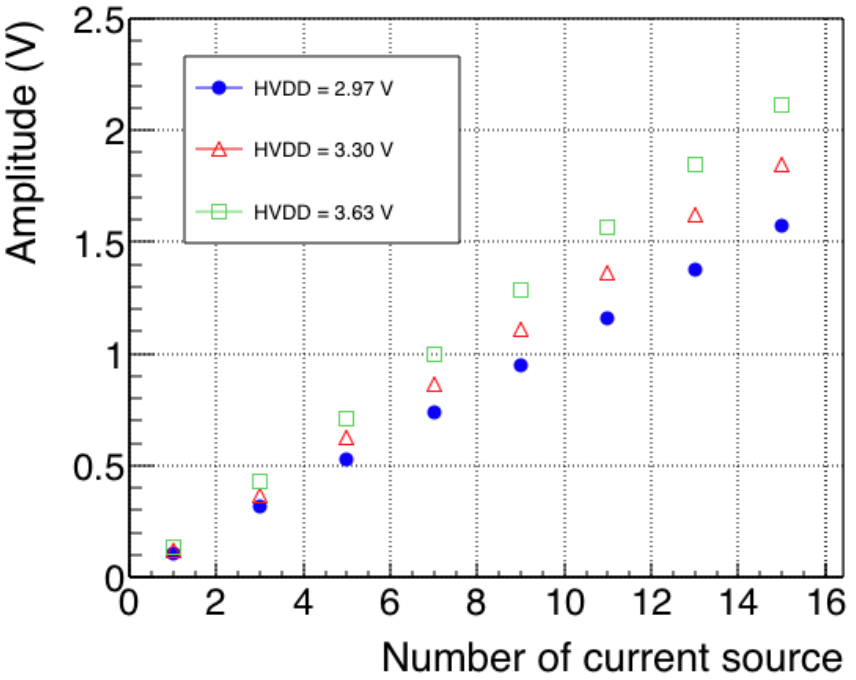
TPG Driver Test Results

The amplitude was measured depending on temperature and VDD.

- Dependence on temperature



- Dependence on VDD



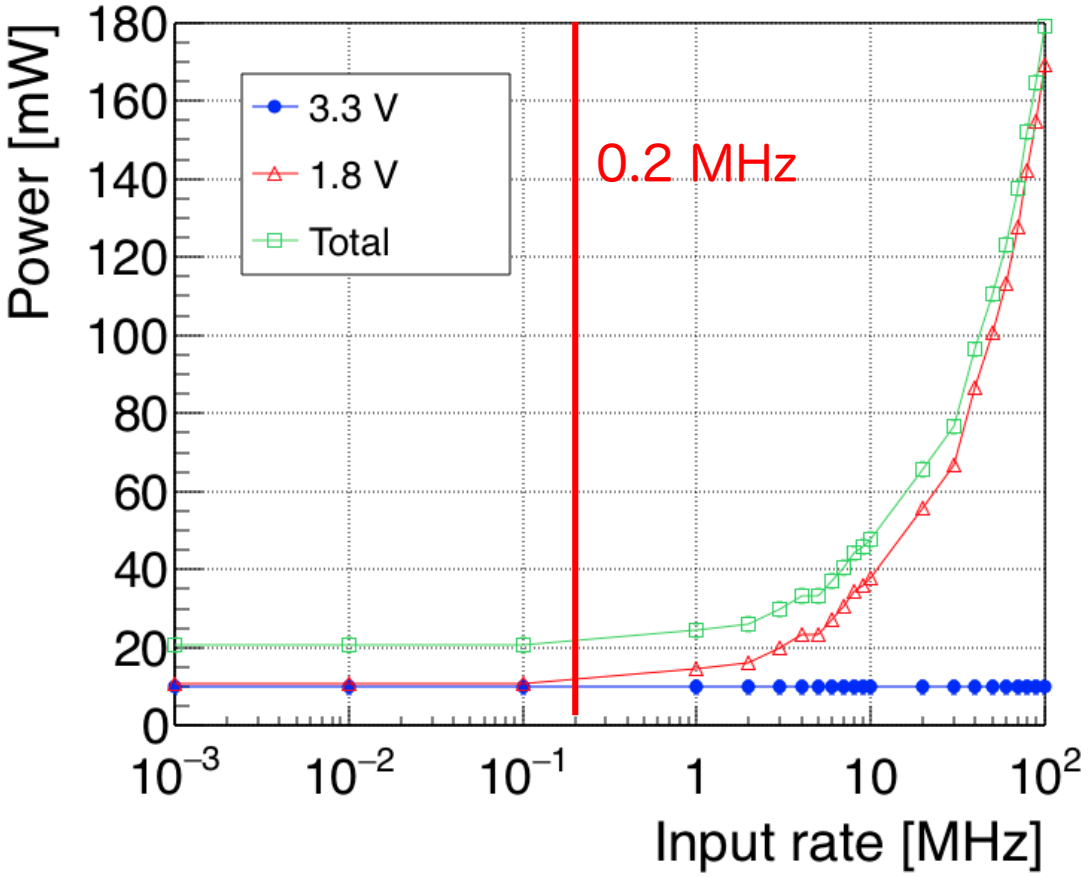
The amplitude used for daily calibration in Run 1 and Run 2 is ~300 mV.

A similar value is assumed for Run 4 and the beyond.

The dependence on VDD is safely small for the daily calibration.

Power Consumption

- 10 pF load capacitance at LVCMOS outputs
- Power consumption of TPG driver is not included.



The power consumption is ~ 20 mW (0.63 mW/ch) under an expected hit rate of ~0.2 MHz per channel at a luminosity of 7.5×10^{34} $cm^{-2}s^{-1}$.

Note that the chip of the current system consumes ~130 mW.

Yield

The yield has been studied by measuring the performance of prototype v.0 chips.

In total 20 chips were produced, and 19 of them were measured.

One chip was damaged before the measurement by a wrong setup of power supply outside the chip.

For all channels of 19 chips, two sets of pulse input were provided: 10 kHz and 10 MHz.

For all channels, output signals were observed.

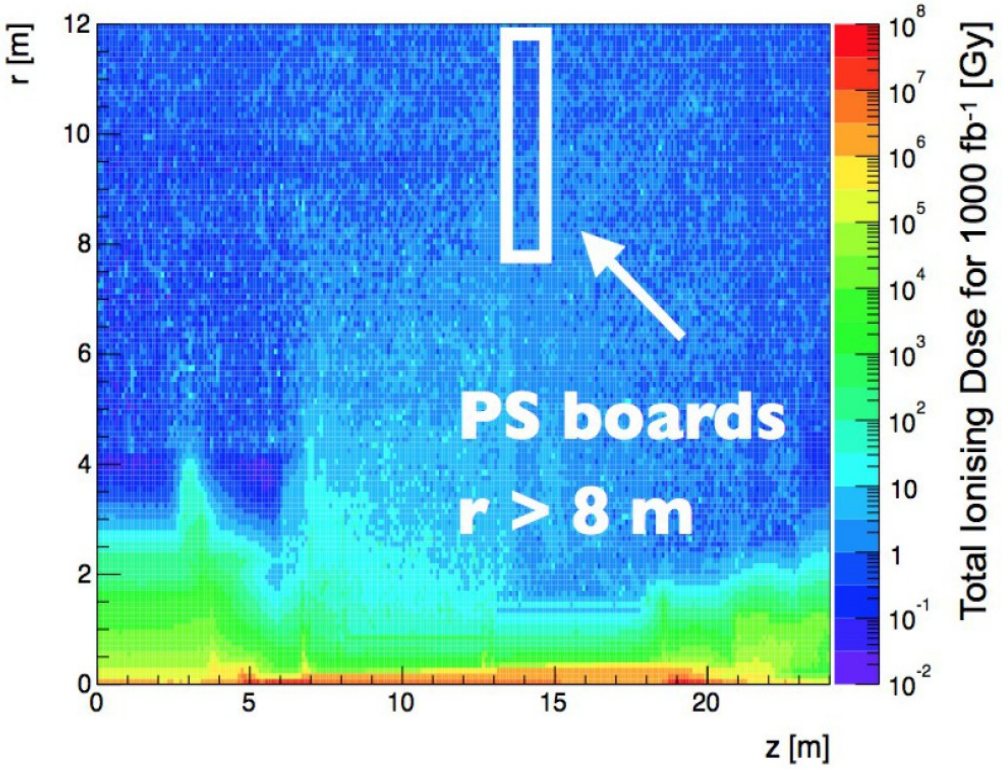
The power consumption for 10 kHz (10 MHz) input ranges

from 17 mW to 21 mW (from 44 mW to 51 mW) depending on the chips.

Although the measurements performed for all chips were limited,

the results indicate that the 19 chips have no significant failures.

Radiation Tolerance for Total Ionising Dose



Total ionising dose for $\mathcal{L}$ = 4000 fb^{-1} is estimated to be 6.0 Gy.

Requirement for PP ASIC is 27 Gy.

($SF_{sim} \times SF_{ldr} \times SF_{lot} = 1.5 \times 1.5 \times 2 = 4.5$)

Gamma Irradiation Test Setup

Facility: Cobalt 60 facility in Nagoya University

Dose rate: 8.2 Gy/min

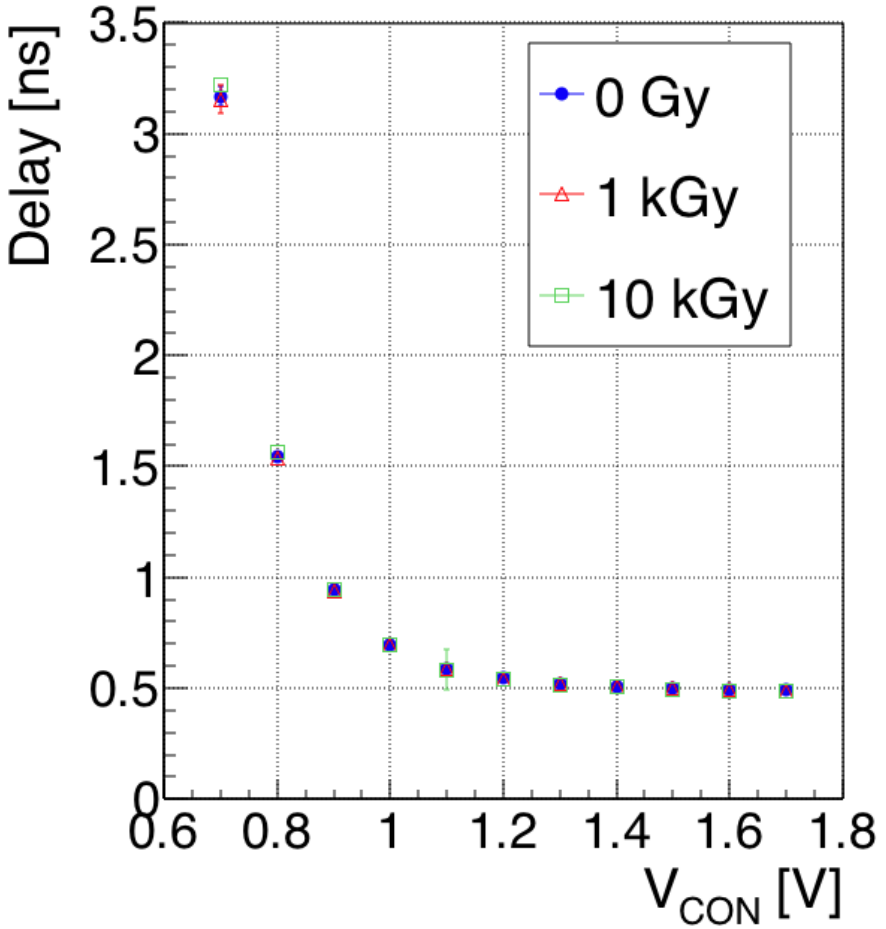
Total dose: 1 kGy for three chips, 10 kGy for one chip

Gamma Irradiation Test Result

- PLL and Variable Delay

  Relation between the control voltage V_{CON} and the measured delay of a delay cell unit for total ionizing doses of 0 Gy, 1 kGy, and 10 kGy.

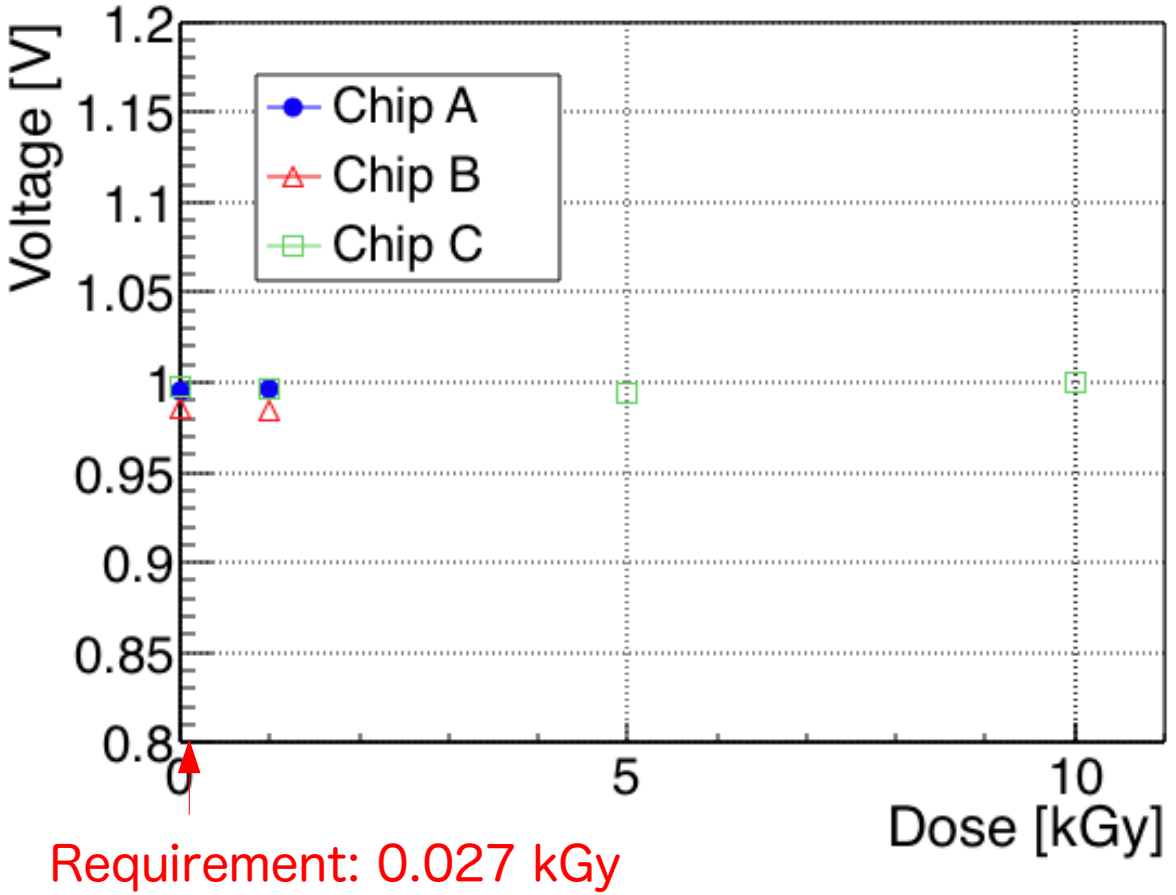
No significant change was observed.



Gamma Irradiation Test Result

- PLL and Variable Delay

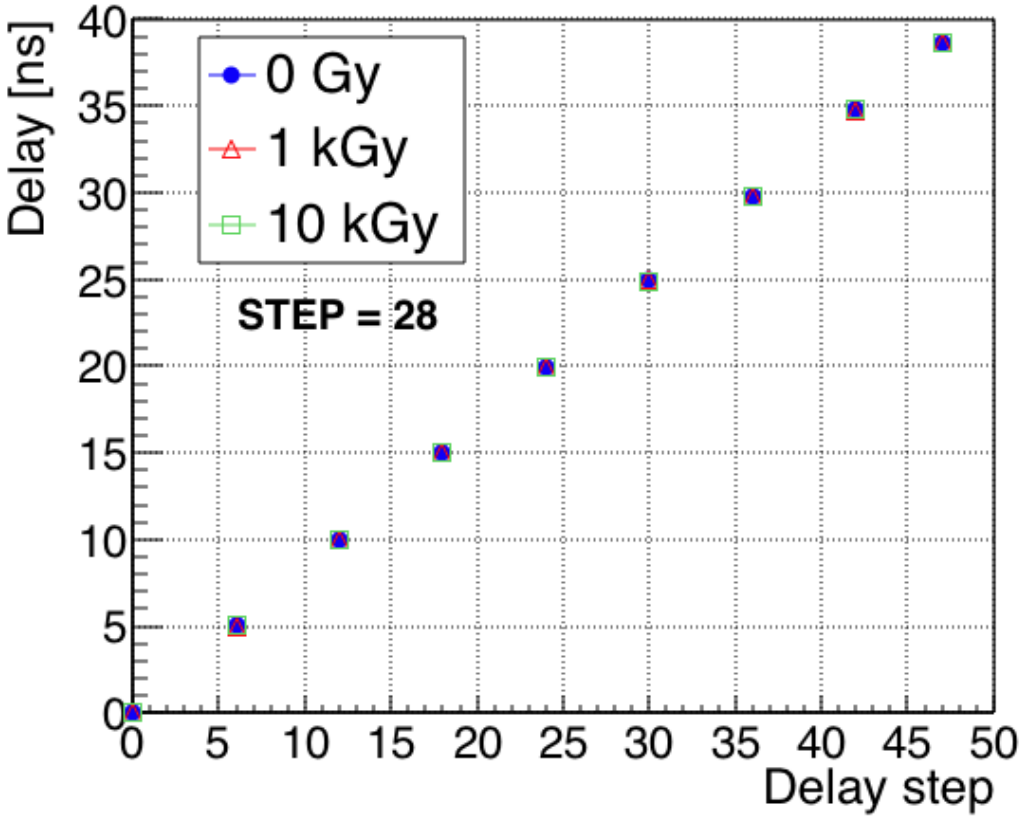
  The control voltage V_{CON} for the PLL circuit locked with an external reference clock of 40 MHz depending on the ionizing dose.
  No significant change was observed.



Gamma Irradiation Test Result

- PLL and Variable Delay

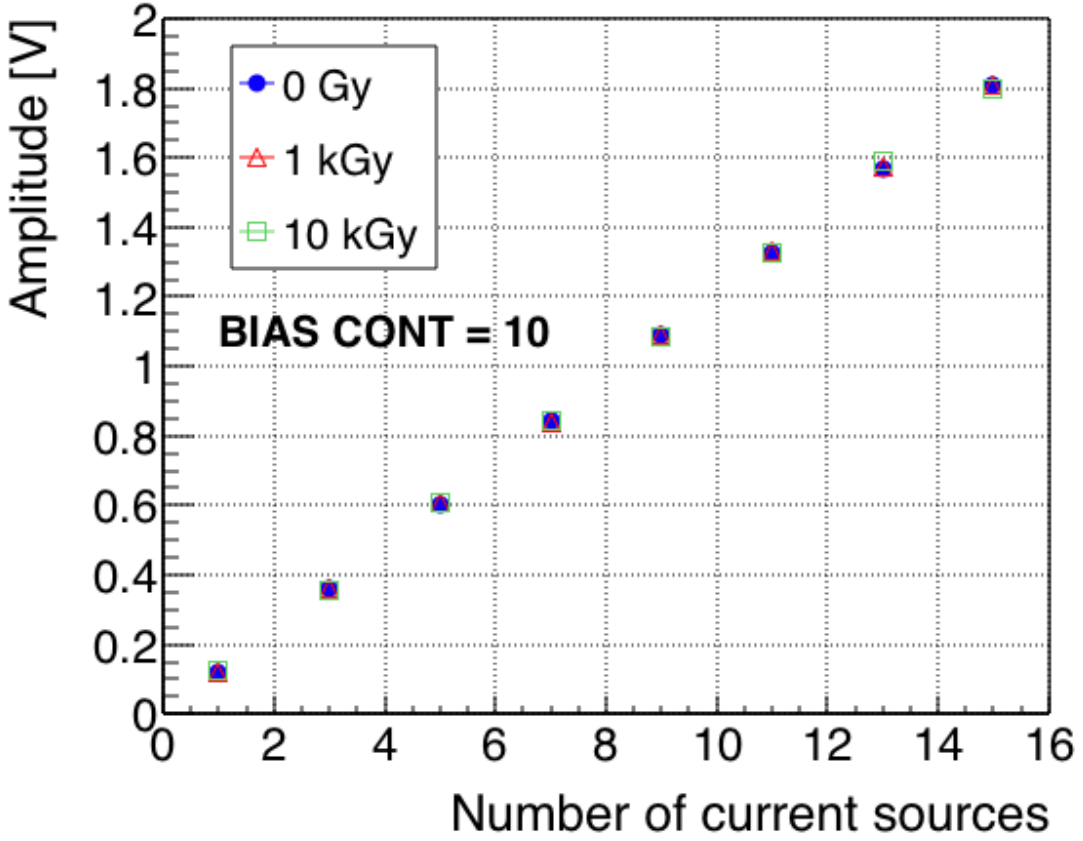
  Relation between the setup of the number of delay cell units (“delay step”) and the measured delay of the variable delay for total ionizing doses of 0 Gy, 1 kGy, and 10 kGy. No significant change was observed.



Gamma Irradiation Test Result

- Test Pulse Generator

  The amplitude of the test pulse generator output depending on the number of current sources for total ionizing doses of 0 Gy, 1 kGy, and 10 kGy.
  No significant change was observed.

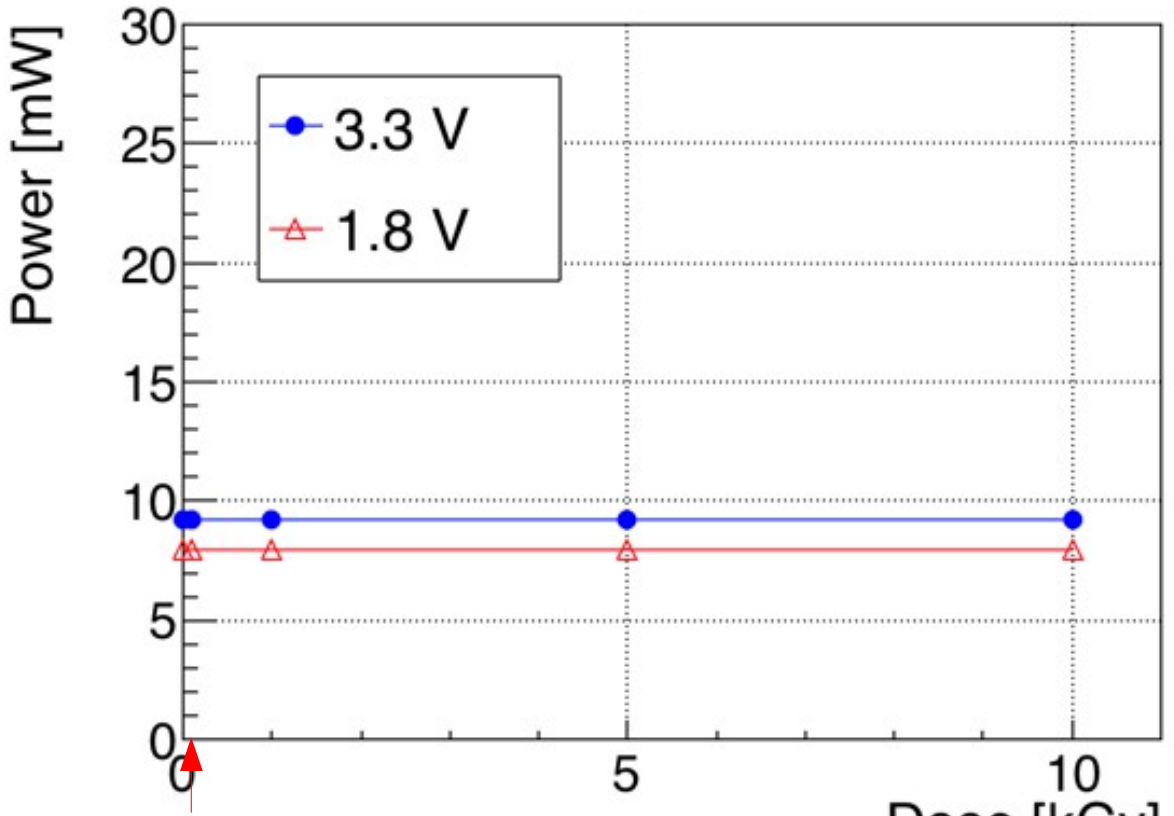


Gamma Irradiation Test Result

- Power consumption

The power consumption depending on the ionizing dose.

No significant change was observed.



Prototype ASIC v.0 Specification

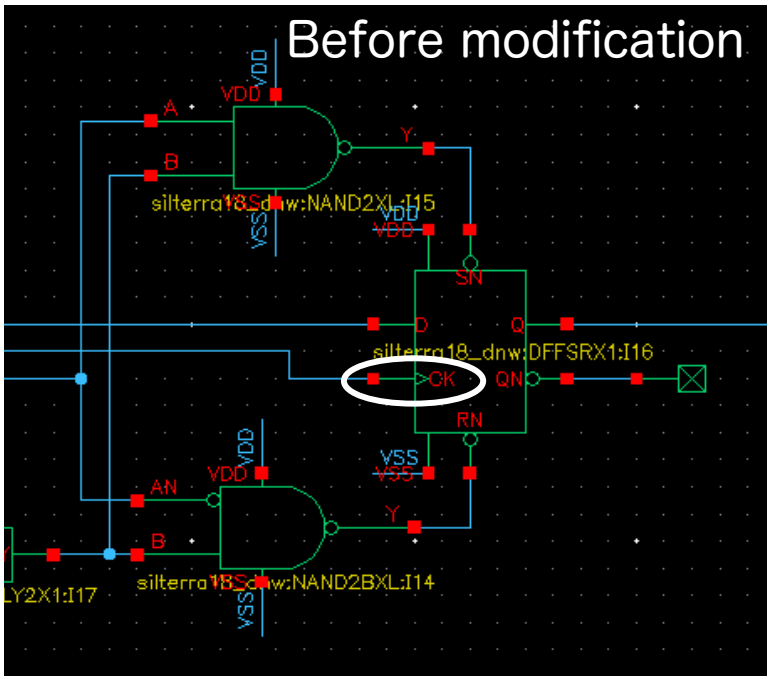
Design process	Silterra 0.18 μs CMOS 6M1P
Supply voltage	3.3 V (LVDS Rx, TPG Driver) 1.8 V (PLL, Delay line, CMOS input and output) Voltage tolerance : ± 10 %
# of channels	Group A (16 ch), Group B (16 ch)
Timing control resolution	< 1 ns
Timing control range	> 40 ns
Timing jitter	~40 ps (LVDS Rx), ~40 ps (Variable Delay)
Temperature range	0 ~ 80 ℃
Power consumption	~20 mW (Previous design: 130 mW)

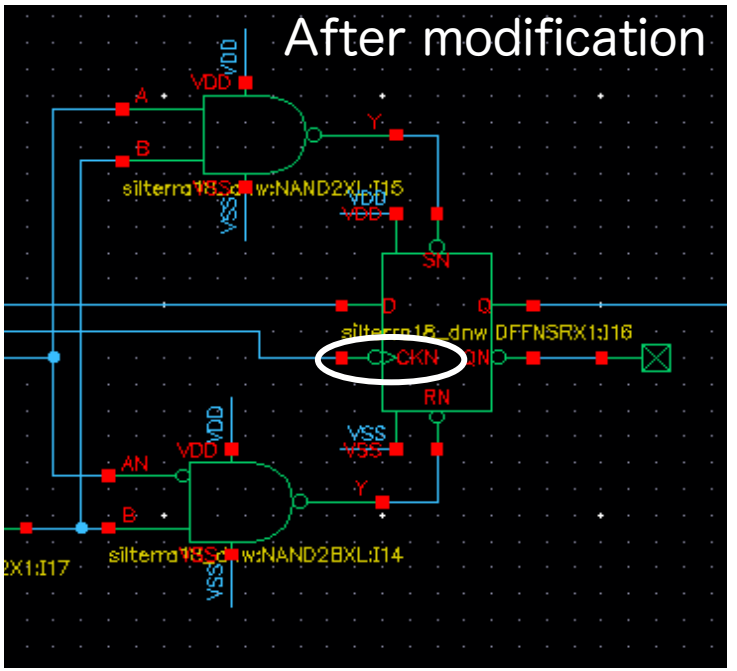
All requirements are satisfied.

Modification for Next Version

- Change the gate length of transistor in the delay units for reducing the delay time for an improved margin. See page 14.

- Prototype v.0 has a wrong edge setup of SPI MISO signal. Although it is fine for the use if the device controlling the PP ASIC uses the corresponding edge, as done for prototype v.0 measurement, we modified the circuit for next version.





The modifications are very simple and already completed.

Backup