Patch-Panel ASIC Design Report for Final Design Review

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3 Dec. 2018

1. Overview

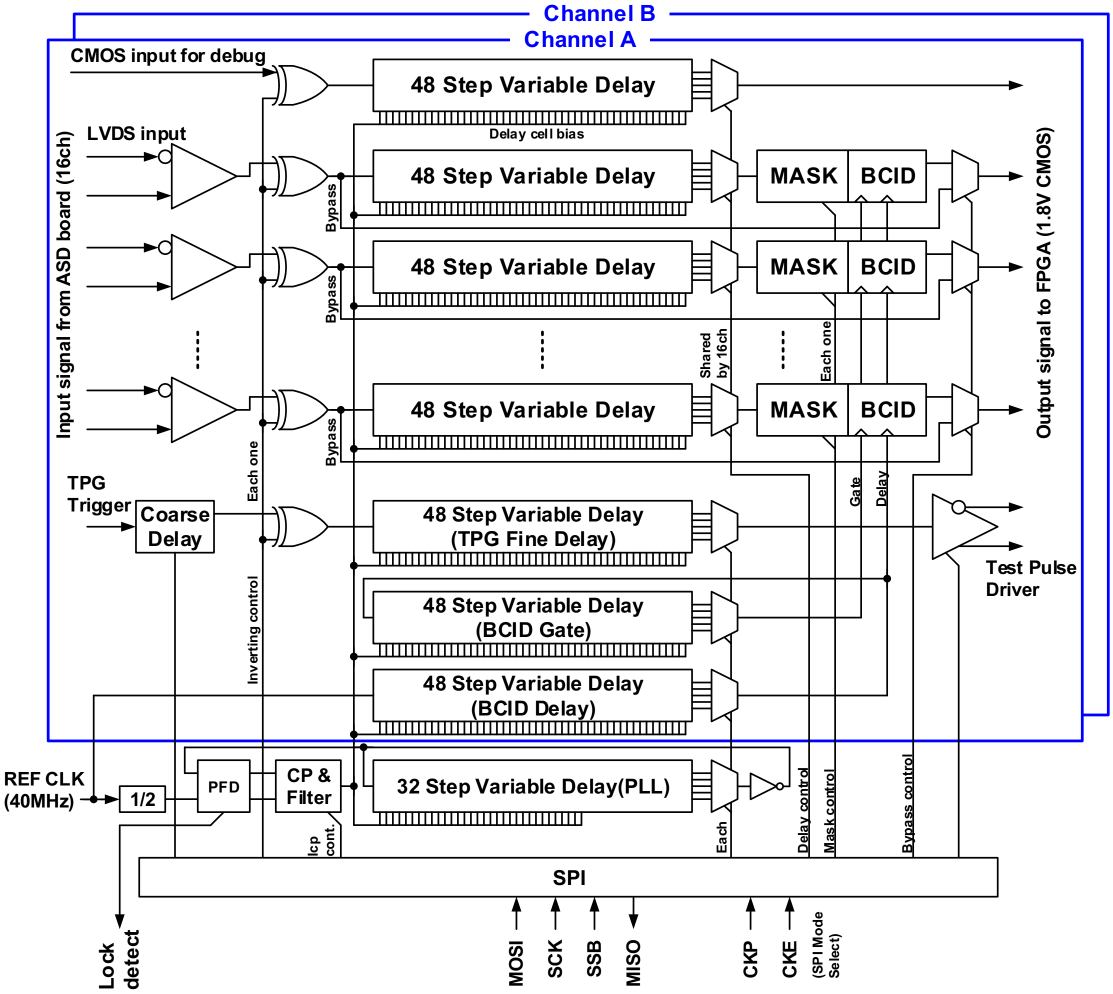


Figure 1 Block diagram of the Patch-Panel ASIC.

The Patch-Panel ASIC is a full custom CMOS IC to be implemented on a PS board in the PS pack of the TGC system. Figure 1 shows a block diagram. It receives discriminator output signals from two 16-channel ASD boards by LVDS receivers and performs bunch-crossing identification (BCID). The signals from the ASD board are transmitted with the LVDS level via twisted-pair cables. Prior to the BCID, variable delay is introduced to each signal from ASD boards in order to adjust the delay difference from time of flight and cable length and also to adjust the phase difference between LHC 40 MHz clock and signals from ASD boards. The BCID circuit contains two blocks of variable delay. A block is used to adjust for the phase difference between the clock and hit signals, and the other is used to provide a gate width greater than 25 ns so that a hit can be assigned to either one or two bunch crossings. The BCID circuit can mask individual channels. The IC has test pulse generator in order to provide pulse to ASD boards. The test pulse generation is initiated by the test pulse trigger signal from a CMOS receiver. The delay is programmable in a range from 0 ns to 35 ns with sub-nanosecond resolution. Additional coarse delay is implemented to the test pulse generators.

The IC is subdivided into two parts: Channel A and Channel B. Each part corresponds to a single 16-channel ASD board. Setting of the delay is common to group of signals that come from the same ASD board. The amplitude and the delay of the test pulse trigger are programmable for each ASD board. The SPI protocol is adopted to the control of the IC.

2. Process

We have developed Patch-Panel ASIC prototype v.0 using 0.18 μm full custom CMOS technology of Silterra Malaysia. We used the library provided from ARM for standard logic circuits. We designed the circuits of an LVDS receiver, a PLL, a variable delay, and a test pulse generator. LVDS receivers and test pulse generators are based on power supply of 3.3 V and other I/O and internal circuits are based on 1.8 V. We have provided an entire layout by ourselves. The size of a chip is 2.47 mm x 2.47 mm including seal-ring as shown in Figure 2. The plots in the following sections show the results of the measurement of prototype v.0 except where otherwise stated.

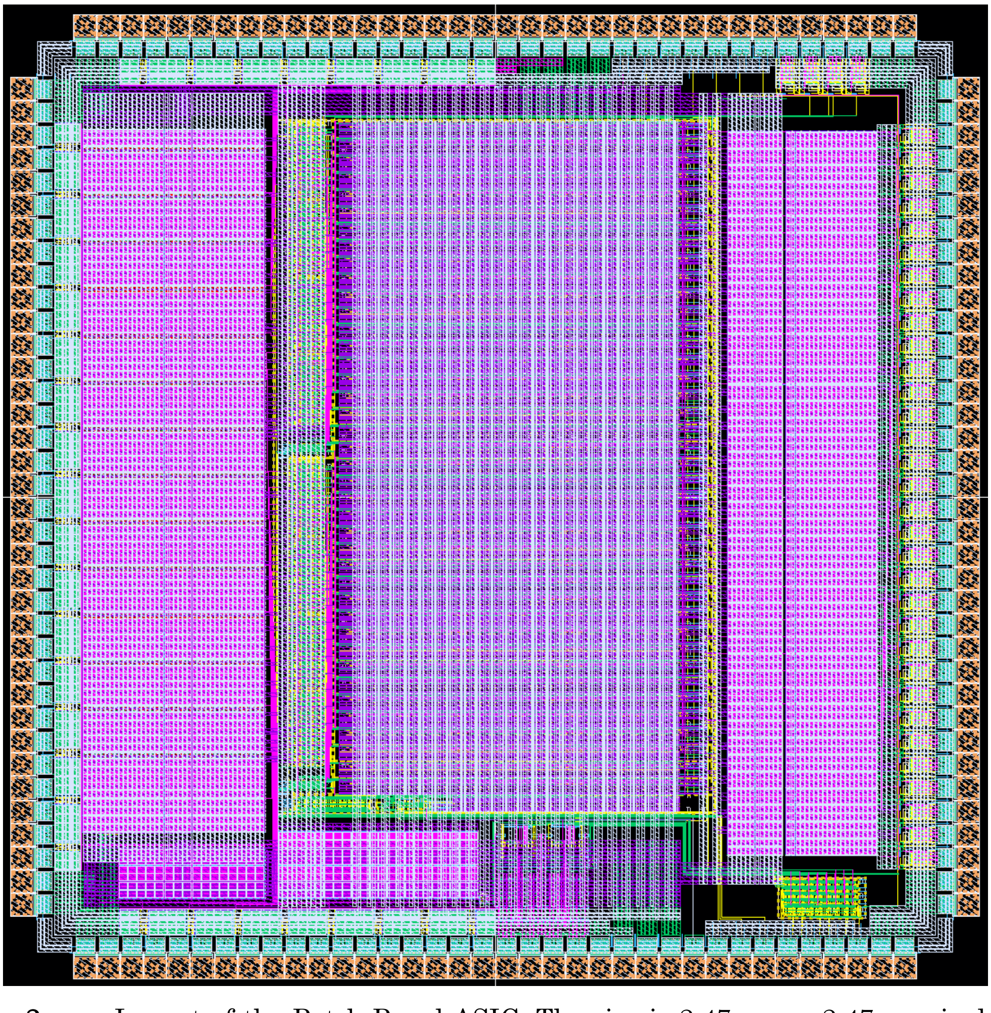


Figure 2 Layout of the Patch-Panel ASIC. The size is 2.47 mm x 2.47 mm including seal-ring.

3. LVDS Receiver

Figure 3 shows a schematic of the LVDS receiver, which consists of two differential amplifiers and two stages of inverter circuits. Bias current can be controlled via two-bit SPI register. We have measured the performance of the receiver of prototype v.0 with bias current control code set to d'2. Figure 4 shows propagation delay for various amplitudes and offset voltages of the input differential signals. The offset voltage is defined to be the central voltage of "low" and "high" levels of input differential signals. The amplitude and the offset voltage of the differential signals from the ASD board are 400 mV and 1.2 V, respectively. Figure 5 shows the measured propagation delay depending on the offset voltages for supply voltages of 2.7-3.9 V. The propagation delay shown in Figures 4 and 5 is the sum of the delay of the receiver, the multiplexer, and the output buffer. The variation of the propagation delay due to the change of the operation conditions is less than 1 ns, which satisfies the system requirement. Figure 6 shows the measured propagation delay depending on bias current control codes. Propagation delay is reduced by increasing control code, while the power consumption of LVDS receiver is increased. A typical control code is d'2, which is implemented as the SPI's initial code.

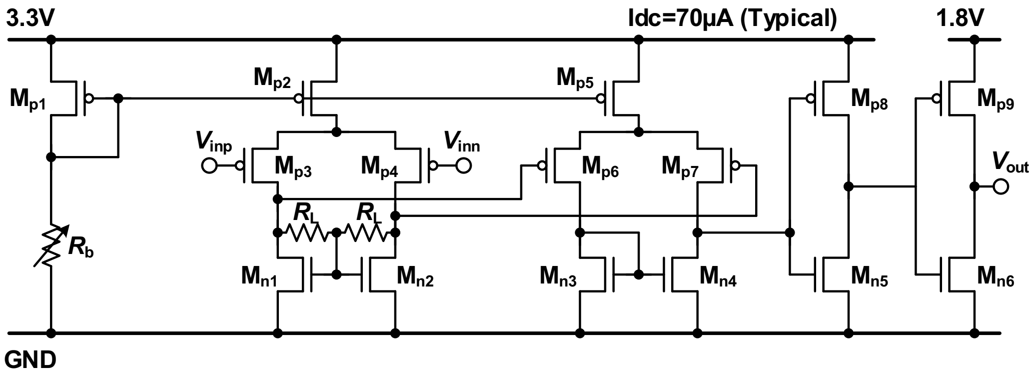


Figure 3 Schematic of the LVDS receiver.

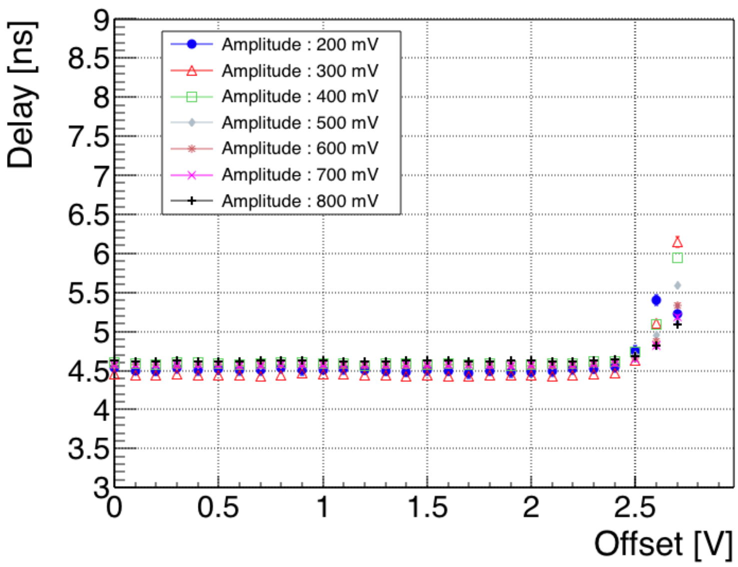


Figure 4 Propagation delay depending on offset voltage for various amplitudes of the input signals.

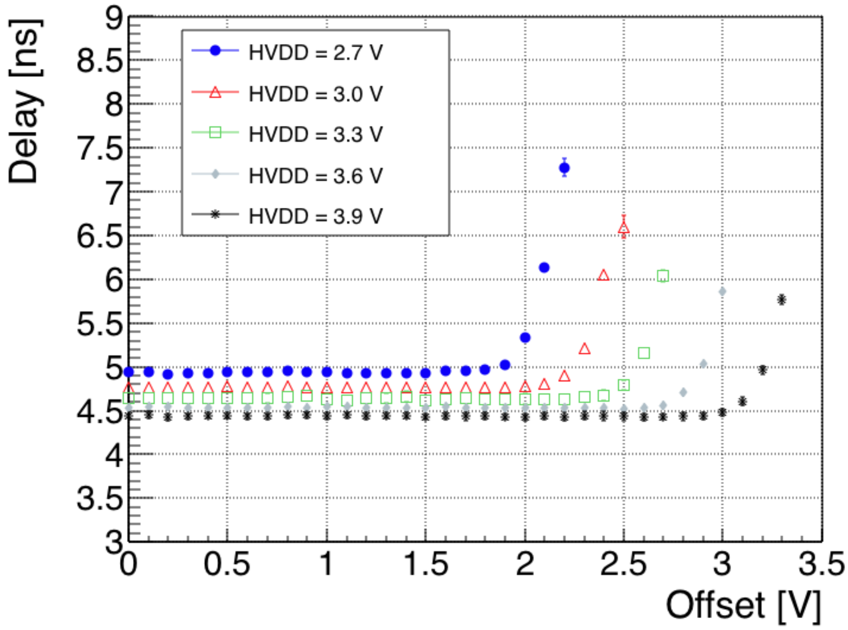


Figure 5 Propagation delay depending on offset voltage for power supplies of 2.7-3.9 V.

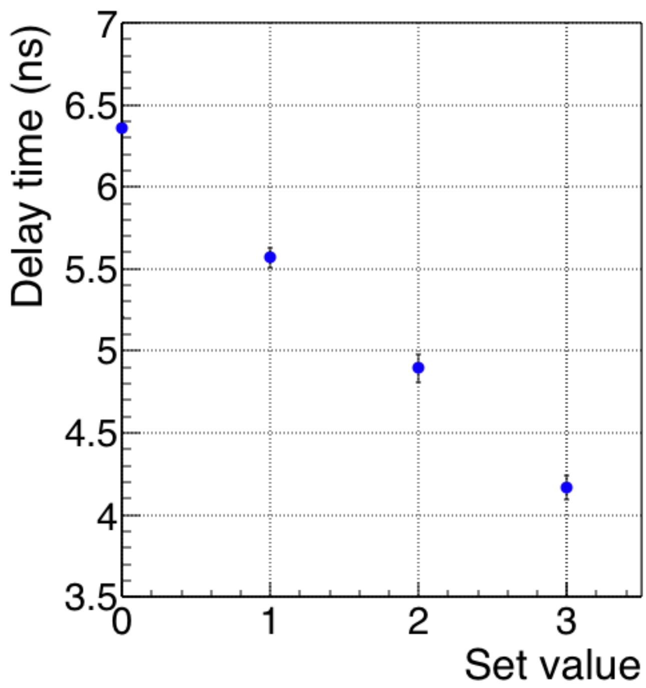


Figure 6 Propagation delay depending on the set value for bias current control. The offset voltage is set to 1.2 V, and the amplitude 400 mV.

4. Variable Delay

Variable delay circuit with a precision of sub-nanosecond is implemented with a PLL technique for stable delay against changes of operation conditions. Figure 7 shows a block diagram.

The PLL circuit consists of Voltage Controlled Ring Oscillator (VCRO), Phase Frequency Detector (PFD), Charge Pump (CP), and low-pass filter circuits. The VCRO is formed with 32 stages of delay units and a buffer gate. A selector is incorporated in the VCRO in order to change the number of the delay units in the ring (20, 24, 28, or 32). The selector can adapt fluctuation of the IC production process, and also can change the dynamic range of the variable delay. Each delay unit contains two inverter gates. The propagation delay of a delay unit is controlled by the control voltage (V_{CON}, which is separated to V_{C_N} and V_{C_P}). Since the signal passing through the ring is inverted by an extra inverter gate after MUX (see Figure 7), the ring works as an oscillator. When a signal takes 25 ns for a round of the ring, the frequency of the VCRO is 20 MHz. The PFD compares the output from the VCRO with a reference clock. When the phase of the VCRO clock is going forward (backward) against the reference clock, the CP decreases (increases) the voltage of V_{CON}. This loop works as negative feedback and stabilizes the frequency of the VCRO. The negative feedback circuit stabilizes the propagation delay for a round of the ring at 25 ns when a reference clock of 40 MHz is used.

The schematics of the delay unit, PFD, CP, and the low-pass filter are shown in Figure 8. The capacitor of the low-pass filter is implemented outside the chip. In the operation, we will use a 150 pF capacitor. The same design is used for the delay units in PLL and variable delay. The control voltage V_{CON} is common for the delay units in PLL and variable delay. As far as the PLL circuit is in the locked state and all the delay units behave equally, the propagation delay of the variable delay is kept constant against any changes of the operation conditions (e.g. supply voltage, temperature). One can set the signal delay of the variable delay in accordance with 6-bit register controlled via SPI.

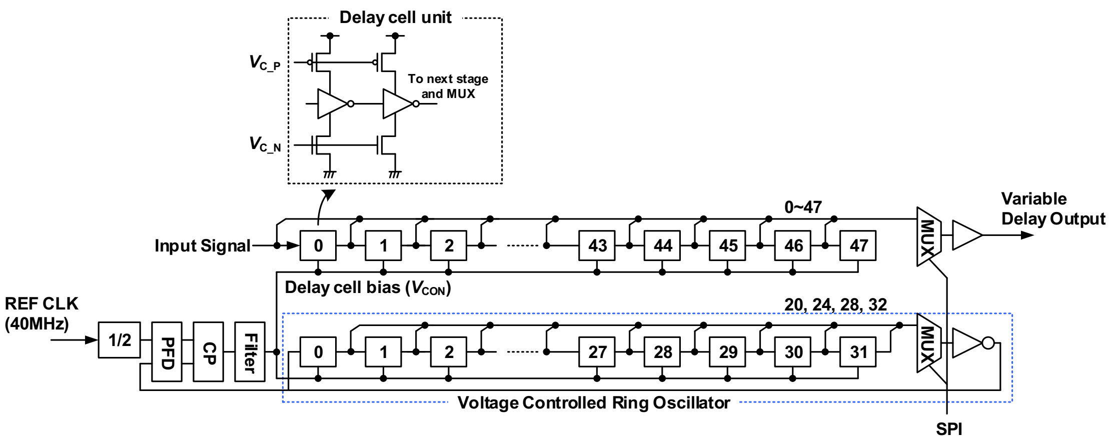
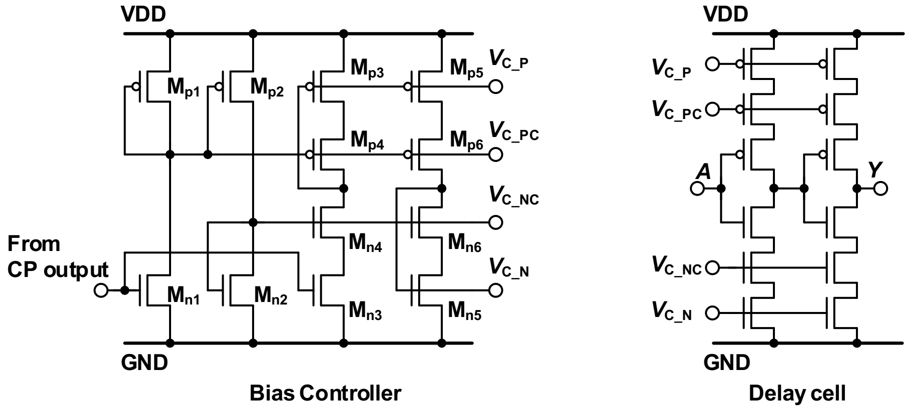
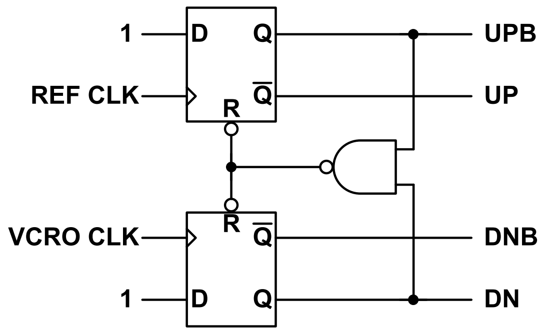


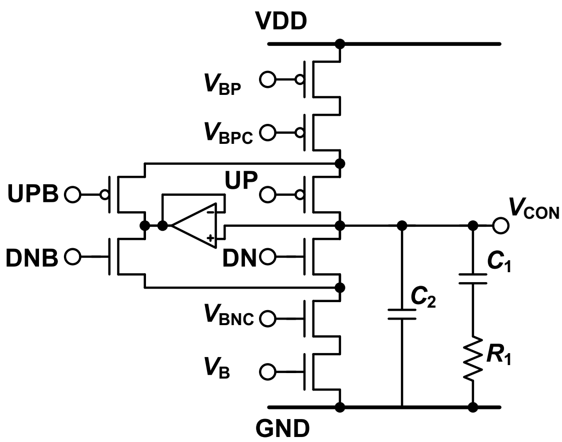
Figure 7 Block diagram of PLL and variable delay.



(a) Block diagram of bias controller (left) and delay unit (right).



(b) Block diagram of PFD.



(c) Block diagram of CP and low-pass filter.

Figure 8 Schematics of delay unit, phase detector, charge pump, and low-pass filter.

We measured the propagation delay of the signal that passes through a delay unit as a function of V_{CON}. Figure 9 shows the result of the measurement for ambient temperatures of 0, 20, 40, 60, and 80 degrees. Sub-nanosecond delay is achieved in all temperature values.

Figure 10 shows the measurement of the delay as well as the simulation with Layout Parasitic Extraction (LPE). The result agrees with the LPE simulation. From a view point of Process-Voltage-Temperature (PVT) variation, the prototype v.0 may not have enough margin in case of the number of the delay units in the VCRO ("PLL STEP") is 32. Therefore, the propagation delay is reduced by changing the gate length of transistors in the delay units for next version (v.1). The expected minimum propagation delay for prototype v.1 is 0.45 ns in a typical condition. Figure 11 shows corner simulation of the propagation time of a delay unit for prototype v.1. The LPE simulation shows that all conditions cover PLL STEP = 20-32. PLL STEP of 24 or 28 is assumed for the actual operation. PLL STEPs 20 and 32 provide margin.

Figure 12 shows the measured delay of the variable delay depending on the number of delay units for a reference clock of 40 MHz. By changing PLL STEP, we can change the dynamic range and the resolution of the variable delay. The resolutions of the variable delay are 0.73 ns, 0.82 ns, 0.96 ns, and 1.15 ns for PLL STEPs 32, 28, 24, and 20, respectively. The dynamic range is derived by multiplying the resolution by 47 (the maximum of the six bit). The results indicate that the variable delay can have a dynamic range of 40 ns with a resolution of sub-nanosecond. Figure 13 shows the measured delay depending on the supply voltage. The delay dependence on the supply voltage is small (< 0.3 ns). The dependence on ambient temperature is small (Figure 14).

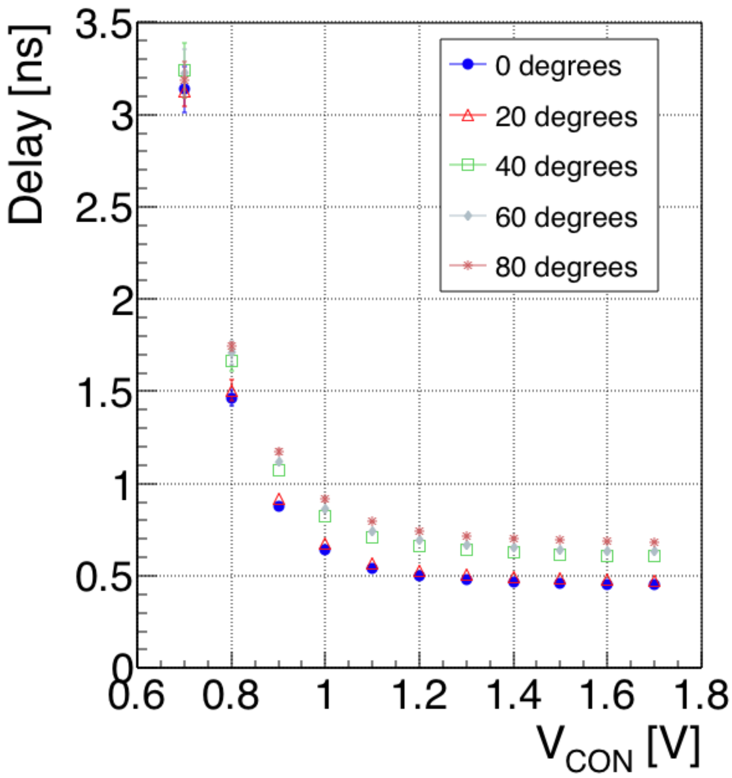


Figure 9 Measured propagation delay of a delay unit as a function of V_{CON}. The delay for ambient temperatures of 0, 20, 40, 60, and 80 degrees is shown. Sub-nanosecond delay is covered for all temperatures.

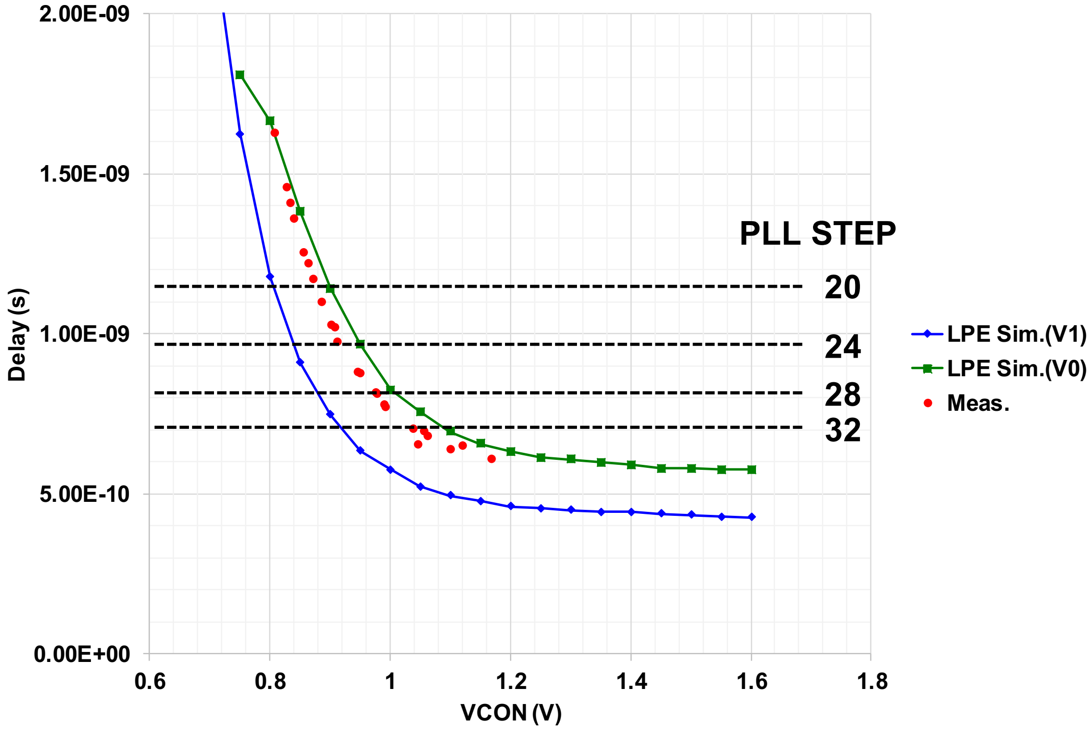


Figure 10 Propagation delay for a delay unit as a function of V_{CON}. The measurement for prototype v.0 (red) and LPE simulation for prototype v.0 (green) and v.1 (blue) are shown.

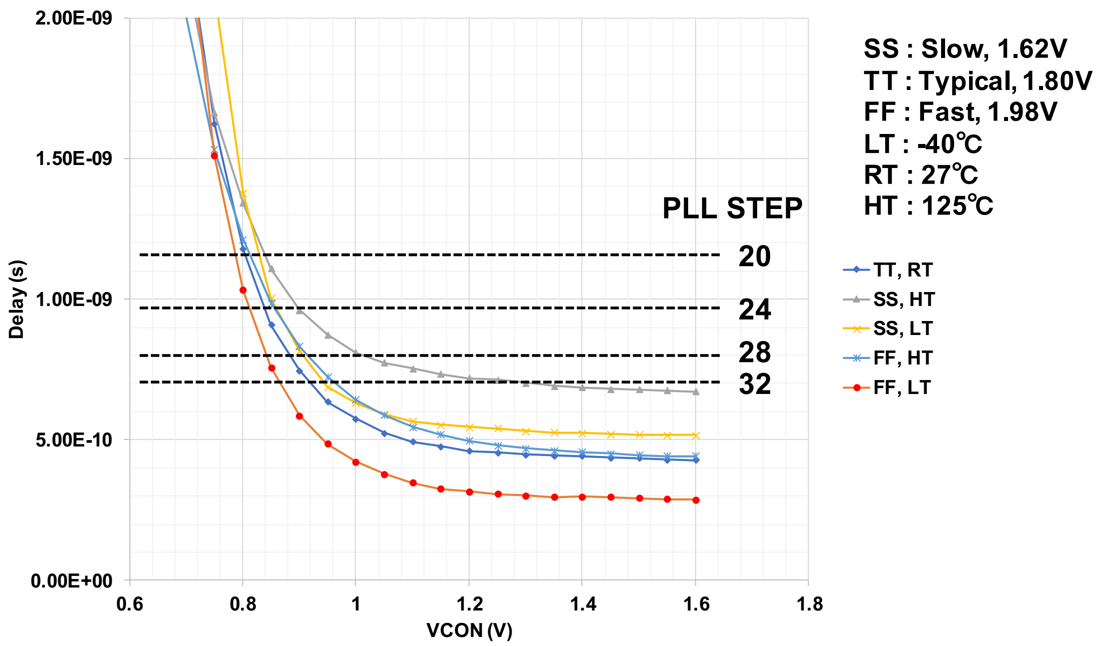


Figure 11 LPE simulation for the propagation delay of a delay unit for prototype v.1.

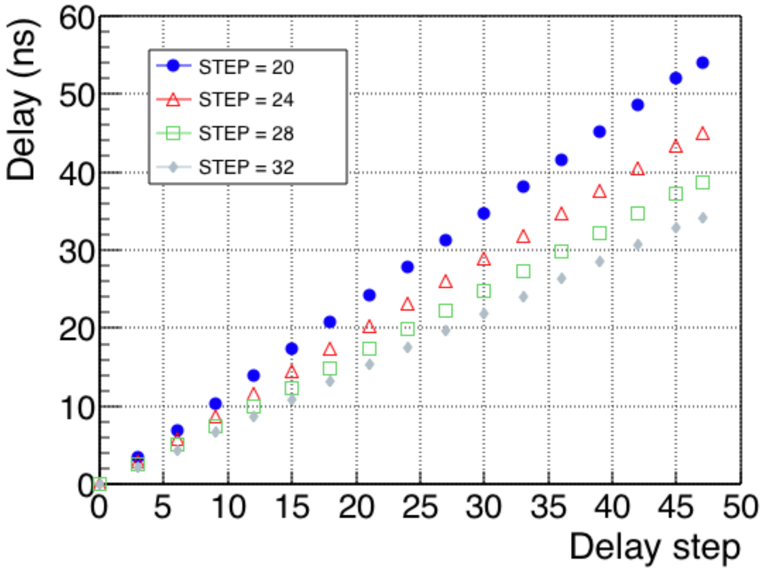


Figure 12 The measured propagation delay of the variable delay depending on the number of delay units ("delay step"). The results are shown for PLL STEPs 20, 24, 28, and 32.

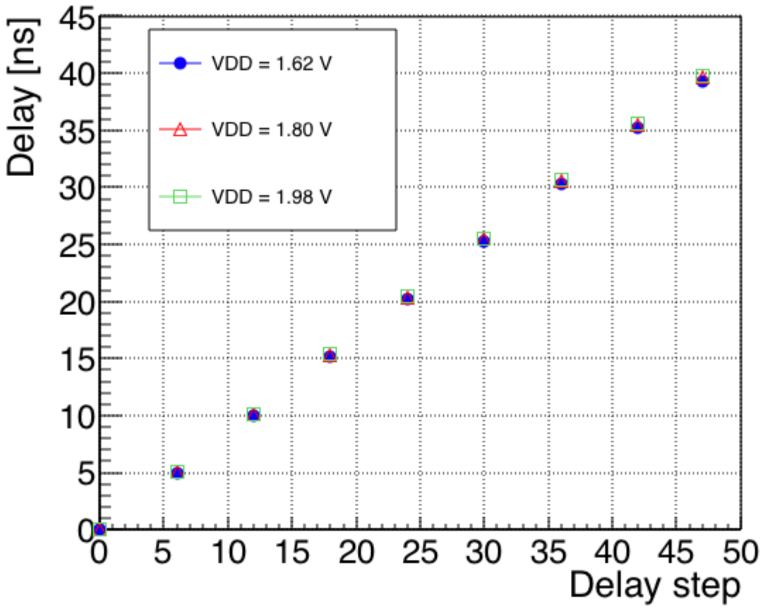


Figure 13 The measured propagation delay of the variable delay depending on the number of delay units ("delay step"). The results are shown for supply voltages 1.62 V, 1.80 V, and 1.98 V. The PLL STEP is set to 28.

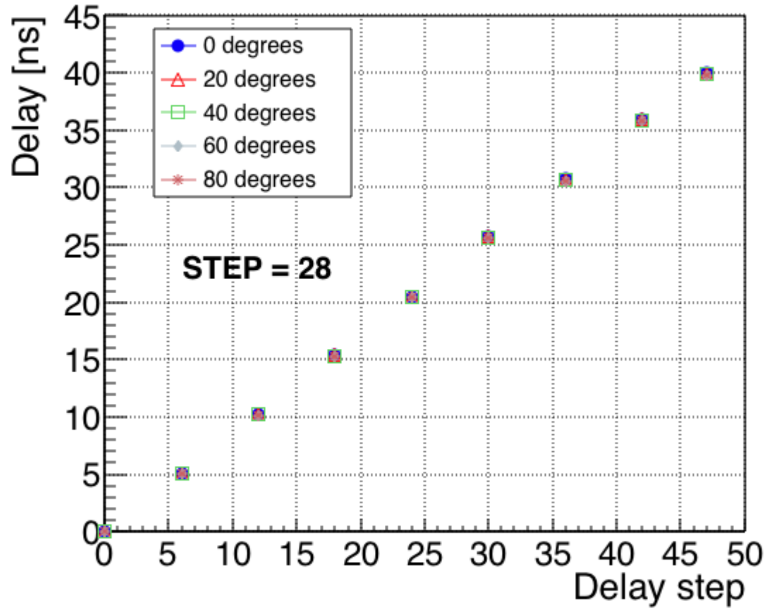


Figure 14 Temperature dependence of the variable delay. The PLL STEP is set to 28.

5. BCID

Figure 15 shows a block diagram of the BCID circuit. It contains two delayed clocks: BCID_Delay and BCID_Gate as shown in Figures 1 and 15. The BCID_Delay is used to adjust for the phase difference between the 40 MHz clock on the PS board and the earliest arrival times of signals from the ASD boards. The BCID_Gate is used to adjust the effective gate width. Set values for each delay are common to a group of 16-channel signals from an ASD board. The BCID circuit has a mask function, which can be set via SPI. Figure 16 shows the effective gate width of BCID circuit for a clock frequency of 40 MHz. The effective gate width was confirmed to cover a range from 26 ns to 49 ns. Figure 17 shows the BCID output for several set values of the BCID_Delay. Each signal has either one or two BCID outputs depending on the effective gate width. This function makes it possible to assign a hit to either one or two bunch crossings depending on the timing of the hit.

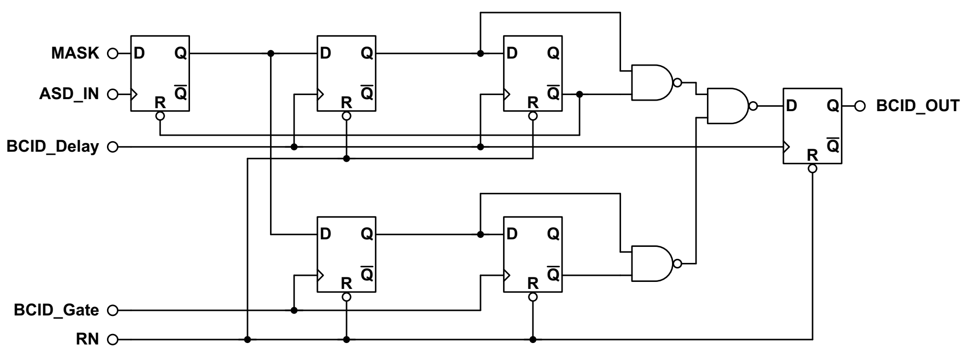
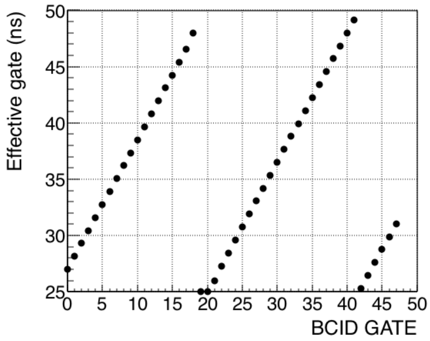
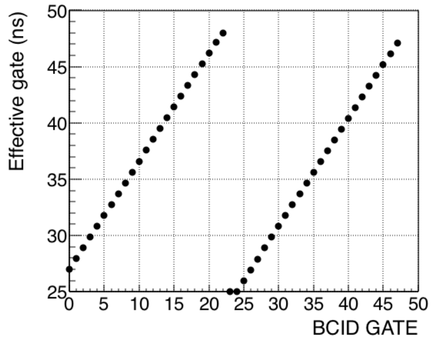


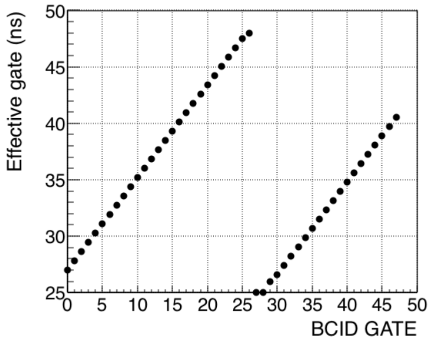
Figure 15 Block diagram of the BCID circuit.



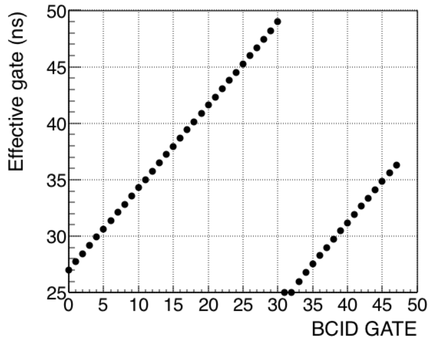
(a) PLL STEP = 20



(b) PLL STEP = 24



(c) PLL STEP = 28



(d) PLL STEP = 32

Figure 16 Effective gate width of BCID.

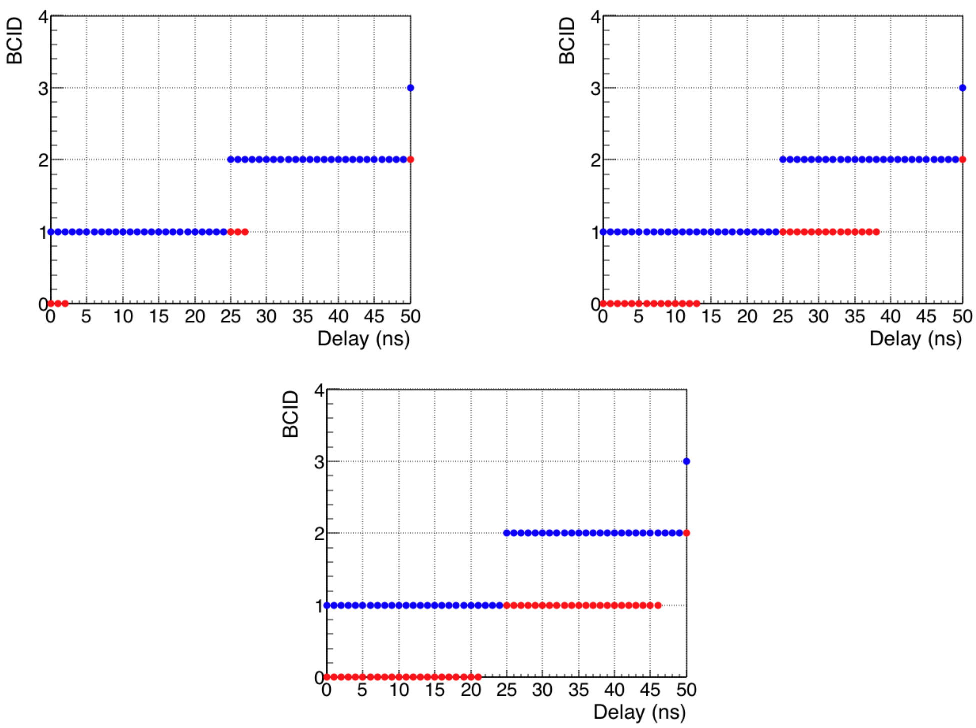


Figure 17 The measured BCID output for BCID_Delay values of 1 (top left), 15 (top right), and 26 (bottom). The horizontal axis shows the delay of input signal with respect to the 40 MHz clock, where the offset is subtracted. Each signal has either one or two BCID outputs depending on the effective gate width setting.

6. Test Pulse Generator

Figure 18 shows a schematic of the test pulse generator. When the ASIC receives a test pulse trigger signal, the test pulse generator outputs a differential square pulse with certain width, which is set via SPI in a range from 25 ns to 102.4 μs (12-bit control code, default = 10 μs). The amplitude setting is based on 4-bit register (0 to 15) controlled via SPI. The signal of POL defines the polarity of the test pulse. The test pulse trigger signal from outside of the ASIC can be taken with either a rising edge or a falling edge (programmable) of the 40 MHz clock in the ASIC. The delay of the test pulse after receiving a test pulse trigger signal can be programmed with a coarse delay (0 to 7 clocks) and a fine delay (0 ns to 40 ns in the case of PLL STEP = 28). Figure 19 shows a schematic of the output driver part. The amplitude versus the setting is shown in Figure 20, where the amplitude was measured with a load of 100 ohm and 8.0 pF for each output. The amplitude can be changed from 60 mV to 2.8 V. The amplitude used for daily calibration in Run 1 and Run 2 is ~300 mV. A similar value is assumed for Run 4 and the beyond. Figures 21 and 22 show the amplitude dependence on the ambient temperature and the supply voltage. The data indicate that the amplitude depends on supply voltage, while the dependence is safely small for the daily calibration. The coarse and fine delay control is shown in Figure 23.

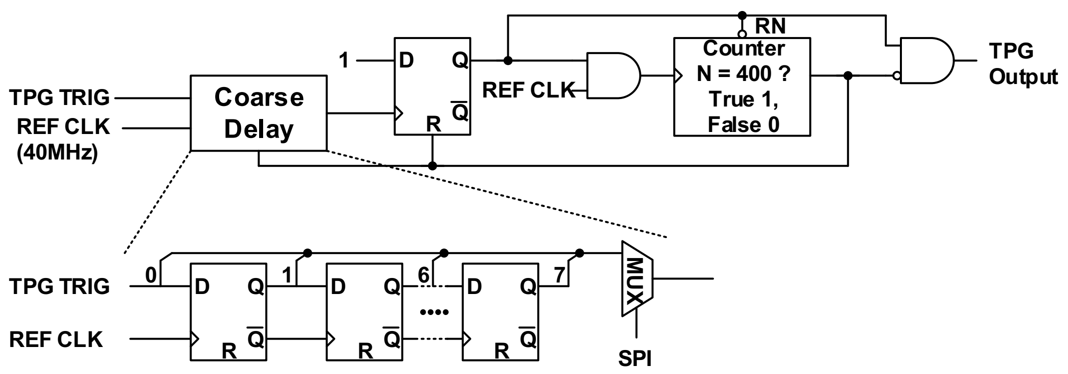


Figure 18 Schematic of the test pulse generator.

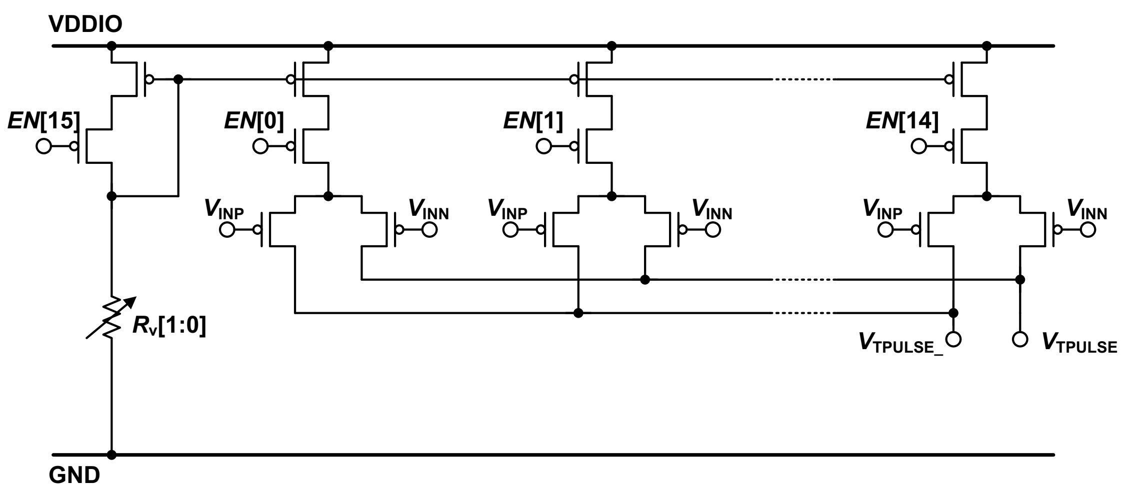


Figure 19 Schematic of the test pulse generator unit.

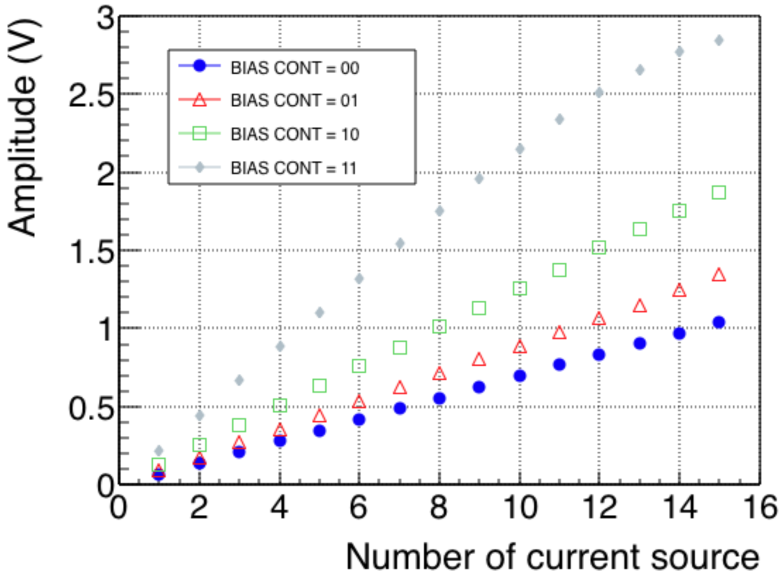


Figure 20 Amplitude of the differential output of the test pulse generator with 100 ohm load for each output pin. The values are shown for four bias control values.

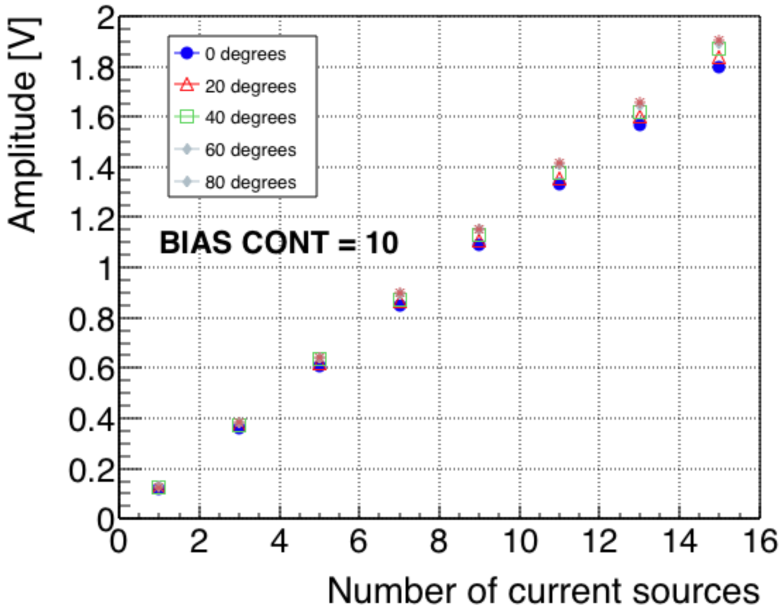


Figure 21 Amplitude of the test pulse generator depending on the number of current sources for various ambient temperature values.

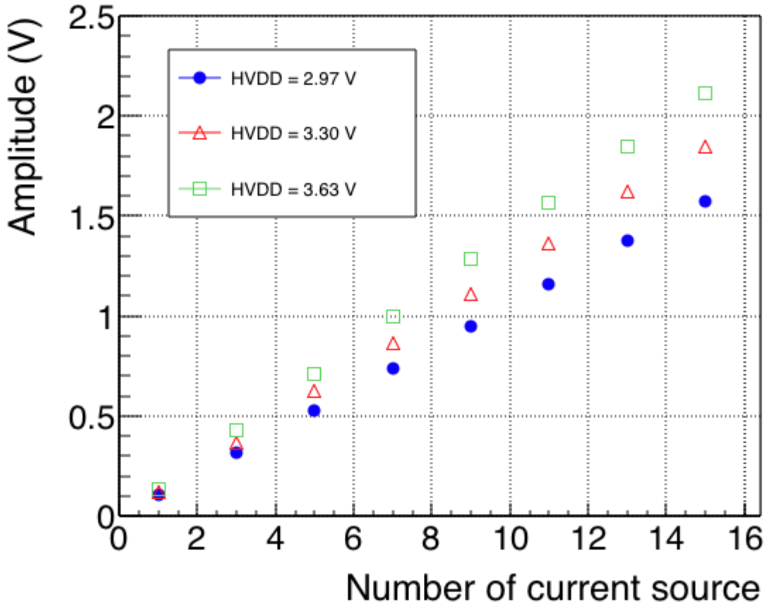
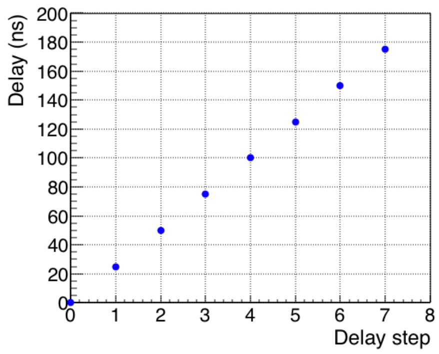
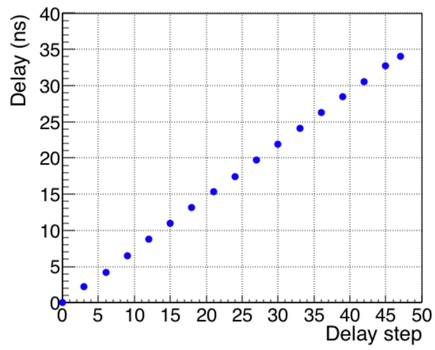


Figure 22 Amplitude of the test pulse generator depending on the number of current sources for supply voltages of 2.97 V, 3.30 V, and 3.63 V.



(a) Coarse delay control



(b) Fine delay control

Figure 23 Coarse and fine delay of the test pulse generator. PLL STEP is set to 32.

7. Power Consumption

The power consumption was measured as a function of the rate of input signals (Figure 24). The input signals are provided simultaneously to all of the 32 channels of a chip. A chip consumes ~20 mW under an expected hit rate of ~0.2 MHz per channel at a luminosity of 7.5 x 10^{34} $cm^{-2}s^{-1}$.

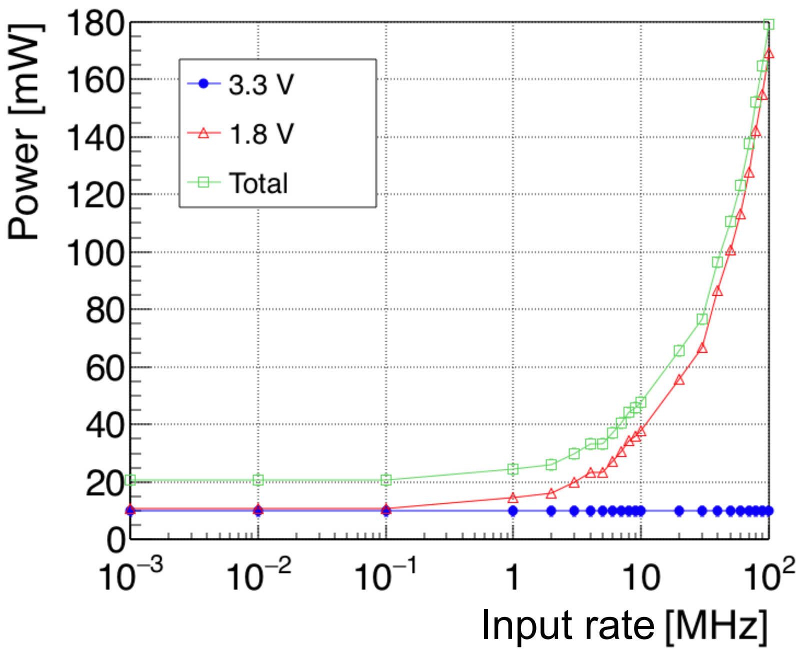


Figure 24 Power consumption as a function of the rate of input signal for each channel.

8. Yield

The yield has been studied by measuring the performance of prototype v.0 chips. In total 20 chips were produced, and 19 of them were measured. One chip was damaged before the measurement by a wrong setup of power supply outside the chip. For all channels of 19 chips, two sets of pulse input were provided: 10 kHz and 10 MHz. For all channels, output signals were observed. The power consumption for 10 kHz (10 MHz) input ranges from 17 mW to 21 mW (from 44 mW to 51 mW) depending on the chips. Although the measurements performed for all chips were limited, the results indicate that the 19 chips have no significant failures.

9. Signal I/O Definition

The assignment of the signals and pins are summarized in Figure 25 and Table 1.

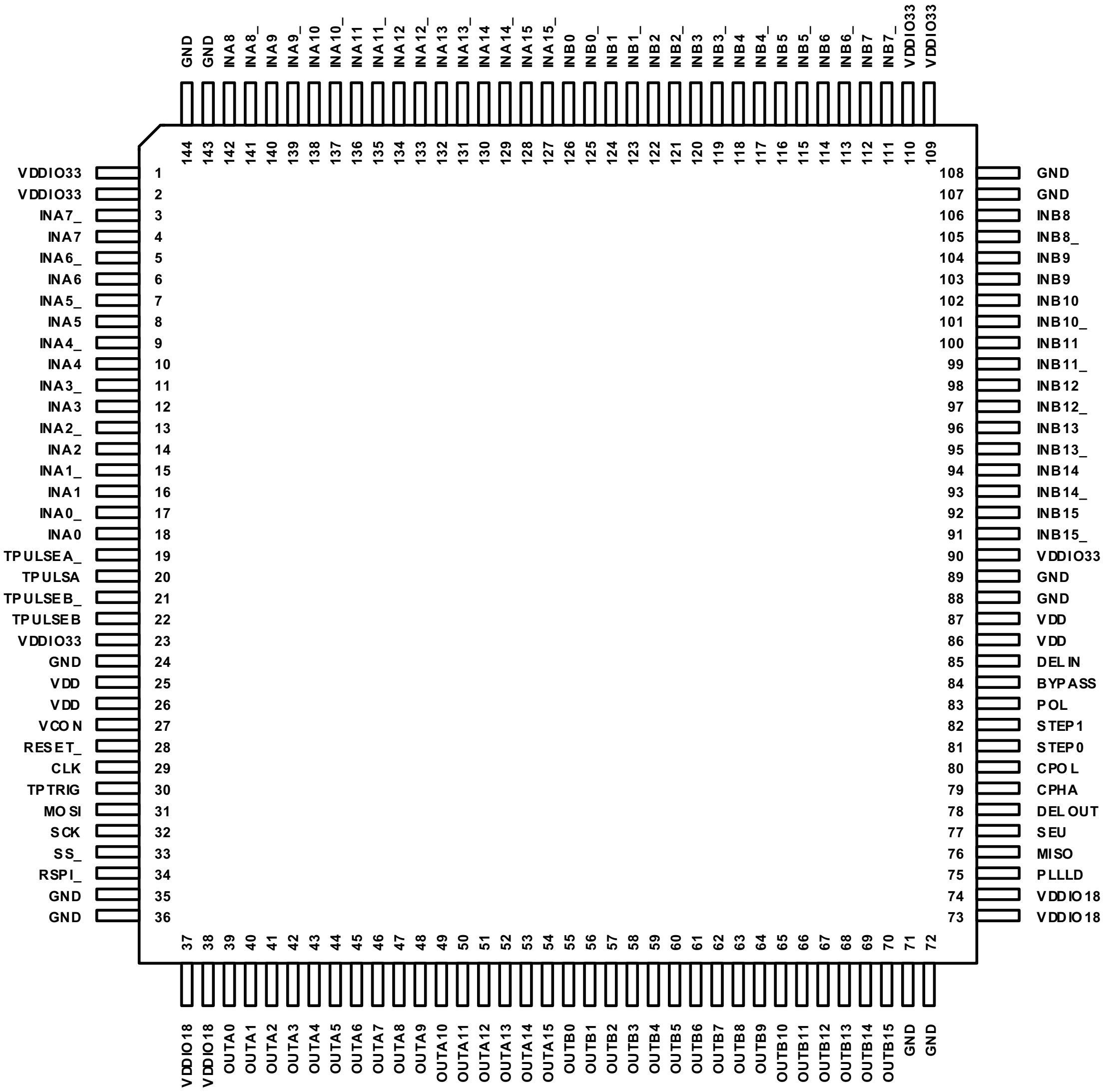


Figure 25 Pin assignment of the Patch-Panel ASIC.

Table 1 Signal I/O definition of Patch-Panel ASIC.

Name	Pin	Type	Signal
Port-A			
INA0 INA 0_ INA1 INA1_ INA2 INA2_ INA3 INA3_ INA4 INA4_ INA5 INA5_ INA6 INA6_ INA7 INA7_ INA8 INA8_ INA9 INA9_ INA10 INA10_ INA11 INA11_ INA12 INA12_ INA13 INA13_ INA14 INA14_ INA15 INA15_	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 142 141 140 139 138 137 136 135 134 133 132 131 130 129 128 127	LVDS IN	**Raw LVDS Signals from an ASD Board:** 16-channel raw LVDS signals from an ASD Board are received by LVDS receivers and are converted to CMOS level. Further signal processing is decided by POL and BYPASS signals. Signal from anode: INA receives a positive logic signal (hit=H). INA_ receives a negative logic signal (hit=L). Signal from cathode: INA receives a negative logic signal (hit=L). INA_ received a positive logic signal (hit=H). POL = L Raw signals from anode wires. Output signals from LVDS receivers are not inverted. POL = H Raw signals from strips Output signals from LVDS receivers are inverted. BYPASS = L Signals are fad to variable delay circuits and then bunch-identification circuits. BYPASS = H Signals are fad to outputs as OUTA signals directly. Neither variable delay circuit nor bunch-identification circuit.
OUTA0 OUTA1 OUTA2 OUTA3 OUTA4 OUTA5 OUTA6 OUTA7 OUTA8 OUTA9 OUTA10 OUTA11 OUTA12 OUTA13 OUTA14	39 40 41 42 43 44 45 46 47 48 49 50 51 52 53	CMOS OUT	**Hit Signals:** 16-bit hit signals are output. Positive logic. BYPASS=L Bunch-identified hit signals are output. BYPASS=H Asynchronous hit signals are output.

OUTA15	54		
TPULSEA TPULSEA_	19 20	Open-Drain OUT	**Test Pulse Output Signal to an ASD Board:** Test pulse is output to an ASD Board. The signal is differential. The amplitude and the delay from TPTRG can be set via SPI. The pulse width is 3 μs (fixed value, to be defined). POL=L (anode) TPULSEA is a positive logic signal. TPULSEA_ is a negative logic signal. POL=H (cathode) TPULSEA is a negative logic signal. TPULSEA_ is a positive logic signal.
Port-B			
INB0 INB0_ INB1 INB1_ INB2 INB2_ INB3 INB3_ INB4 INB4_ INB5 INB5_ INB6 INB6_ INB7 INB7_ INB8 INB8_ INB9 INB9_ INB10 INB10_ INB11 INB11_ INB12 INB12_ INB13 INB13_ INB14 INB14_ INB15 INB15_	126 125 124 123 122 121 120 119 118 117 116 115 114 113 112 111 106 105 104 103 102 101 100 99 98 97 96 95 94 93 93 91	LVDS IN	**Raw LVDS Signals from an ASD Board:** 16-channel raw LVDS signals from an ASD Board are received by LVDS receivers and are converted to CMOS level. Further signal processing is decided by POL and BYPASS signals. Signal from anode: INB receives a positive logic signal (hit=H). INB_ receives a negative logic signal (hit=L). Signal from cathode: INB receives a negative logic signal (hit=L). INB_ received a positive logic signal (hit=H). POL = L Raw signals from anode wires. Output signals from LVDS receivers are not inverted. POL = H Raw signals from strips Output signals from LVDS receivers are inverted. BYPASS = L Signals are fad to variable delay circuits and then bunch-identification circuits. BYPASS = H Signals are fad to outputs as OUTA signals directly. Neither variable delay circuit nor bunch-identification circuit.
OUTB0 OUTB1 OUTB2 OUTB3 OUTB4	55 56 57 58 59	CMOS OUT	**Hit Signals:** 16-bit hit signals are output. Positive logic. BYPASS=L Bunch-identified hit signals are output.

OUTB5 OUTB6 OUTB7 OUTB8 OUTB9 OUTB10 OUTB11 OUTB12 OUTB13 OUTB14 OUTB15	60 61 62 63 64 65 66 67 68 69 70		BYPASS=H Asynchronous hit signals are output.
TPULSEB TPULSEB_	21 22	Open-Drain OUT	**Test Pulse Output Signal to an ASD Board:** Test pulse is output to a ASD Board. The signal is differential. The amplitude and the delay from TPTRG can be set via SPI. The pulse width is 3 μs (fixed value, to be defined). POL=L (anode) TPULSEA is a positive logic signal. TPULSEA_ is a negative logic signal. POL=H (cathode) TPULSEA is a negative logic signal. TPULSEA_ is a positive logic signal.
COMMON			
DELIN	85	CMOS IN	**Input Signal to Variable Delay:** The input signal is delayed in the Variable Delay circuit. The delay can be set via SPI.
DELOUT	78	CMOS OUT	**Output Signal from Variable Delay:** The delayed signal from the Variable Delay circuit. The delay can be set via SPI.
POL	83	CMOS IN	**Signal Polarity:** Polarity selection of raw input signals. POL = L Raw LVDS signals from a wire ASD Board. POL = H Raw LVDS signals from a strip ASD Board.
BYPASS	84	CMOS IN	**Bypass of Variable Delay and BCID:** Selection of bunch-identification mode or bypass mode. BYPASS = L Signals are fad to variable delay circuits and then bunch-identification circuits. BYPASS = H Signals are fad to outputs as OUTA signals directly. Neither variable delay circuit nor bunch-identification circuit.
CLK	29	CMOS IN	**System Clock:** 40 MHz system clock from TTC Rx.
TPTRIG	30	CMOS IN	**Test Pulse Trigger:** Test pulse trigger signal from TTC Rx. Positive logic. The signal is taken at a rising edge of CLK.

SEU	77	CMOS OUT	**Single Event Upset signal:** Single event upset is detected in SPI registers. SEU = H : SEU is detected. SEU = L : SEU is not detected.
RESET_	28	CMOS IN	**System Reset:** System Reset signal from TTC Rx. Negative logic. The signal sets all registers defaults.
PLL			
PLLLD	75	CMOS OUT	**PLL Lock status:** PLL lock detection signal PLLLD=L Unlocked. PLLLD=H Locked.
STEP0 STEP1	81 82	CMOS IN	**PLL Depth:** Setting of the number of delay units in the ring oscillator of the PLL STEP=0: 32 STEP=1: 28 STEP=2: 24 STEP=3: 20
VCON	25		**Control Voltage:** DC voltage to control delay units. An R/C network for the low pass filter shall be connected to the pin.
SPI			
MOSI	28	CMOS IN	**Master Out Slave In:** Input Data signal of SPI.
SS_	30	CMOS IN	**Slave Select:** Slave Select signal of SPI.
SCK	29	CMOS IN	**Serial ClocK:** Serial Clock signal of SPI.
MISO	76	CMOS OUT	**Master In Slave Out:** Output data signal of SPI.
CPOL CPHA	80 79	CMOS IN	**Configuration signals of SPI:** Polarity and edge selection of SCK. See Appendix 1.
RSPI_	34	CMOS IN	**SPI Reset:** SPI reset. Negative logic. The signal sets all registers defaults (See section 9).
POWER			
GND	24 35 36 71 72 88 89 107 108 143 144		**Ground:** 0 volts.
VDD	25 26 86 87		**Power:** 1.8 volts for core circuits.
VDDIO33	1 2 23 90 109 110		**Power:** 3.3 volts for IO circuits.

VDDIO18	37 38 73 74		**Power:** 1.8 volts for IO circuits.

10. Control

Most of the control are based on SPI protocol. The instruction is given in Table 2. A Patch-Panel ASIC covers two 16-channel ASD boards (Channels A and B), and one can set parameters for each part independently. The voting logic is introduced to the data registers in order to cope with the radiation immunity against single event upset. Figure 26 shows the data input order of SPI. Figure 27 shows basic information of the SPI protocol.

Table 2 Patch-Panel ASIC SPI Instructions

(a) Channel A and B (12 byte / each)

Name	# of bit	Initial condition	Function	Remarks	Address
DL_POL	16	ALL 0	Delay line polarity control 0:non-inverted, 1:inverted	External cotrol pin can be used. Default:External	<15:0>
DL_BYPASS	16	ALL 1	Delay line bypass control 0:non-bypass, 1:bypass	External cotrol pin can be used. Default:External	<31:16>
DL_MASK	16	ALL 1	Delay line mask control 0:masked, 1:non-masked		<47:32>
DL_DLY_CONT	6	101111	Delay line delay control 000000 (min)-101111 (max)	1ns step (PLL dependent)	<53:48>
TEST_POL	1	0	Test input polarity control 0:non-inverted, 1:inverted	External cotrol pin can be used. Default:External	<54>
TEST_DLY_CONT	6	101111	Test input delay control 000000 (min)-101111 (max)	1ns step (PLL dependent)	<60:55>
TPG_POL_IN	1	0	TPG TRIG edge control 0:rising edge, 1:falling edge		<61>
TPG_POL_OUT	1	0	TPG output polarity control 0:positive, 1:negative		<62>
TPG_DLY_CONT_C	3	111	TPG coarse delay control 000 (min)-111 (max)	1 CLK step (25ns)	<65:63>
TPG_DLY_CONT_F	6	101111	TPG fine delay control 000000 (min)-101111 (max)	1ns step (PLL dependent)	<71:66>
TPG_PW_CONT	12	000110010000	TPG pulse width control ALL0 (min)-ALL1 (max)	1 CLK step (25ns) Initial: 10us	<83:72>
BCID_DLY_CONT	6	000000	BCID delay control 000000 (min)-101111 (max)	1ns step (PLL dependent)	<89:84>
BCID_GATE_CONT	6	000000	BCID gate control 000000 (min)-101111 (max)	1ns step (PLL dependent)	<95:90>

(b) PLL (1 byte)

Name	# of bit	Initial condition	Function	Remarks	Address
PLL_DLY_CONT	5	11111	PLL delay line control 00000 (min)-11111 (max)	11111 (32), 11011 (28) 10111 (24), 10011 (20)	<4:0>
PLL_CP_CONT	2	01	CP bias current control 00 (min)-11 (max)		<6:5>
PLL_CP_ON	1	1	CP Enable 1:Enable, 0:Disable	In case of 0, VCON is floating.	<7>

(c) Common (3 byte)

Name	# of bit	Initial condition	Function	Remarks	Address
PLL_DLY_SEL	1	1	PLL delay line control code EXT (1)/INT (0) select		<0>
DL_POL_SEL	1	1	Delay line polarity control EXT (1)/INT (0) select		<1>
DL_BYPASS_SEL	1	1	Delay line polarity control EXT (1)/INT (0) select		<2>
TPG_DRV_CONT_A	4	0000	TPG_A Drivability control 0000 (min)-1111 (max)	0000:TPG Driver is disabled	<6:3>
TPG_DRV_CONT_B	4	0000	TPG_B Drivability control 0000 (min)-1111 (max)	0000:TPG Driver is disabled	<10:7>
TPG_BIAS_CONT	2	00	TPG Bias current control 00 (min)-11 (max)	0.5, 0.75, 1.0, 2.0	<12:11>
TPG_BIAS_ENB	1	0	TPG Bias Enable 0:Bias Enable 1:Disable		<13>
RX_BIAS_CONT	2	10	LVDS (Rx) Bias current control 00 (min)-11 (max)	0.5, 0.75, 1.0, 2.0	<15:14>
CMOS_OUT_CONT	2	01	CMOS Drivability control 00 (min)-11 (max)	0.5, 1.0, 1.5, 2.0	<17:16>
NC	6	000000	Non-connect	reserve	<23:18>

- Circuit order
  - Common→PLL→Channel A→Channel B
- Data input order
  - Channel B→Channel A→PLL→Common, MSB First

Ex.) For PLL

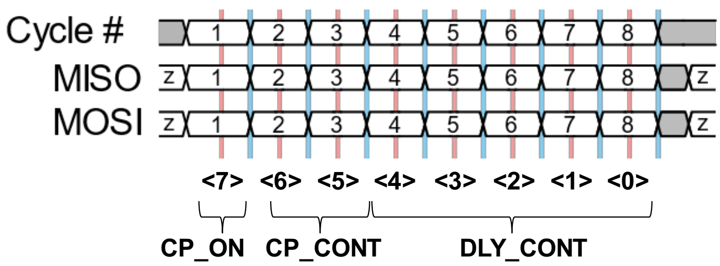


Figure 26 SPI data input order.

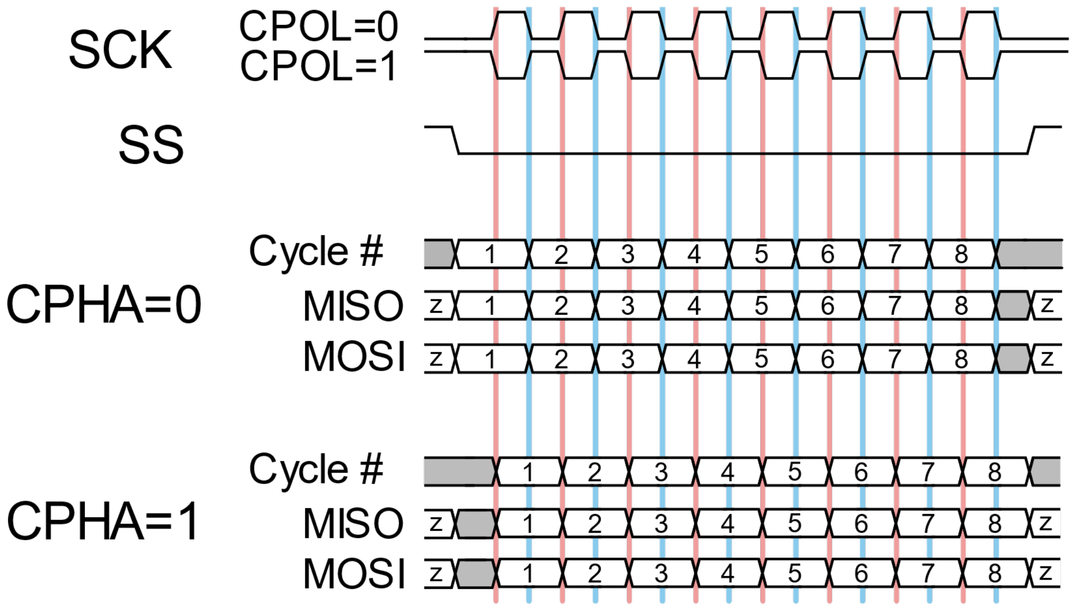


Figure 27 SPI mode and timing chart taken from Wikipedia (https://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus).

11. Radiation Tolerance for Total Ionizing Dose

The Patch-Panel ASIC produced for the ATLAS experiment at HL-LHC shall have the radiation tolerance sufficient for the use in the experimental cavern during the whole duration of the machine operation. The requirement on the total ionizing dose is 27 Gy. This value is obtained from a product of the simulated radiation level (6 Gy) and the safety factor (4.5). The radiation level has been simulated with FLUGG for an integrated luminosity of 4000 fb^{-1}. The value for a radial coordinate of 8 m, the innermost region of the Patch-Panel ASIC location, has been extracted. The safety factor is obtained from a product of the safety factor for the simulation uncertainty (1.5), the safety factor for the difference in the dose rate between the test and the actual experiment (1.5), and the safety factor for the variations of radiation tolerance from lot to lot and within lots (2).

Three prototype chips of the Patch-Panel ASIC produced in 2018 were irradiated, and no degradation of the performance was observed. The test was performed at the Cobalt-60 facility of Nagoya University in Japan. The three chips were irradiated up to 1 kGy. One chip among the three was further irradiated up to 10 kGy. The dose rate was 8.2 Gy/min. Figures 28-30 show the test results for PLL and variable-delay blocks. No significant change was observed in the relations between the control voltage and the delay. The frequency of the reference clock for which PLL is locked ranges from 28-31 MHz to 57-58 MHz. This range covers the frequency for the actual operation 40 MHz with margin. Figure 31 shows the test result for the test pulse generator. The linearity was unchanged by the irradiation. Figure 32 shows the power consumption depending on the dose. No significant increase was observed. For all tests, no failure was observed in the chip control with SPI.

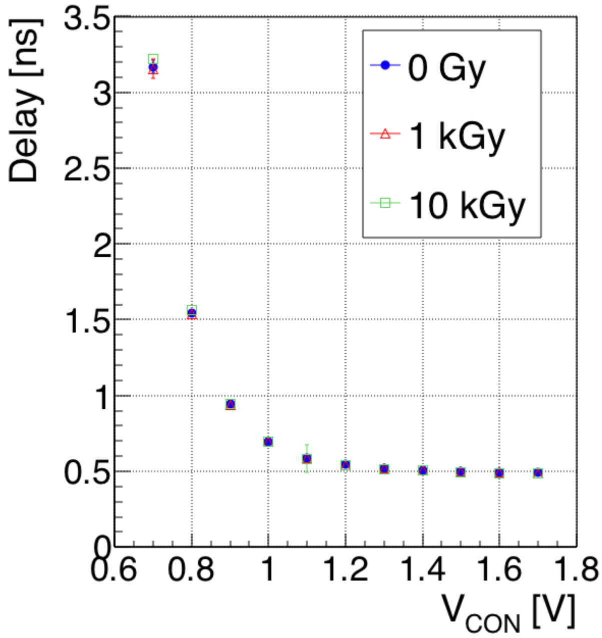


Figure 28 Relation between the control voltage V_{CON} and the measured delay of a delay unit for total ionizing doses of 0 Gy, 1 kGy, and 10 kGy. The result is shown for one prototype chip.

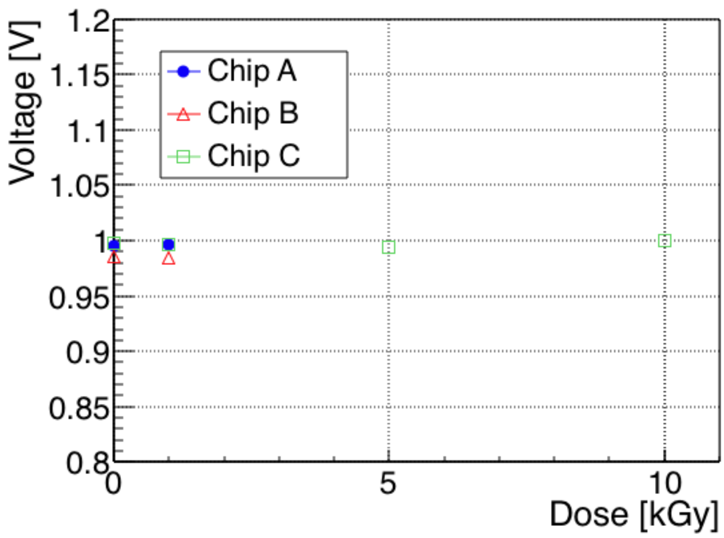


Figure 29 The control voltage V_{CON} for the PLL circuit locked with a reference clock of 40 MHz depending on the ionizing dose. The result is shown for three prototype chips. One of them is irradiated up to 10 kGy, while the other two up to 1 kGy.

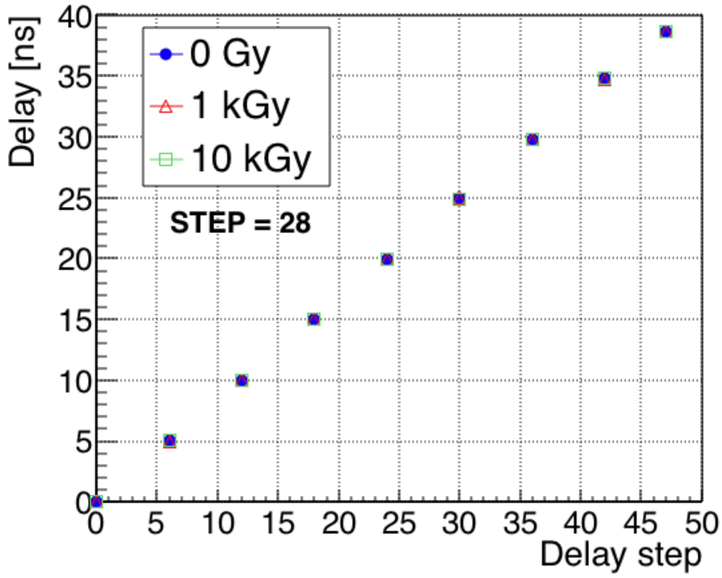


Figure 30 Relation between the setup of the number of delay units ("delay step") and the measured delay of the variable delay for total ionizing doses of 0 Gy, 1 kGy, and 10 kGy. The result is shown for one prototype chip.

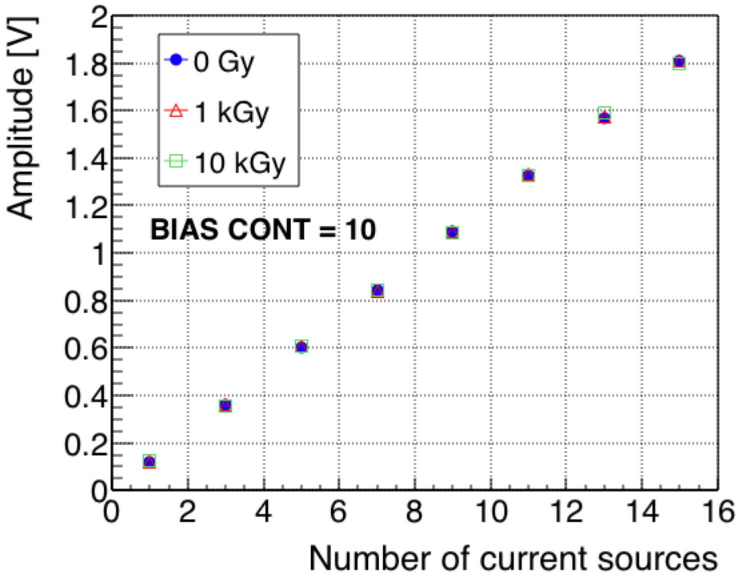


Figure 31 The amplitude of the test pulse generator output depending on the number of current sources for total ionizing doses of 0 Gy, 1 kGy, and 10 kGy. The result is shown for one prototype chip.

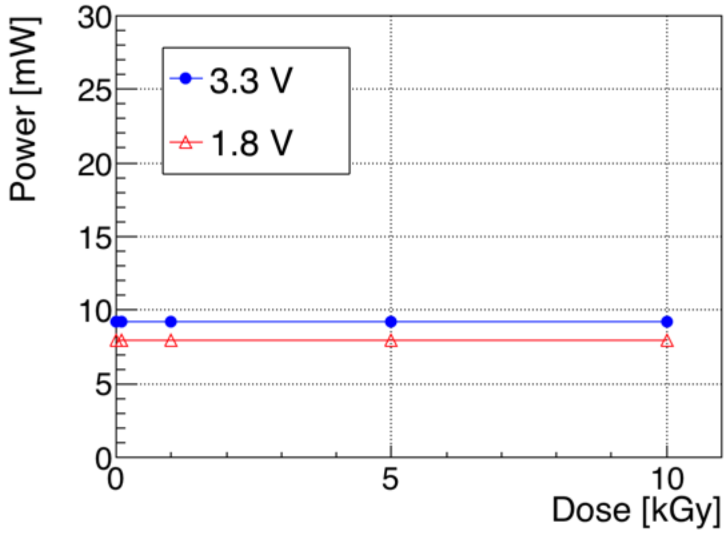


Figure 32 The power consumption depending on the ionizing dose. The result is shown for one prototype chip.

12. Radiation Tolerance for Single Event Effect and Non-Ionizing Energy Loss

The Patch-Panel ASICs have voting logic for the registers as described in Section 10, and would have a high tolerance to the single event effect. We plan a neutron irradiation test in March 2019 for confirmation. The tolerance to non-ionizing energy loss will also be checked with neutron.