アトラス前後方ミューオン トリガーシステムアップグレードのためのエレクトロニクス開発

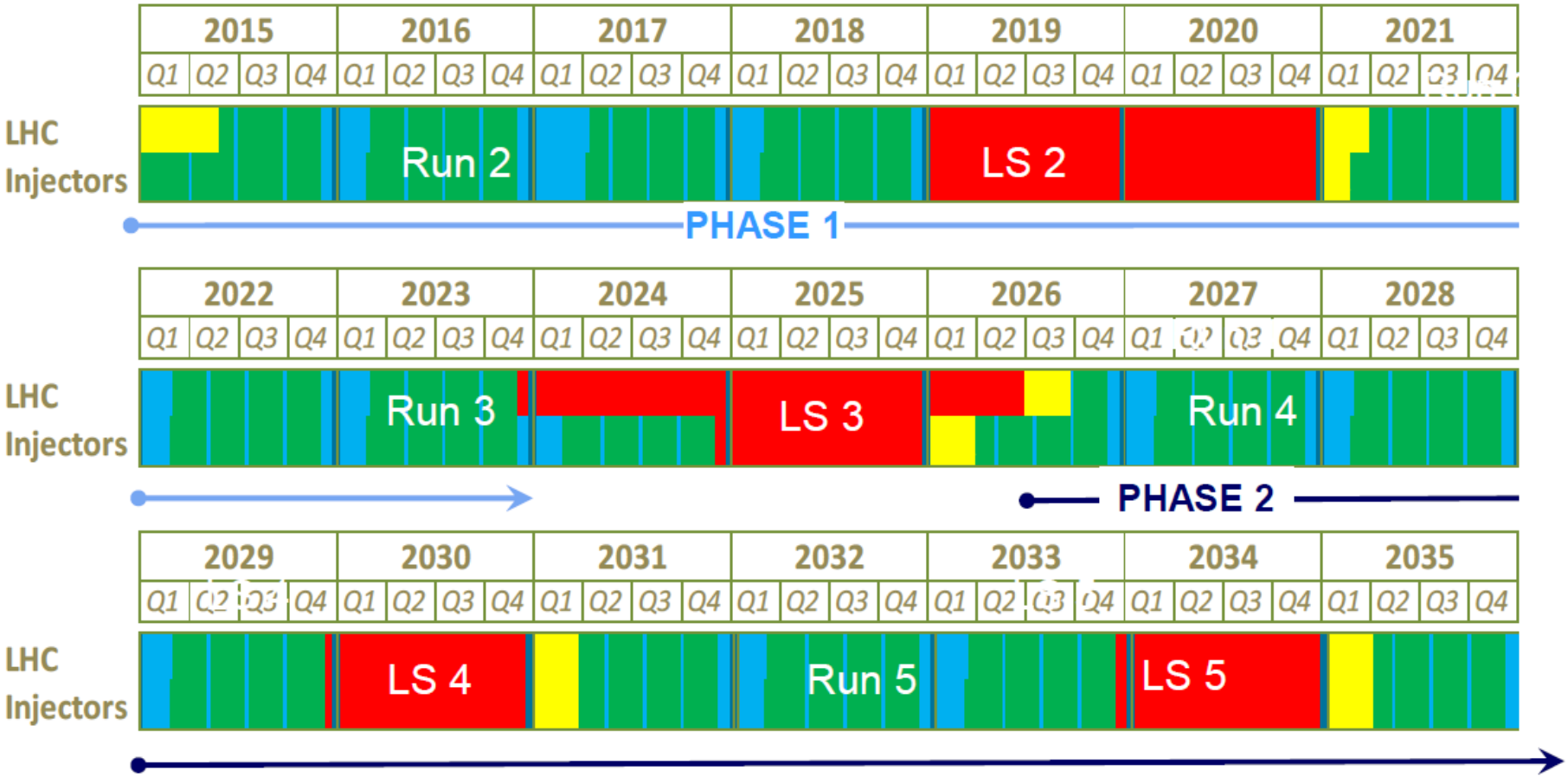
東京大学素粒子物理国際研究センター
坂本　宏

目次

- ATLASアップグレードスケジュール
- フェーズ0アップグレード
- フェーズ1アップグレード
- フェーズ2アップグレード
- 関連するOpenItプロジェクト
- 今後の開発方針～特にフェーズ2に向けて

LHC roadmap: according to MTP 2016-2020 V1

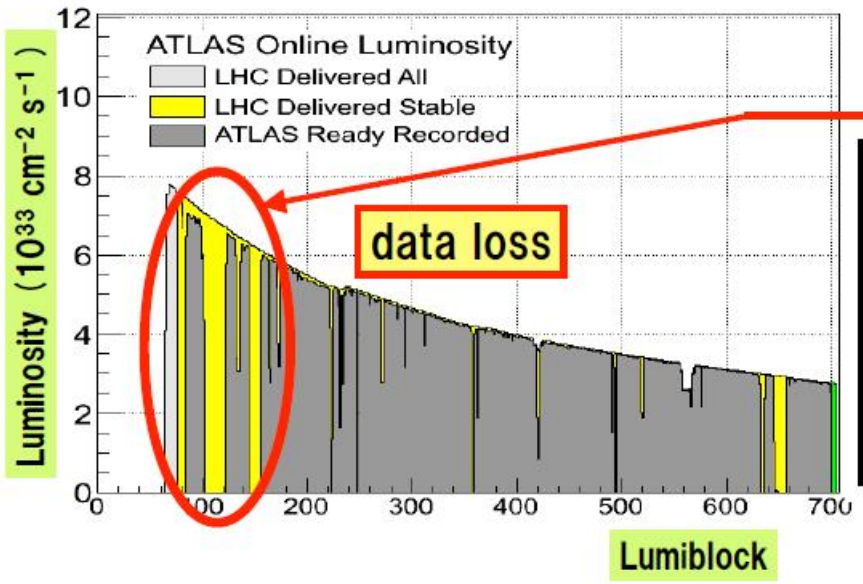
LS2 starting in 2019 => 24 months + 3 months BC
LS3 LHC: starting in 2024 => 30 months + 3 months BC
Injectors: in 2025 => 13 months + 3 months BC



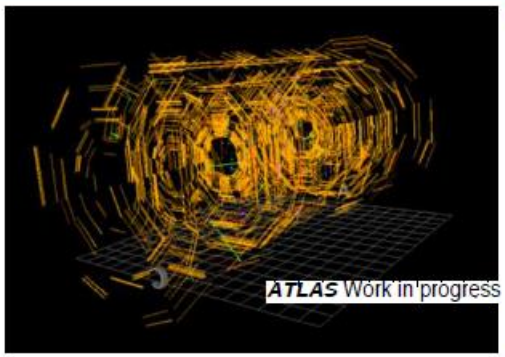
Phase 0 Upgrade

- Long Shutdown 1 (LS1)
  - 2013~2014
- Consolidation of the Trigger System
  - Include EI/FI
  - CALO-MU Coincidense
  - Burst Stopper

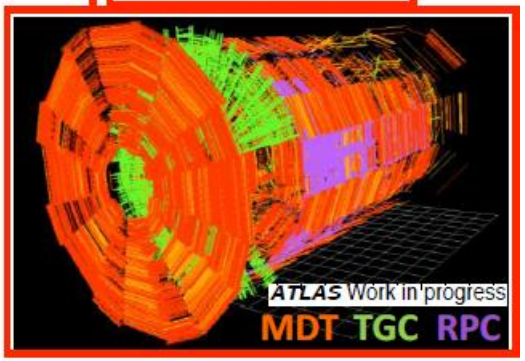
Burst stopper logic in Sector Logic



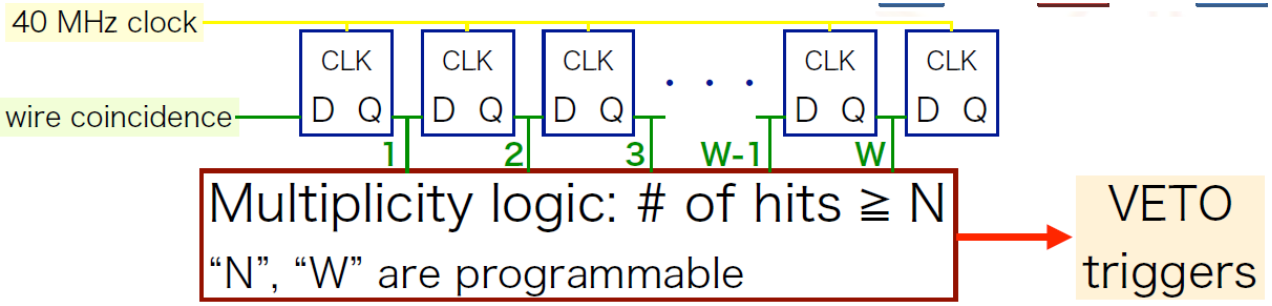
x100 hits
~μs



Normal event

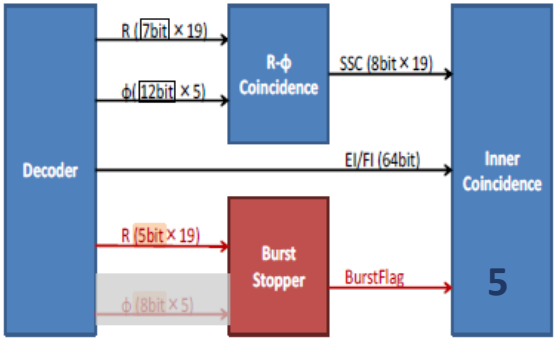


Burst event



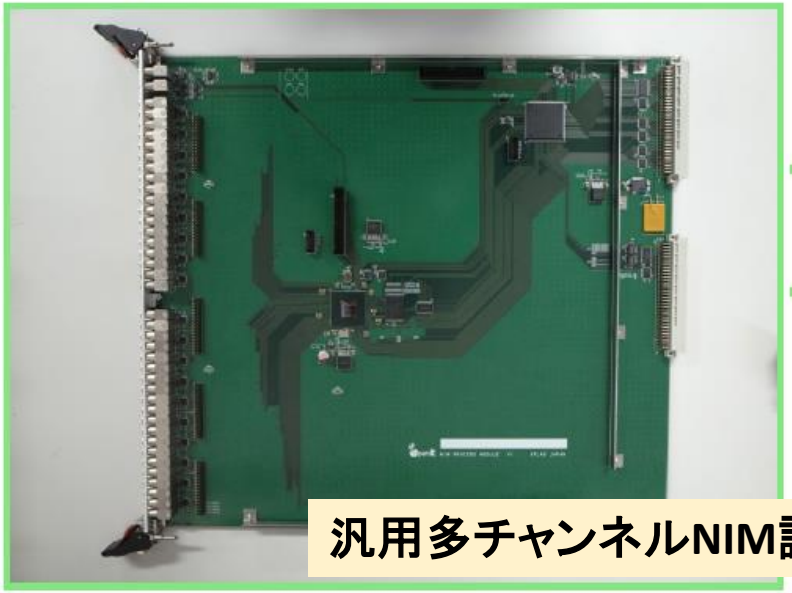
Multiplicity logic: # of hits ≧ N
"N", "W" are programmable

VETO triggers

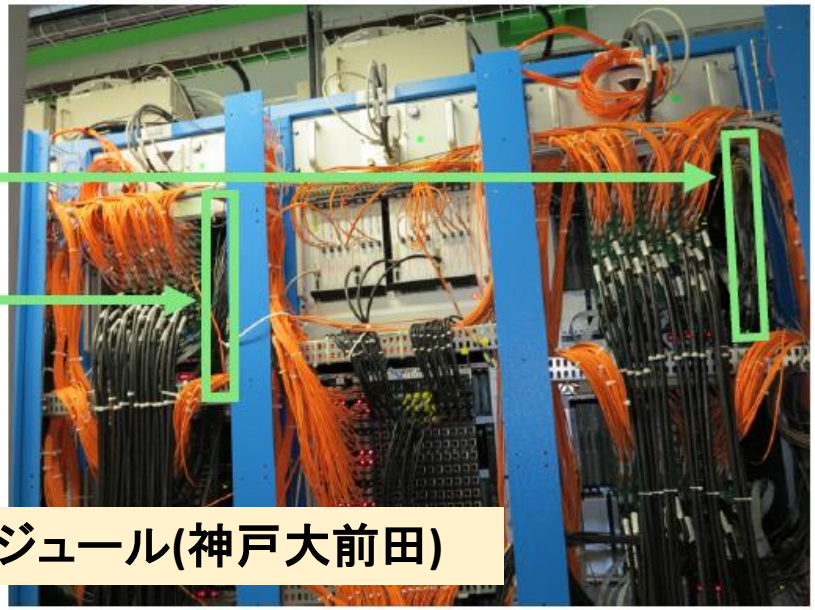


Burst stopper module

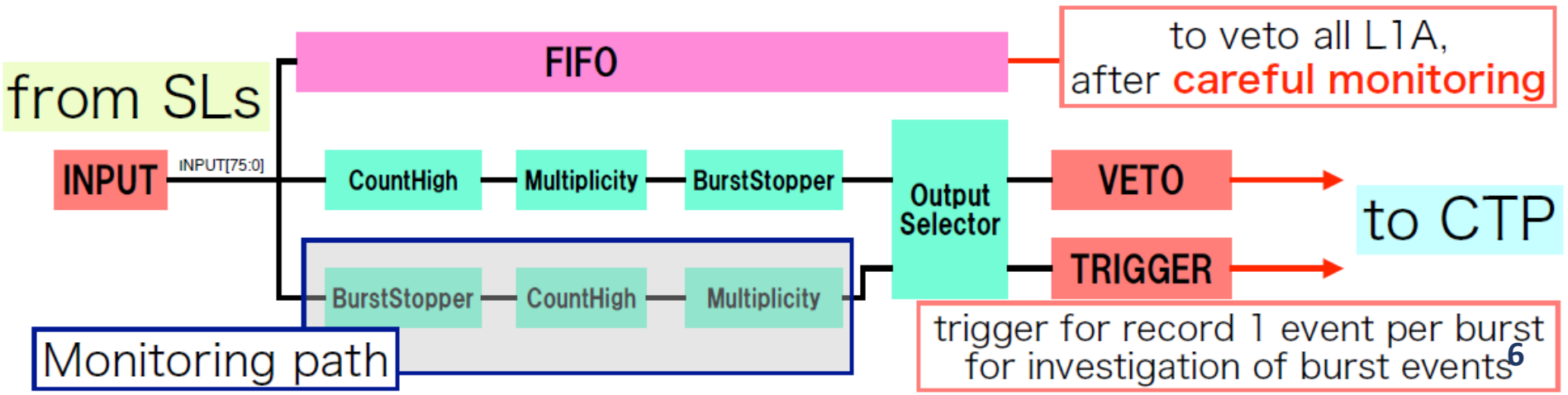
finished production



installed in USA15

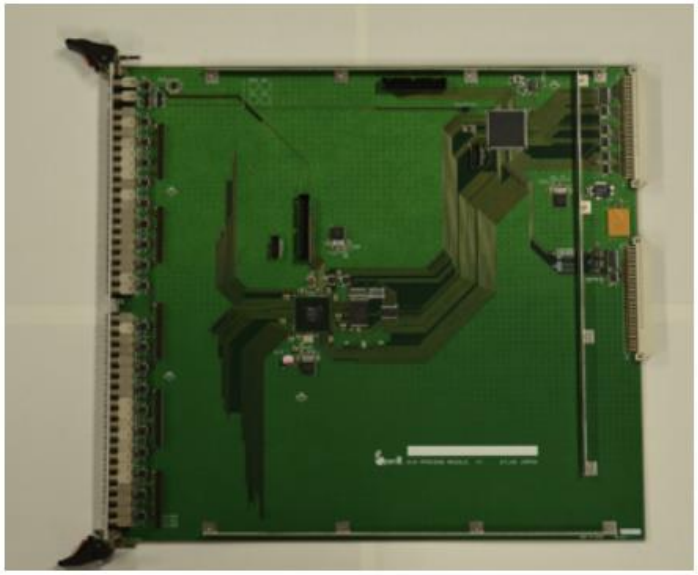


汎用多チャンネルNIM論理回路モジュール(神戸大前田)

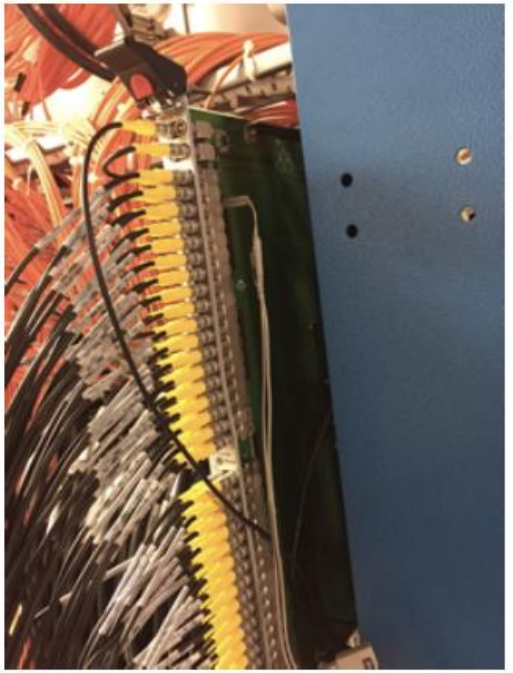


汎用多チャンネルNIM論理回路モジュール

- 多チャンネルのNIMシグナルINPUTの汎用論理回路ボードを開発
  - ATLASエンドキャップミューオン検出器TGCにおいて今夏から運用中
  - 神戸大・KEK・総研大・京都大が参加 (うち学生２名)
- 特徴
  - VMEスレーブモジュール (9Uサイズ)
  - NIMシグナル、76チャンネルのLEMOタイプINPUTを搭載
  - FPGA (Artix-7) を搭載し、論理計算したシグナルを出力（２チャンネル）
  - CPLD (CoolRunner-II) によりVME制御・FPGAのコンフィギュアが可能
  - BPIメモリを搭載、FPGAの高速コンフィギュアも可能
  - 内部クロック (CMOS 40.08 MHz)の他、外部クロックサポート



完成したモジュール



ATLASにインストールした様子

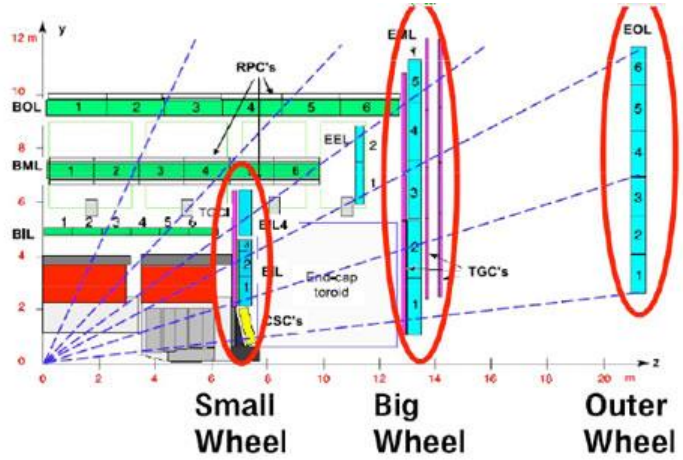
By Junpei Maeda (Kobe)

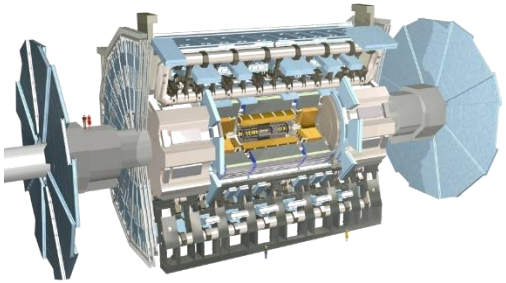
http://openit.kek.jp/project/atlas_nim_logic/public

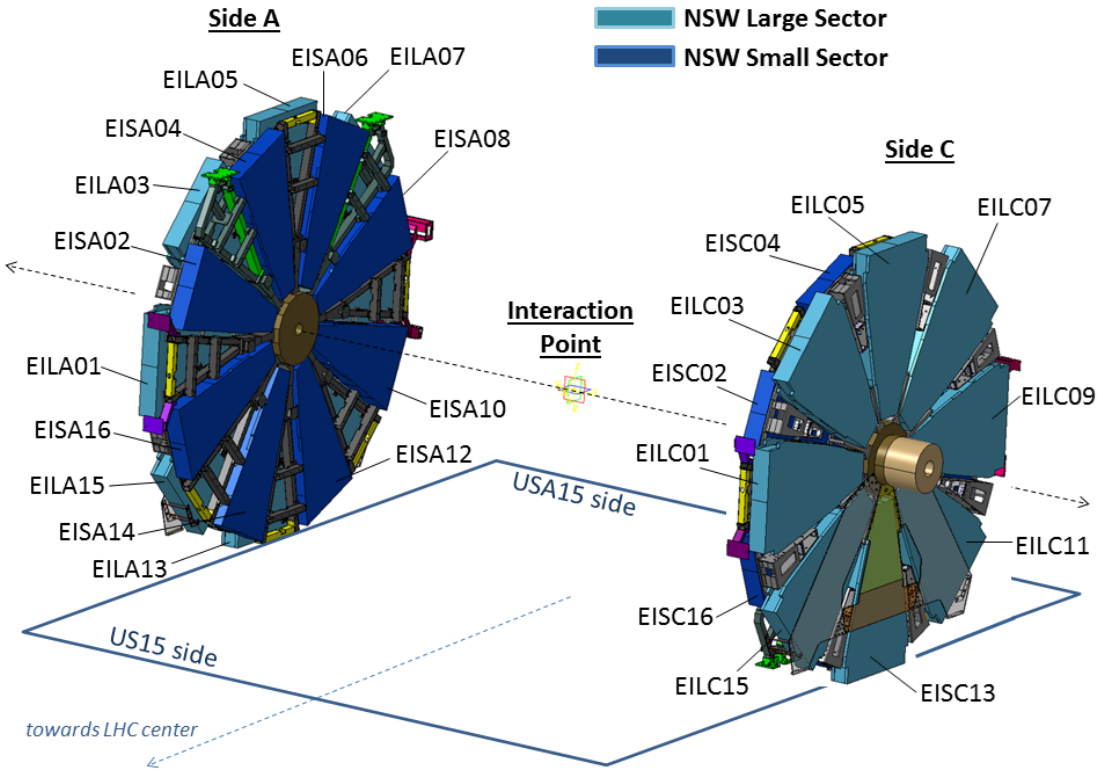
Phase 1 Upgrade

- Long Shutdown 2 (LS2)
  - 2019~2020
- New Small Wheel
  - Fine grained chambers at the Inner Station
  - Replacing existing EI/FI chambers
  - Upgrade of “Sector Logic” trigger processor

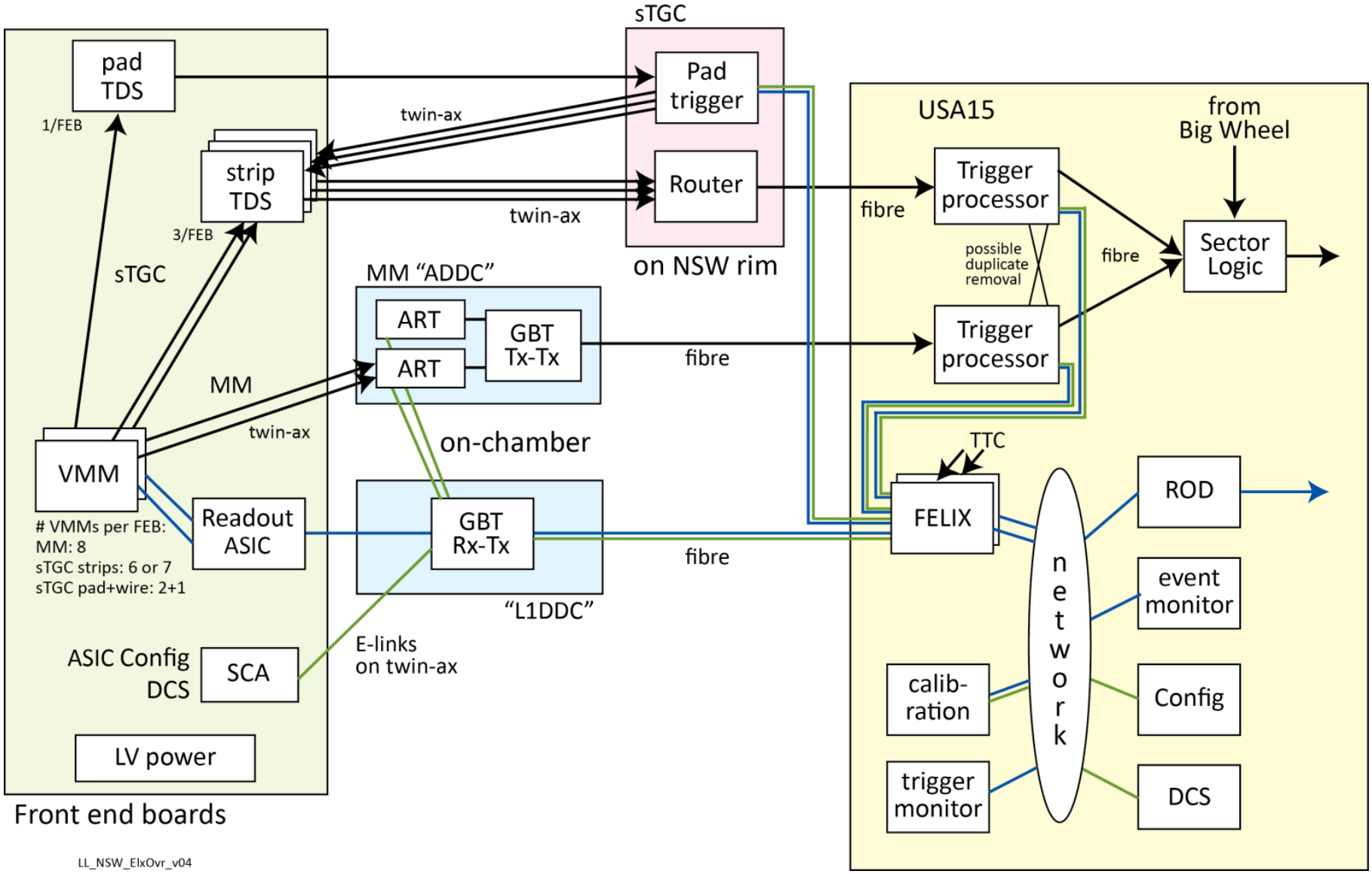
New Small Wheel



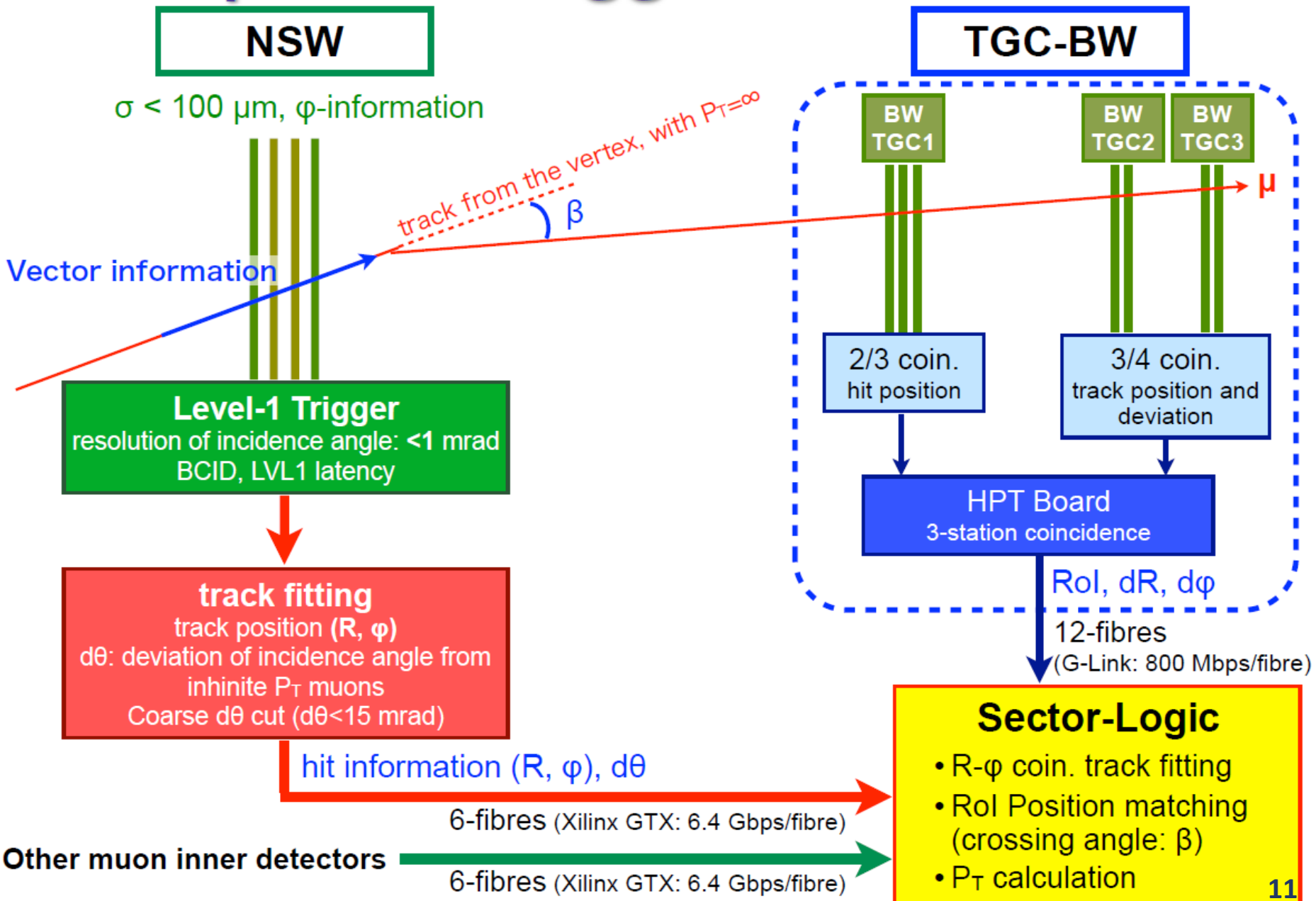




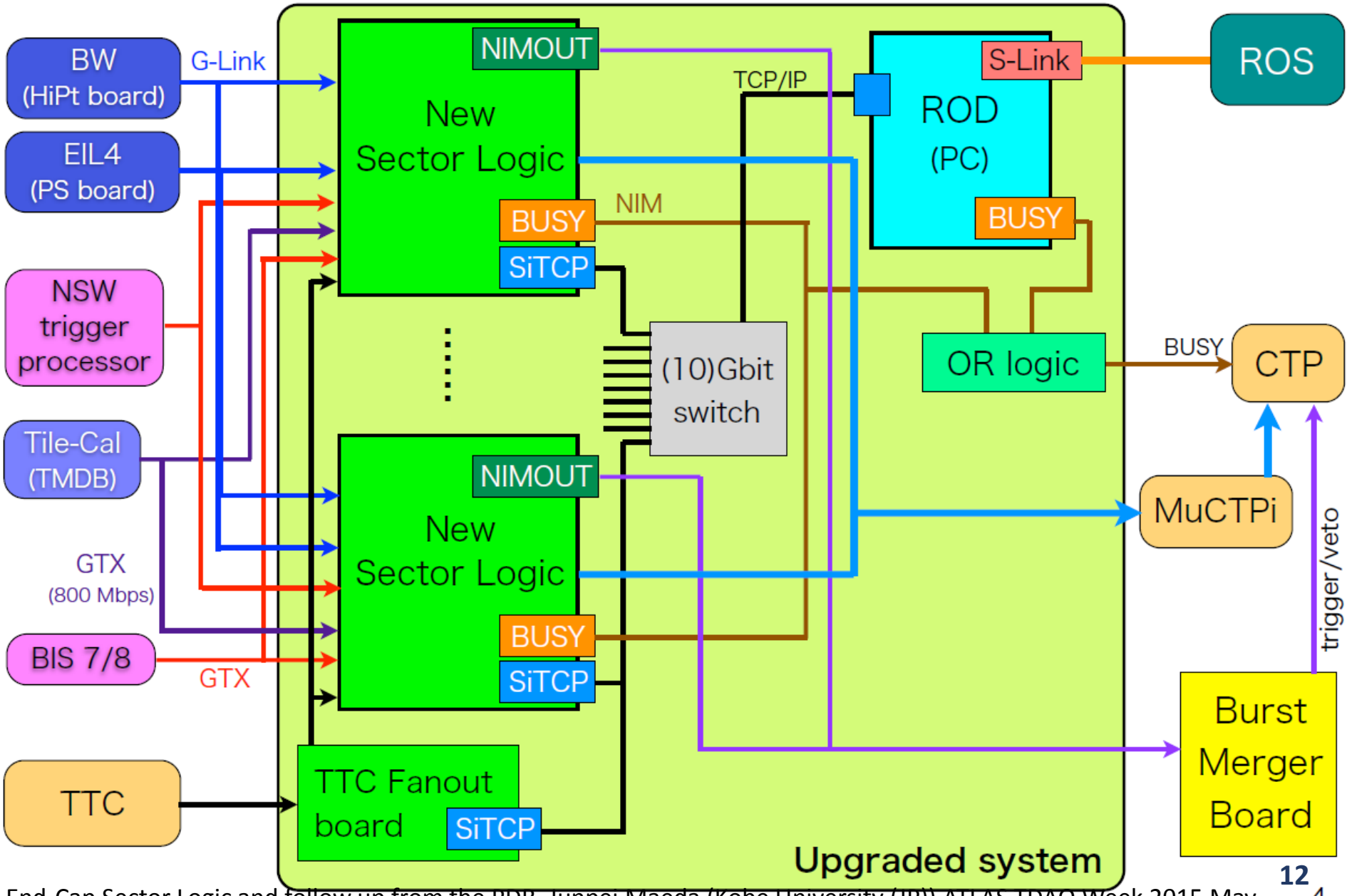
NSW Electronics Trigger & DAQ dataflow



Endcap muon trigger scheme @ Run-3



New Sector Logic and data flow

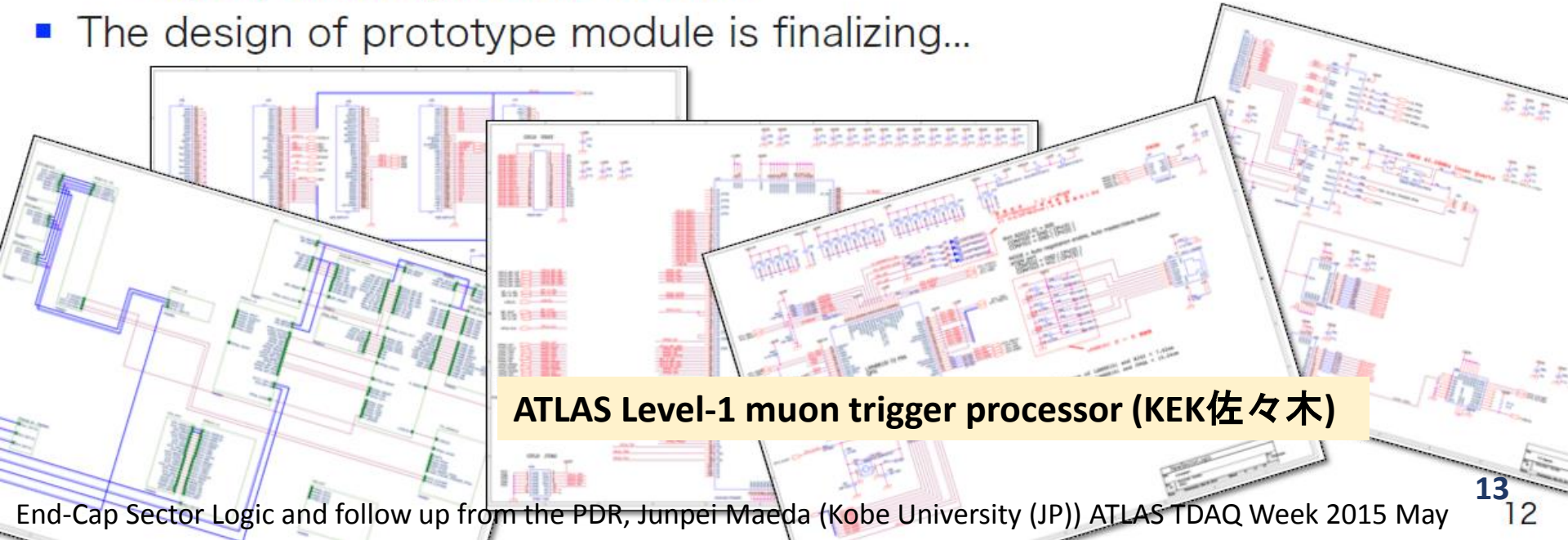


R&D status

- Many R&D tests have been done using PT7 test boards.
  - GTX latency
    → 57ns fixed latency
  - L1A rate test for readout
    → no error at 200 kHz
  - Capability of neighboring L1A
    → works even if L1A comes in 3 bunches
  - zero suppress for readout of trigger data
    → o(10^{-4}) according to 2012 raw data
- The design of prototype module is finalizing...

PT7-汎用VMEマザーボード (東大坂本)

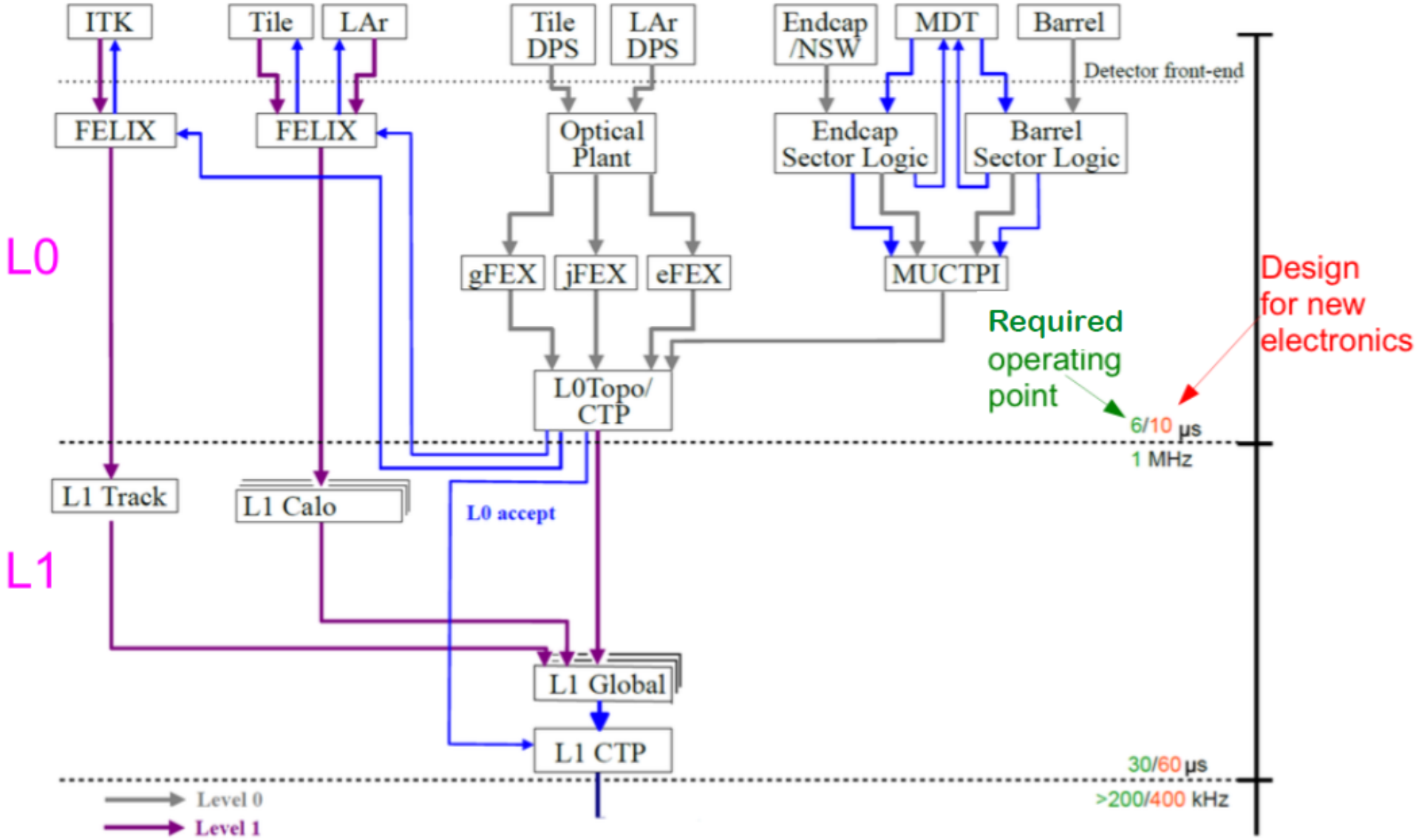
general purpose test board (PT7)



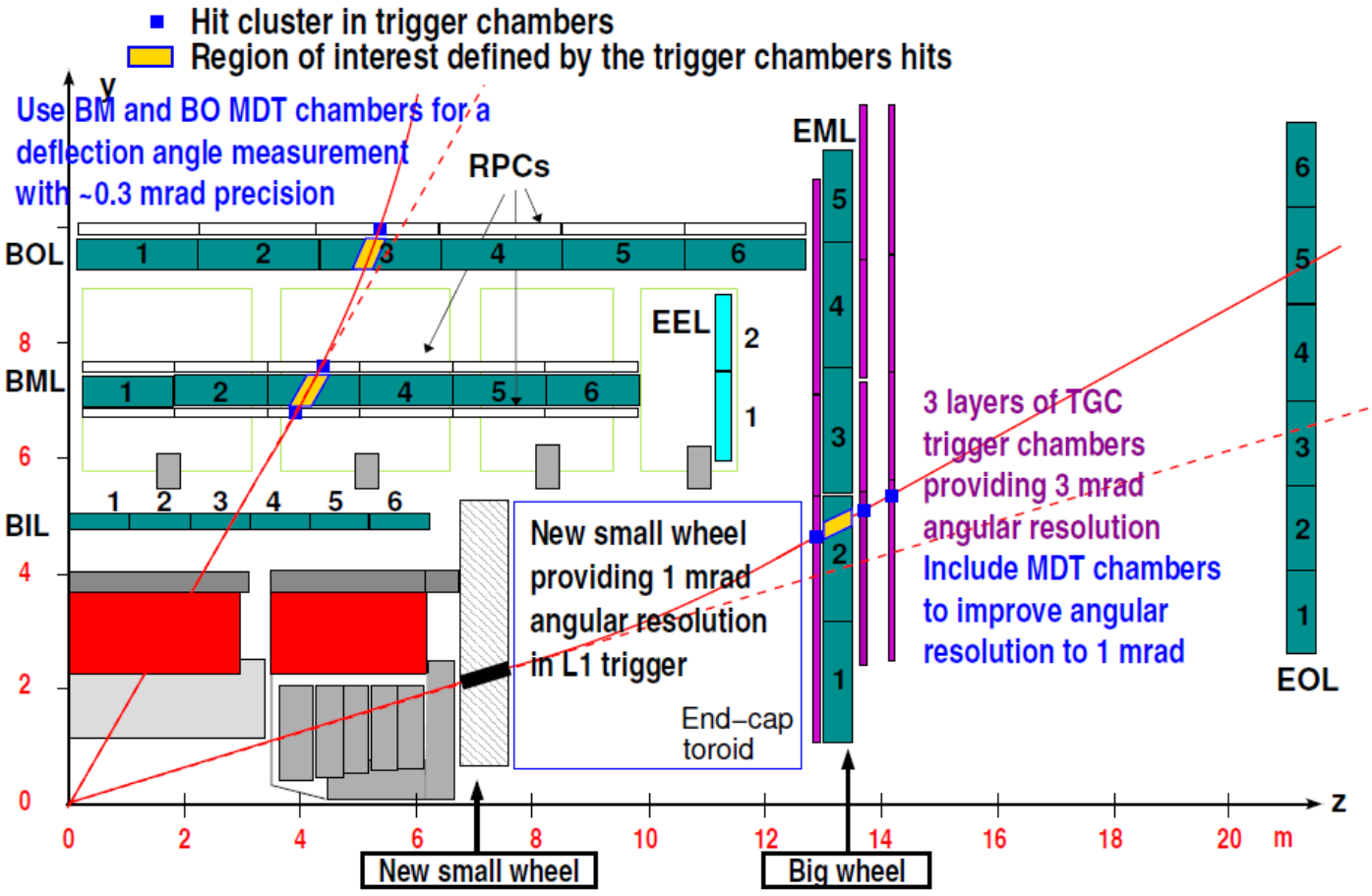
ATLAS Level-1 muon trigger processor (KEK佐々木)

Phase 2 Upgrade

- Long Shutdown 3 (LS3)
  - 2024~2026
- Replace All Frontend Electronics
  - Introduction of Level 0 Trigger
  - Longer latency for Level 1 Trigger


ITK
Tile
LAr
Tile DPS
LAr DPS
Endcap /NSW
MDT
Barrel
Detector front-end
FELIX
FELIX
Optical Plant
Endcap Sector Logic
Barrel Sector Logic
L0
gFEX
jFEX
eFEX
MUCTPI
Design for new electronics
Required operating point
L0Topo/ CTP
6/10 µs
1 MHz
L1 Track
L1 Calo
L0 accept
L1
L1 Global
L1 CTP
30/60 µs
>200/400 kHz
Level 0
Level 1

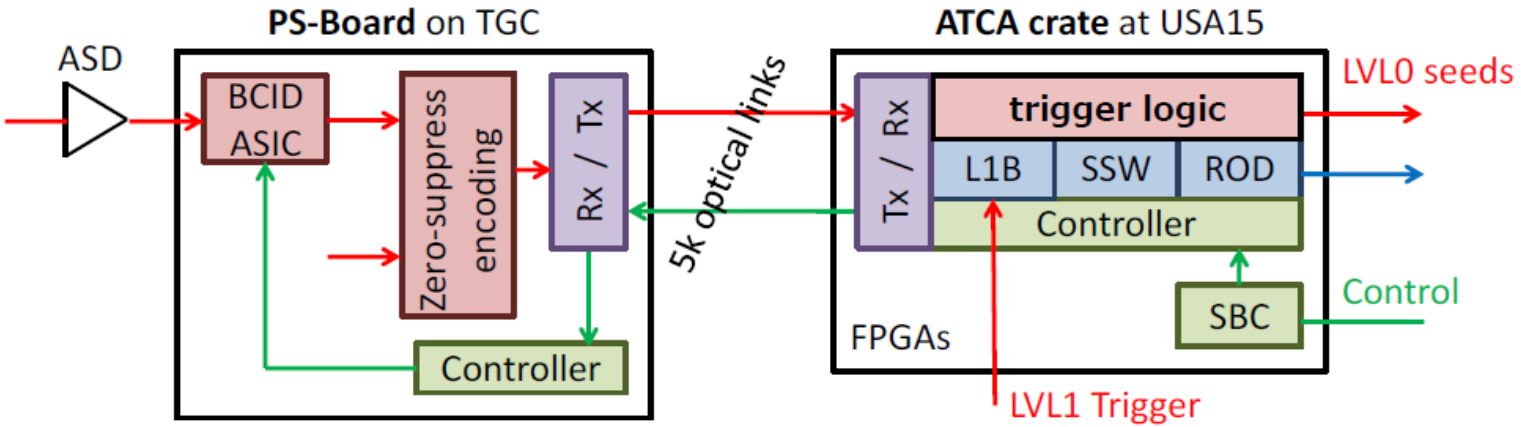
Minimal level-0 MDT trigger concepts



- Use deflection angle between BM and BO, NSW and EM as a measure for the muon momentum.
- Expected rate reduction $\sim 50\%$.

アトラス実験 MDT μ粒子検出器トリガー用TDC (名大戸本)

TGC L1 trigger electronics scheme for Phase- II



✓ ASIC's for PS-Board

➡ LVDS, variable delay, BCID, test pulse generator

➡ Zero-suppress and encoding logic of hit signals and interface to GB transfer

✓ module with FPGAs for trigger/readout at USA15

➡ output LVL0 seeds for MDT level-0 trigger logic

➡ receive LVL1 trigger signals for readout

➡ long L1-buffer memory to cope with L1 latency(60μs)

➡ **optimize the trigger logic**

According to Xilinx literature [8], the three MicroBlaze configurations listed in Table 4.2 can achieve no more than 260DMIPs on Zynq in speed grade -3, whereas the dual-core ARM is projected to reach 5000DMIPs (2500DMIPs per core), assuming a PS clock frequency of 1GHz [17]

The Zynq Book
Embedded Processing with the ARM® Cortex®-A9 on the Xilinx® Zynq®-7000 All Programmable SoC
Louise H. Crockett Ross A. Elliot Martin A. Enderwitz Robert W. Stewart
This edition first published July 2014 by Strathclyde Academic Media.

Zynq-7000 All Programmable SoC First Generation Architecture

The Zynq®-7000 family is based on the Xilinx All Programmable SoC architecture. These products integrate a feature-rich dual-core ARM® Cortex™-A9 based processing system (PS) and 28 nm Xilinx programmable logic (PL) in a single device. The ARM Cortex-A9 CPUs are the heart of the PS and also include on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces.

Processing System (PS)

Dual-core ARM® Cortex™-A9 Based Application Processor Unit (APU)

- 2.5 DMIPS/MHz per CPU
- CPU frequency: Up to 1 GHz
- Coherent multiprocessor support
- ARMv7-A architecture
  - TrustZone® security
  - Thumb®-2 instruction set
- Jazelle® RCT execution Environment Architecture
- NEON™ media-processing engine
- Single and double precision Vector Floating Point Unit (VFPU)
- CoreSight™ and Program Trace Macrocell (PTM)
- Timer and Interrupts
  - Three watchdog timers
  - One global timer
  - Two triple-timer counters

Caches

- 32 KB Level 1 4-way set-associative instruction and data caches (independent for each CPU)
- 512 KB 8-way set-associative Level 2 cache (shared between the CPUs)
- Byte-parity support

On-Chip Memory

- On-chip boot ROM
- 256 KB on-chip RAM (OCM)
- Byte-parity support

External Memory Interfaces

- Multiprotocol dynamic memory controller
- 16-bit or 32-bit interfaces to DDR3, DDR3L, DDR2, or LPDDR2 memories
- ECC support in 16-bit mode
- 1GB of address space using single rank of 8-, 16-, or 32-bit-wide memories
- Static memory interfaces
  - 8-bit SRAM data bus with up to 64 MB support
  - Parallel NOR flash support
  - ONFI1.0 NAND flash support (1-bit ECC)
  - 1-bit SPI, 2-bit SPI, 4-bit SPI (quad-SPI), or two quad-SPI (8-bit) serial NOR flash

8-Channel DMA Controller

- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and scatter-gather transaction support

I/O Peripherals and Interfaces

- Two 10/100/1000 tri-speed Ethernet MAC peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
  - Scatter-gather DMA capability
  - Recognition of 1588 rev. 2 PTP frames
  - GMII, RGMII, and SGMII interfaces
- Two USB 2.0 OTG peripherals, each supporting up to 12 Endpoints
  - USB 2.0 compliant device IP core
  - Supports on-the-go, high-speed, full-speed, and low-speed modes
  - Intel EHCI compliant USB host
  - 8-bit ULPI external PHY interface
- Two full CAN 2.0B compliant CAN bus interfaces
  - CAN 2.0-A and CAN 2.0-B and ISO 118981-1 standard compliant
  - External PHY interface
- Two SD/SDIO 2.0/MMC3.31 compliant controllers
- Two full-duplex SPI ports with three peripheral chip selects
- Two high-speed UARTs (up to 1 Mb/s)
- Two master and slave I2C interfaces
- GPIO with four 32-bit banks, of which up to 54 bits can be used with the PS I/O (one bank of 32b and one bank of 22b) and up to 64 bits (up to two banks of 32b) connected to the Programmable Logic
- Up to 54 flexible multiplexed I/O (MIO) for peripheral pin assignments

Interconnect

- High-bandwidth connectivity within PS and between PS and PL
- ARM AMBA® AXI based
- QoS support on critical masters for latency and bandwidth control

Programmable Logic (PL)

Configurable Logic Blocks (CLB)

- Look-up tables (LUT)
- Flip-flops
- Cascadeable adders

36 Kb Block RAM

- True Dual-Port
- Up to 72 bits wide
- Configurable as dual 18 Kb

DSP Blocks

- 18 x 25 signed multiply
- 48-bit adder/accumulator
- 25-bit pre-adder

Feature Summary

Table 1: **Zynq-7000 All Programmable SoC**

Zynq-7000 All Programmable SoC								
	Device Name	**Z-7010**	**Z-7015**	**Z-7020**	**Z-7030**	**Z-7035**	**Z-7045**	**Z-7100**
	Part Number	**XC7Z010**	**XC7Z015**	**XC7Z020**	**XC7Z030**	**XC7Z035**	**XC7Z045**	**XC7Z100**
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™						
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor						
	Maximum Frequency	667 MHz (-1); 766 MHz (-2); 866 MHz (-3)			667 MHz (-1); 800 MHz (-2); 1 GHz (-3)			667 MHz (-1) 800 MHz (-2)
	L1 Cache	32 KB Instruction, 32 KB Data per processor						
	L2 Cache	512 KB						
	On-Chip Memory	256 KB						
	External Memory Support(1)	DDR3, DDR3L, DDR2, LPDDR2						
	External Static Memory Support(1)	2x Quad-SPI, NAND, NOR						
	DMA Channels	8 (4 dedicated to Programmable Logic)						
	Peripherals(1)	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Peripherals w/ built-in DMA(1)	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO						
	Security(2)	RSA Authentication, and AES and SHA 256-bit Decryption and Authentication for Secure Boot						
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)		2x AXI 32b Master 2x AXI 32-bit Slave 4x AXI 64-bit/32-bit Memory AXI 64-bit ACP 16 Interrupts						

Table 1: **Zynq-7000 All Programmable SoC *(Cont'd)***

	Zynq-7000 All Programmable SoC							
	Device Name	**Z-7010**	**Z-7015**	**Z-7020**	**Z-7030**	**Z-7035**	**Z-7045**	**Z-7100**
	Part Number	**XC7Z010**	**XC7Z015**	**XC7Z020**	**XC7Z030**	**XC7Z035**	**XC7Z045**	**XC7Z100**
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Kintex®-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates)(3)	28K Logic Cells (~430K)	74K Logic Cells (~1.1M)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	275K Logic Cells (~4.1M)	350K Logic Cells (~5.2M)	444K Logic Cells (~6.6M)
	Look-Up Tables (LUTs)	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)	380 KB (95)	560 KB (140)	1,060 KB (265)	2,000 KB (500)	2,180 KB (545)	3,020 KB (755)
	Programmable DSP Slices (18x25 MACCs)	80	160	220	400	900	900	2,020
	Peak DSP Performance (Symmetric FIR)	100 GMACs	200 GMACs	276 GMACs	593 GMACs	1,334 GMACs	1,334 GMACs	2,622 GMACs
	PCI Express® (Root Complex or Endpoint)(4)	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs						
	Security(2)	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication						

Notes:

1. Restrictions apply for CLG225 package. Refer to the UG585, *Zynq-7000 AP SoC Technical Reference Manual* (TRM) for details.
2. Security is shared by the Processing System and the Programmable Logic.
3. Equivalent ASIC gate count is dependent on the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.
4. Refer to PG054, *7 Series FPGAs Integrated Block for PCI Express* for PCI Express support in specific devices.

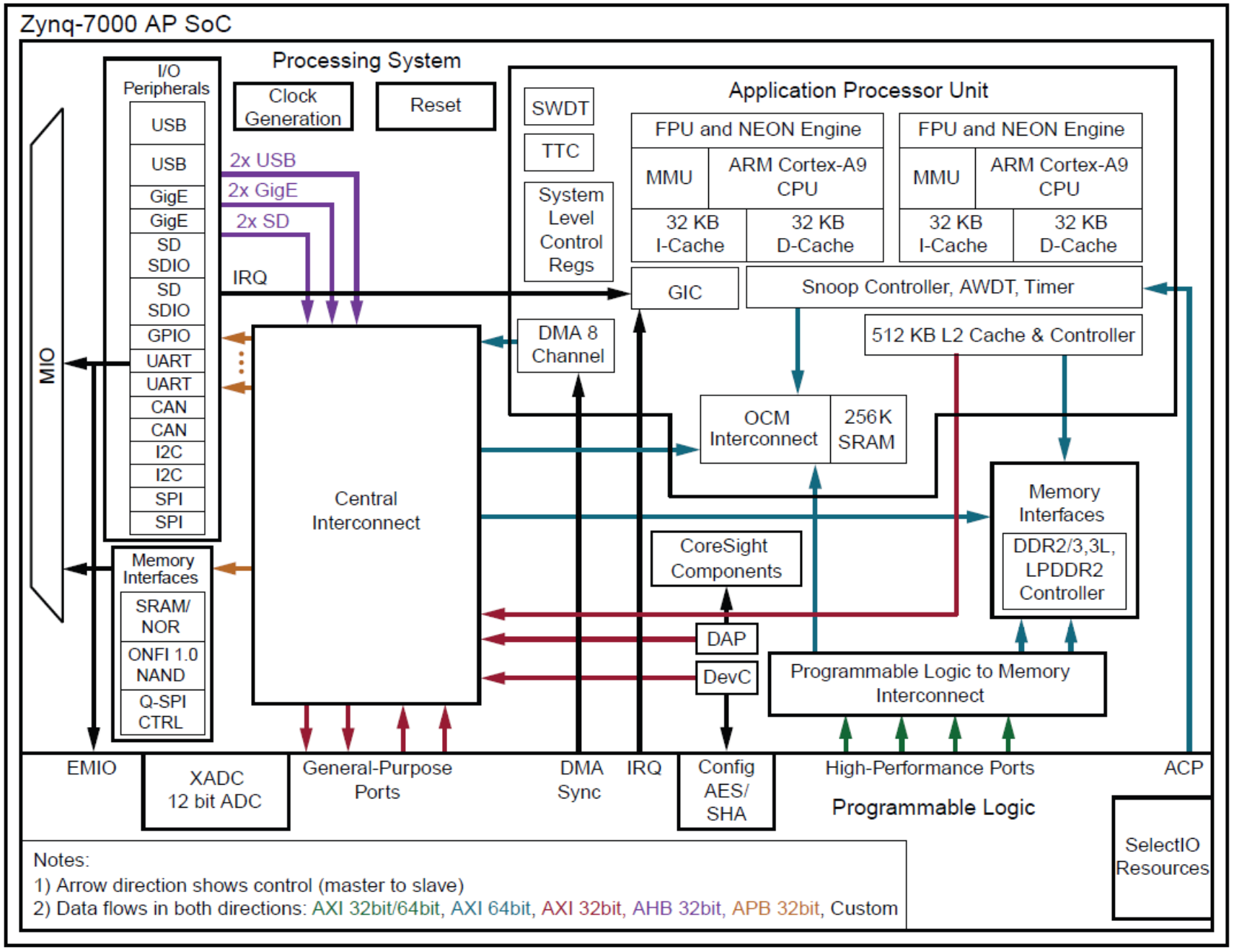


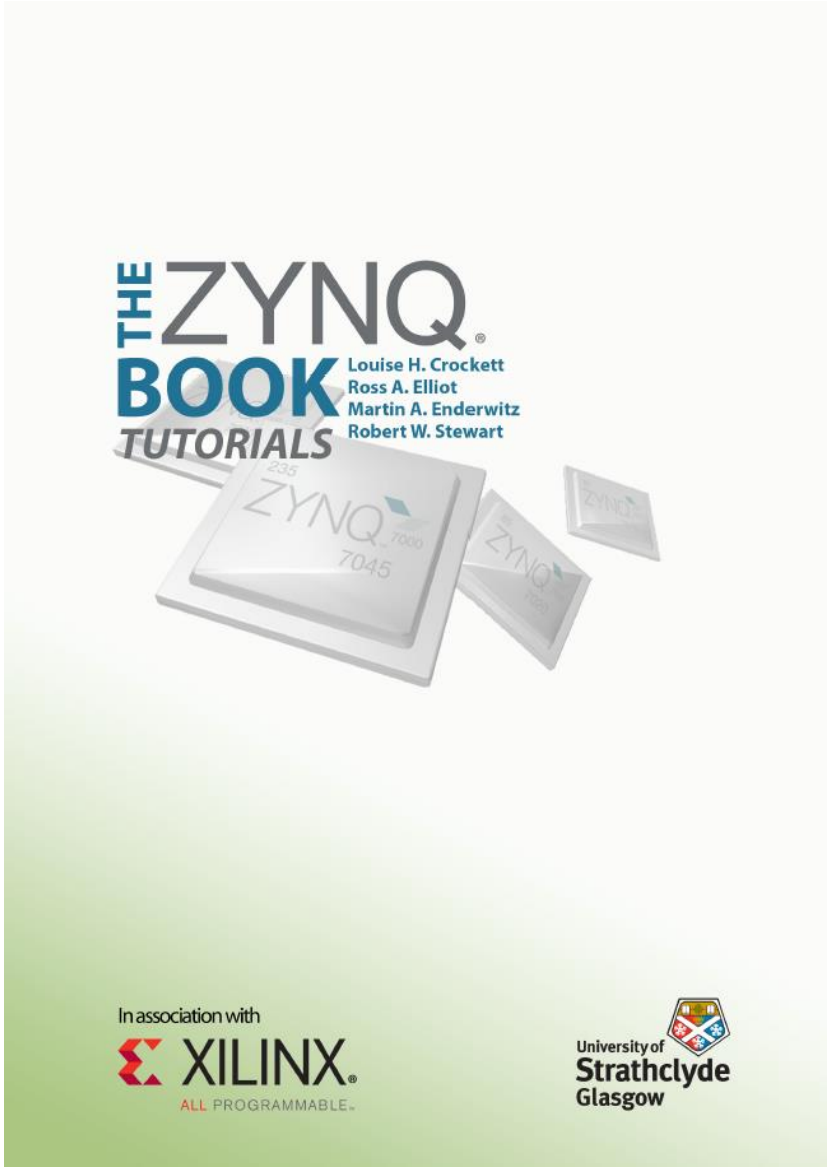
Figure 1-1: **Zynq-7000 AP SoC Overview**

The Zynq Book

Embedded Processing with the
ARM® Cortex®-A9 on the Xilinx®
Zynq®-7000 All Programmable SoC

In association with
XILINX
ALL PROGRAMMABLE

University of Strathclyde Glasgow

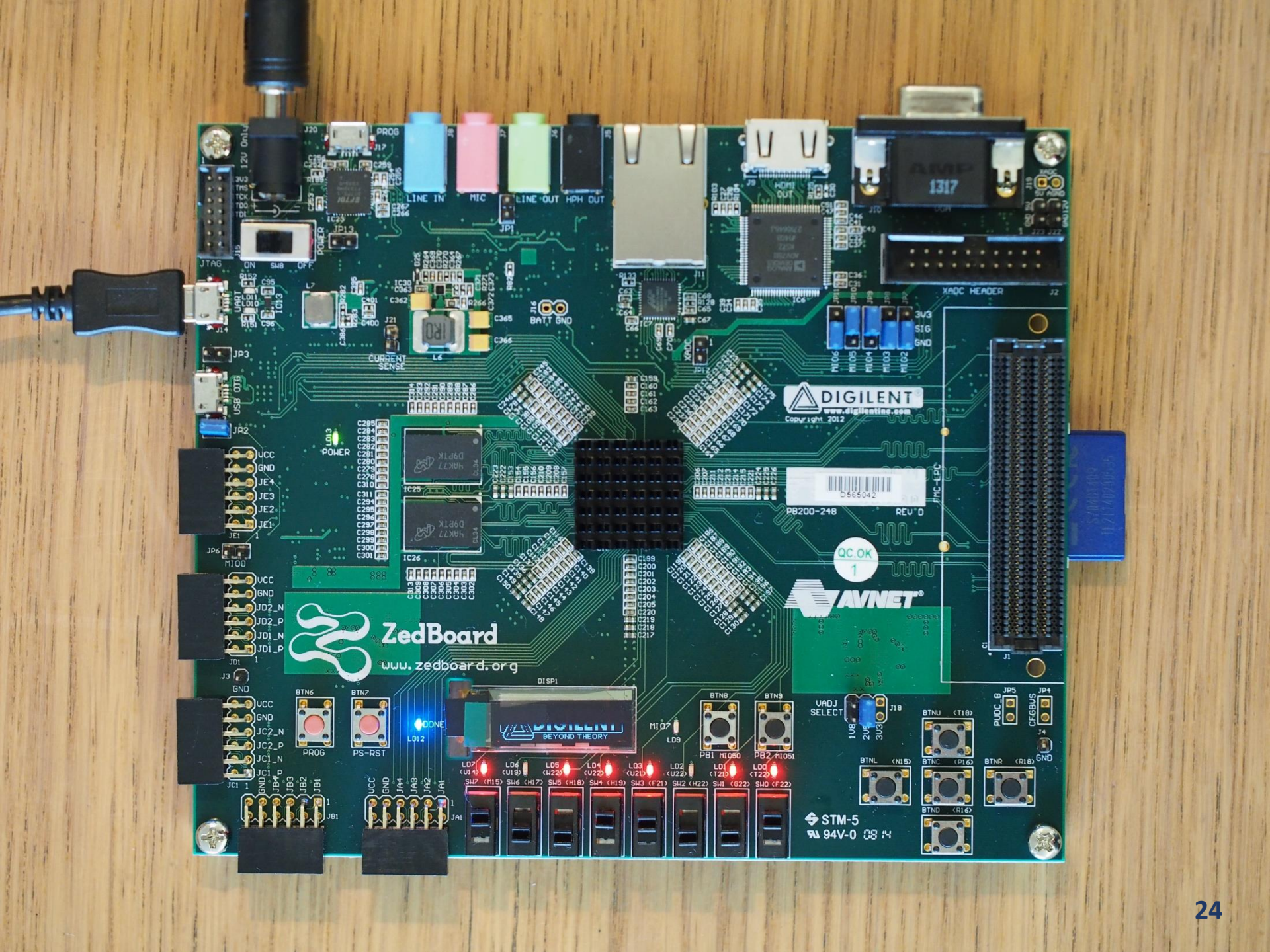


ZedBoard

(Zynq™ Evaluation and Development)
Hardware User's Guide

Version 2.2
27 January 2014

http://www.avnet.co.jp/kits/Xilinx/AES-Z7EV-7Z020-G-J.aspx 55,800円


ZedBoard
www.zedboard.org
DIGILENT
AVNET
PROG
LINE IN
MIC
LINE OUT
HPH OUT
XADC HEADER
POWER
PROG
PS-RST
DISP1
BEYOND THEORY
PB200-248
REV D
QC.OK
STM-5
94V-0

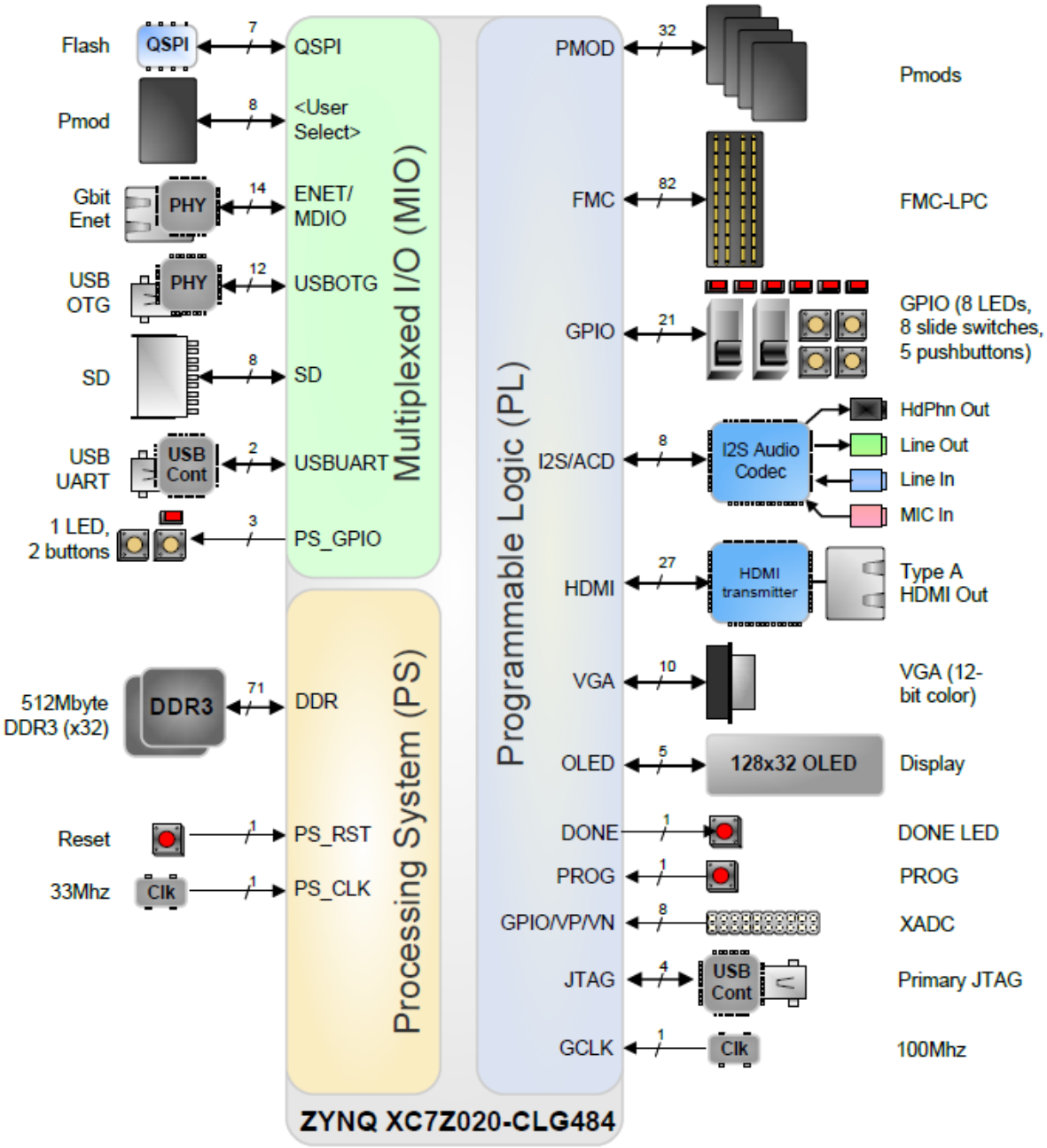
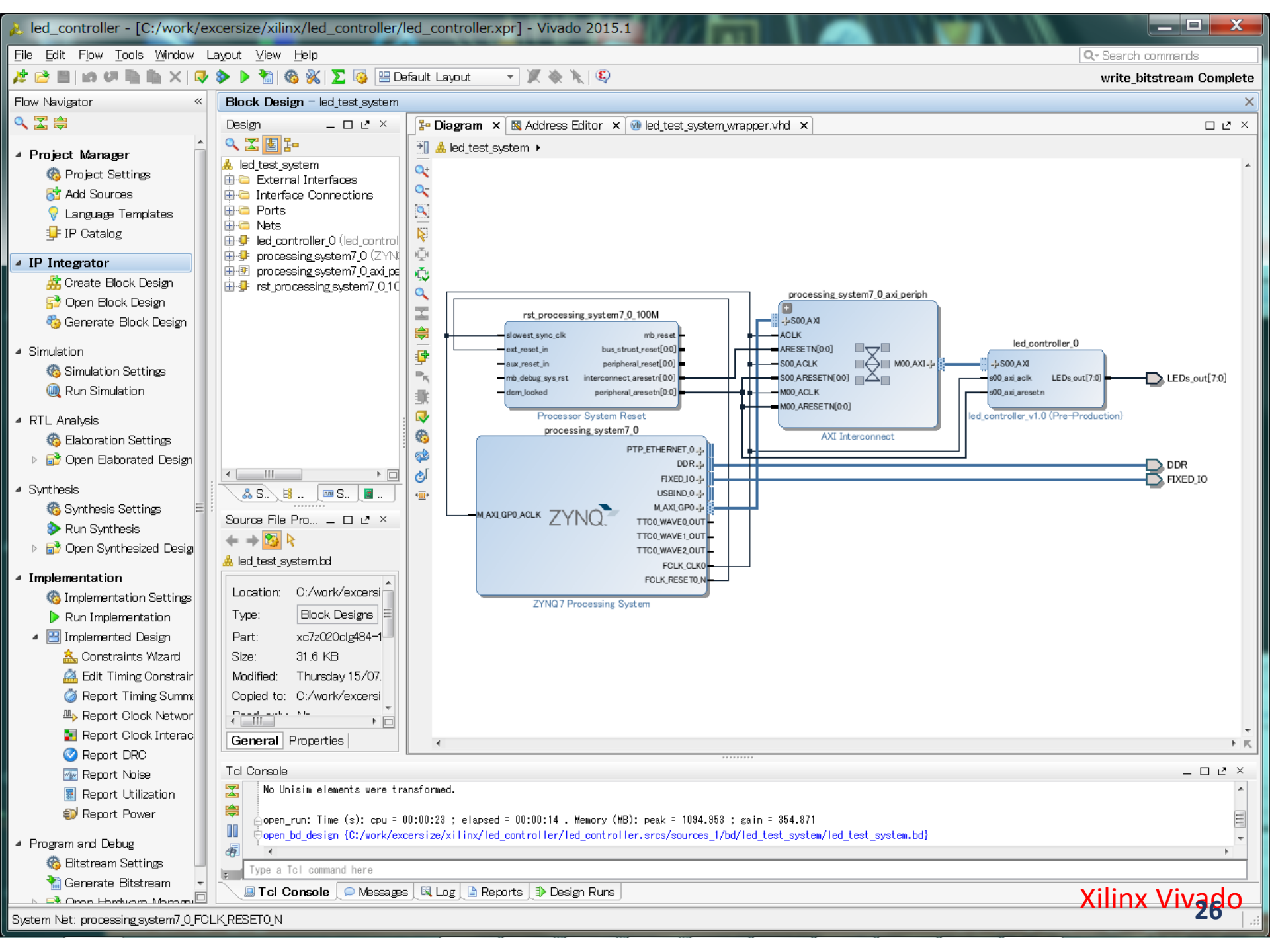


Figure 1 – ZedBoard Block Diagram


led_controller - [C:/work/excersize/xilinx/led_controller/led_controller.xpr] - Vivado 2015.1
File Edit Flow Tools Window Layout View Help
Search commands
Default Layout
write_bitstream Complete
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Implementation Settings
Run Implementation
Implemented Design
Constraints Wizard
Edit Timing Constrair
Report Timing Summ
Report Clock Networ
Report Clock Interac
Report DRC
Report Noise
Report Utilization
Report Power
Program and Debug
Bitstream Settings
Generate Bitstream
Block Design – led_test_system
Design
led_test_system
External Interfaces
Interface Connections
Ports
Nets
led_controller_0 (led_control
processing_system7_0 (ZYN
processing_system7_0_axi_pe
rst_processing_system7_0_10
Diagram
Address Editor
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led_test_system
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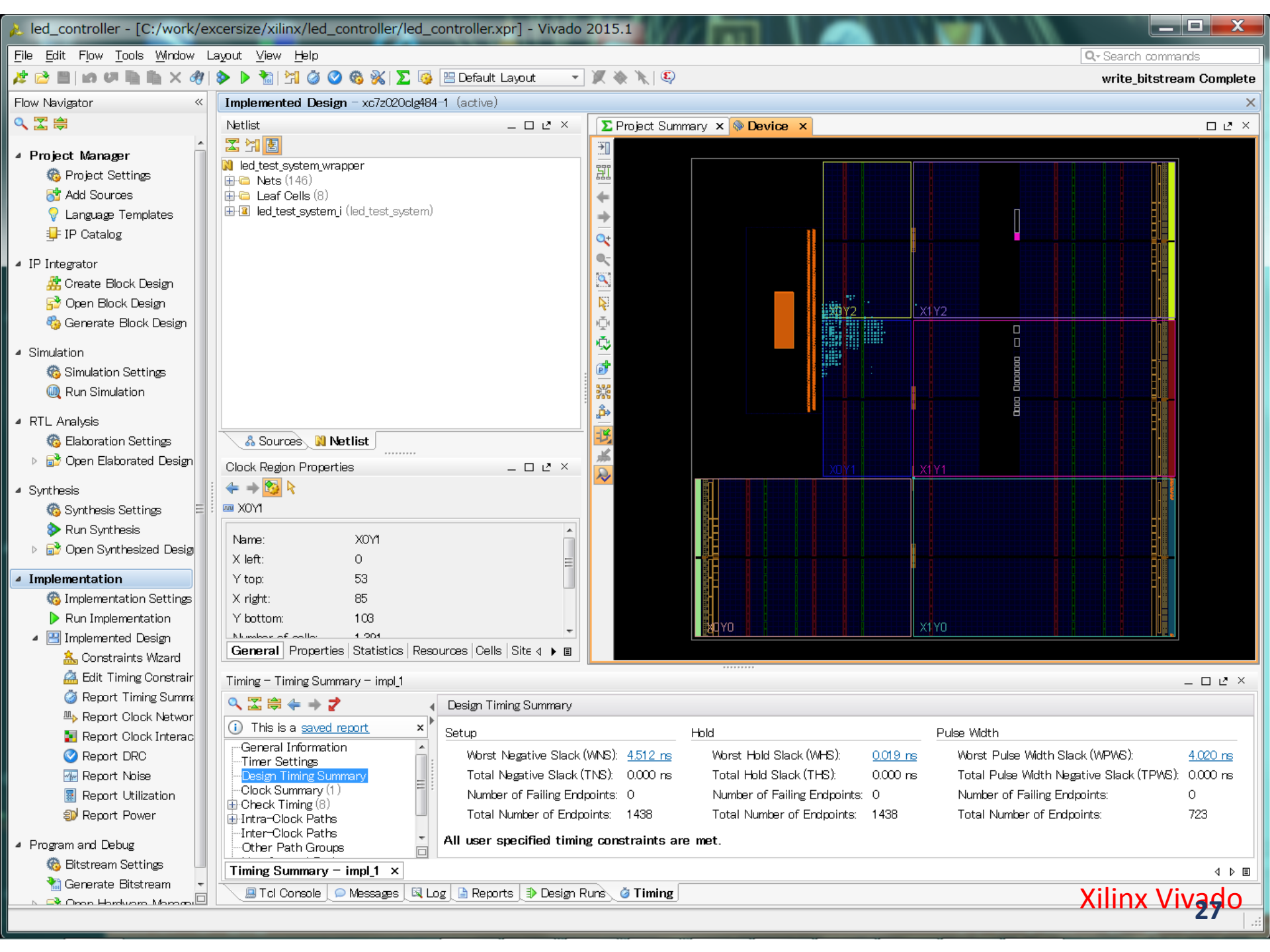
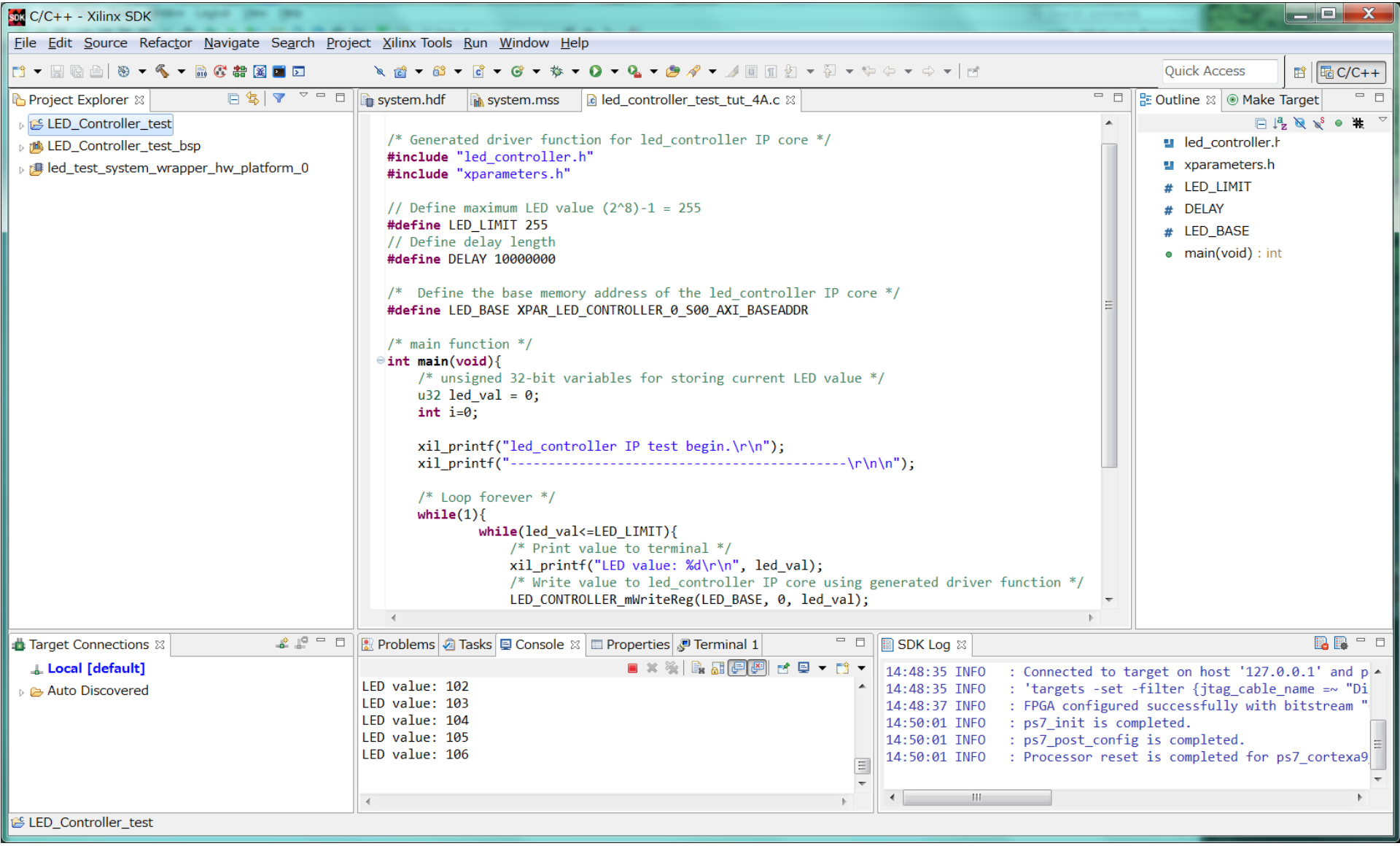
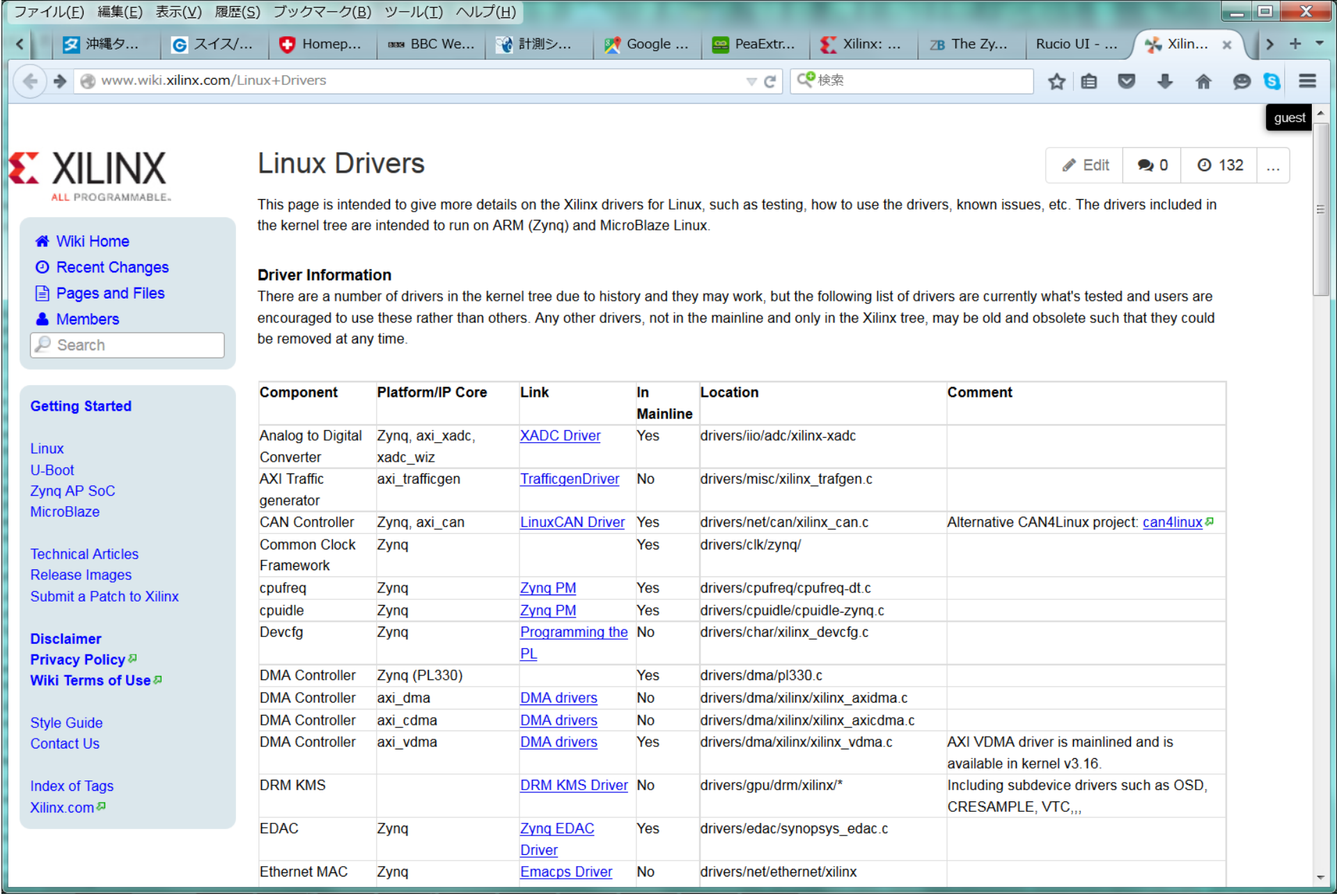
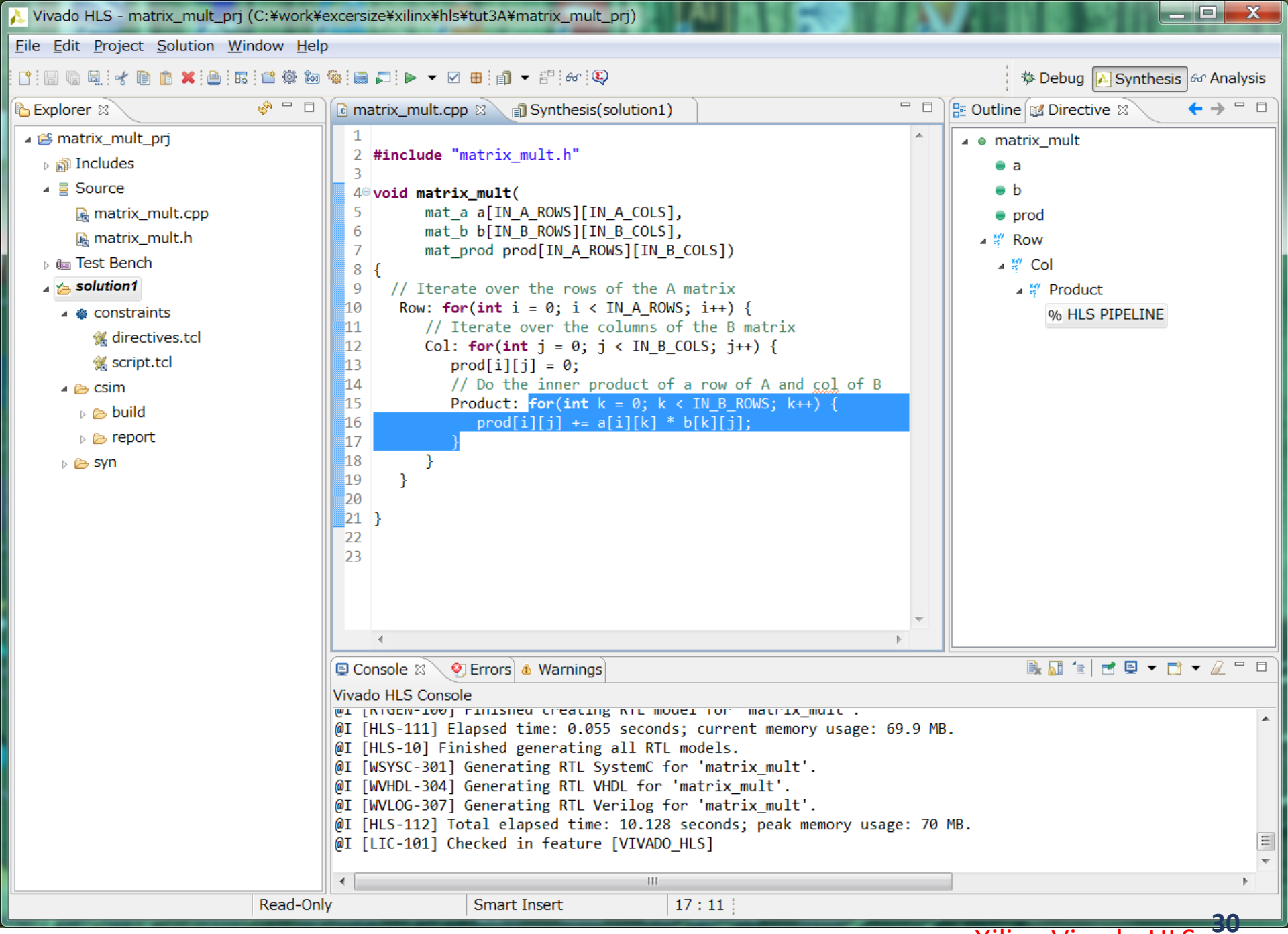
ACLK
ARESETN[0:0]
S00_ACLK
S00_ARESETN[0:0]
M00_ACLK
M00_ARESETN[0:0]
M00_AXI
AXI Interconnect
rst_processing_system7_0_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
led_controller_0
S00_AXI
s00_axi_aclk
s00_axi_aresetn
LEDs_out[7:0]
led_controller_v1.0 (Pre-Production)
LEDs_out[7:0]
processing_system7_0
PTP_ETHERNET_0
DDR
FIXED_IO
USBIND_0
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
M_AXI_GP0_ACLK
ZYNQ
ZYNQ7 Processing System
DDR
FIXED_IO
Source File Pro...
led_test_system.bd
Location: C:/work/excersi
Type: Block Designs
Part: xc7z020clg484-1
Size: 31.6 KB
Modified: Thursday 15/07.
Copied to: C:/work/excersi
General
Properties
Tcl Console
No Unisim elements were transformed.
open_run: Time (s): cpu = 00:00:23 ; elapsed = 00:00:14 . Memory (MB): peak = 1094.953 ; gain = 354.871
open_bd_design {C:/work/excersize/xilinx/led_controller/led_controller.srcs/sources_1/bd/led_test_system/led_test_system.bd}
Type a Tcl command here
Tcl Console
Messages
Log
Reports
Design Runs
System Net: processing_system7_0_FCLK_RESET0_N
Xilinx Vivado
26


led_controller - [C:/work/excersize/xilinx/led_controller/led_controller.xpr] - Vivado 2015.1
File Edit Flow Tools Window Layout View Help
Search commands
Default Layout
write_bitstream Complete
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Implementation Settings
Run Implementation
Implemented Design
Constraints Wizard
Edit Timing Constrair
Report Timing Summ
Report Clock Networ
Report Clock Interac
Report DRC
Report Noise
Report Utilization
Report Power
Program and Debug
Bitstream Settings
Generate Bitstream
Implemented Design – xc7z020clg484-1 (active)
Netlist
led_test_system_wrapper
Nets (146)
Leaf Cells (8)
led_test_system_i (led_test_system)
Sources
Netlist
Clock Region Properties
X0Y1
Name: X0Y1
X left: 0
Y top: 53
X right: 85
Y bottom: 103
General
Properties
Statistics
Resources
Cells
Site
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Timing – Timing Summary – impl_1
This is a saved report
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (8)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
Timing Summary – impl_1
Design Timing Summary
Setup
Worst Negative Slack (WNS): 4.512 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1438
Hold
Worst Hold Slack (WHS): 0.019 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1438
Pulse Width
Worst Pulse Width Slack (WPWS): 4.020 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 723
All user specified timing constraints are met.
Tcl Console
Messages
Log
Reports
Design Runs
Timing


C/C++ - Xilinx SDK
File Edit Source Refactor Navigate Search Project Xilinx Tools Run Window Help
Quick Access
C/C++
Project Explorer
LED_Controller_test
LED_Controller_test_bsp
led_test_system_wrapper_hw_platform_0
system.hdf
system.mss
led_controller_test_tut_4A.c
/* Generated driver function for led_controller IP core */
#include "led_controller.h"
#include "xparameters.h"
// Define maximum LED value (2^8)-1 = 255
#define LED_LIMIT 255
// Define delay length
#define DELAY 10000000
/* Define the base memory address of the led_controller IP core */
#define LED_BASE XPAR_LED_CONTROLLER_0_S00_AXI_BASEADDR
/* main function */
int main(void){
/* unsigned 32-bit variables for storing current LED value */
u32 led_val = 0;
int i=0;
xil_printf("led_controller IP test begin.\r\n");
xil_printf("---\r\n\n");
/* Loop forever */
while(1){
while(led_val<=LED_LIMIT){
/* Print value to terminal */
xil_printf("LED value: %d\r\n", led_val);
/* Write value to led_controller IP core using generated driver function */
LED_CONTROLLER_mWriteReg(LED_BASE, 0, led_val);
Outline
Make Target
led_controller.h
xparameters.h
LED_LIMIT
DELAY
LED_BASE
main(void) : int
Target Connections
Local [default]
Auto Discovered
Problems
Tasks
Console
Properties
Terminal 1
LED value: 102
LED value: 103
LED value: 104
LED value: 105
LED value: 106
SDK Log
14:48:35 INFO : Connected to target on host '127.0.0.1' and p
14:48:35 INFO : 'targets -set -filter {jtag_cable_name =~ "Di
14:48:37 INFO : FPGA configured successfully with bitstream "
14:50:01 INFO : ps7_init is completed.
14:50:01 INFO : ps7_post_config is completed.
14:50:01 INFO : Processor reset is completed for ps7_cortexa9
LED_Controller_test



Component	Platform/IP Core	Link	In Mainline	Location	Comment
Analog to Digital Converter	Zynq, axi_xadc, xadc_wiz	XADC Driver	Yes	drivers/iio/adc/xilinx-xadc	
AXI Traffic generator	axi_trafficgen	TrafficgenDriver	No	drivers/misc/xilinx_trafgen.c	
CAN Controller	Zynq, axi_can	LinuxCAN Driver	Yes	drivers/net/can/xilinx_can.c	Alternative CAN4Linux project: can4linux
Common Clock Framework	Zynq		Yes	drivers/clk/zynq/	
cpufreq	Zynq	Zynq PM	Yes	drivers/cpufreq/cpufreq-dt.c	
cpuidle	Zynq	Zynq PM	Yes	drivers/cpuidle/cpuidle-zynq.c	
Devcfg	Zynq	Programming the PL	No	drivers/char/xilinx_devcfg.c	
DMA Controller	Zynq (PL330)		Yes	drivers/dma/pl330.c	
DMA Controller	axi_dma	DMA drivers	No	drivers/dma/xilinx/xilinx_axidma.c	
DMA Controller	axi_cdma	DMA drivers	No	drivers/dma/xilinx/xilinx_axicdma.c	
DMA Controller	axi_vdma	DMA drivers	Yes	drivers/dma/xilinx/xilinx_vdma.c	AXI VDMA driver is mainlined and is available in kernel v3.16.
DRM KMS		DRM KMS Driver	No	drivers/gpu/drm/xilinx/*	Including subdevice drivers such as OSD, CRESAMPLE, VTC,,,
EDAC	Zynq	Zynq EDAC Driver	Yes	drivers/edac/synopsys_edac.c	
Ethernet MAC	Zynq	Emacps Driver	No	drivers/net/ethernet/xilinx	


Vivado HLS - matrix_mult_prj (C:¥work¥excersize¥xilinx¥hls¥tut3A¥matrix_mult_prj)
File Edit Project Solution Window Help
Debug Synthesis Analysis
Explorer
matrix_mult_prj
Includes
Source
matrix_mult.cpp
matrix_mult.h
Test Bench
solution1
constraints
directives.tcl
script.tcl
csim
build
report
syn
matrix_mult.cpp
Synthesis(solution1)
#include "matrix_mult.h"
void matrix_mult(
mat_a a[IN_A_ROWS][IN_A_COLS],
mat_b b[IN_B_ROWS][IN_B_COLS],
mat_prod prod[IN_A_ROWS][IN_B_COLS])
{
// Iterate over the rows of the A matrix
Row: for(int i = 0; i < IN_A_ROWS; i++) {
// Iterate over the columns of the B matrix
Col: for(int j = 0; j < IN_B_COLS; j++) {
prod[i][j] = 0;
// Do the inner product of a row of A and col of B
Product: for(int k = 0; k < IN_B_ROWS; k++) {
prod[i][j] += a[i][k] * b[k][j];
}
}
}
}
Outline
Directive
matrix_mult
a
b
prod
Row
Col
Product
% HLS PIPELINE
Console
Errors
Warnings
Vivado HLS Console
@I [HLS-111] Elapsed time: 0.055 seconds; current memory usage: 69.9 MB.
@I [HLS-10] Finished generating all RTL models.
@I [WSYSC-301] Generating RTL SystemC for 'matrix_mult'.
@I [WVHDL-304] Generating RTL VHDL for 'matrix_mult'.
@I [WVLOG-307] Generating RTL Verilog for 'matrix_mult'.
@I [HLS-112] Total elapsed time: 10.128 seconds; peak memory usage: 70 MB.
@I [LIC-101] Checked in feature [VIVADO_HLS]
Read-Only
Smart Insert
17 : 11

開発フロー

- HDLによるロジックデザイン
- AXIインターフェースを付加したIP化
- Board Support Package (BSP)ソフトウエア
- Linuxデバイスドライバー
- アプリケーションソフト
- Software-Hardware Co-design
  - ソフトウエアアルゴリズムとしての検証
  - High Level Synthesis (HLS)によるIP化

OpenItプロジェクトの提案

- ハードウエアからソフトウエアまで包括的な開発フローの確立
- 評価ボード用IPの蓄積
  - AVNET ZedBoard (XC7Z020評価ボード)
  - Xilinx ZC702 (XC7Z020評価ボード)
  - Xilinx ZC706 (XC7Z045評価ボード)
- ハードウエアデザイン
  - XC7Z045を搭載したVMEモジュール(PT8?PTZ?)
  - IPレポジトリ
- Linuxソフトウエアレポジトリ
  - デバイスドライバー