

KEKB入射器におけるタイミング配信システム監視用 TDCの開発

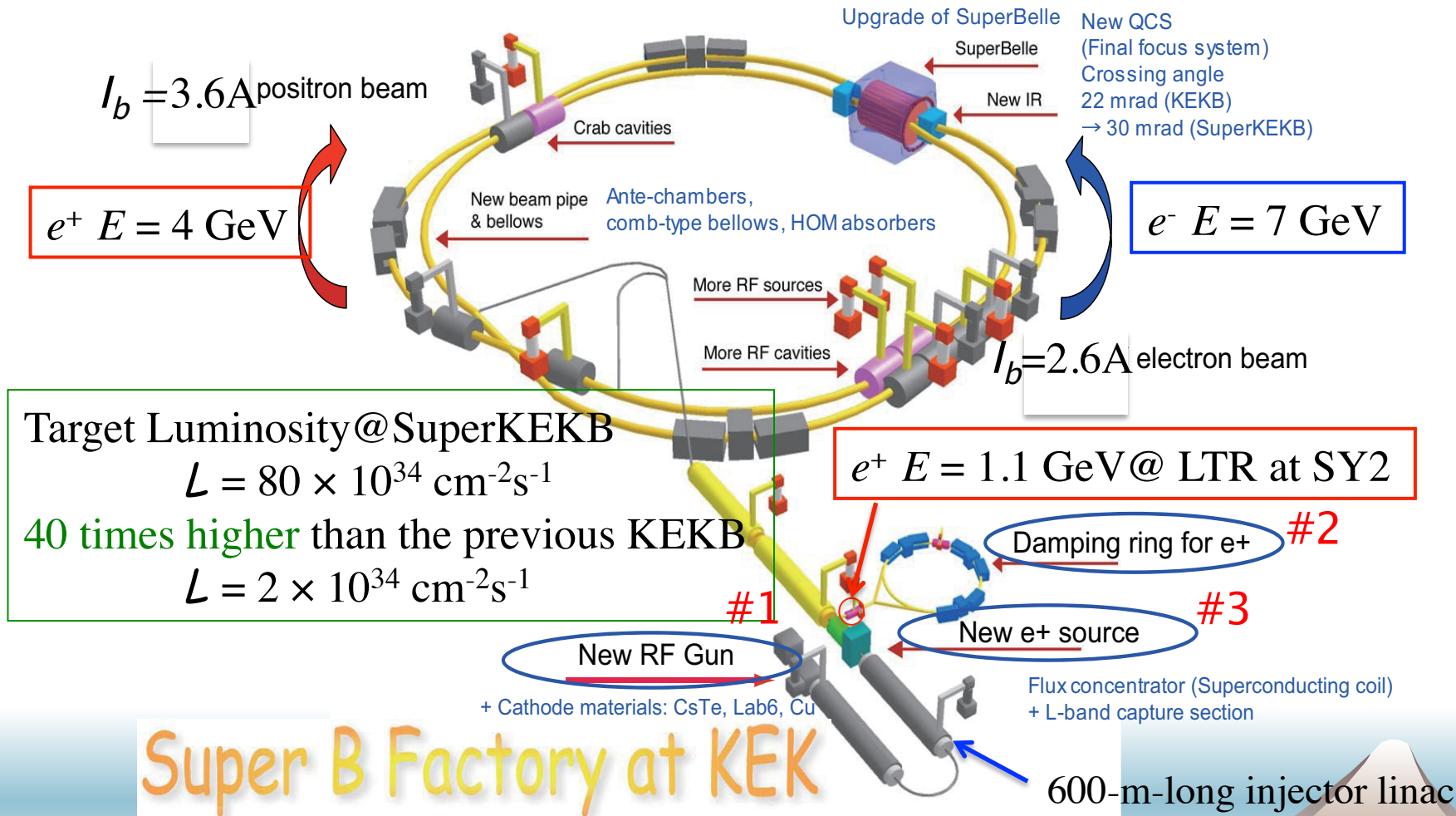
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Introduction

- 現在入射器では、次期計画SuperKEKB(Super B-factory)に向けた入射器増強とその高度化が進行中.
- タイミング配信システムは入射器高度化に向けた重要項目の1つ.
- Event-basedタイミング配信システムを現在増強中.
- タイミング配信システムに対しTDC-based 監視システムも構築中.
- VME/FPGA-based TDC (dynamic range > 20ms, time resolution ~ 1ns)の量産を終了した.

Super KEKB Accelerator Complex

Upgraded components for SuperKEKB



Super B Factory at KEK

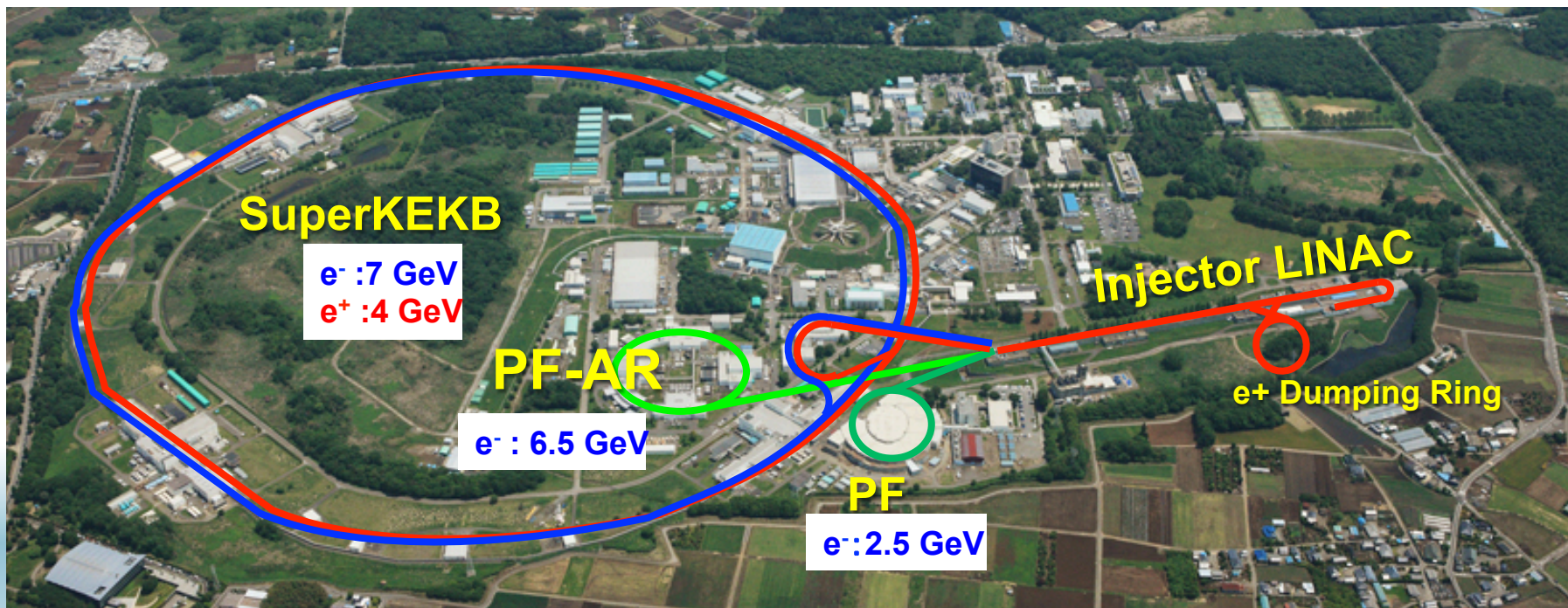
SuperKEKB Injector Linac

	KEKB (e+/e-) achieved	SuperKEKB (e+/e-) required
beam energy	3.5 GeV / 8.0 GeV	4.0 GeV / 7.0 GeV
stored current	1600 mA / 1200 mA	3600 mA / 2620 mA
beam lifetime	150 min / 200 min	10 min / 10 min
bunch charge	primary e ⁻ e ⁺ e ⁻ 10 -> 1.0 nC / 1.0 nC	primary e ⁻ e ⁺ e ⁻ 10 -> 4.0 nC / 5.0 nC
# of bunches	2 / 2	2 / 2
beam emittance ($\gamma\varepsilon$) _[1σ]	2100 mm / 300 mm	10 mm / 20 mm
energy spread σ_E/E	0.125 % / 0.05 %	0.07 % / 0.08 %
bunch length σ_z	2.6 mm / 1.3 mm	0.5* mm / 1.3 mm

* (assuming bunch compression after DR)

ICFA Mini-Workshop on Commissioning of SuperKEKB and e^+e^- Colliders

Essential Timing Issues for Simultaneous Injection



Takako Miura (KEK)

Tuesday 12 November 2013

Simultaneous top-up injection

Linac provides quite different types of beams for each ring.

⇒ More than 150 of Linac parameters are different.

Four rings are operated with top-up filling mode, “simultaneously”.

- The beam direction is changed in 50Hz.
- The above parameters are changed in each time.

Direction	Particle	Energy	Charge
KEKB HER	e^-	7.0 GeV	5.0 nC
KEKB LER	e^+	4.0 GeV	4.0 nC
PF	e^-	2.5 GeV	0.2 nC
PF-AR	e^-	6.5 GeV	5.0 nC

Fast control system is needed.

(The “star-topology” optical network is used also for this.)

Note, # of top-up rings:

3(KEKB) ⇒

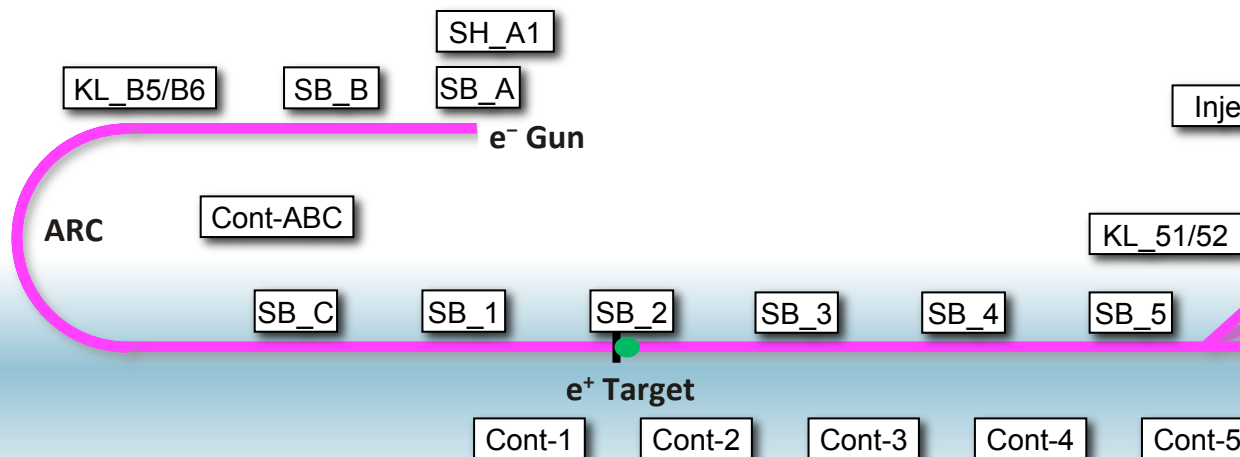
4(SuperKEKB)

e^- BT (PF: 2.5GeV, 0.2nC)

e^- BT (PF-AR: 6.5GeV, 5nC)

e^+ BT (SuperKEKB: 4GeV, 4nC)

e^- BT (SuperKEKB: 7GeV, 5nC)



Trigger timing distribution system (I)

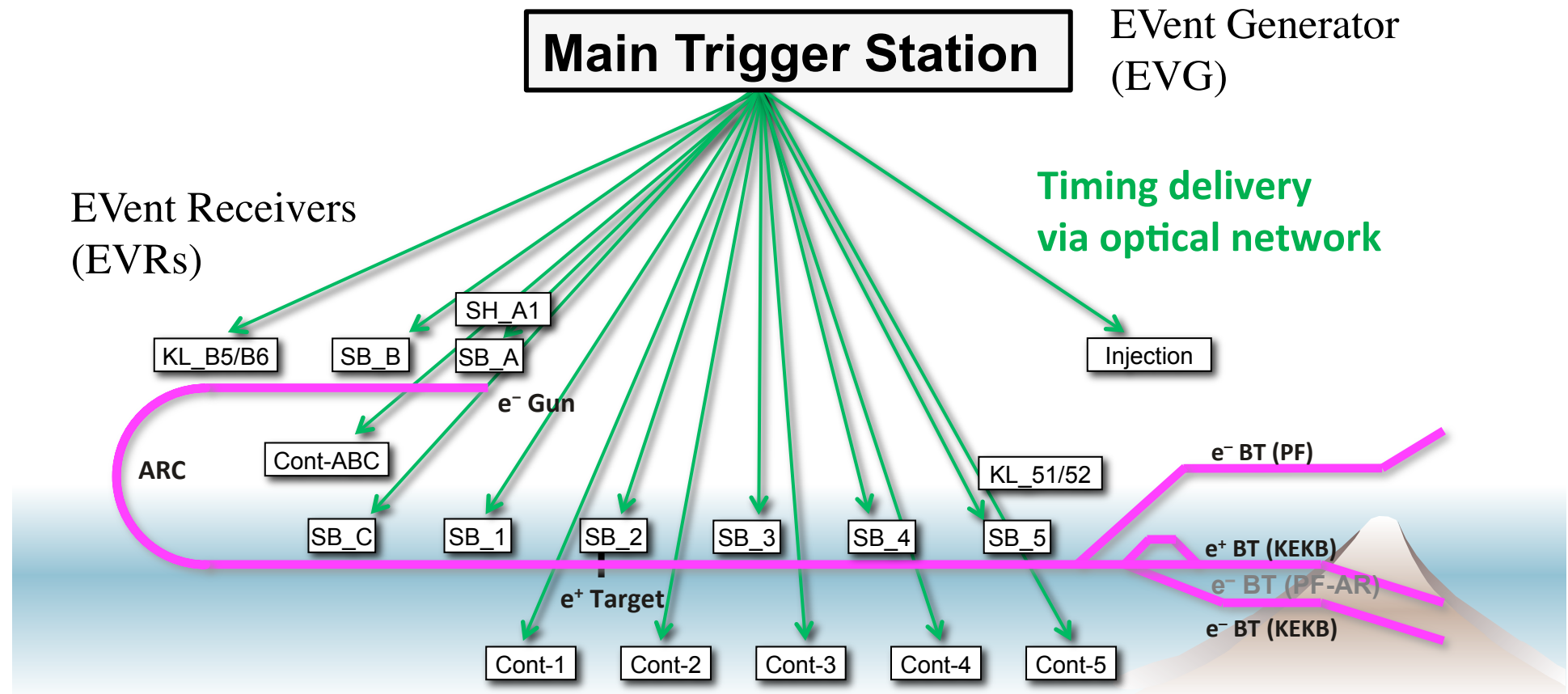
1. 4種類の異なるエネルギーをもつ電子陽電子を下流リングへ入射
 - SKEKB(高エネルギー実験): $E_{e^-}=7$ GeV, $E_{e^+}/E_{e^-}=4/3.5$ GeV,
 - PF, PF-AR(放射光実験): $E_{e^-}=2.5$ GeV, $E_{e^-}=3$ GeV
2. これを達成するために e^-/e^+ ビームをパルスごと(50Hz毎)に切り換え下流のリングへ供給(**Top-up injection**、蓄積電流を保持しながら継ぎ足し入射する方式、現在では主流)
3. 入射器では様々なパルスデバイスに異なるタイミングをパルスごとに切換えて配信(150パラメータ以上)
4. KEKB後半から**CAMAC-based system**から**VME-based Event Generator/Receiver (EVG/EVR) system**へ移行
5. KEKBでは、KEKB/PF両者へのTop-up injectionに成功(世界初)!
6. タイミング配信のわずかな誤動作も多大なマシン損傷へと発展
7. 信頼できるタイミング配信システムの監視システムが肝要

Large area synchronization

The functions of all Linac devices belonging to beamline must be synchronized, otherwise a beam cannot be transferred.

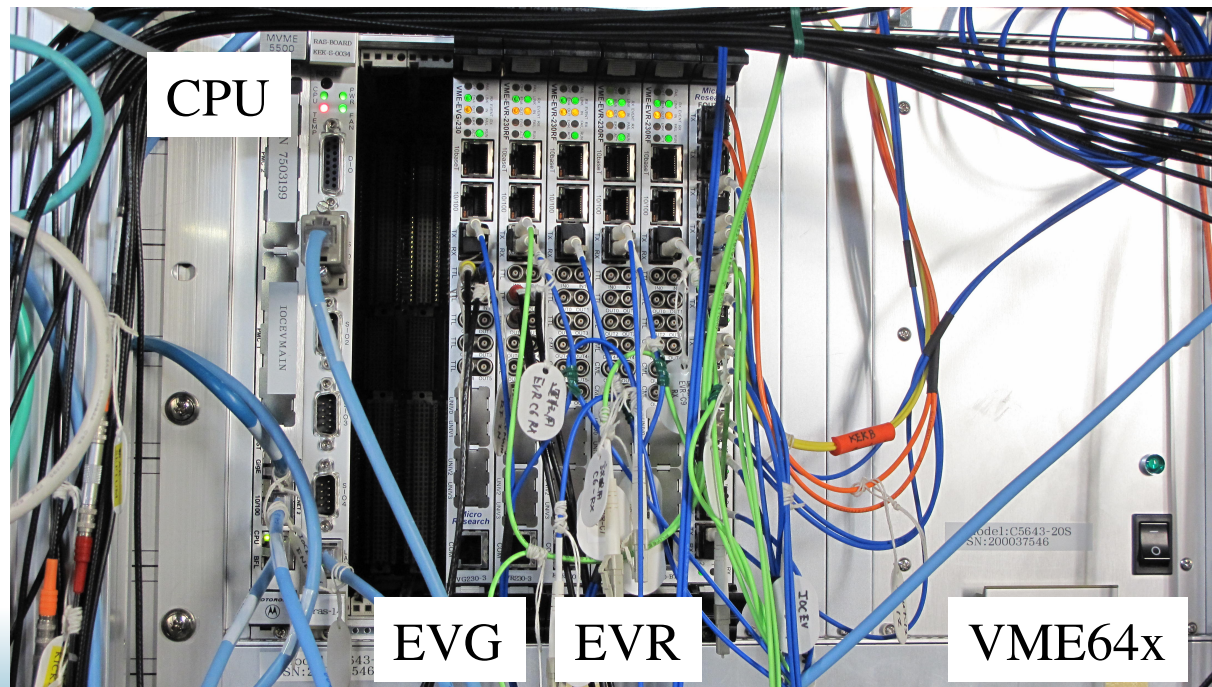
Main Trigger Station (or Main Timing Station) controls the operation.

- Timing synchronization of all devices.
- Delivering trigger via the “star-topology” optical network.



Trigger timing distribution system (II)

- 市販のEVG-EVRシステム(VME EVG230-EVR230R, Micro-Research Finland/MRF, CPU MVME-5500)を購入
- 複雑なタイミング配信スキームをソフトウェアで自在に生成可
- 2kB データバッファーをもち様々な情報の送受信可
- 送受信速度 57.12MB/s, EVG-EVR間は2.3GHz内部クロックで同期



117MHz rf clockに同期

Trigger timing distribution system (III)

- 入射器におけるパルスデバイス
 - パルス電磁石、電子銃、ビームモニター、高電圧クライストロン
 - キッカー/セプトム電磁石、

Table 1: Timing specifications required for the new trigger timing distribution system

Parameter	Value	Units
Trigger fiducial frequency	50	Hz
RF clock frequency	114.24	MHz
Clock precision (rms)	4.4	ps
Coarse time step	8.75	ns
Fine time step	400	ps
Timing jitter (rms)	10	ps
Delay dynamic range	> 1	s

VME/FPGA-based TDCの開発

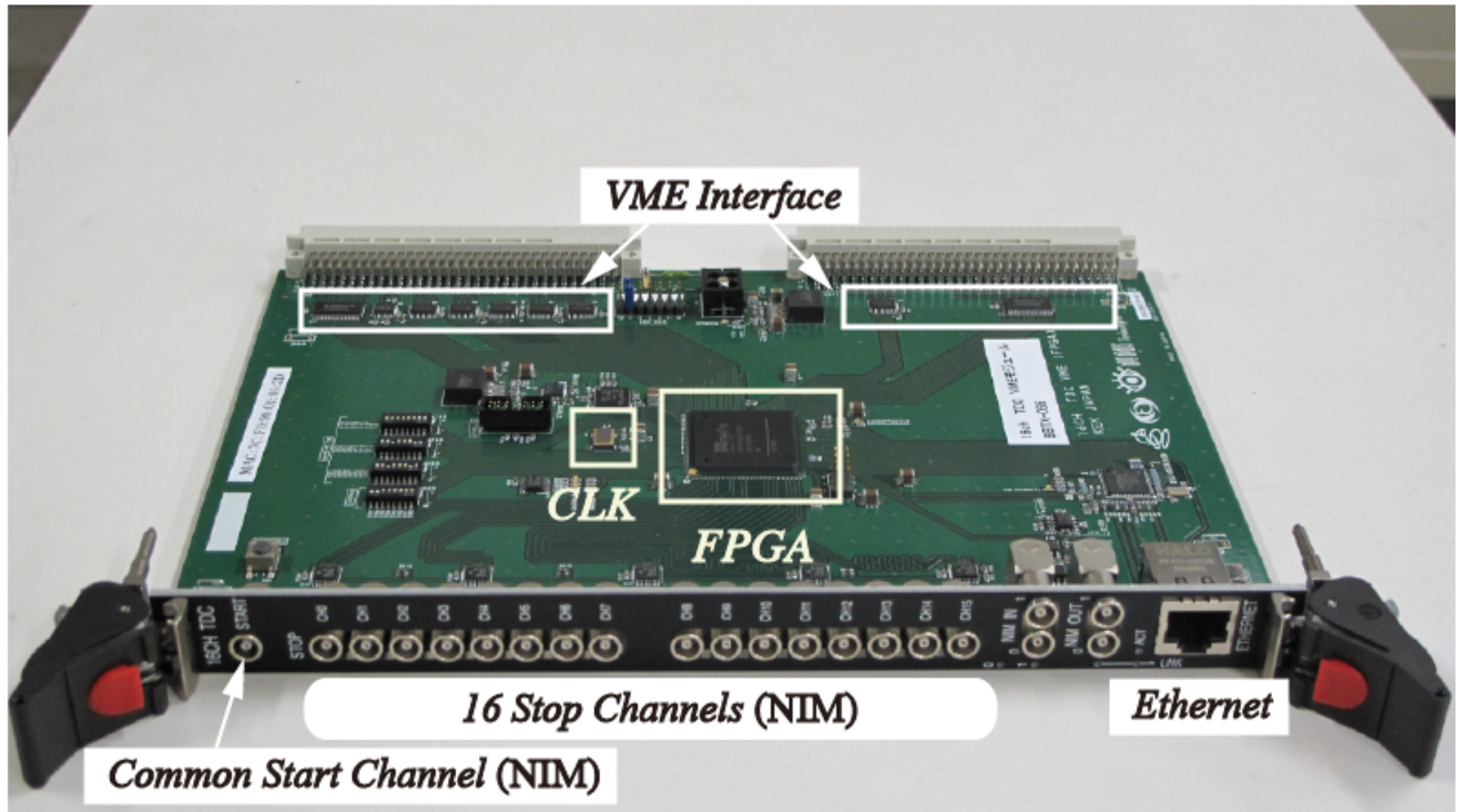
- タイミング配信システムに対する監視
 - 光ファイバーによるタイミングドリフト、タイミングジッターを監視
- 要求仕様
 - VME/FPGA-basedシステムで構築 (VME64x)
 - 入射器の基本トリガー周波数 50 Hz (リング周回周波数と同期)の監視
 - クライストロンの点火タイミングの要請、 20 ± 1 msの精度が必要
 - 広ダイナミックレンジの要請 (> 20 ms)
 - ビーム位置モニターへのトリガータイミングの要請 → 高精度の要請 (~ 1 ns)

Table 2: Basic specifications designed for the VME/FPGA-based TDC

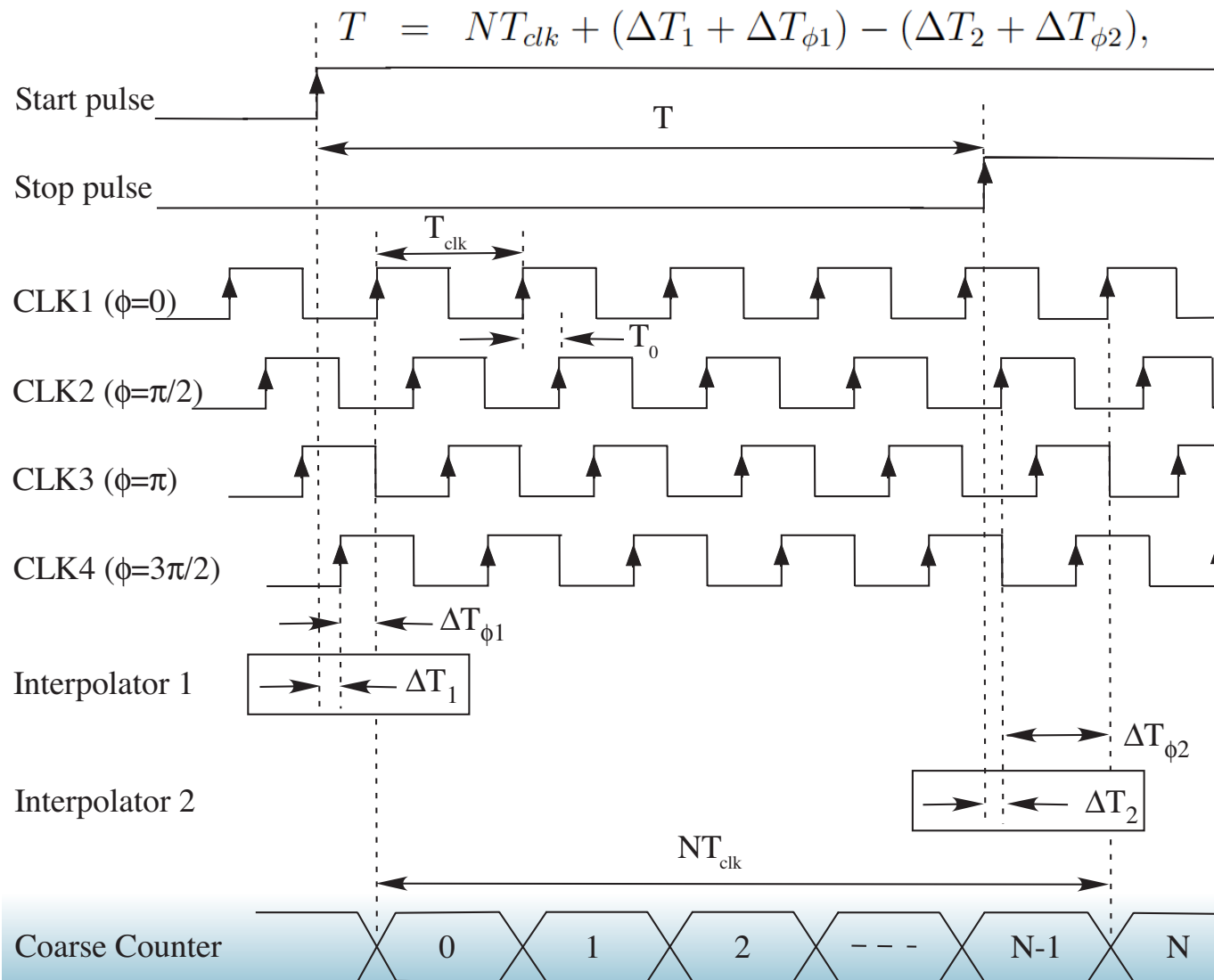
Basic parameter	Value	Units
Number of common starts	1	
Number of stops	16	
Number of multistops	4	
Number of bits	32	
Dynamic range (max.)	4.3	s
Resolution	1	ns
Clock frequency	250	MHz
Gigabit Ethernet	available	

- Xilinx Spartan-6 (XC6SLX75) FPGA
- SiTCP giga-bit Ethernet embedded

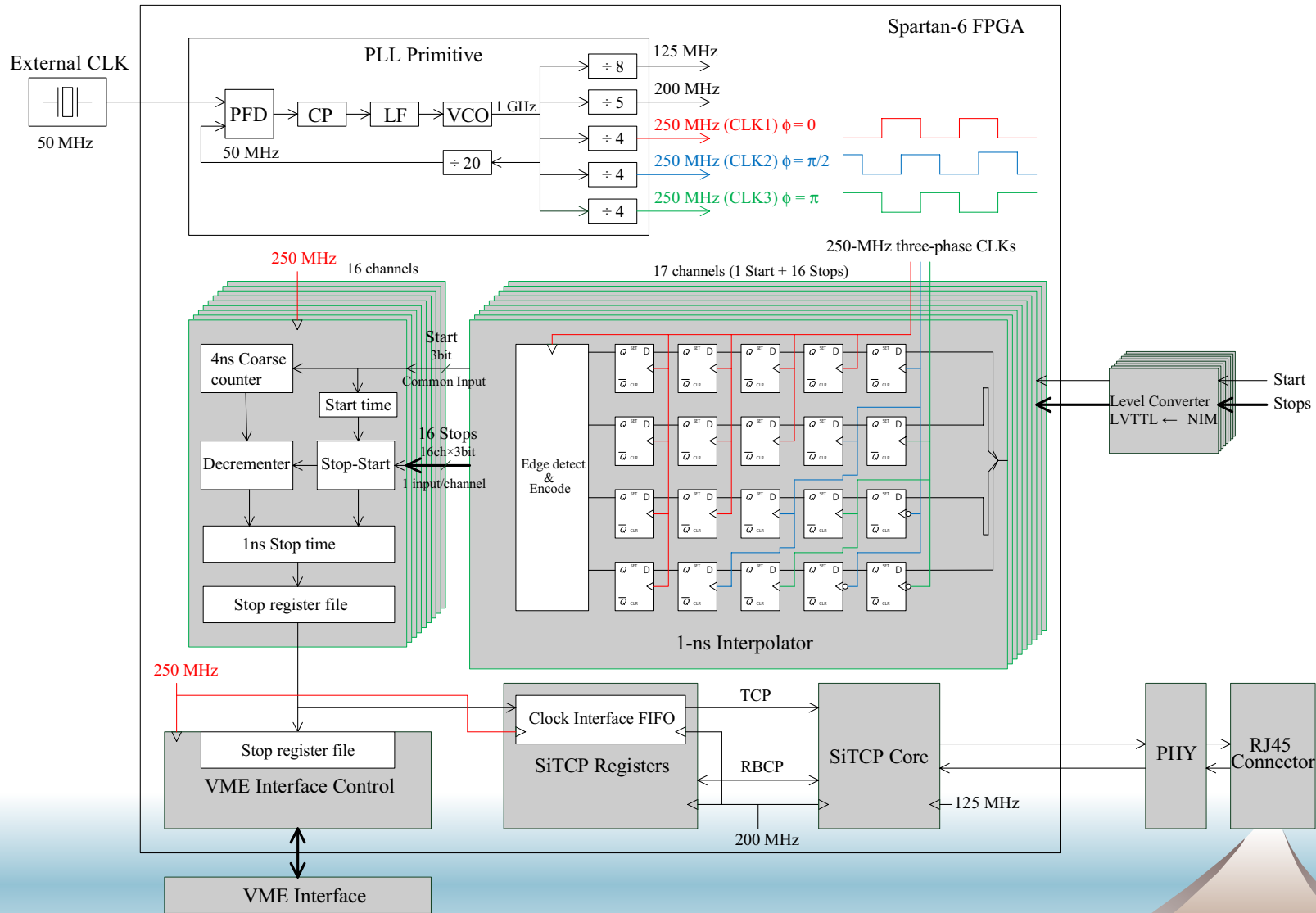
VME/FPGA-based TDCの開発



TDC with multisampling technique



Circuit architecture of FPGA-based TDC



Specification of an external clock with TCXO

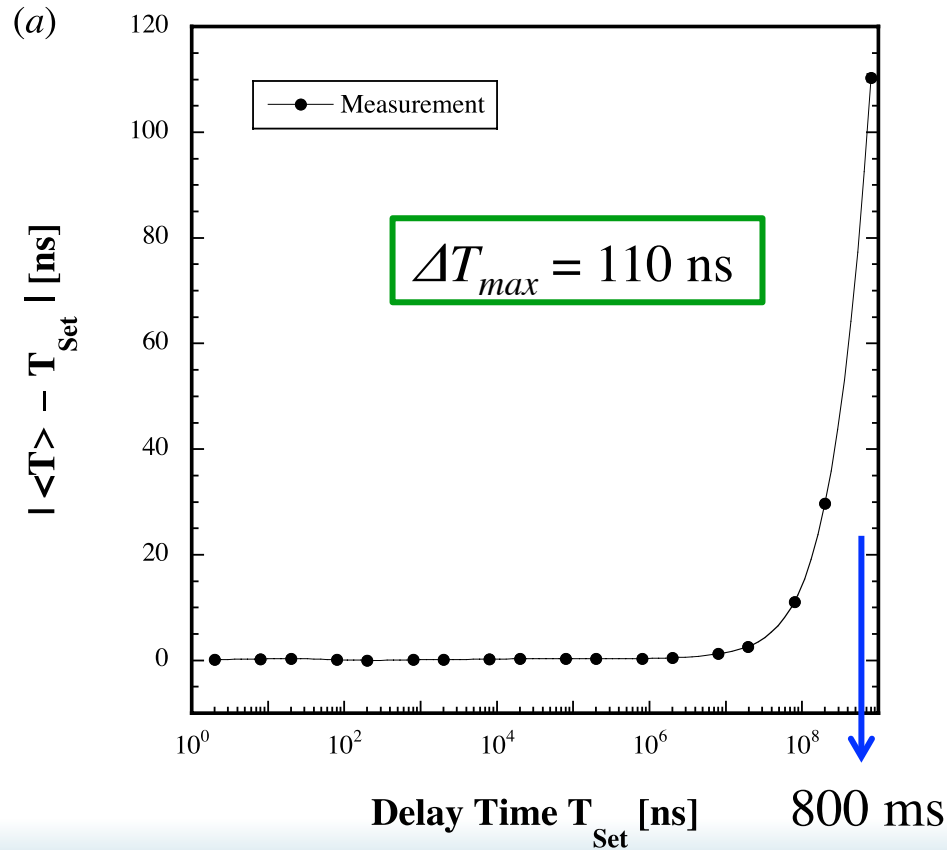
TCXO, EPSON TG-5501CA

Table 3: Specifications of the external clock

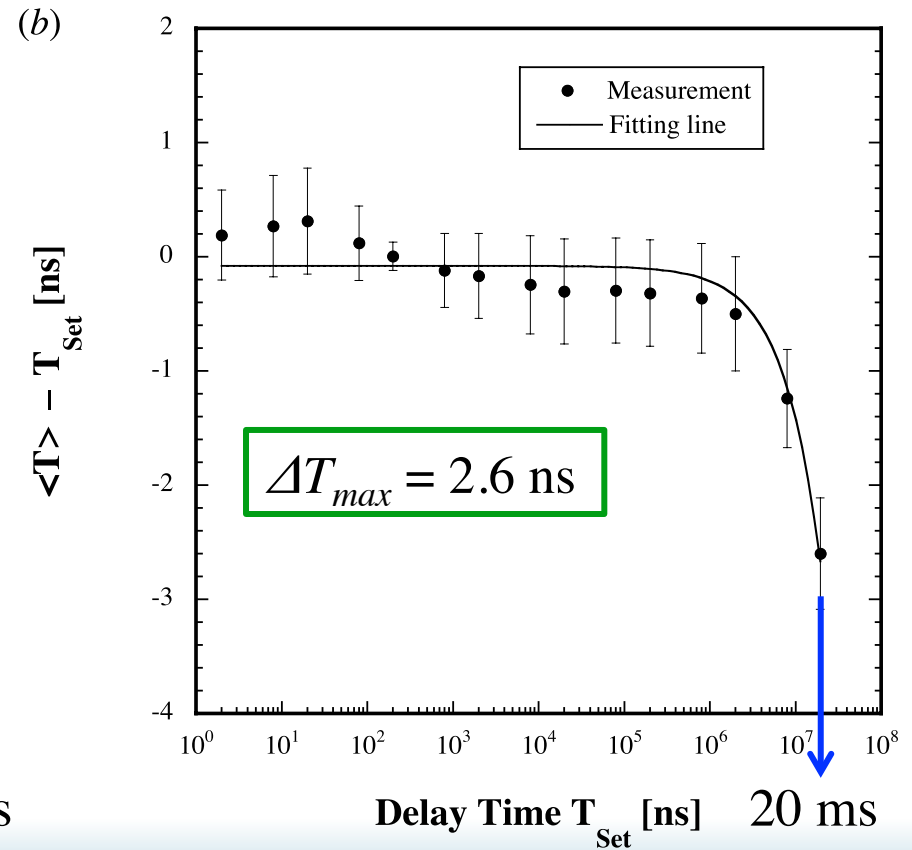
Parameter	Value	Remarks
Clock frequency	50 MHz	
Frequency stability	$< \pm 1.0 \times 10^{-6}$	$T_e = 25 \pm 2^\circ\text{C}$
Temperature characteristics	$< \pm 0.28 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$	$T_e = -40 \text{ to } 85^\circ\text{C}$

Delay time T_{set} vs. $\langle T \rangle - T_{set}$

with a test pulser, SRS Model DG645

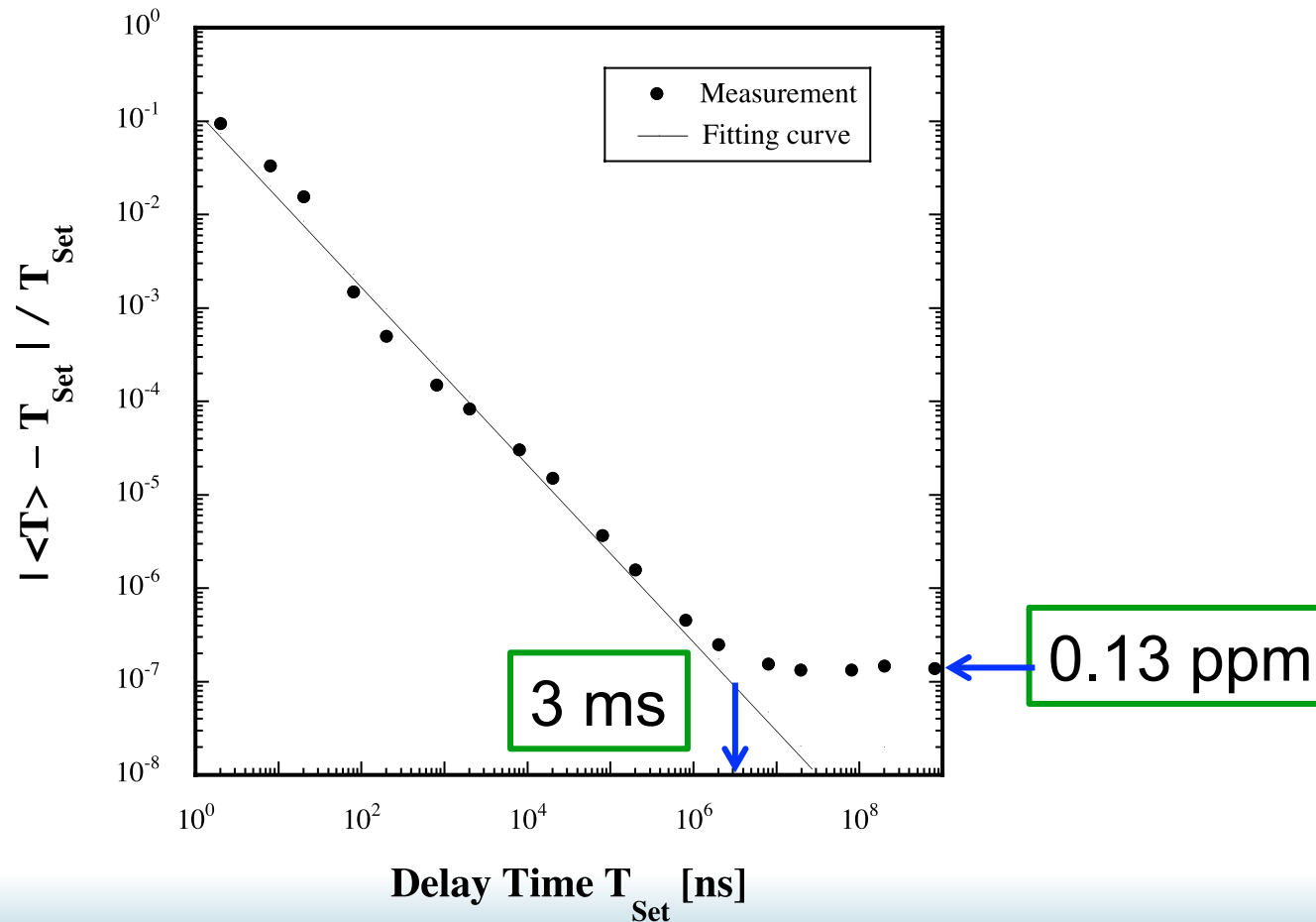


Wide range

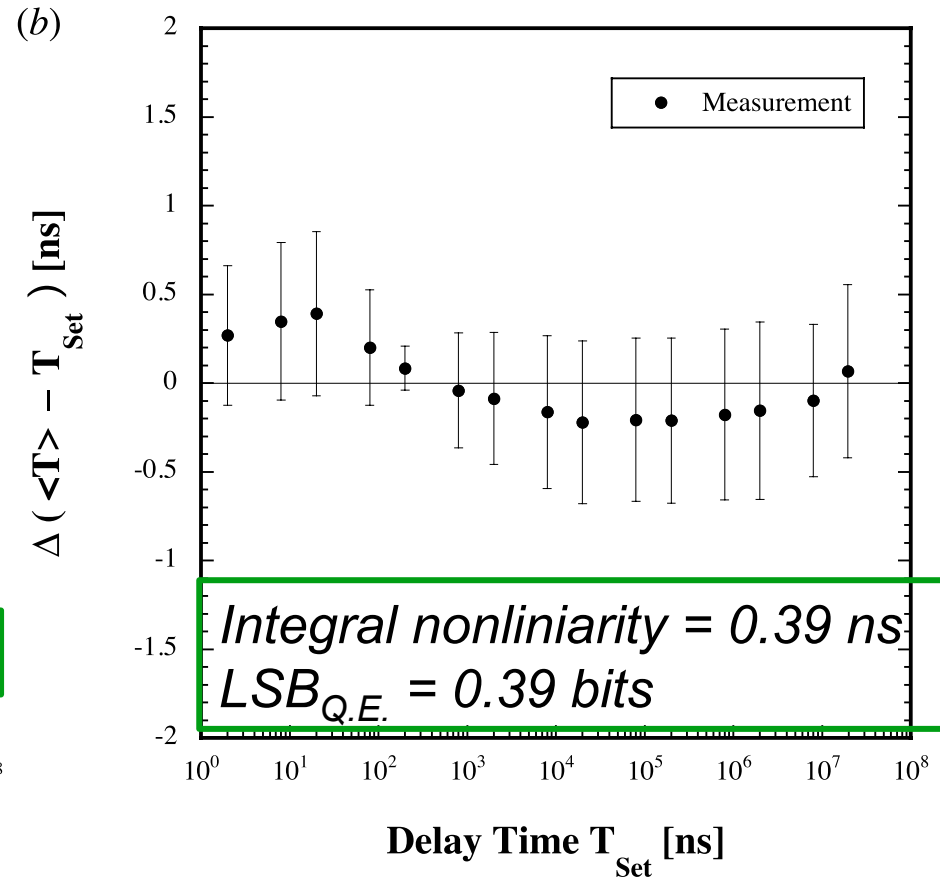
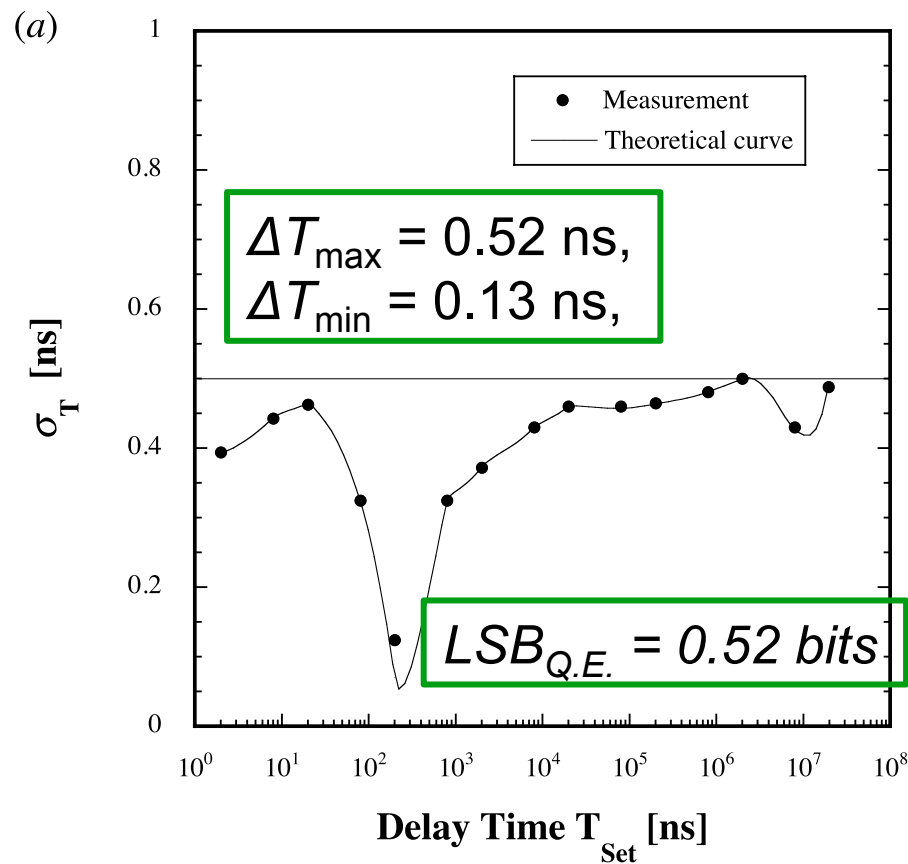


Required range

Delay time T_{set} vs. $|\langle T \rangle - T_{\text{set}}| / T_{\text{set}}$

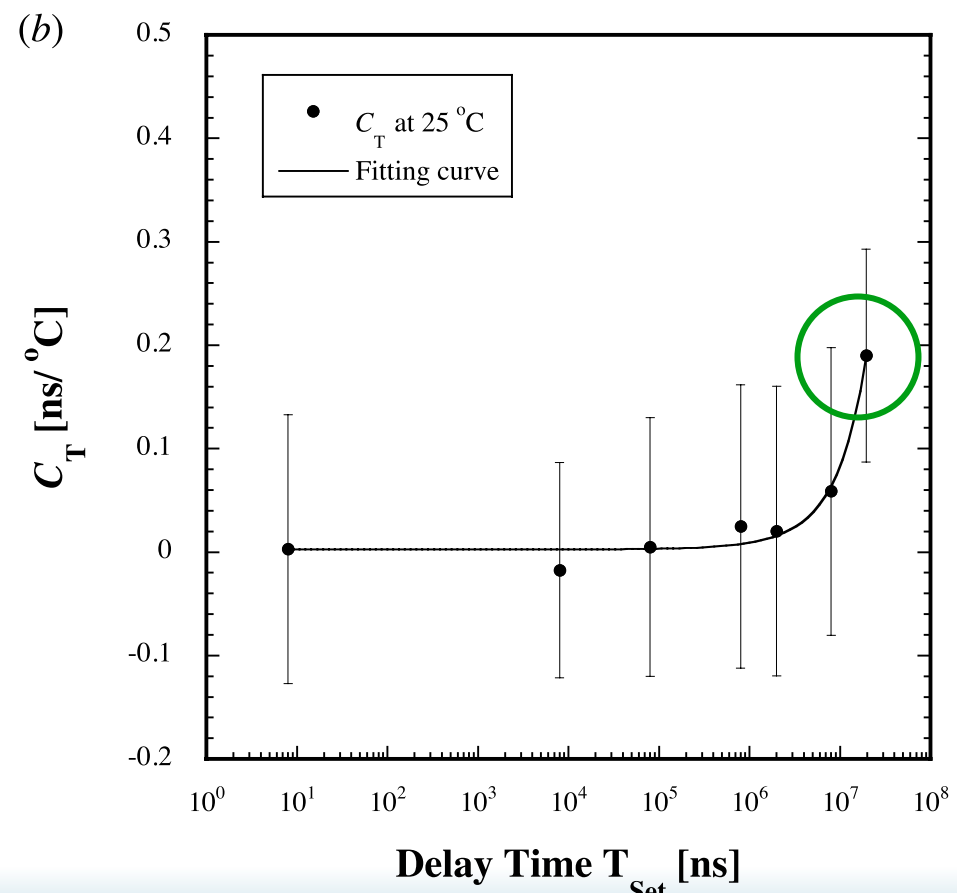
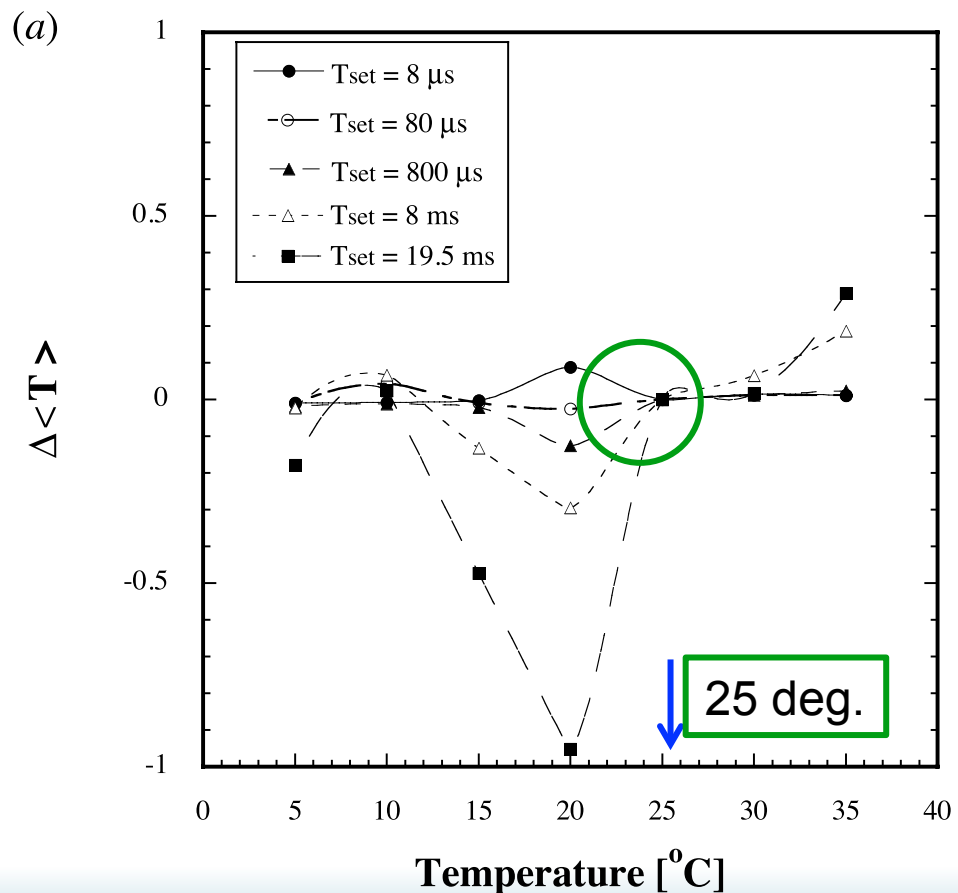


Quantization error & Integral nonlinearity measurements



$$c = Frc [T/T_0], \sigma_T = T_0 \sqrt{c(1-c)}$$

Temperature dependence and gradient measurements



$$C_T = \sim 0.2 \text{ ns/deg.} @ T_{set} = 20 \text{ ms}$$

Summary

1. We have successfully fabricated and tested a new VME/FPGA-based TDC with a wide dynamic range greater than 20 ms and a resolution of 1 ns.
2. The required specifications of the TDC were realized on the basis of the suitable design with a high-precision temperature-compensated external clock with an accuracy of 0.13 ppm.
3. The obtained results show that the accuracies of the time-duration measurements are less than 1 ns and 2.6 ns within dynamic ranges of 7.5 ms and 20 ms, respectively.

Acknowledgment

1. The authors wish to thank the Open Source Consortium of Instrumentation (Open-It) of KEK for its cooperation and advice on the electronics design of this work.

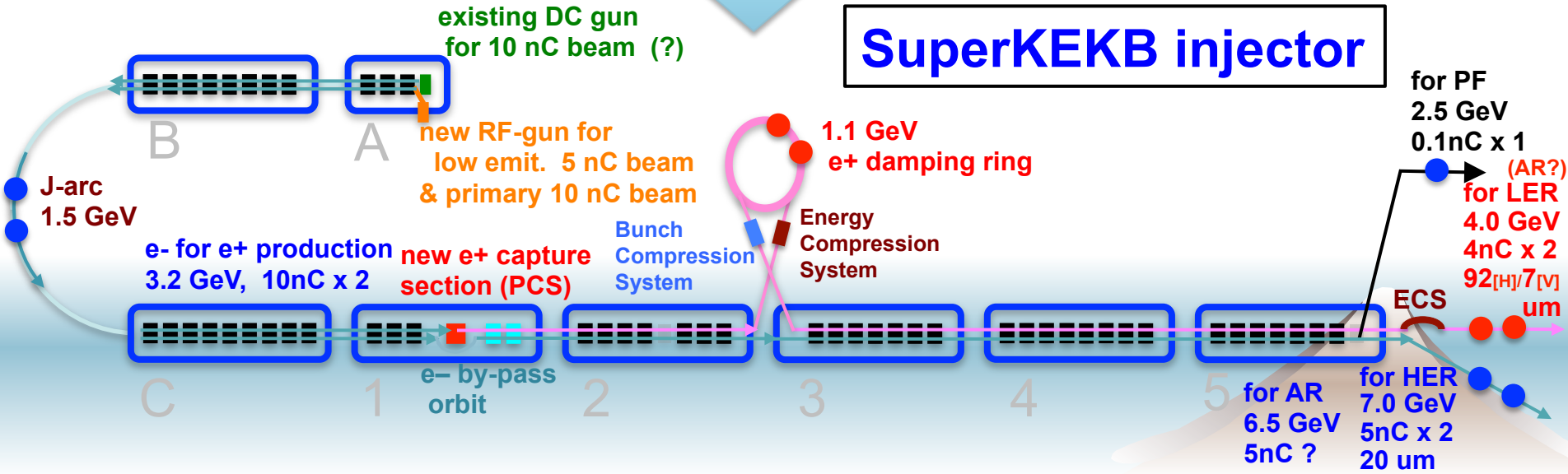
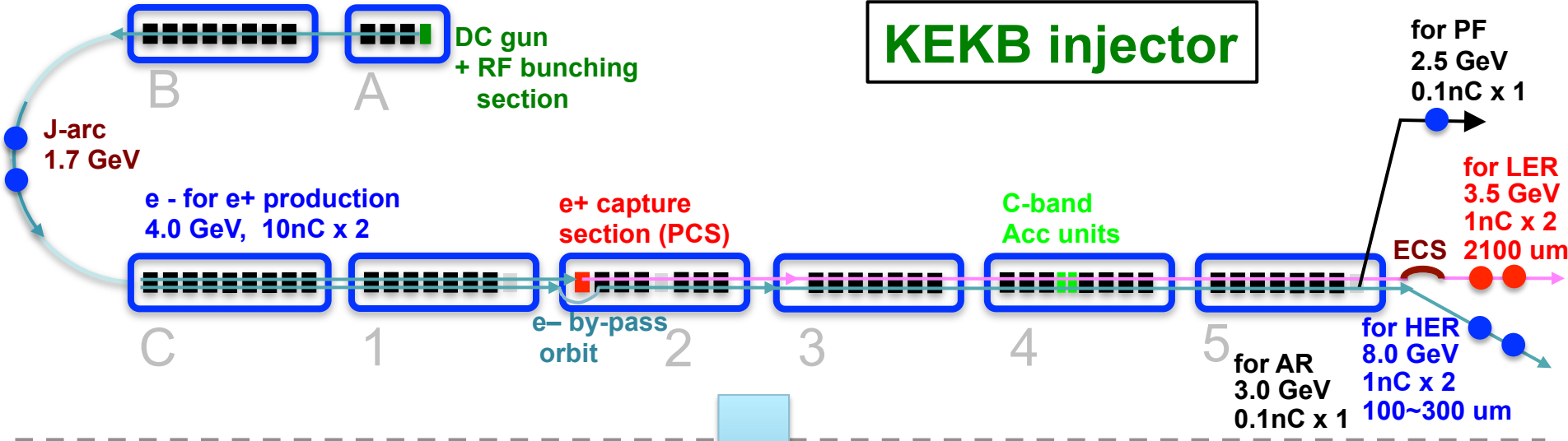
Backup files

SKEKB Parameters

	2011 Feb. HER no wiggler	2012 Feb. HER 60% wigglers
Energy (GeV) (LER/HER)	4.0/7.00729	4.0/7.00729
β_y^* (mm)	0.27/0.30	0.27/0.30
β_x^* (mm)	32/25	32/25
ϵ_x (nm)	3.2/5.3	3.2/4.6
ϵ_y/ϵ_x (%)	0.27/0.24	0.27/0.28
σ_y (nm)	48/62	48/62
ξ_y	0.0897/0.0807	0.0881/0.0801
σ_z (mm)	6/5	6/5
I_{beam} (A)	3.6/2.6	3.6/2.6
N_{bunches}	2500	2500
Luminosity ($10^{34} \text{ cm}^{-2} \text{ s}^{-1}$)	80	80

HER ϵ_x with 60% wigglers is used as the nominal value. Lower HER ϵ_x can relax some other parameters ($\beta_{x/y}^*$, ϵ_y/ϵ_x , etc.). At present, larger ϵ_y/ϵ_x in HER is adopted.

e+/e- injector upgrade



SuperKEKB での Linac の役割

▲ 40 倍の Luminosity のために

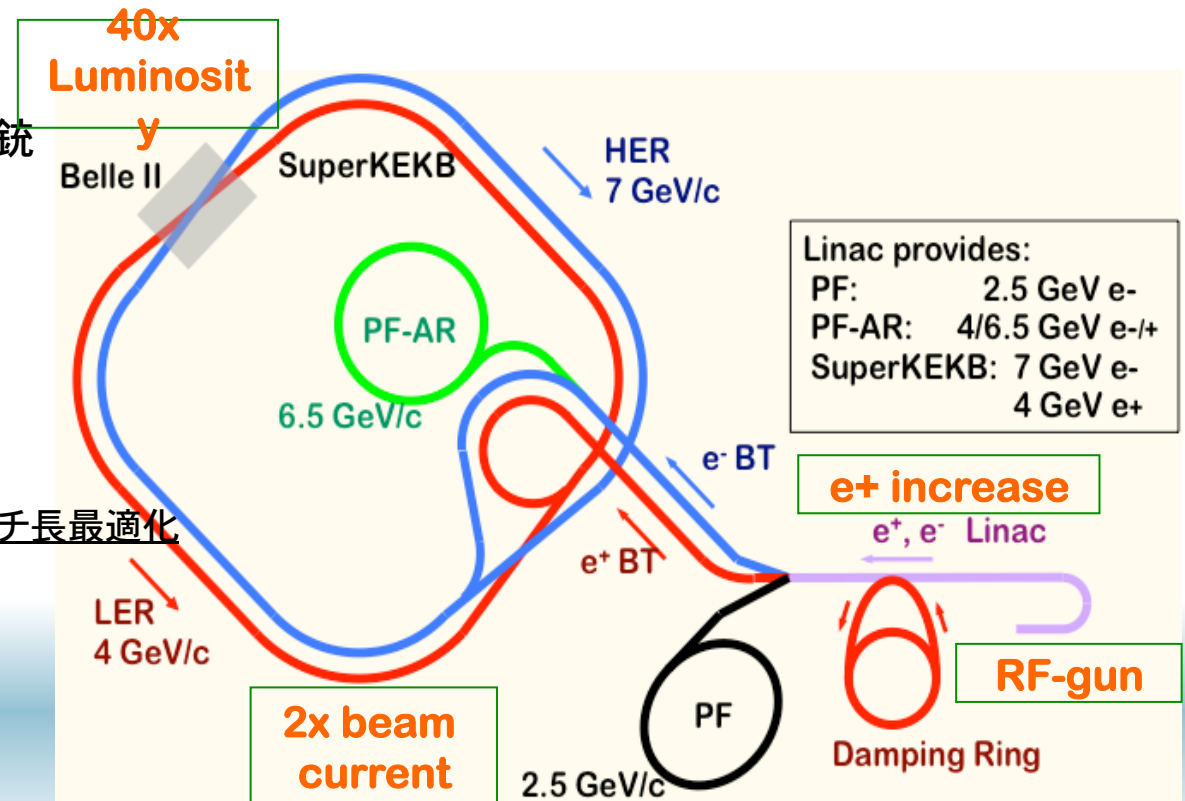
- 2 倍の蓄積電流
- ナノビームによる 20 倍の衝突率
 - → 低エミッタンスの入射ビーム
 - → 短いビーム寿命

→ Linac のビーム電流の増強 (特に陽電子)

→ Linac のビーム電流の増強

▲ Linac での試練

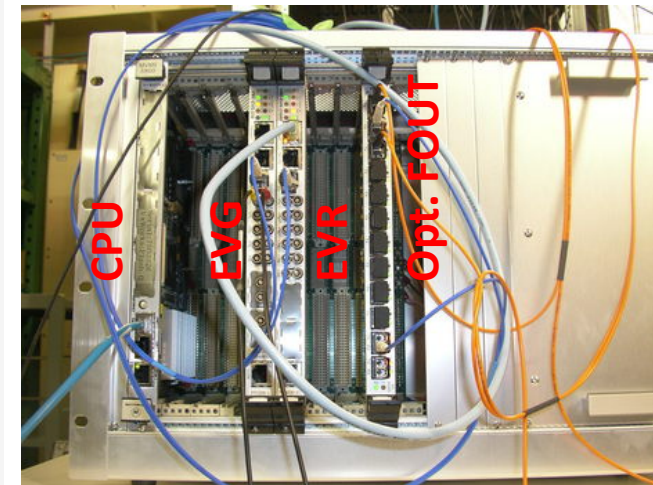
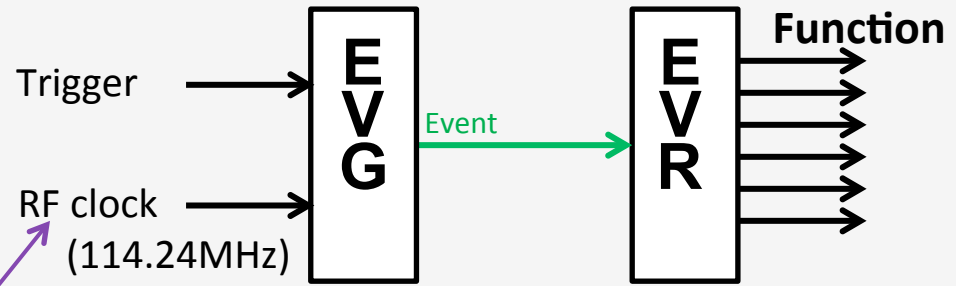
- 低エミッタンス電子
 - 大電流光陰極 RF-電子銃
- 低エミッタンス陽電子
 - ダンプリングリング
- 陽電子ビームの電流増強
 - 新しい Capture section
- 低エミッタンスビーム輸送
 - ベータatron 振動軌道・バンチ長最適化
 - (BNS ダンプング)
 - アライメント、安定化
- 4+1 リングの同時入射
 - ダンプリングリング、レーザ



Event Timing System

MRF modules are used. { Event Generator (EVG) VME-MRF-230
Event Receiver (EVR) VME-MRF-230RF

EVG: sending 256 kinds of Event (Code#0-#255)
EVR: function can be programmed for each Event Code#
One optical cable can be considered as 256 signal lines in parallel. Timing accuracy of this system: typically <15ps.



	EVG	EVR
Internal clock	Synchronized with input RF clock	locked by Event (synchronized with EVG)
Trigger	Input TTL	Event
Function	Event sending, up to 2048 Events in a trigger	NIM/TTL signal production, CPU interrupt



delivered from the KEKB main ring

Trigger timing distribution system (II)

- 入射器中央にタイミング送信機@Main EVGを設置
- 入射器ラインに沿って受信機EVRを設置
- EVG-EVRは光ファイバーでスター接続される

