1. Basics of digital circuit (review)

v3.8
2024/06/20

Outline

- Preview
  - Introduction
    - FPGA
    - Features of digital technology
    - Data acquisition system and digital circuit
    - Standard IO
    - Numbering system
  - Digital circuit
    - The 4 basic elements
    - Combinational circuit
    - Sequential circuit
- Recent Front-End circuit and technology of integration

FPGA

Field Programmable Gate Array (FPGA)
A kind of Programmable Logic Device (PLD)

Digital circuit is easy for integration!

- Integrated circuit
  - Can be realized only with digital circuit
  - For example, a size of ~2x2 cm^2

- To use it, user writes circuit's information
  - Use it just like software
  - But, notice, it is not software!
    - Writing the circuit information, not CPU program

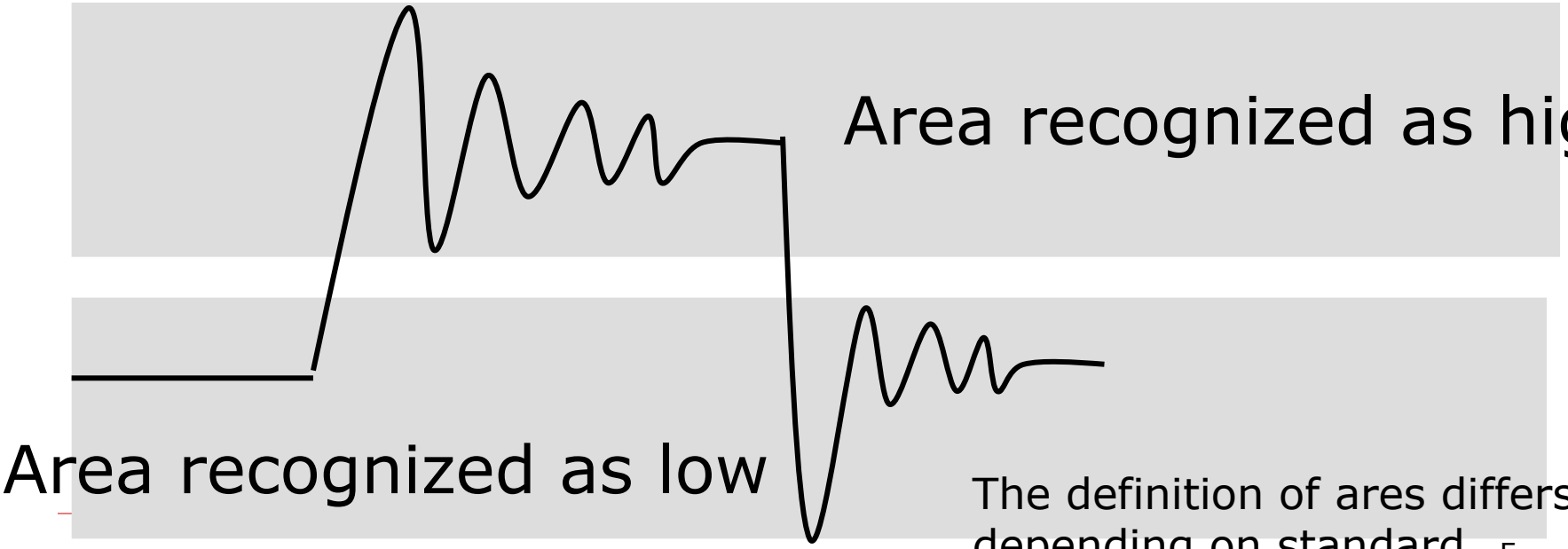
Features of digital circuit

Features of digital circuit

To give an example:

robust against noise!

Still OK for this kind of bad situation



The definition of ares differs depending on standard.

Drawback of digital circuit

- Number of signals increases
  - Only two values (0 and 1) can be sent through a channel
  - Multiple channels = a number
    - Number of channels = number of bits
    - 8 bits can represent from 0 to 255
- Scale of the circuit (number of transistor) increases
  - Huge number compared to analog circuit

No longer a problem the recent development of microfabrication technology

- Easy to generate noise

Be careful about the effect on analog circuit

Data acquisition system and digital circuit

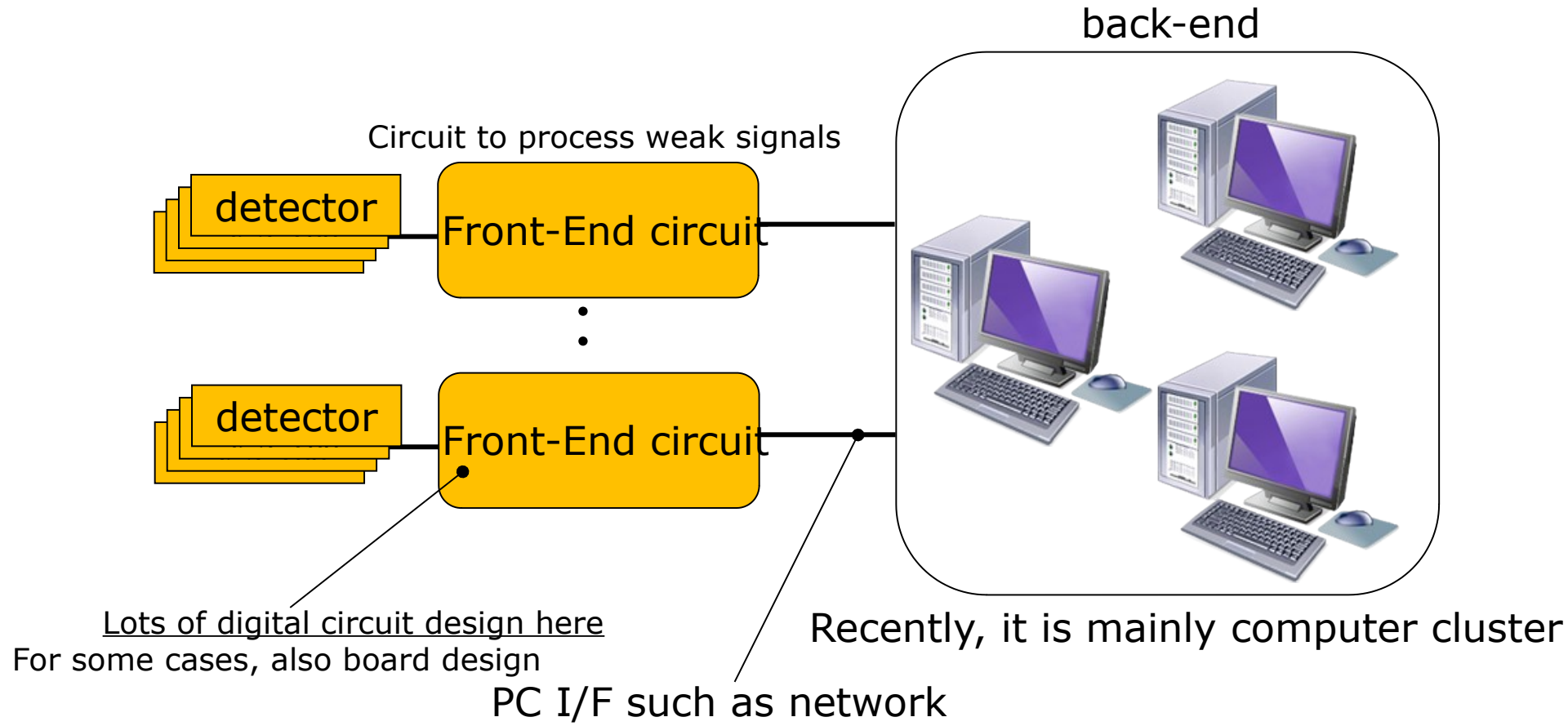
Where to use digital circuit (FPGA)

- The circuits which can be implemented on FPGA is digital circuit.
- Explain the digital circuits utilized in DAQ system
- Finally, explain what kind of functions implemented on the FPGA.

Following content

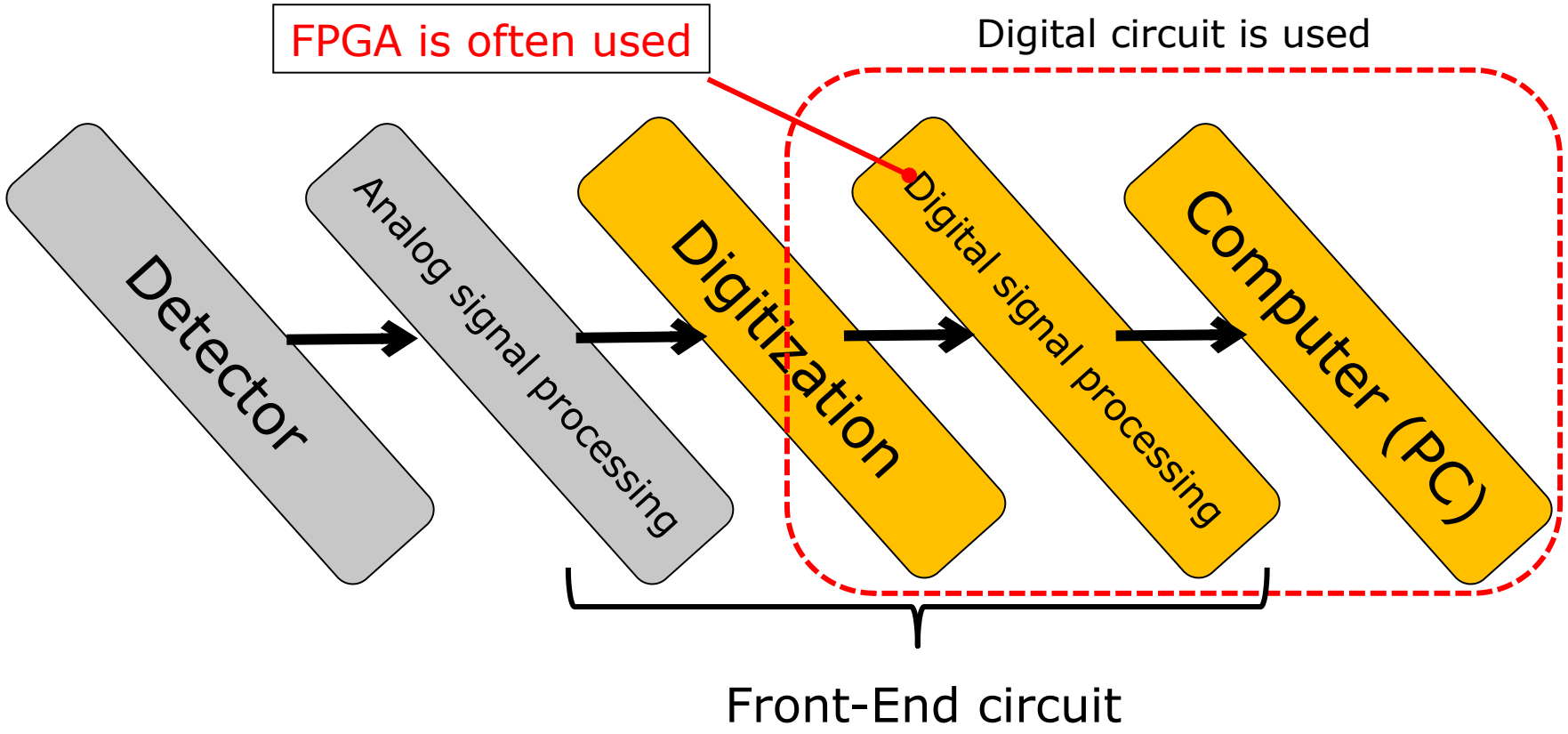
- Measurement system
- Front-End circuit
- Functionalities implemented on FPGA

Measurement system



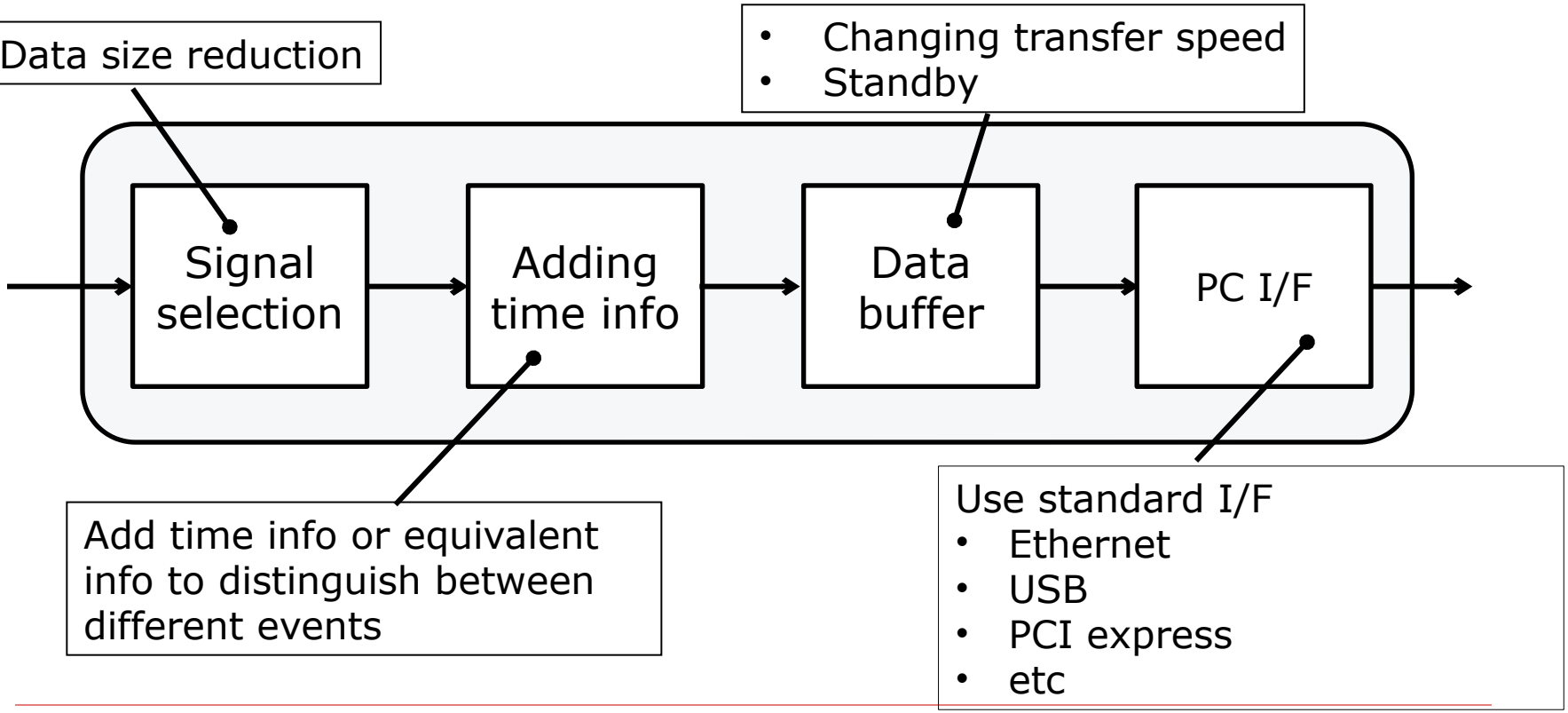
Where to use FPGA

Large fraction of using digital circuit!



Functionalities to be implemented on FPGA

Features are included in many digital processing blocks



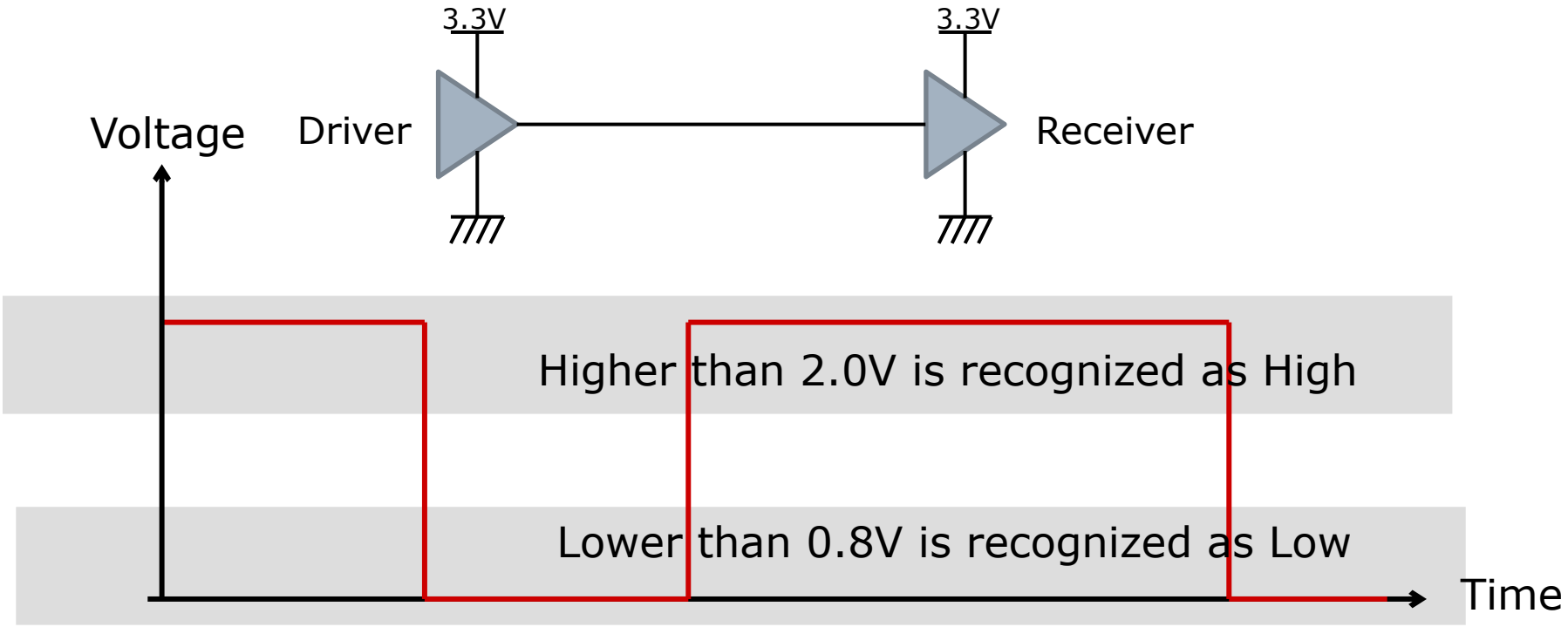
Summary so far

- FPGA is digital circuit
- Where to use digital circuit
  - From the ADC in the Front-End circuit to the back-end
- FPGA is used as a signal processing circuit in Front-End

Standard I/O format

LVCMOS

Here is an example of LVCMOS33
(Different standards are established depending on the power supply voltage)

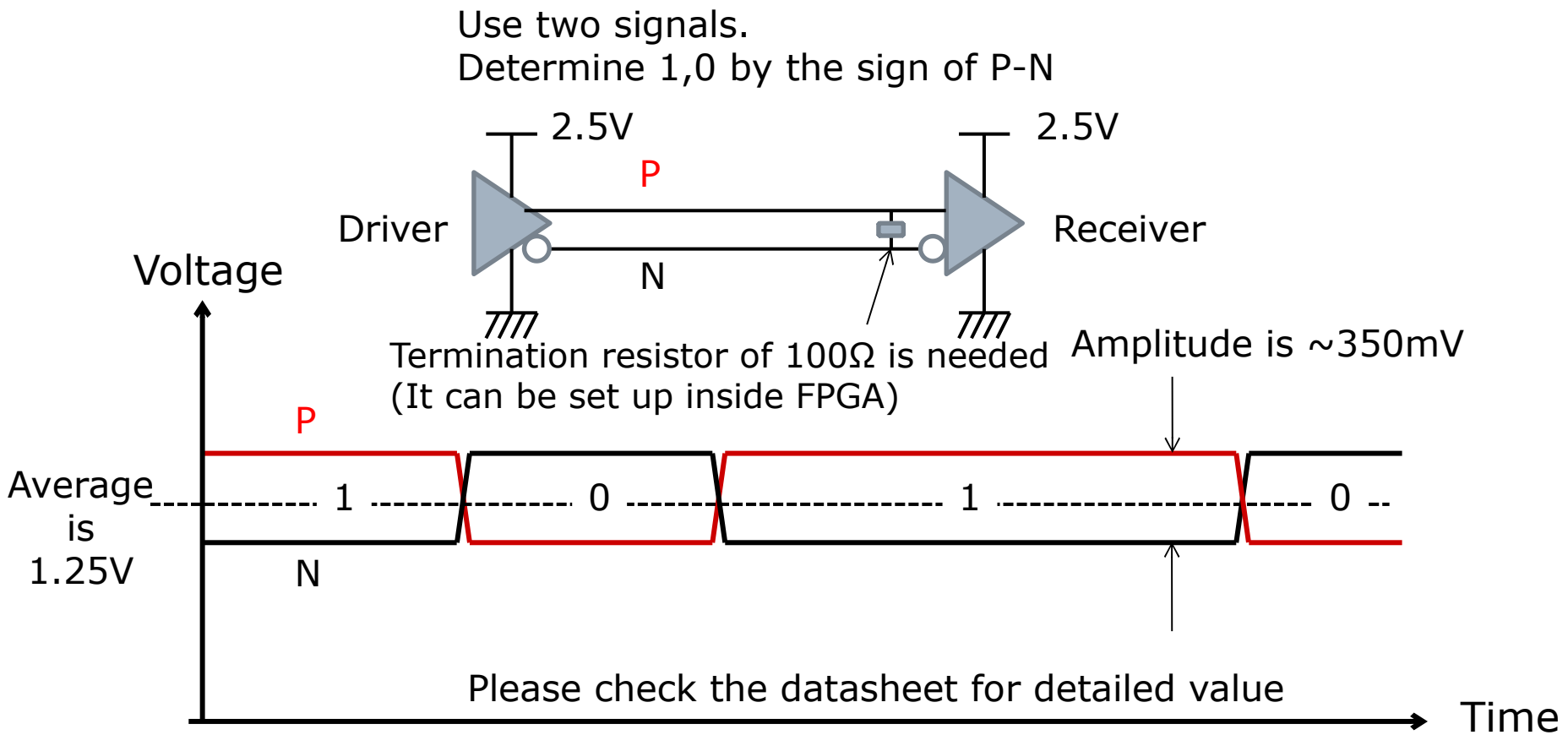


LVDS

Low Voltage Differential Signaling

Signal format suitable for high speed

Typical for different signal



Numbering system

Binary/Hex representation

Integer representation

$$N = \sum_{k=0}^{n} a_k B^k$$

B is base, a_k is coefficient ∋ {0,...,B-1}

ak is expressed by arranging from right to left, from the smallest k

To distinguish from decimal, put "0x" for hex, and put "0b" for binary

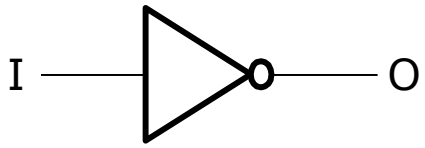
Decimal	Hex	Binary
0	0x0	0b0
1	0x1	0b01
2	0x2	0b10
3	0x3	0b11
4	0x4	0b100
5	0x5	0b101
6	0x6	0b110
7	0x7	0b111

Decimal	Hex	Binary
8	0x8	0b1000
9	0x9	0b1001
10	0xA	0b1010
11	0xB	0b1011
12	0xC	0b1100
13	0xD	0b1101
14	0xE	0b1110
15	0xF	0b1111

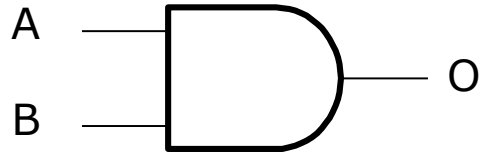
The 4 basic elements for digital circuit

Basic elements for digital circuit

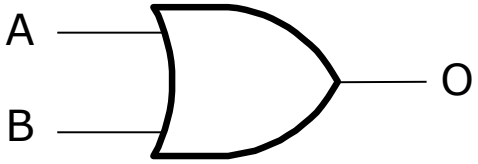
Inverter



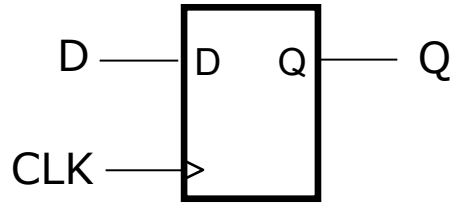
AND gate



OR gate



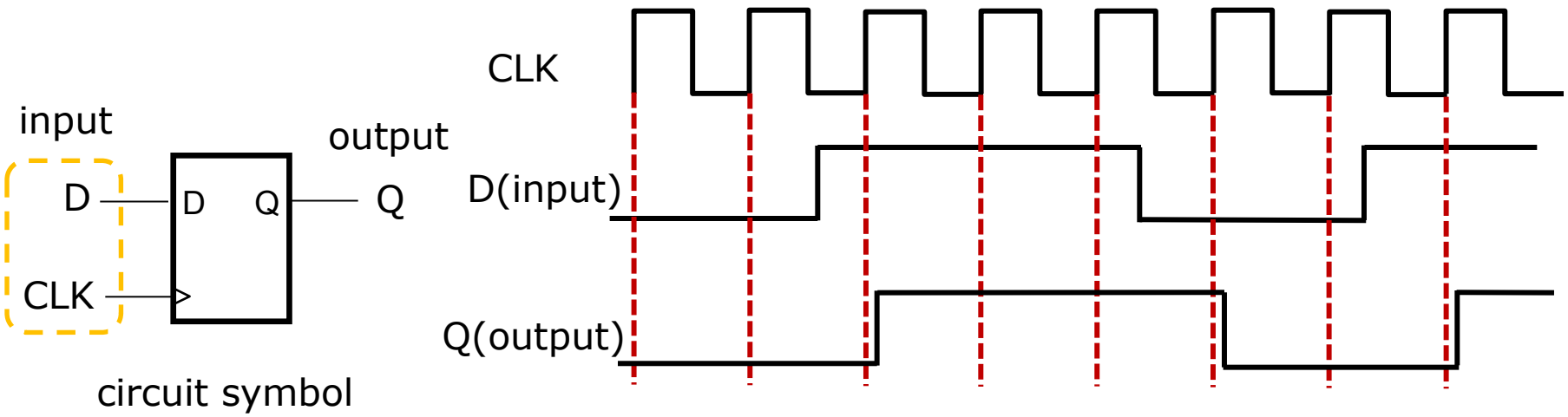
D-type flip-flop (DFF)



All the digital circuits are based on only these 4 elements (circuits).

Even for complicated thing like CPU, still possible to make it with them.

D-type flip-flop (DFF)



- At the rising edge of the CLK, input D is outputted to Q.
- Output Q is held until the next CLK rising edge.

Types of digital circuits

Types of digital circuits

Circuit whose output does not depend on history in the past

- Usually, the output is combination of inputs
- Called combinational circuit

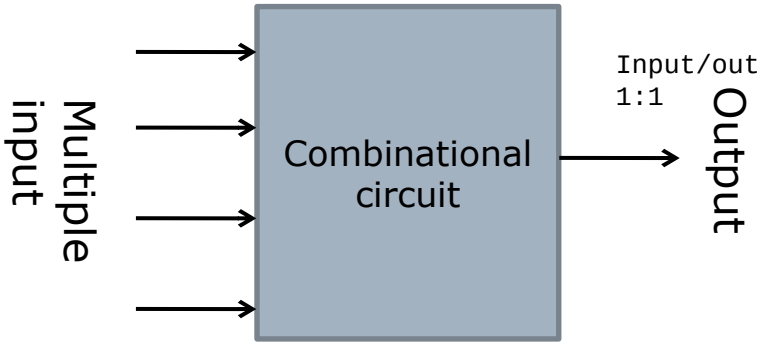
Circuit whose output depends on history in the past

- The output is combination of inputs and the history
- Called sequential circuit

Combination circuit and sequential circuit

Combination circuit

Circuits without memory element

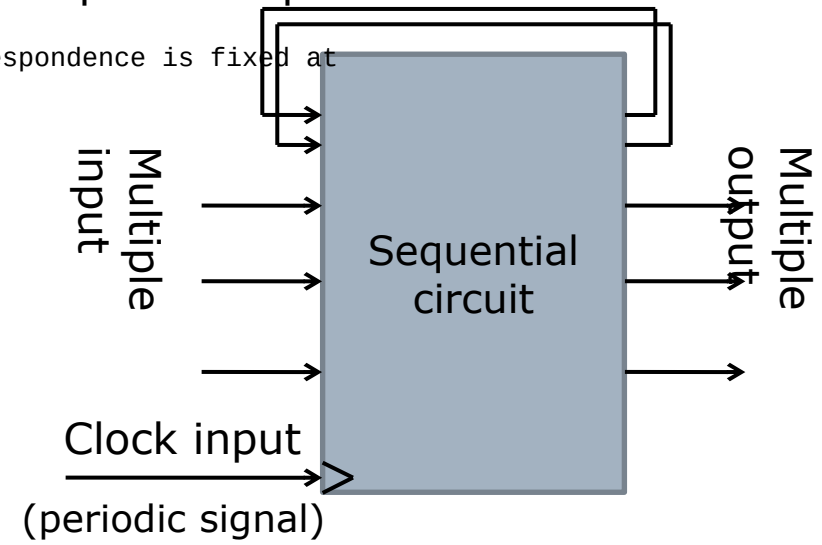


Correspondence between input/output is fixed as 1:1.

Sequential circuit

Circuits with memory element

Connect some of the memory elements' outputs to input



Combination circuit

Combination circuit

- Circuits without memory element
  - Made of only AND, OR, NOT
  - The relation between input and output is uniquely determined
  - Input/output relation can be expressed as a table

Detect the desired state

EX: the coincidence between detected signals

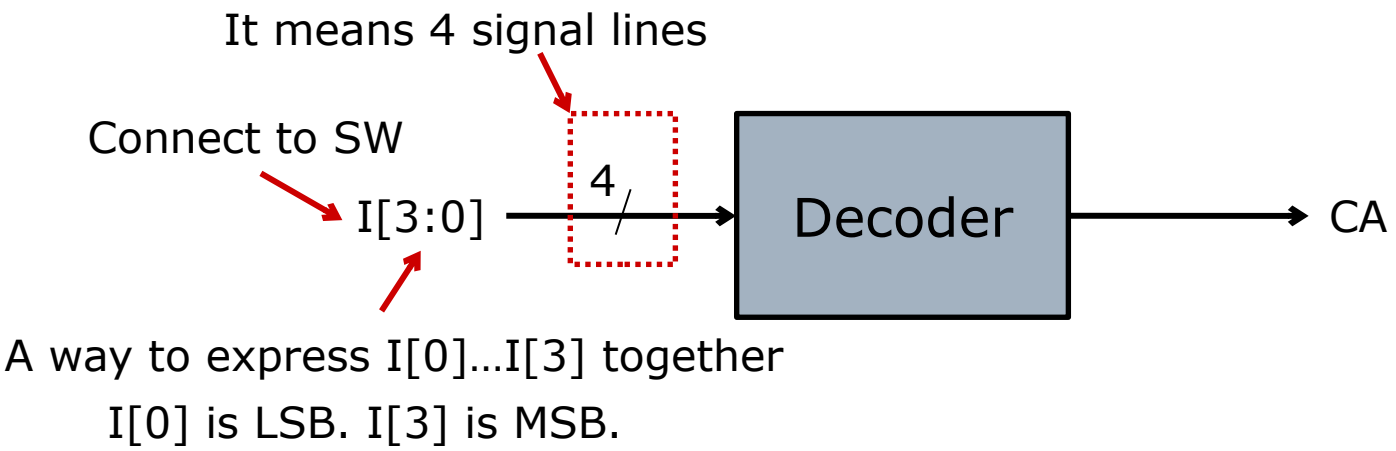
Design guideline for combination circuit

1. Make a truth table
2. For each row's operation, design a condition extraction circuit using AND and NOT
3. Use OR to add each circuit above

Practice

Let's consider C1 question (in the practice later) first!

Design a circuit:
CA=1 only when I=1, I=4, I=11(0xB), I=13(0xD)



Truth table is at the next page

Truth table for the practice

I[3]	I[2]	I[1]	I[0]	CA
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

I[3]	I[2]	I[1]	I[0]	CA
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

A part of C1 question in later practice.
You can use the practice time later to finish it.

Note

- In this way, the circuit might not so elegant, but you can anyway make it.
- Looking bad is not a problem for practice.
  - Development tool can optimize the circuit, such as minimizing logic circuit.
  - When using FPGA, it does not matter at all.
    - Since the truth table is written to a LUT, minimization is basically not needed.
- If you are interested in elegant circuit design, you can refer to the minimization of logic circuits using Karnaugh diagrams, which always can be found in textbooks of digital circuits.

It is important to use a method and description which are easy to understand for designer

Sequential circuit

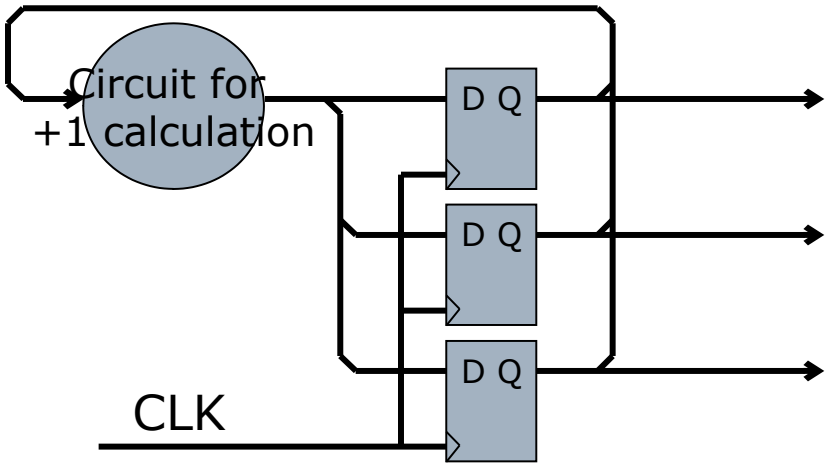
Design method

- Circuits with the same behavior can be designed in two different ways.

- Two different ways to design
  - Asynchronous
  - Synchronous ← main trend for FPGA

We will review synchronous circuits
using synchronous counters as an example
from the next page.

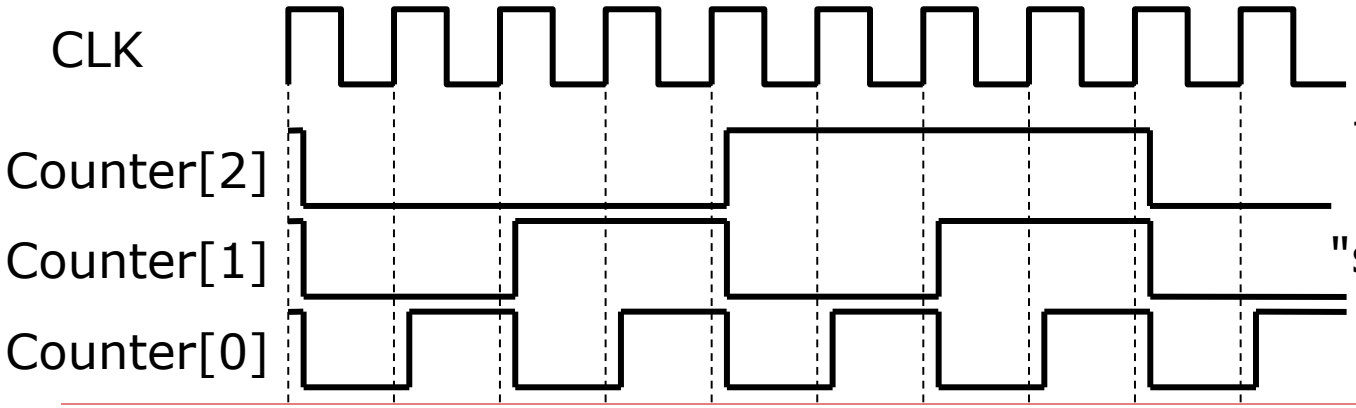
Synchronous counter



Features
- Complicated circuit
- Have delay within a certain range

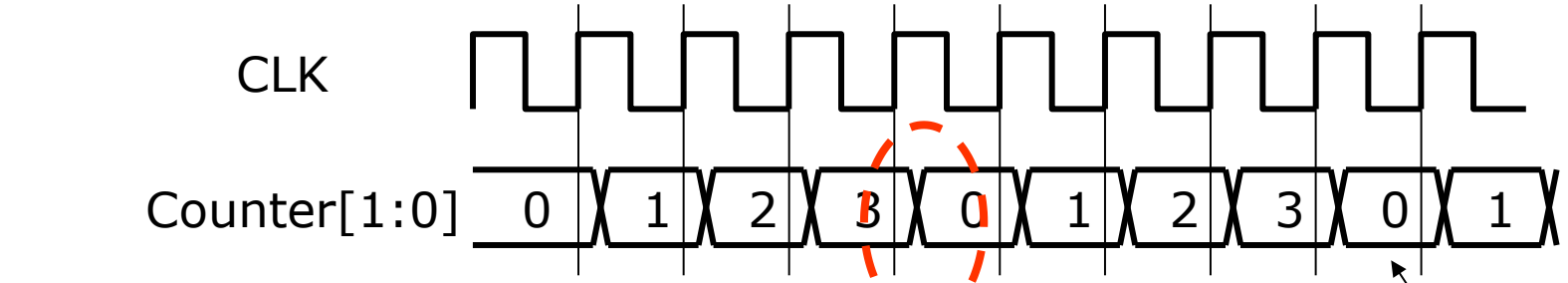
Widely used

A system common clock is inputted to the CLK port of DFF.



This kind of circuit is called "synchronous circuit"

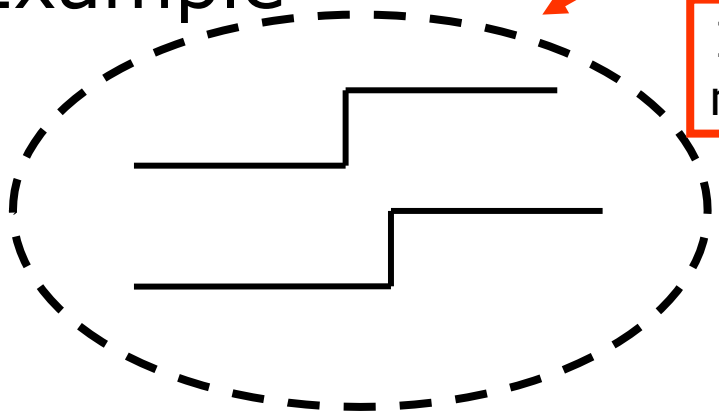
Synchronous counter



DFF operates only at the rising edge of the clock

Write the symbol (multiple signals) like this

Example



If it is decided before the next CLK rises, no need to consider progress in between.

Easy to design!

it actually takes time to determine the value.

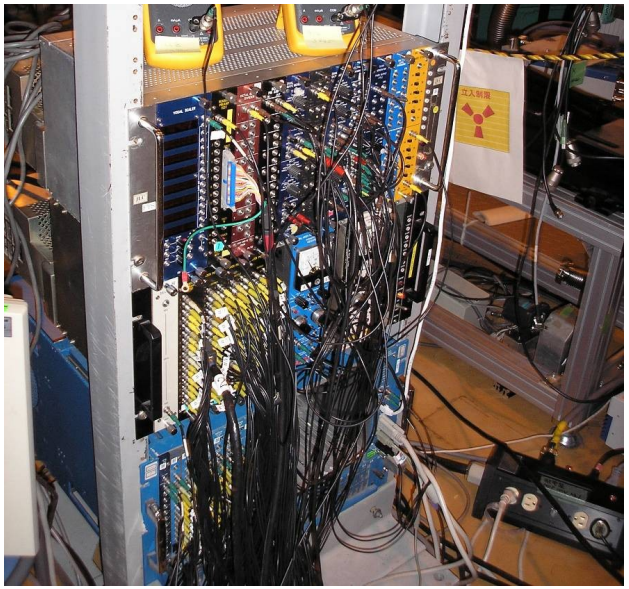
Recent Front-End circuit and integration technology

Evolution of Front-End

First, let's see the comparison between the old and present modules

Example of Front-End: Past

General-purpose modules are largely used and assembled



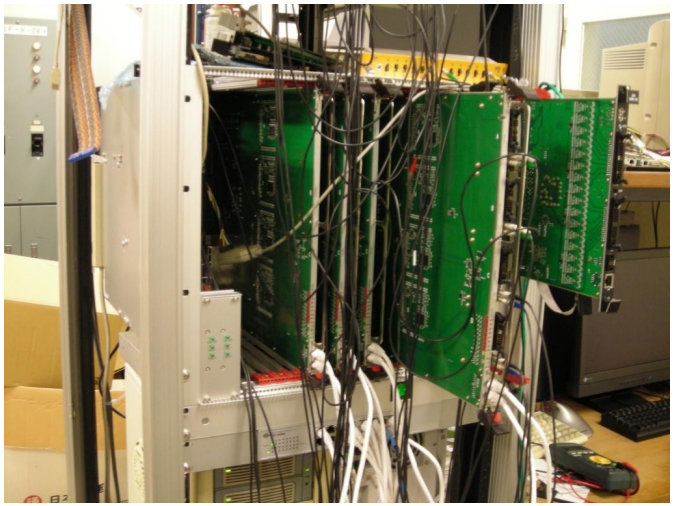
An example of a circuit of processing 64 channel signals

NIM modules, CAMAC modules are assembled

Example of Front-End: Now

Developed by ourselves

size: about 20cm x 15cm



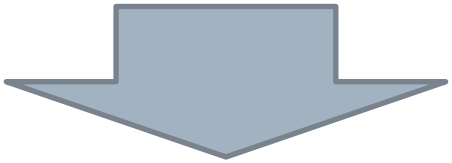
COPPER Lite

Belle II CDC readout module

Integration is the keyword

Background

- Requirements from experiment
  - High-precision measurement
  - Increase channel density (increase number of channels)
  - Increase data amount

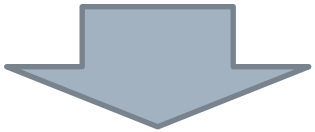


- Integration
- Higher speed

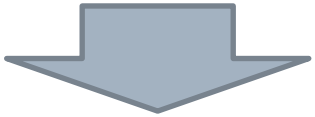
Impact from integration

For integration, it is necessary to specialize based on the application.

Parameters are dedicated to experiment, so limited usage



Circuits to process detector signals are special



(For each experiment) Need to develop by ourselves

Technology of integration

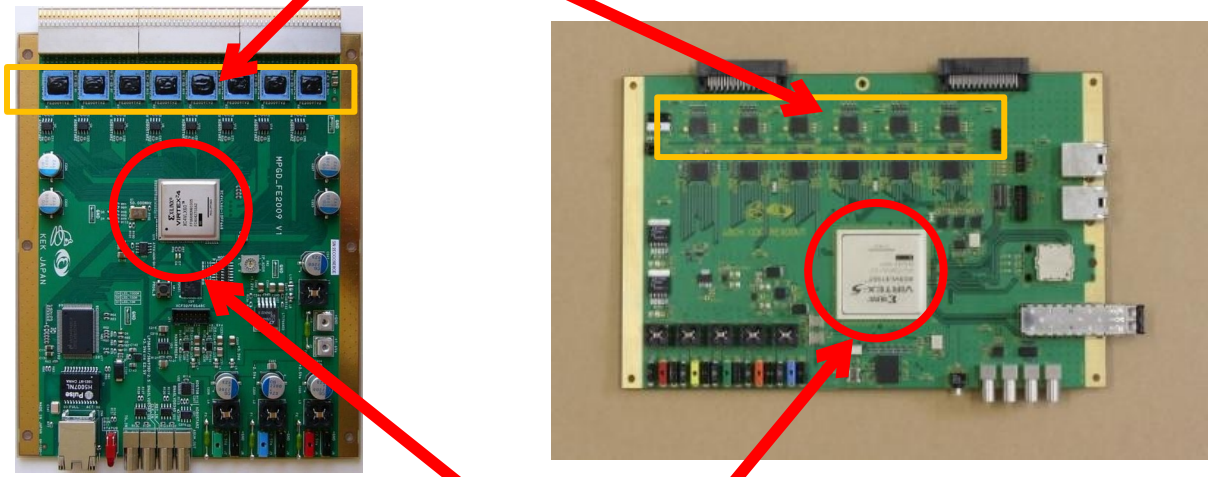
- Application Specific IC (ASIC)
  - Integrated circuit designed from transistor level
  - Can implement analog and digital circuits
- Field Programmable Gate Array (FPGA)
  - Digital integrated circuit
  - Can be rewritten like a program for CPU

They are both ICs but treated separately, since the development approaches are different.

Example of using ASIC, FPGA

It is no exaggeration to say that the major components of current Front-End boards are only ASIC and FPGA.

ASIC

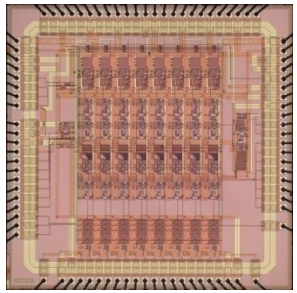


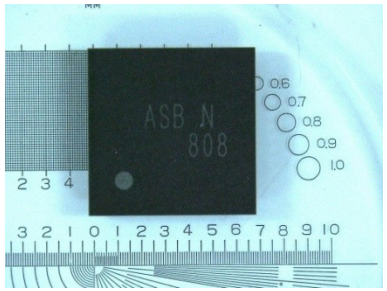
FPGA

Application Specific IC (ASIC)

The only way to integrate analog circuit

- Technology of converting unique circuits into integrated circuits
- Can implement analog and digital circuits
- Can be designed from the transistor level
- Problems in cost and development time





Pros and cons of ASIC implementation

- Pros
  - Lower price for mass production
  - Can do highly technical things
    - High-speed, high-precision, analog-digital mixed circuit, etc
- Cons
  - Time consuming for R&D
    - Problems in cost and development efficiency
  - Costly for prototyping

Pros and cons of FPGA implementation

- Pros
  - Easy to make an IC
  - Easy to modify circuit
- Cons
  - Only for digital
  - Higher unit price

Considering the point that it is for only digital, FPGA is no longer inferior in price and performance compared to ASIC.

Note: The ASIC processes which we can use are older generations. FPGA is manufactured using cutting-edge processes. Therefore, FPGAs have higher or equivalent performance compared to ASIC.

Trend of FPGA technology

Construction of micro system on FPGA

- Various special functions are equipped
- Embedded CPU
  - Many ARM processors
  - It can operate Linux
- Digital Signal Processing (DSP)
  - Arithmetic operation
- High-speed serial transmission
  - ~10Gbps
- Memory controller
  - DDR2/3 SDRAM

History

- 2012/05/17 第 1.0 版 ISE13.4 対応　内田智久 (Esys, KEK/ 総研大)，林達也（大阪大学)
- 2014/08/07 第 2.0 版 章構成変更　内田智久 (Esys, KEK/ 総研大)
- 2015/07/31 第 3.0 版 章構成変更　内田智久 (Esys, KEK/ 総研大)
- 2015/08/05 第 3.1 版 「データ集システムとデジタル回路」追加　内田智久 (Esys, KEK/ 総研大)
- 2015/12/03 第 3.2 版 ページ構成変更　内田智久 (Esys, KEK/ 総研大)
- 2015/12/04 第 3.3 版 組み合わせ回路演習問題追加　内田智久 (Esys, KEK/ 総研大)
- 2016/01/27 第 3.4 版 補足説明追加　内田智久 (Esys, KEK/ 総研大)
- 2016/07/14 第 3.5 版 予習資料との重複内容を削除 (Esys, KEK/ 総研大)
- 2016/09/29 第 3.6 版 誤字修正、構成変更 (Esys, KEK/ 総研大)
- 2017/08/09 第 3.7 版 誤字修正 (Esys, KEK/ 総研大)
- 2023/05/29 第 3.8 版 誤字修正　古田紘己 (NIFS)
- 2024/06/20 v3.8 Translation to English, Yun-Tsung Lai (Esys, KEK/ 総研大)