CMOSプロセス、エレクトロニクス入門

2009年7月27日
エレクトロニクスDAQセミナー
高エネルギー加速器研究機構
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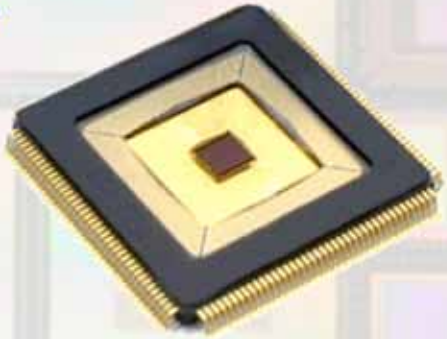
講義内容

- 0.はじめに
- 1. MOSトランジスターの基礎
- 2. MOSアナログ回路
- 3. CMOSデジタル回路
- 4. SOI Pixel回路



［参考文献］

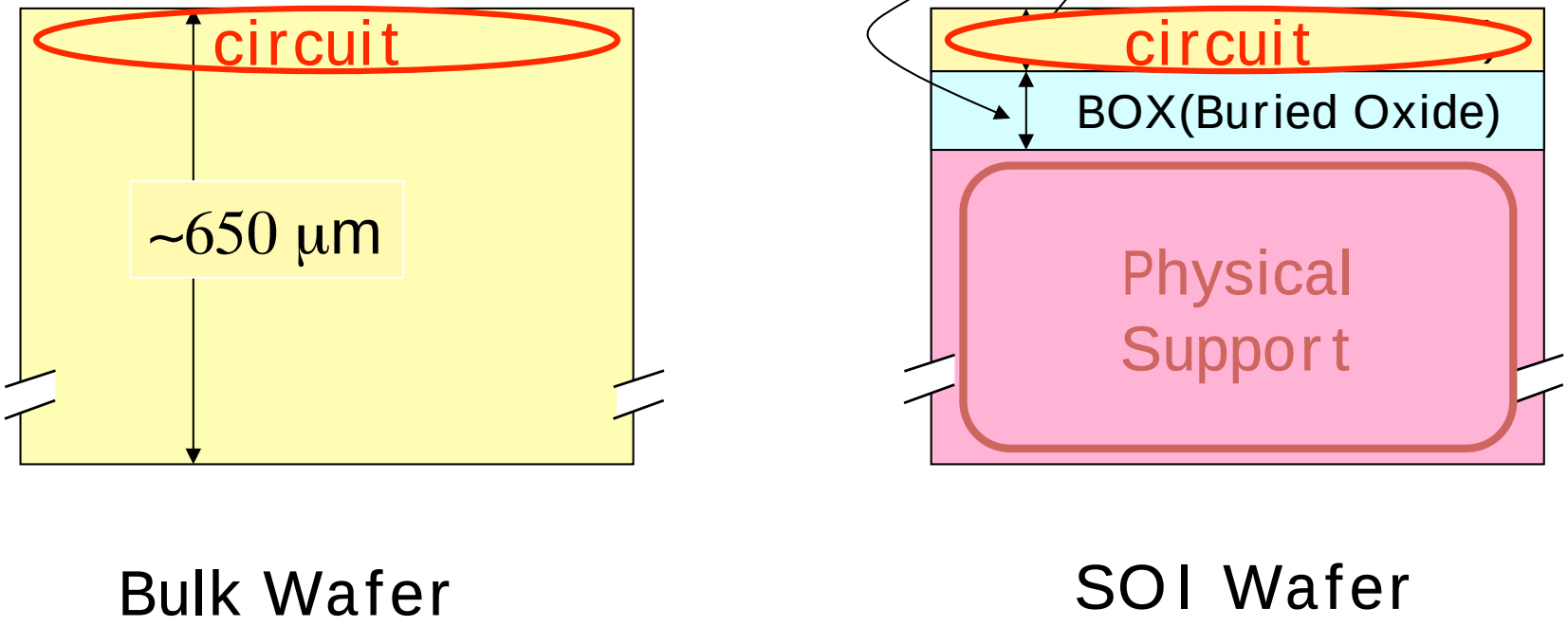
•Pixel Detectors, L. Rossi, P. Fischer, T. Rohe, N. Wermen, Springer, ISBN 3-540-28332-3

•Semiconductor Detector Systems, H. Spieler, Oxford University Press, ISBN 0-19-852784-5

•CCD/CMOSイメージ・センサの基礎と応用、米本一弥、CQ出版、ISBN 978-4-7898-3626-5

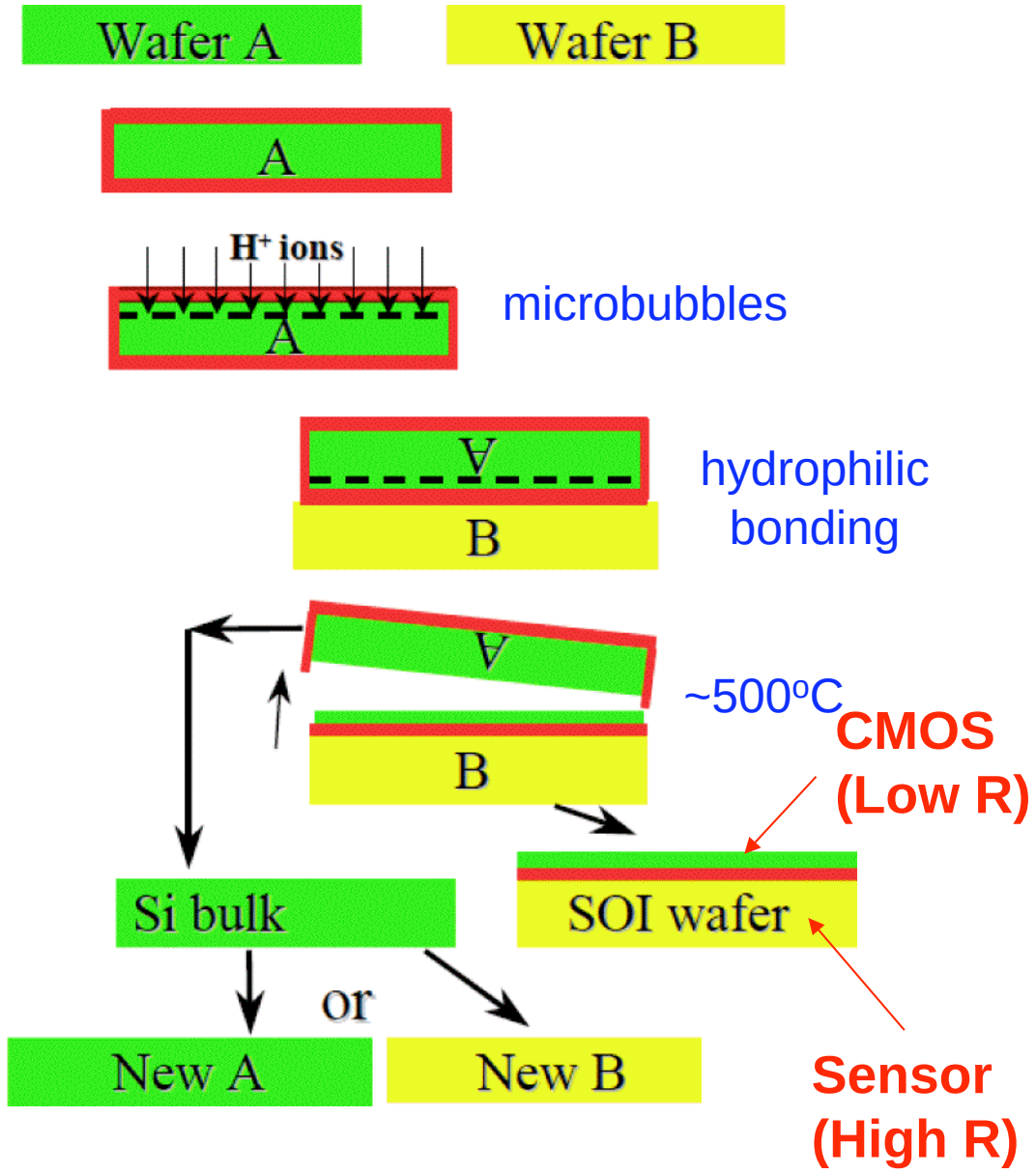
•Silicon-On-Insulator Technology: Materials to VLSI, 3rd Edition, J-P Colinge, ISBN 1-4020-7773-4

Bulk and SOI(Silicon-On-Insulator) Wafer

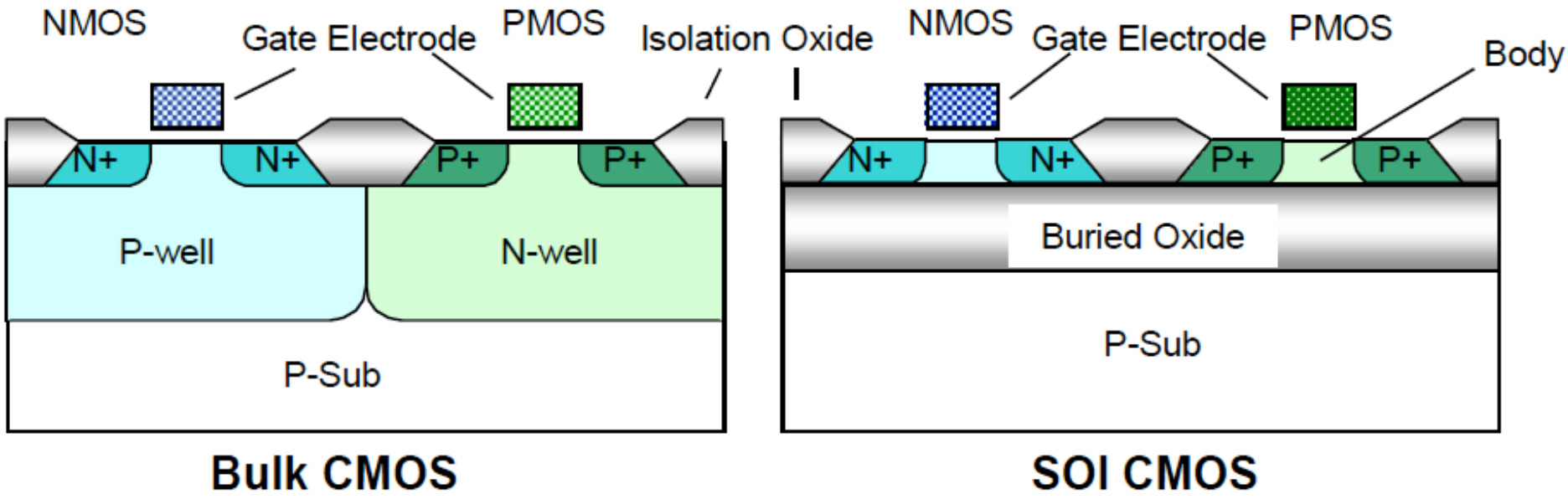


UNIBOND™ Process (1995, France LETI) -> SOITEC

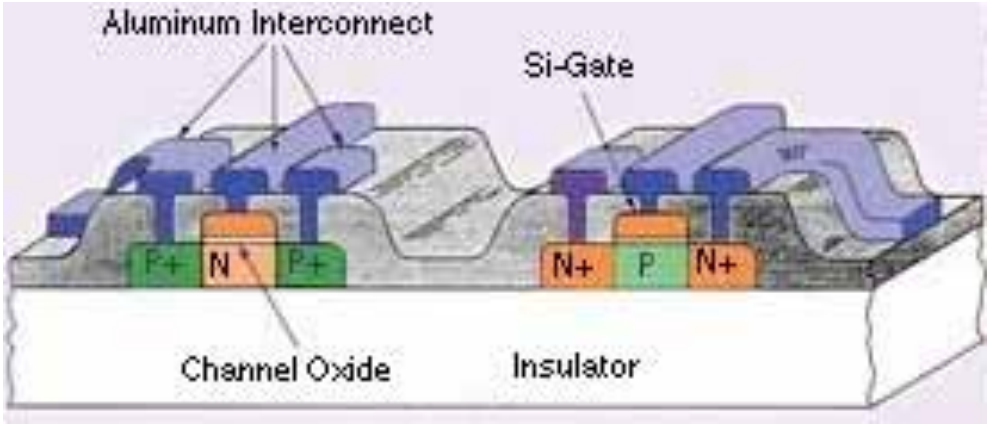
1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
8. Split-off wafer A is recycled, becoming the new wafer A or B



Bulk CMOS vs. SOI CMOS



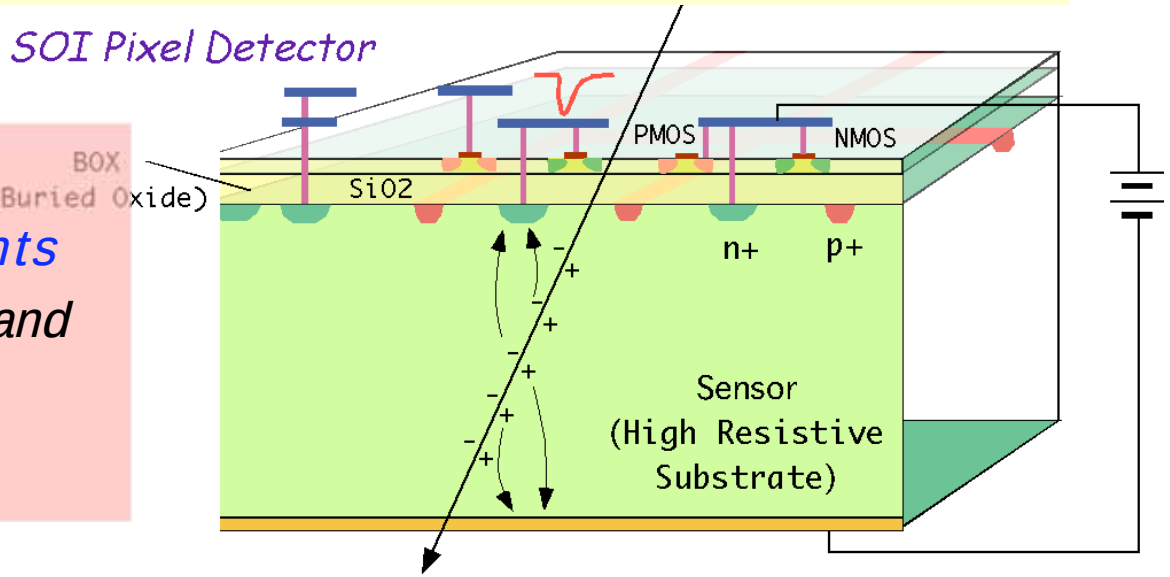
In SOI, Each Device is completely isolated by Oxide.



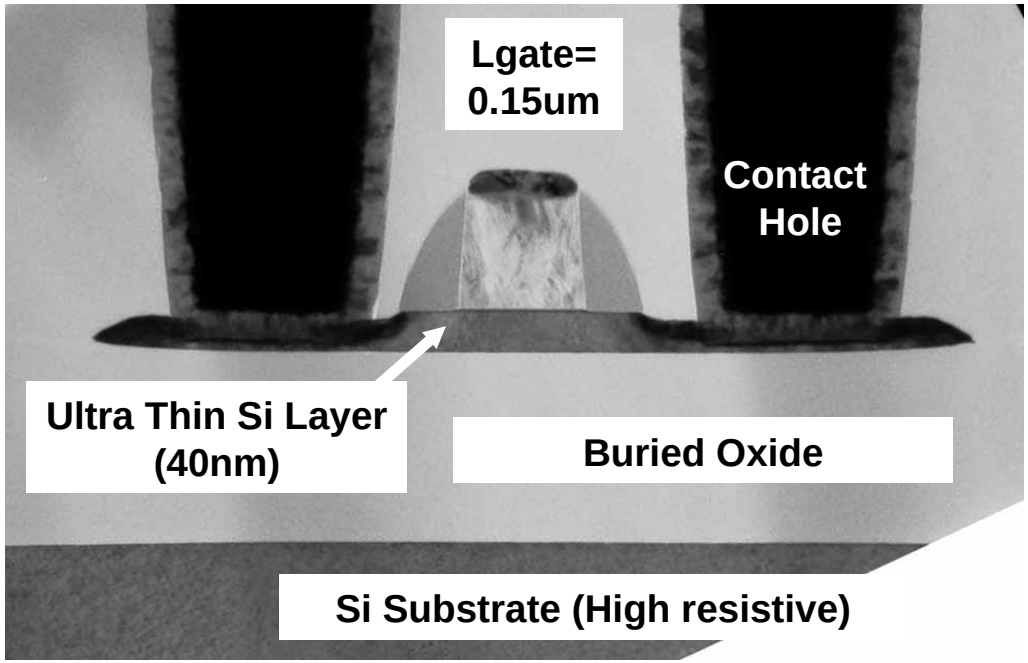
Features of SOI Monolithic Pixel detector

- Bonded Wafer (High Resistive Substrate + Low Resistive Top Si).
- Standard CMOS Electronics (NMOS, PMOS, MIM Cap etc.).
- Monolithic Detector, No Bump Bonds (Lower cost, Thin Device).
- High density (Smaller Pixel Size is possible).
- Small capacitance of the sense node (High gain V=Q/C)
- Industrial standard technology (Cost benefit and Scalability)

Explore the possibility of SOI detector for future experiments (ILC, SLHC, Super-Belle etc.) and other applications (Medical, Material etc.)

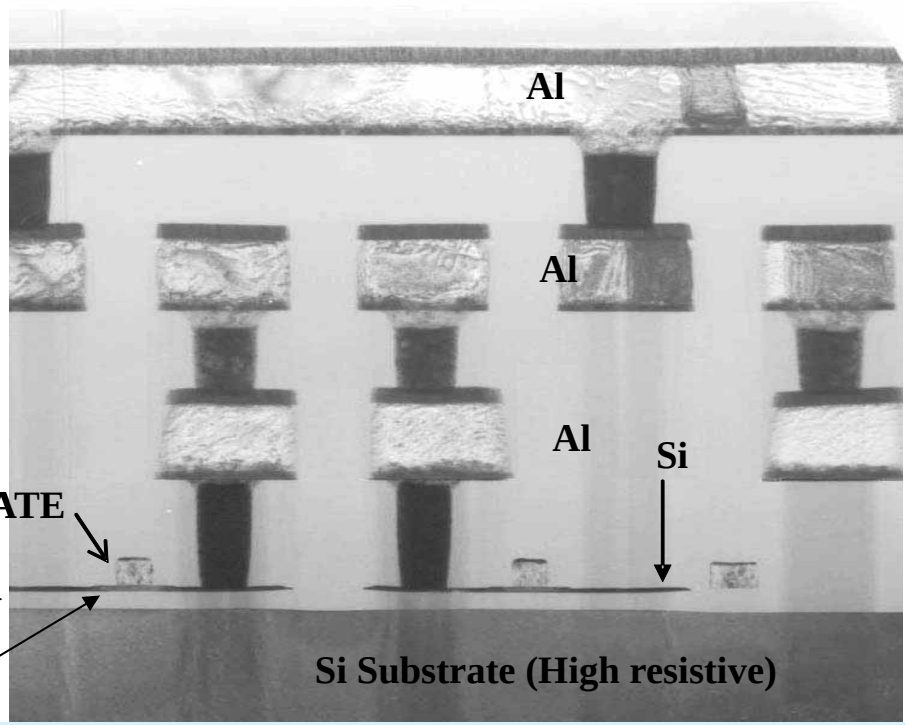


FD-SOI Structure



Close up of MOSFET

Cross Sectional SEM Photograph



Ultra Thin Si Layer (40nm)

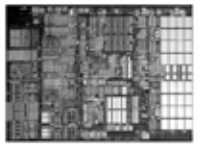
Cross Sectional View of FD-SOI Device

Current Status of PD-SOI and FD-SOI

◆ PD-SOI (Partially Depleted)

High-speed microprocessors

- IBM: PowerPC , mainframe CPU's, Wii(Nintendo), Xbox
- Free scale: PowerPC
- AMD: Athlon processors
- Sony (with IBM and Toshiba) : Cell, PS3



◆FD-SOI (Fully Depleted)

Low-power application

- Oki: solar cell watch, long-wave RF decoder

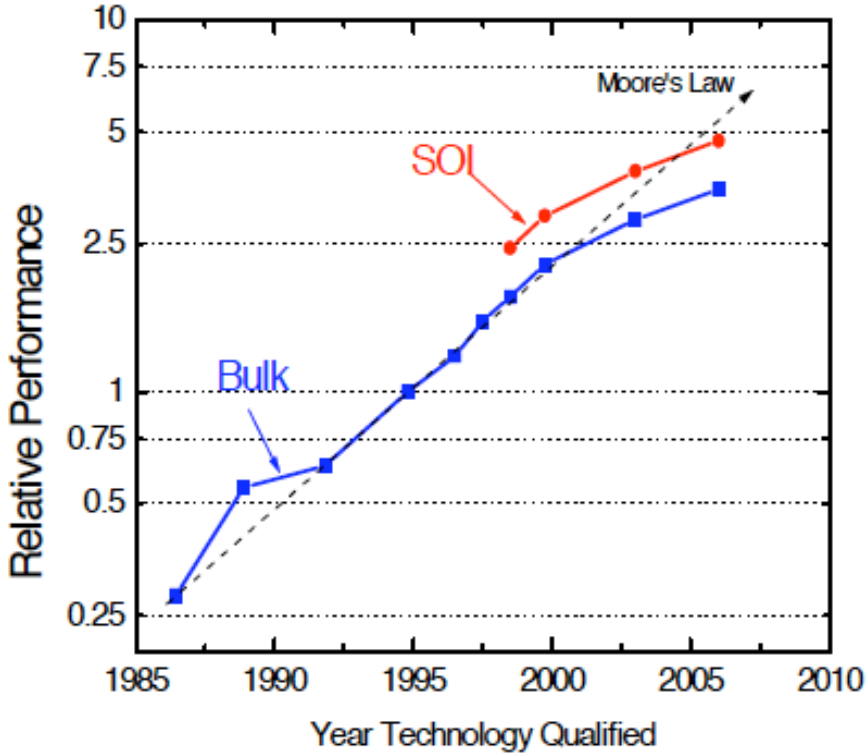
Technology Node option beyond 32nm, Next 3D Tr. (R&D)

- Intel, many major companies

At present, only Oki has an experience of mass production of FD-SOI

Features of (FD-)SOI

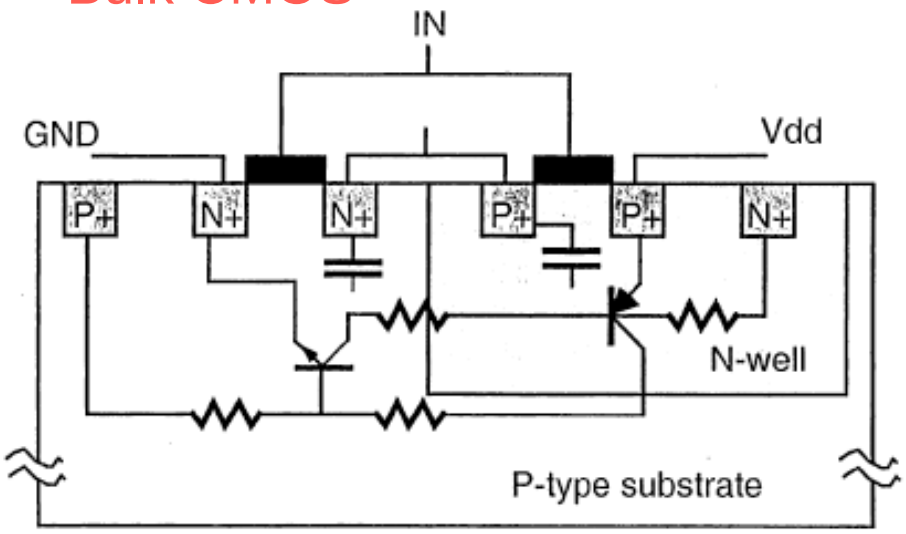
- Full Dielectric Isolation :
  Latchup Free, Small Area,
  Good Circuit Isolation
  No Back Bias Effect
- Low Junction Capacitance :
  High Speed
- Steep Subthreshold Slope
  Low Power
- No Kink Effect
  Good for Analog Desugn
- Less Impurity in Body
  Good Vth Matching,
  Less 1/f Noise



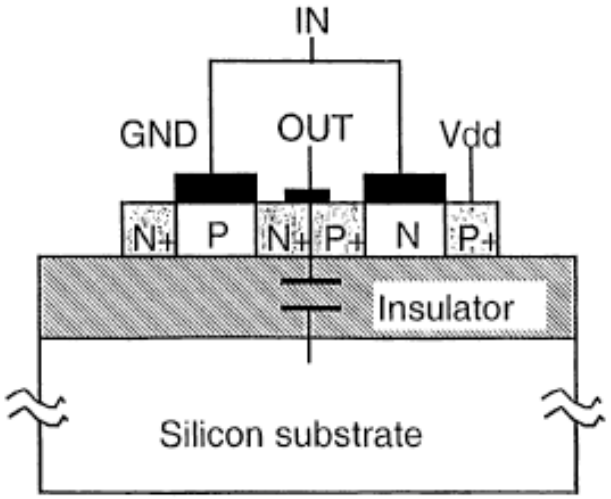
- No Well junction, Thin Film :
  Low Leak,
  Low Vth Shift (High Temp).
- Small Active Volume :
  High Soft Error Immunity
- TID compensation by Back Bias

Latchup Free Structure

Bulk CMOS



SOI CMOS



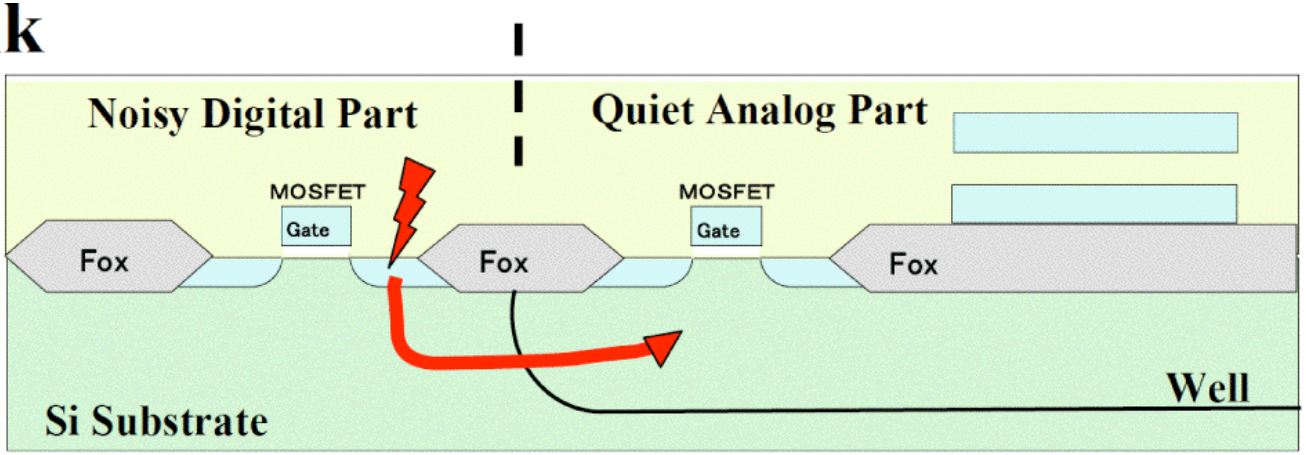
(Ref. 'SOI Technology' by Jean-Pierre Colinge, Springer)

No Parasitic PNPN Structure
外来スパイクによる故障が起こりにくい。

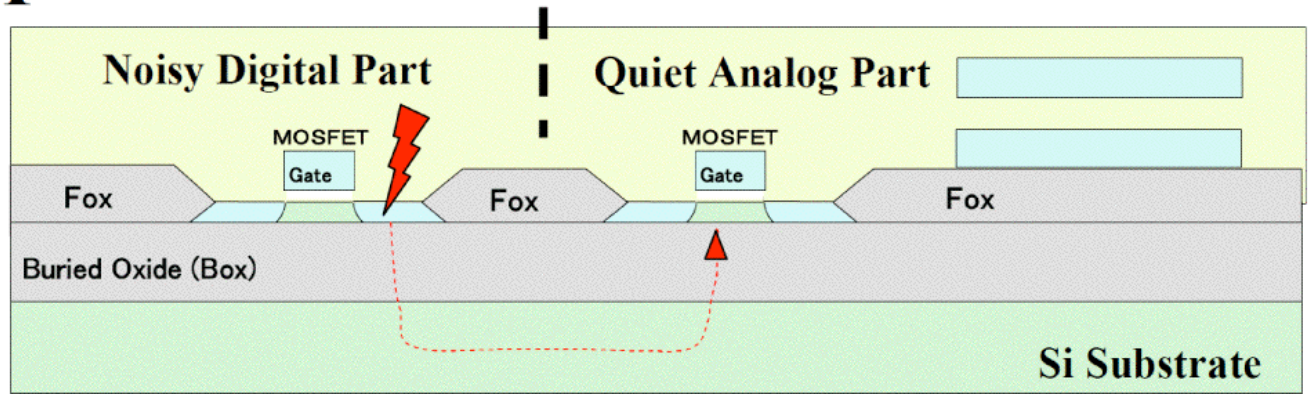
Isolation between Analog and Digital Part

10-40dB lower than Well isolation of Bulk, when High-Resistive Substrate is used

Bulk

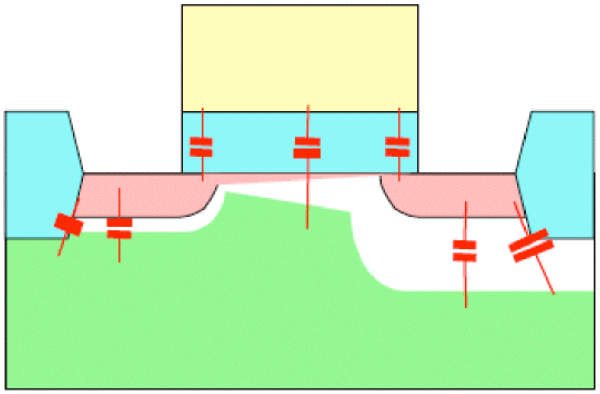


SOI

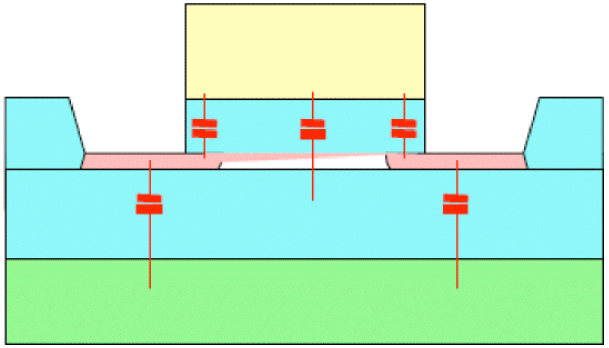


Smaller Junction Capacitance

Bulk



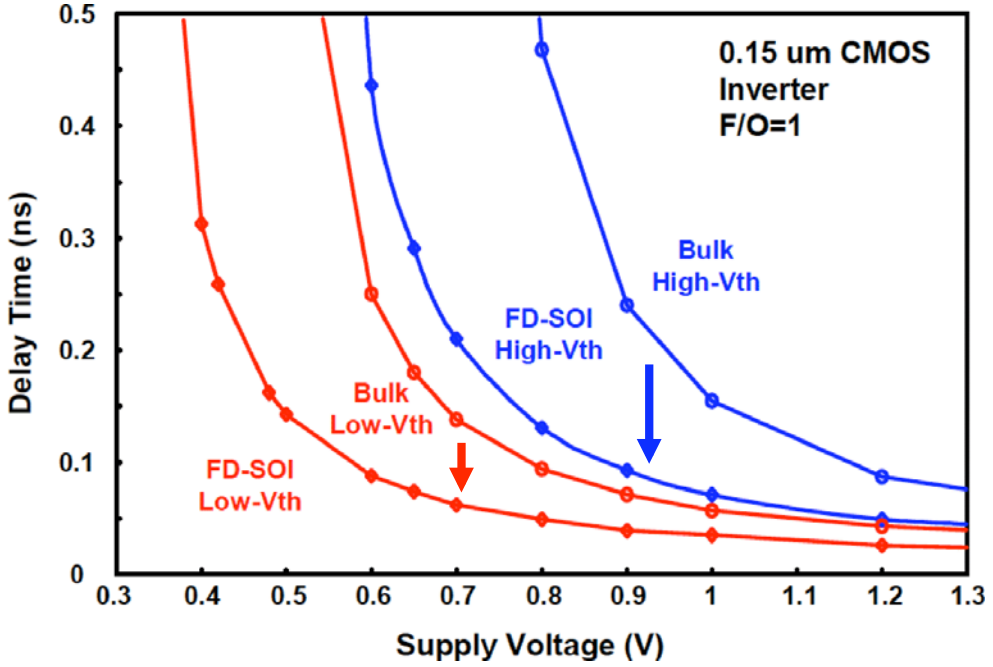
SOI



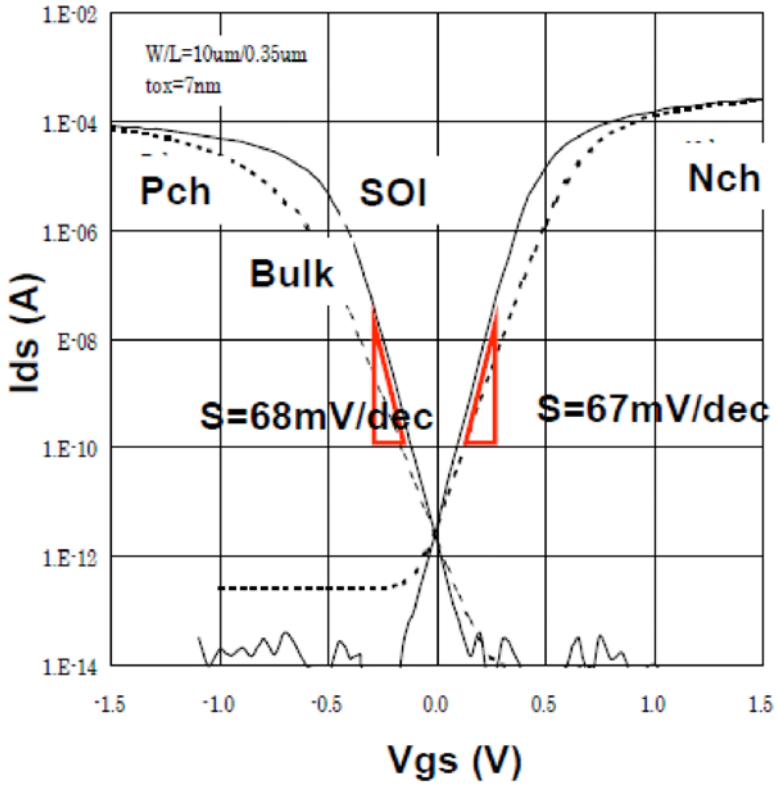
Cj is 1/10 of Bulk technology.

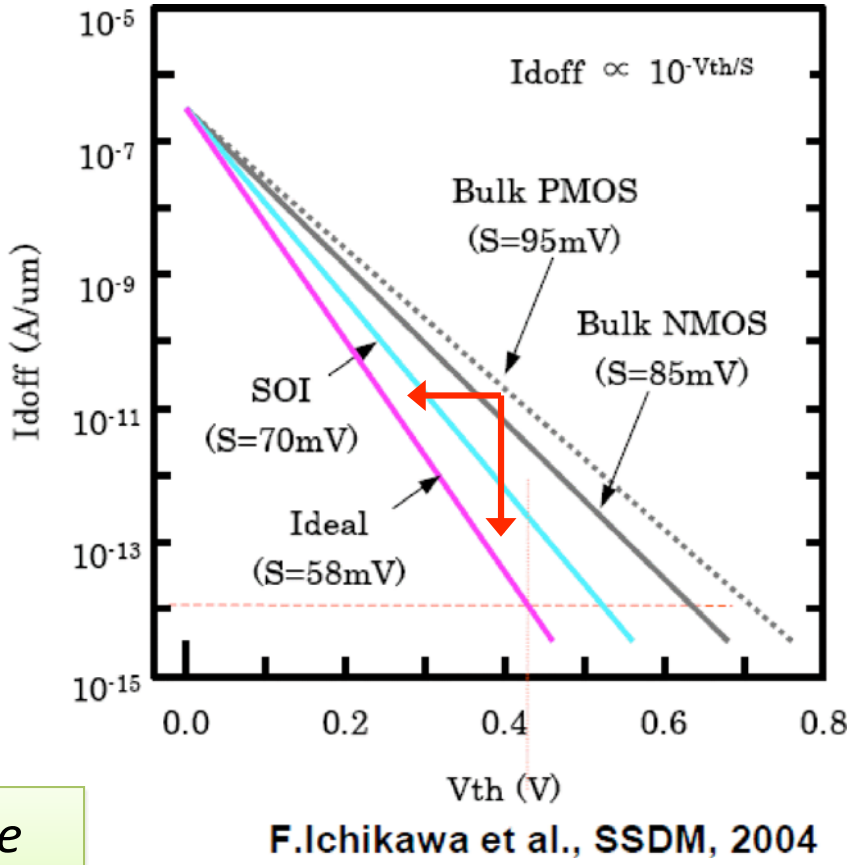
Gate Capacitance is 30-40% Lower.

High Speed / Low Power



Steep Sub Threshold Slope



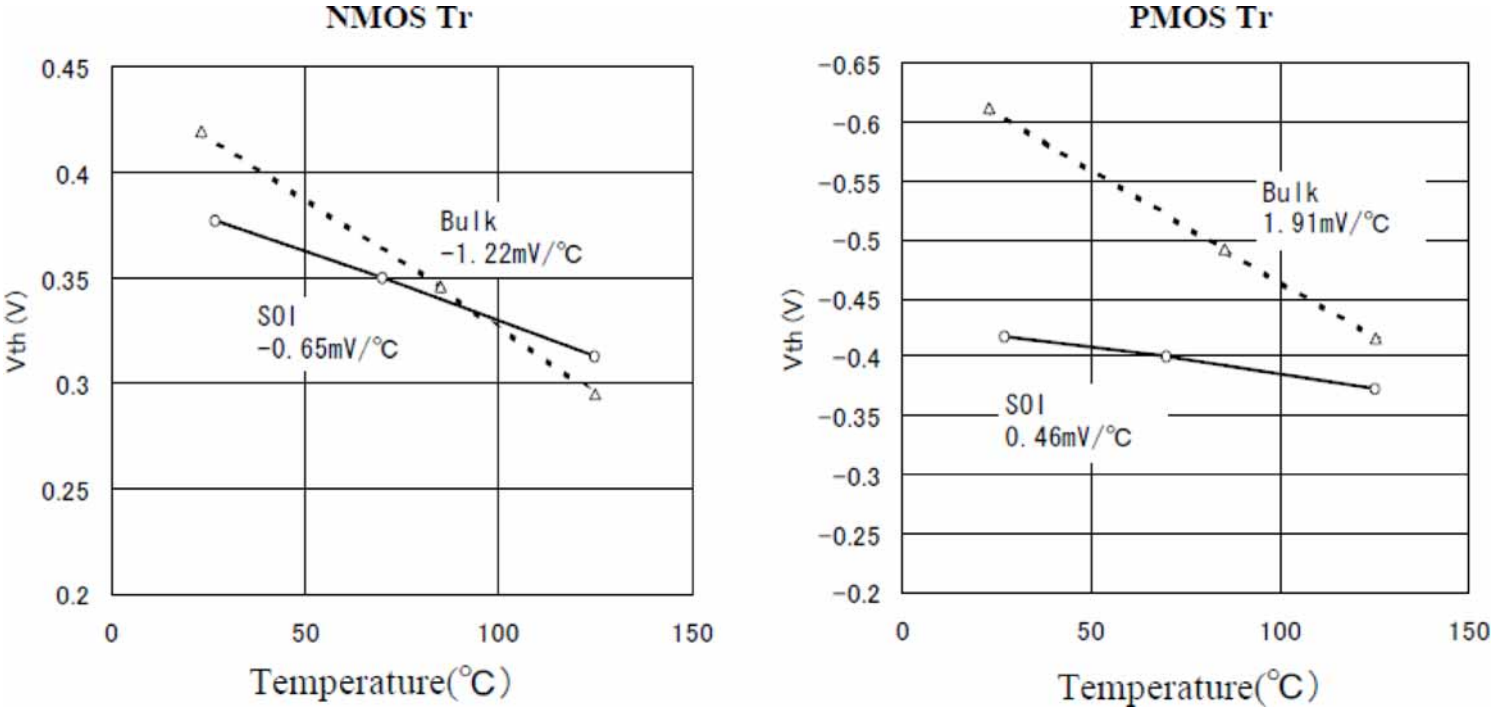


F.Ichikawa et al., SSDM, 2004

Gate voltage is not wasted to deplete the bulk.

Lower Threshold (Leakage Current) is possible without increasing Leakage Current (Vth).

Small Temperature Dependence

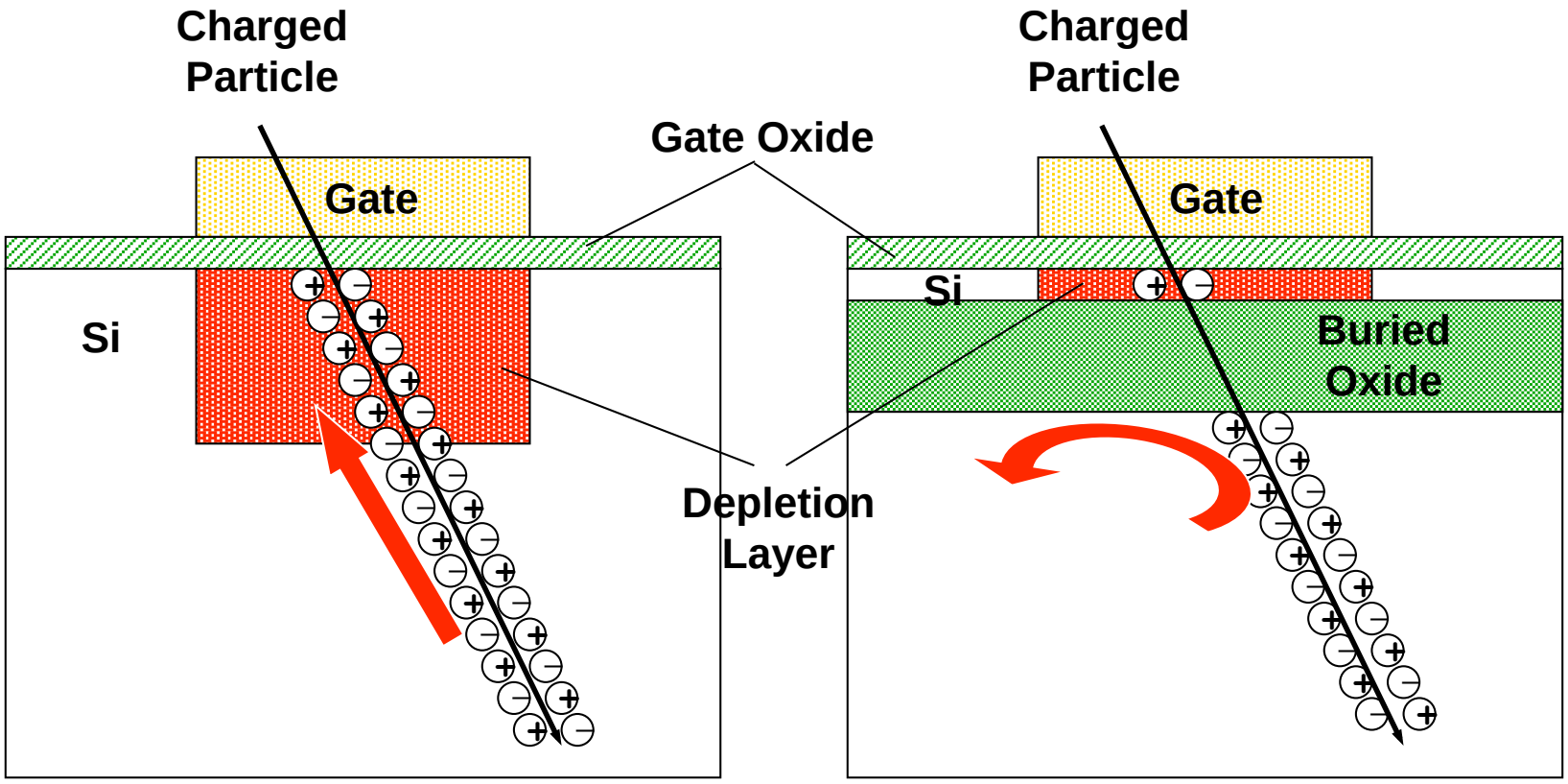


due to less change in depletion width

No latchup, Less leakage, Less Vth shift

→ FD-SOI can be operated in 4K to 300˚C.

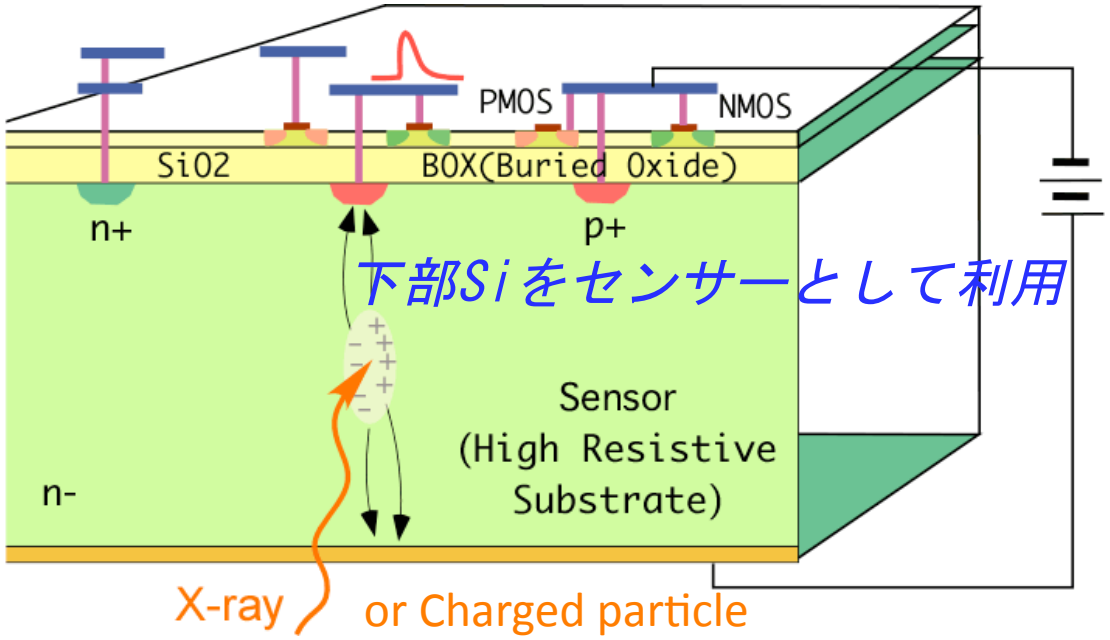
High Soft Error Immunity



Higher soft error immunity due to ultra thin body Silicon.

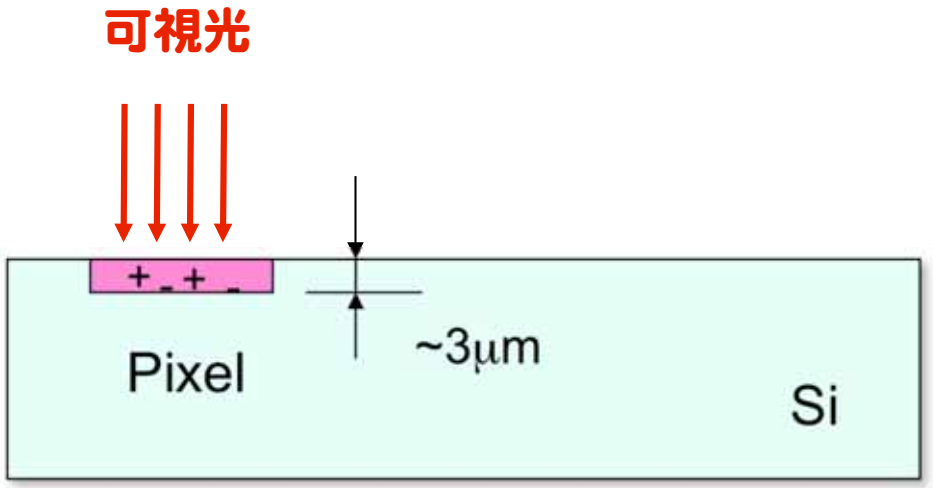
SOI Pixel検出器

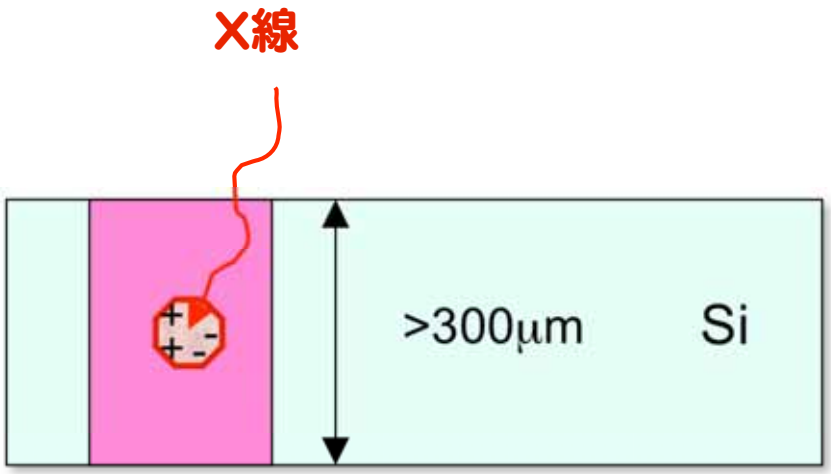
- 高比抵抗Si基板と低比抵抗Si基板を絶縁層を介して張合わせ。
- 高比抵抗部にp-n junctionを生成し、センサーとする。
- 絶縁層(BOX: Buried Oxide)に穴を開けセンサーと回路を接続。

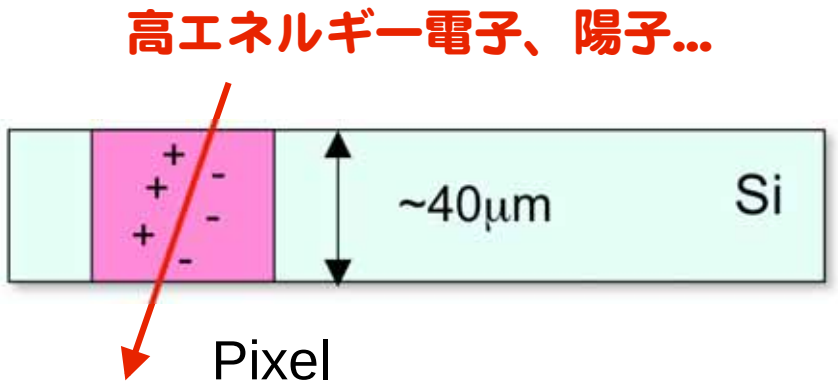


Monolithic Radiation Sensor
として理想的な構造

光センサーと放射線センサー





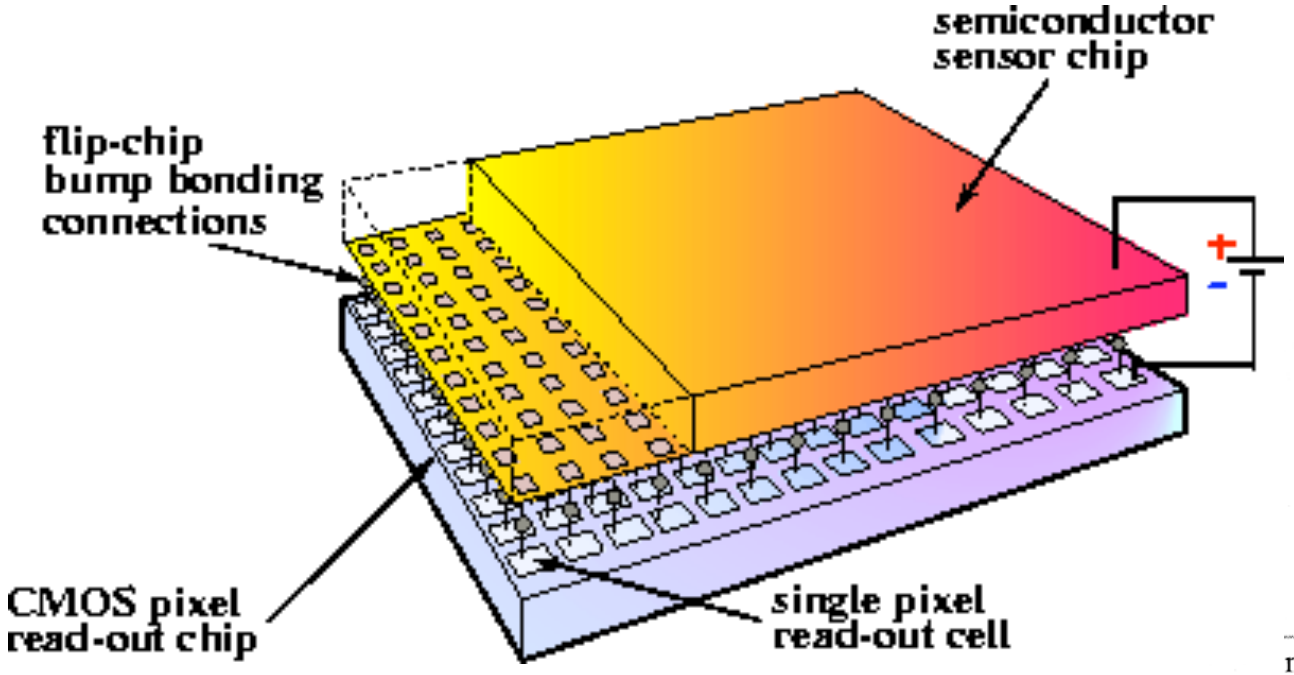


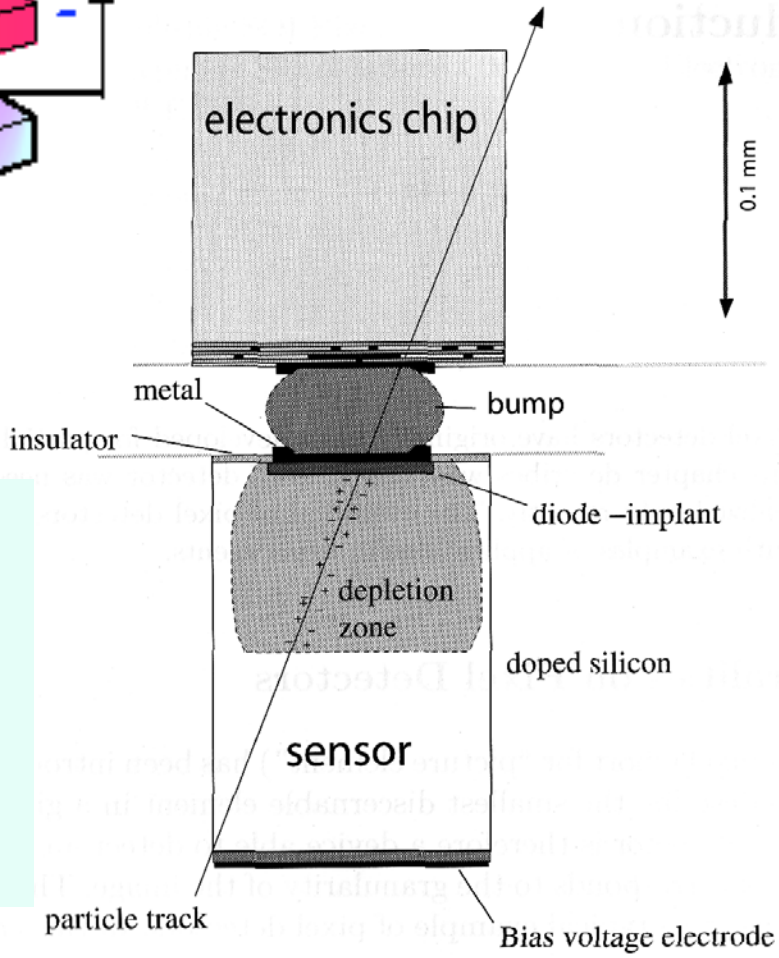
信号量:

可視光	~	1 e-h / 1 photon
X線	~	3000 e-h / X-ray@10keV
荷電粒子	~	3000 e-h / track@40μm

放射線はひとつずつ数えることが出来る。

現在の最先端Pixel検出器(Hybrid Pixel)

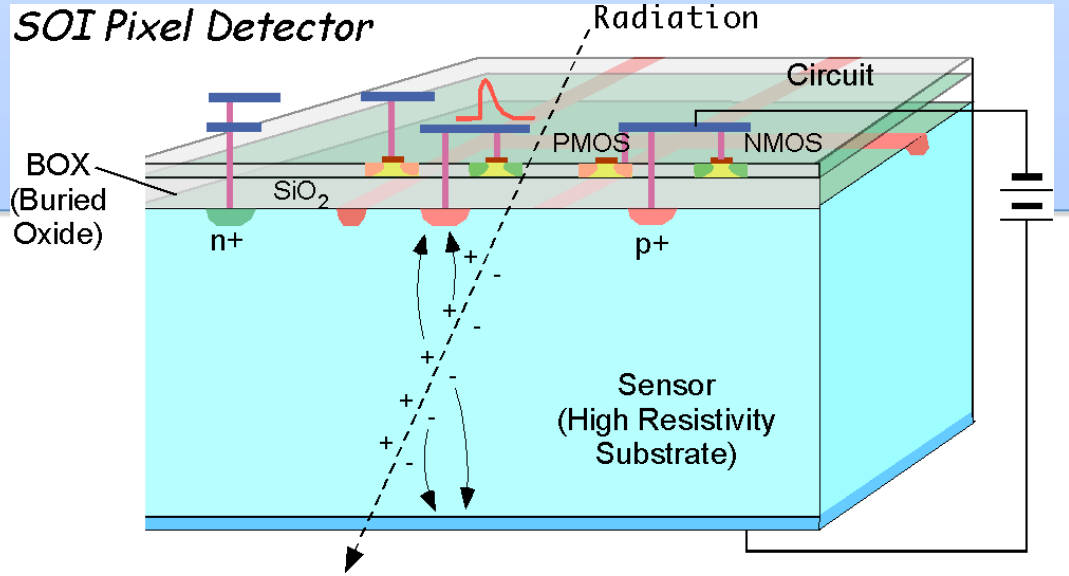




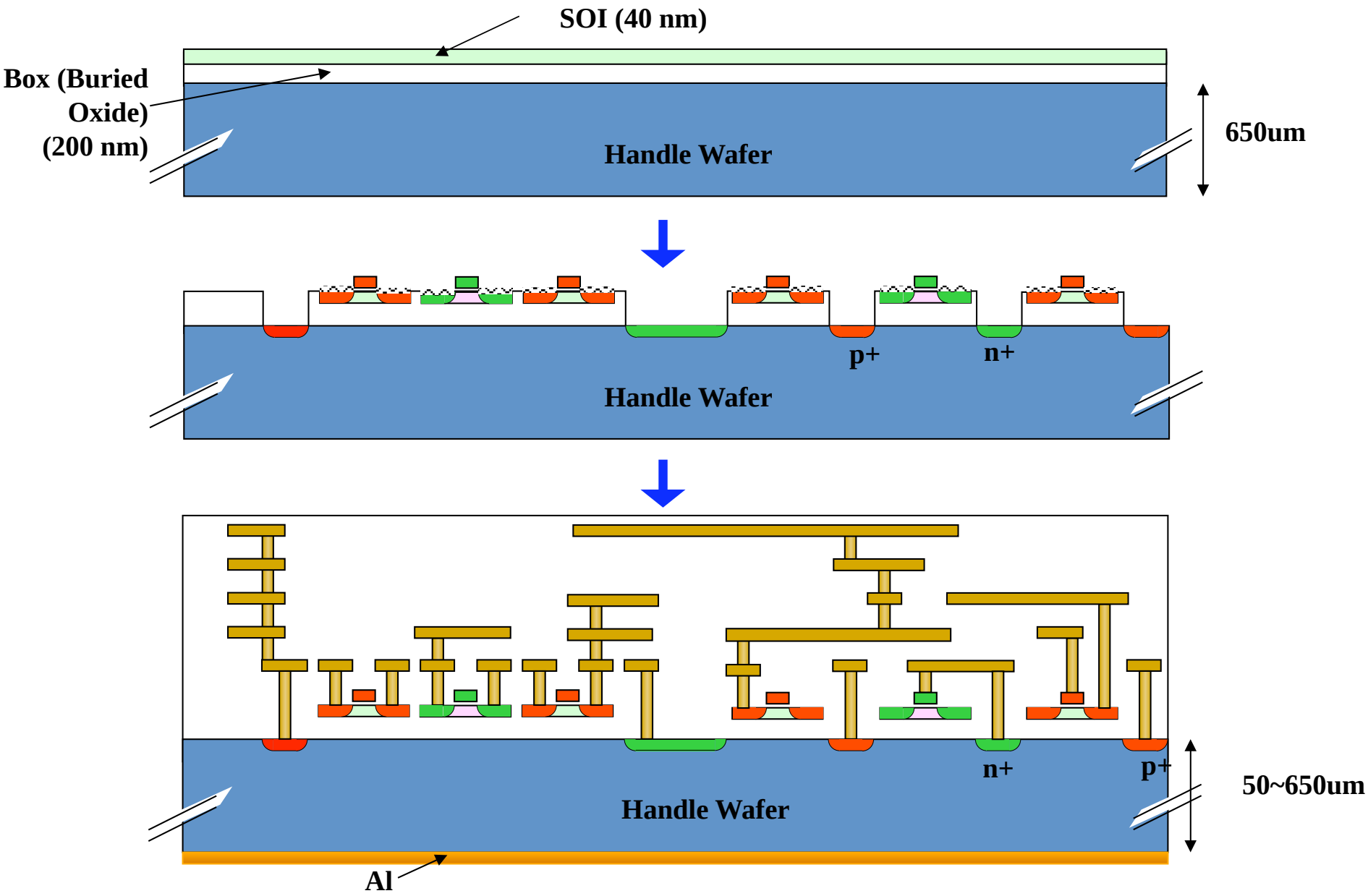
- 検出器と読出しエレクトロニクスを別々に作り、金属バンプにより接合する。
  - 位置分解能に制限。
  - 余分な物質が大量にある。
  - 寄生容量によるスピードの低下。

SOI Pixel検出器の特徴

- 余分な物質が少なく、多重散乱をおさえられる。
- 電極容量が小さく、少ない電荷(薄いセンサー)で大きなS/Nが得られる。
- 複雑な信号処理回路を各ピクセルに持たせられる。
- 高レート、高速読み出しが可能。
- 機械的接合がなく、高分解能化、低価格化が望める。
- 産業界の標準プロセスを基本に開発。

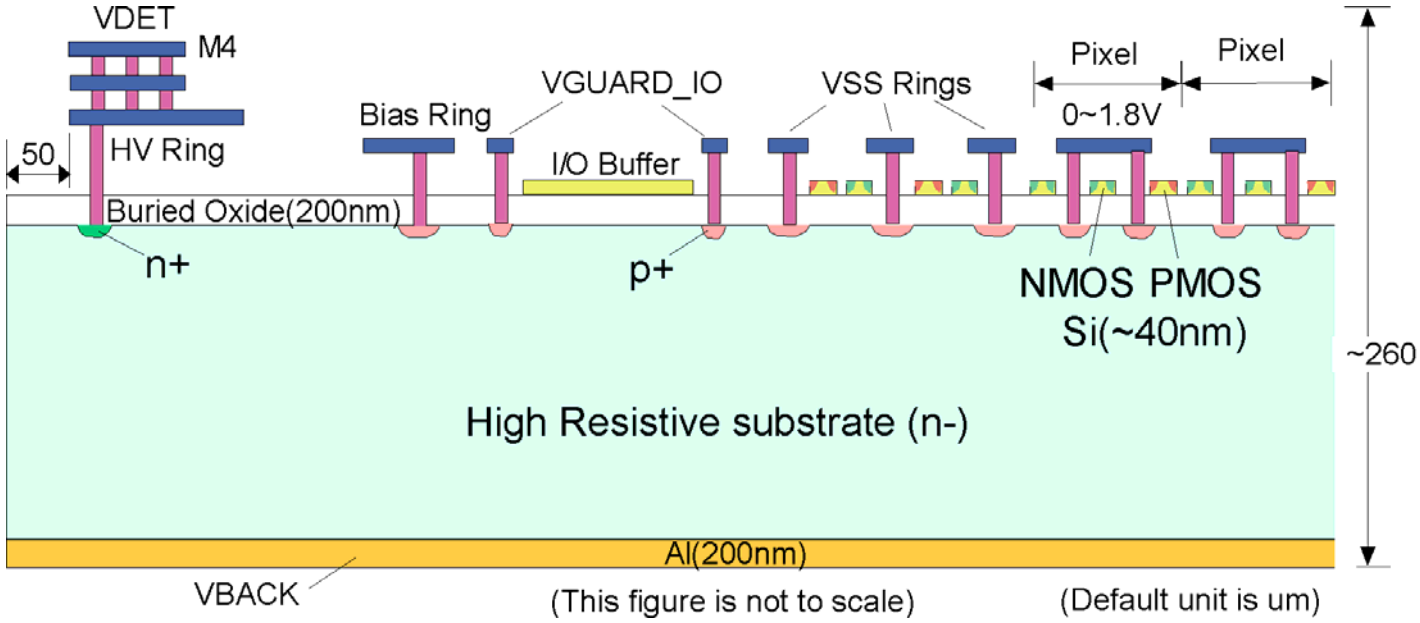


SOI Pixel Process Flow



OKI 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS (OKI) 1 Poly, 4(5) Metal layers, MIM Capacitor, DMOS option Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、700 Ω-cm (*n-type*), 650 μm thick
Backside	Thinned to 260 μm, and sputtered with Al (200 nm).

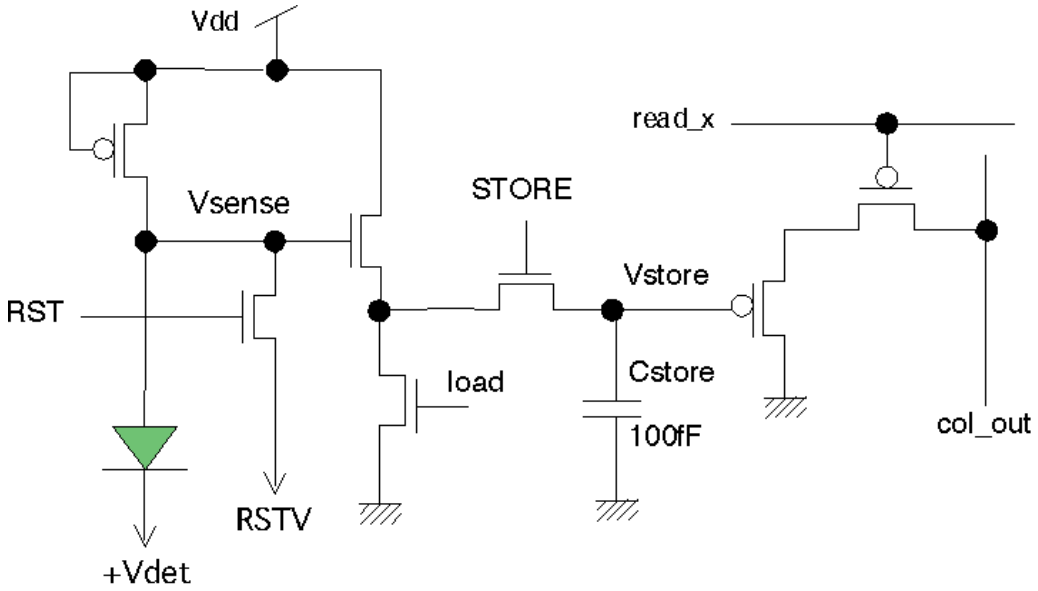


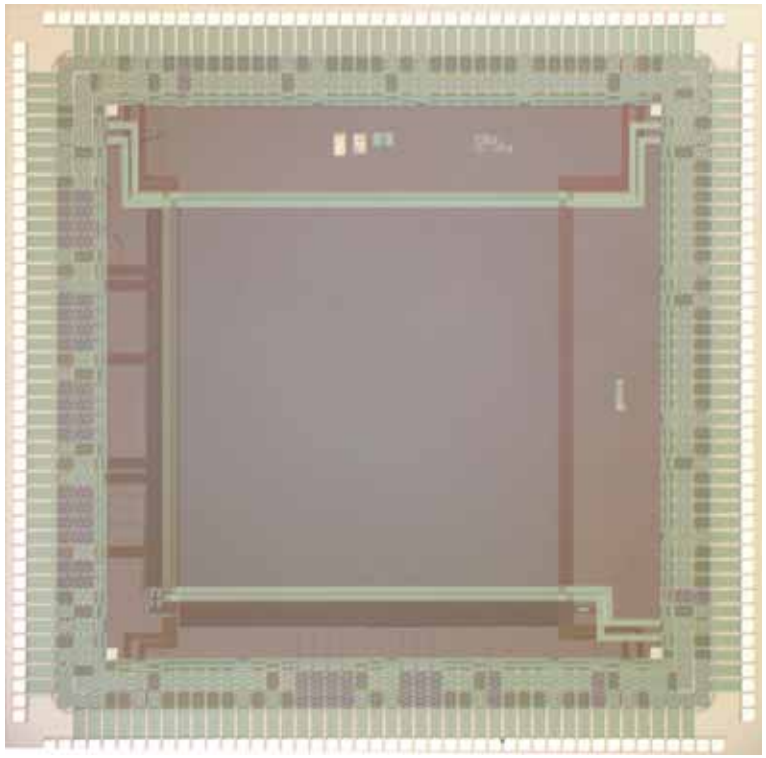
An example of a SOI Pixel cross section

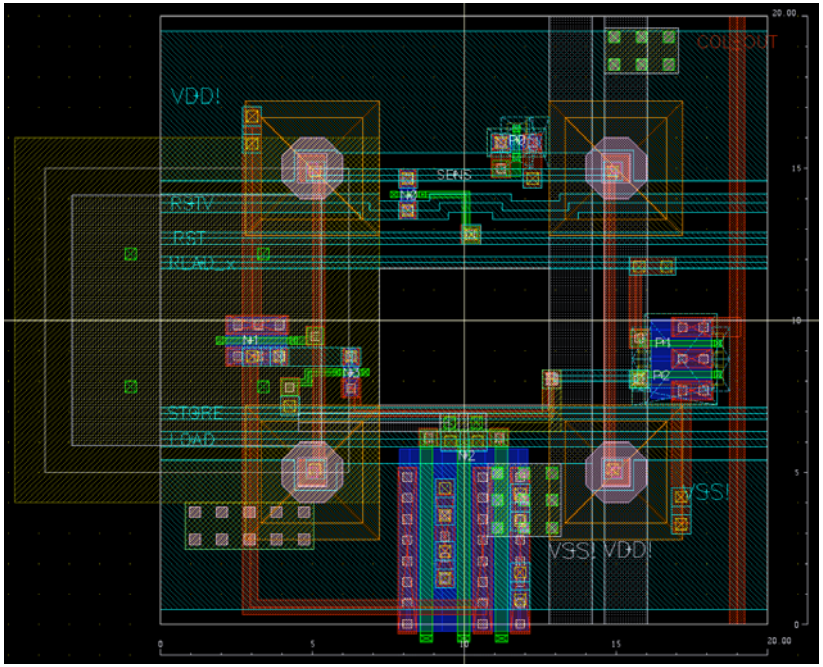
MPW (Multi Project Wafer) run

~Twice per Year

Integration Type Pixel (INTPIX)





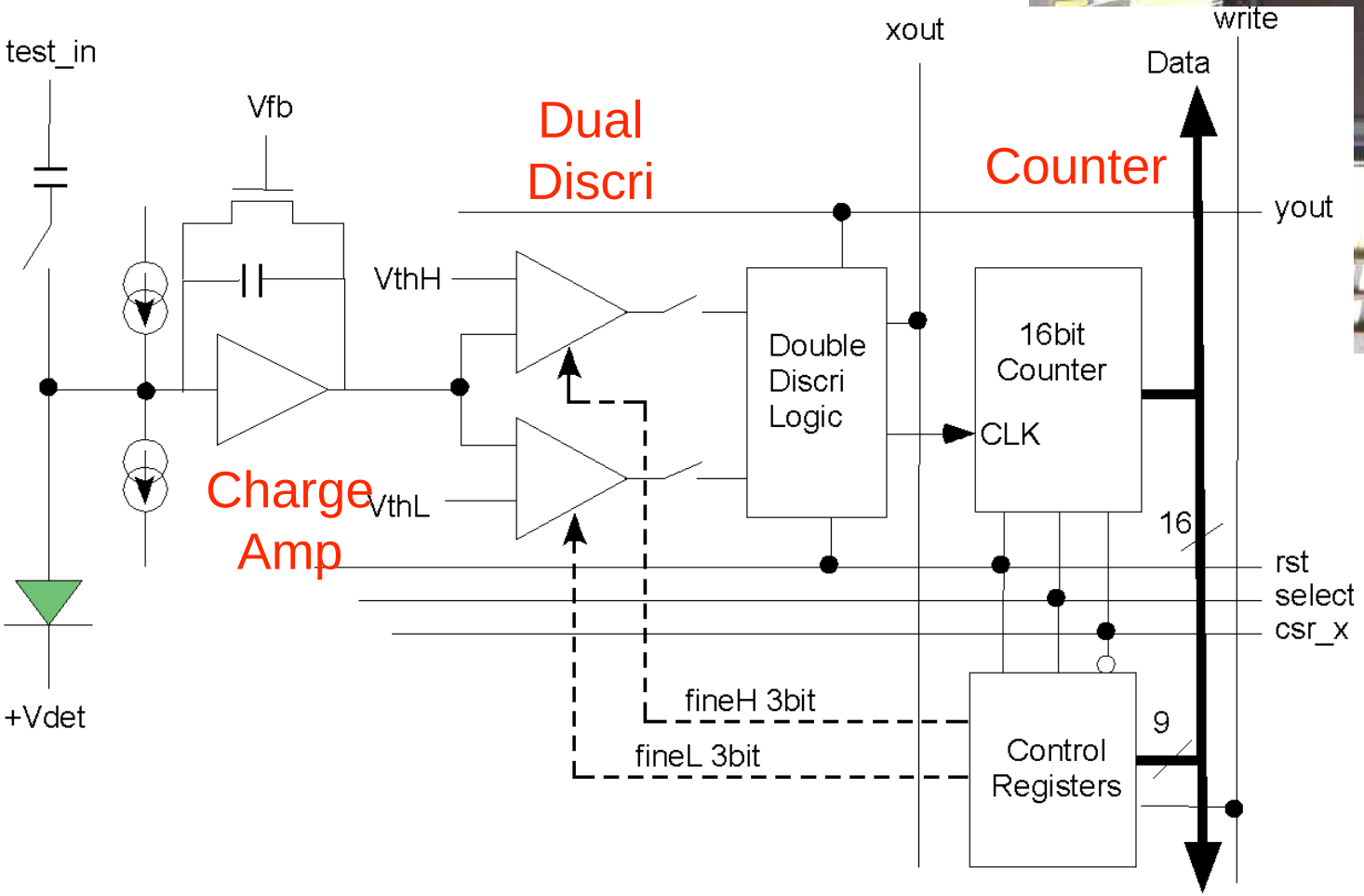


128 x 128 pixels
5 x 5 mm²

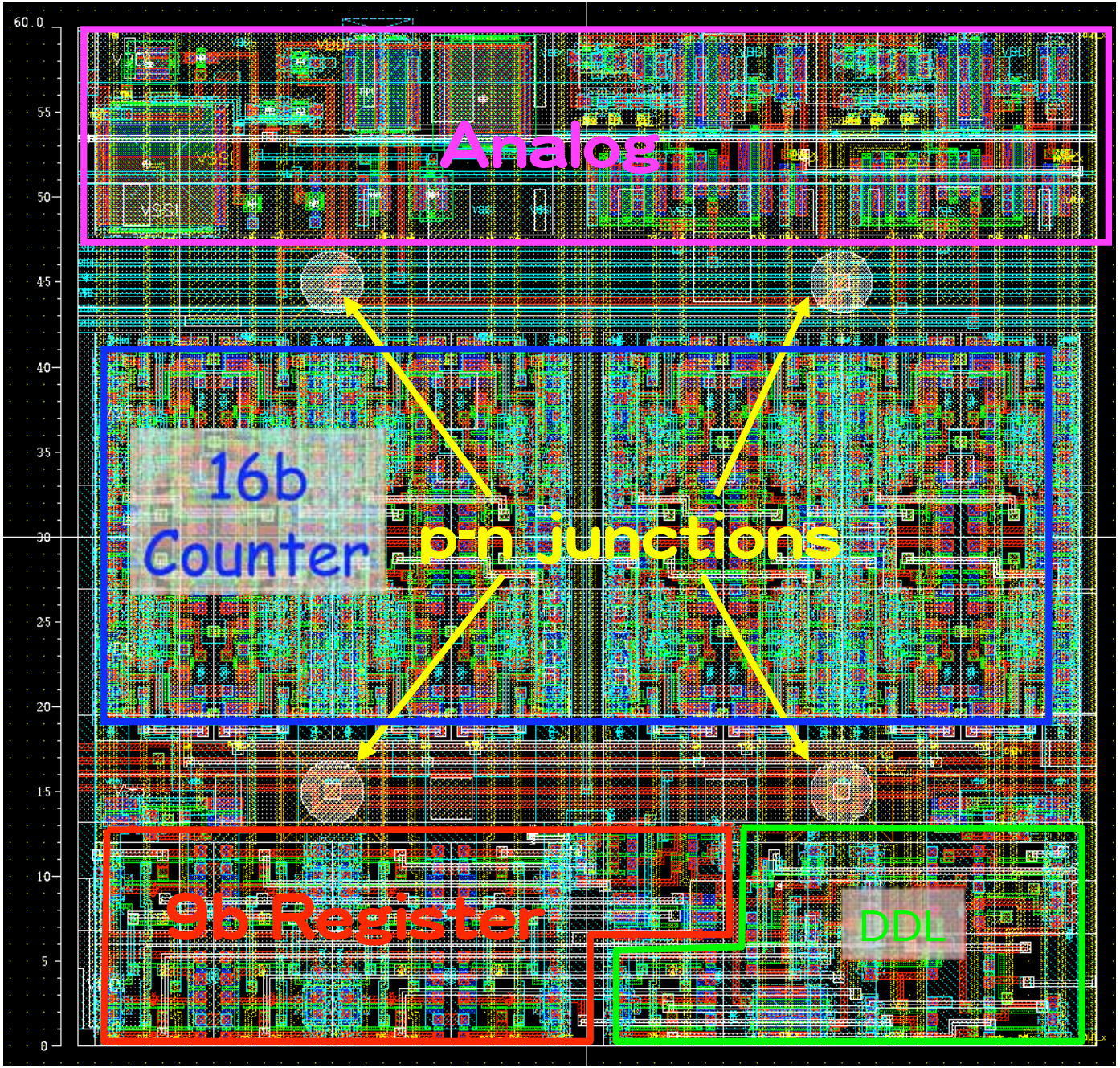
20 μm x 20 μm pixel

Counting Type Pixel

Energy window and counting in each pixel.



10.4 mm□
128 x 128 pix

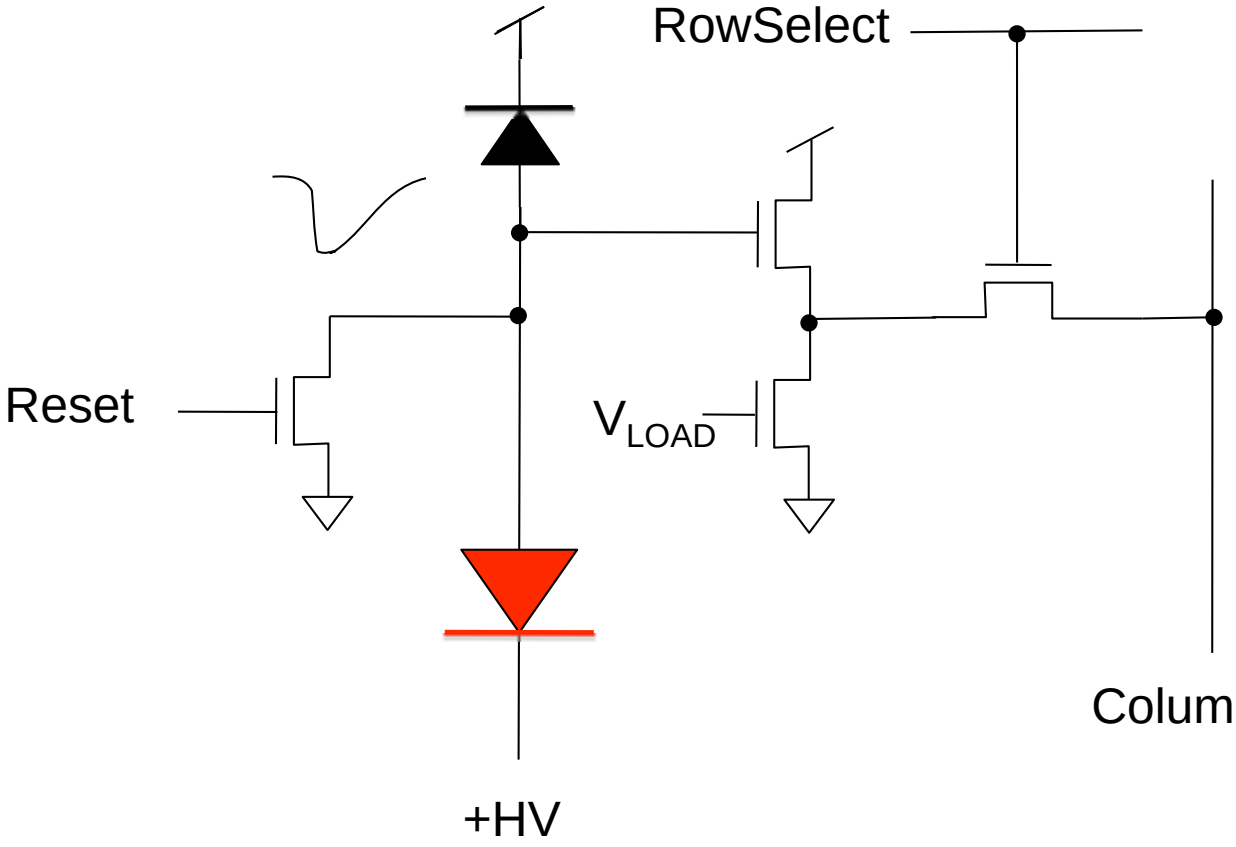


CNTPIX2 Pixel

~600 Tr/pix
x 128 x 128
= 10,000,000 Trs

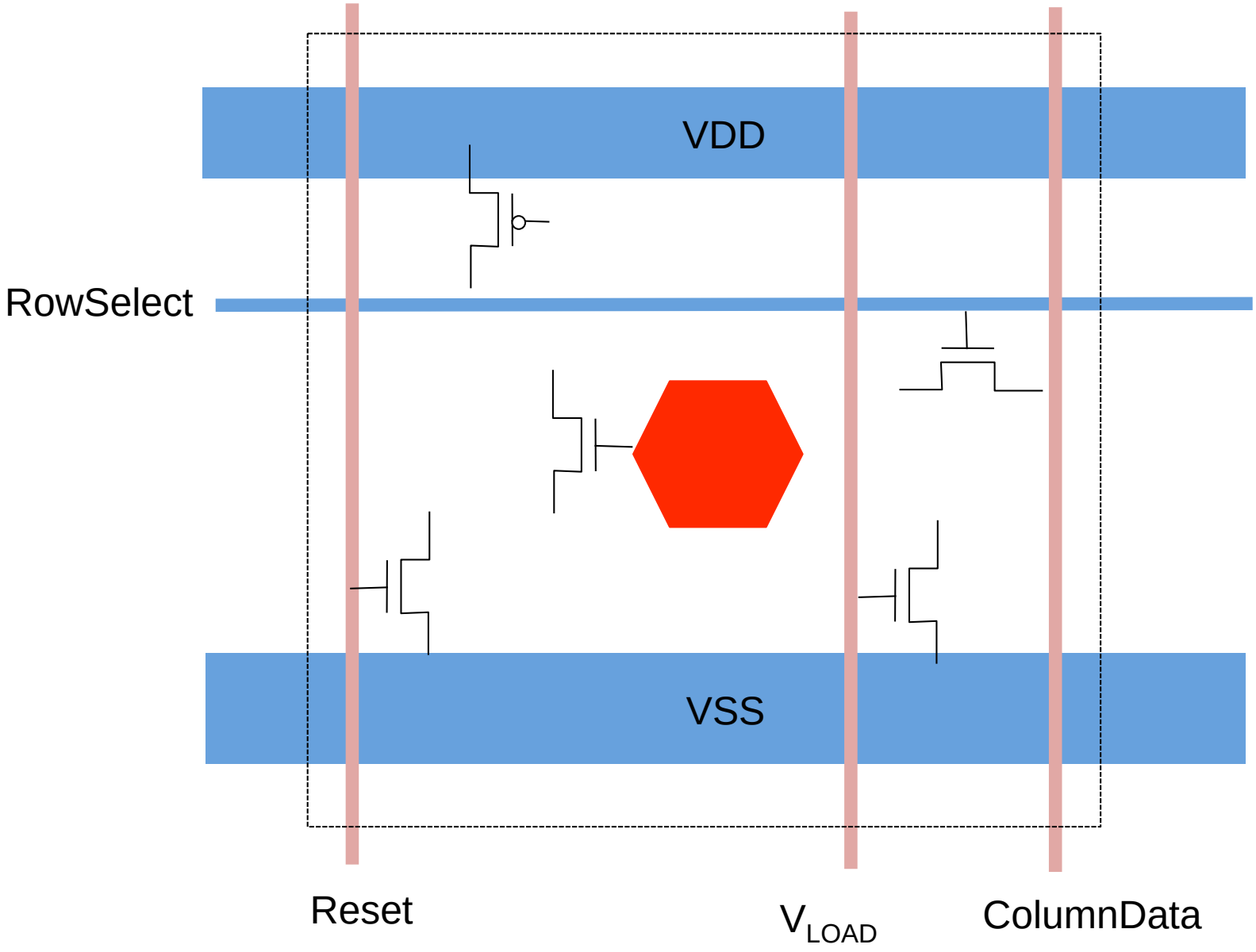
60x60 um²

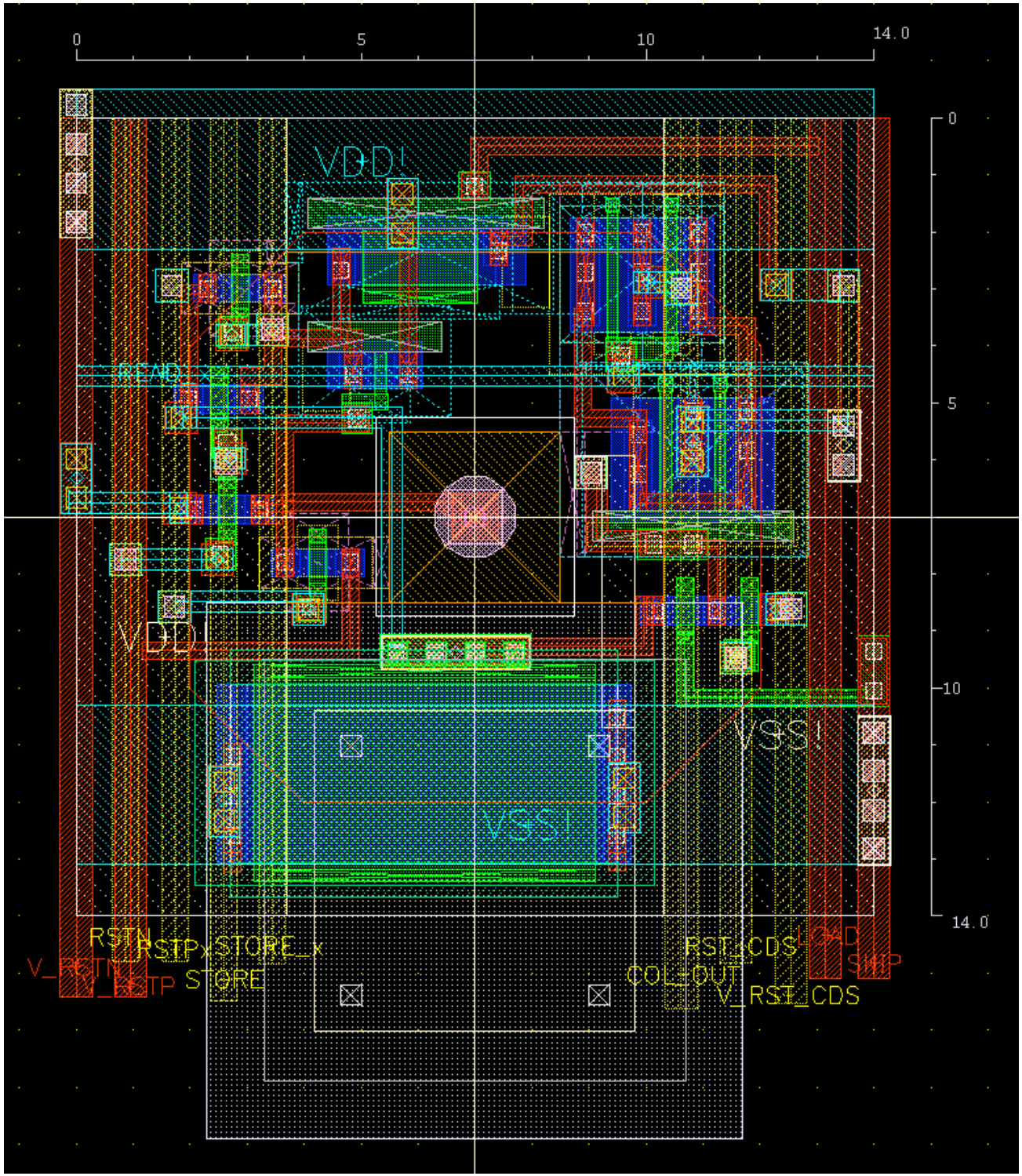
積分型Pixel回路例



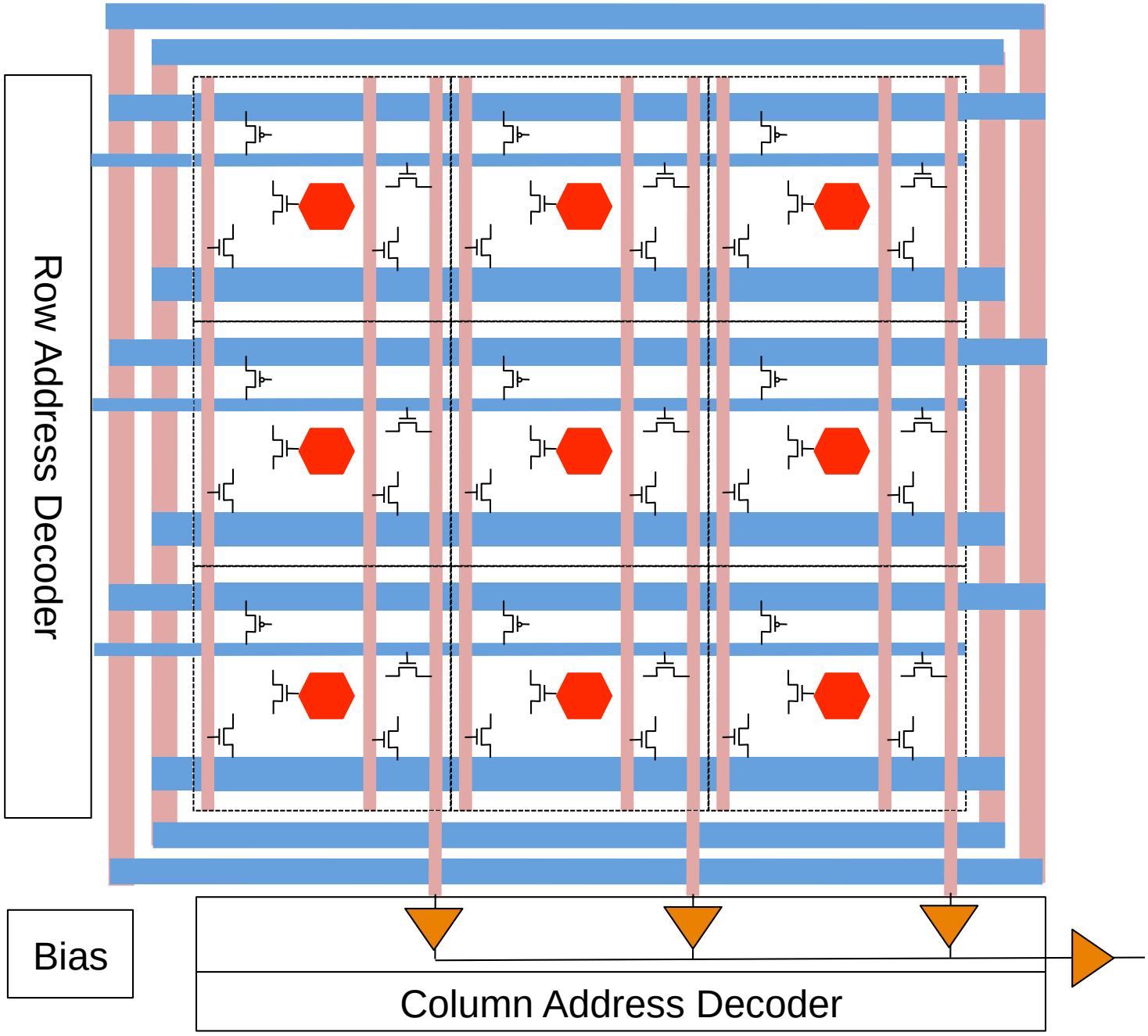
V_{LOAD}は低消費電力モード
にしたい時はGNDに落とす

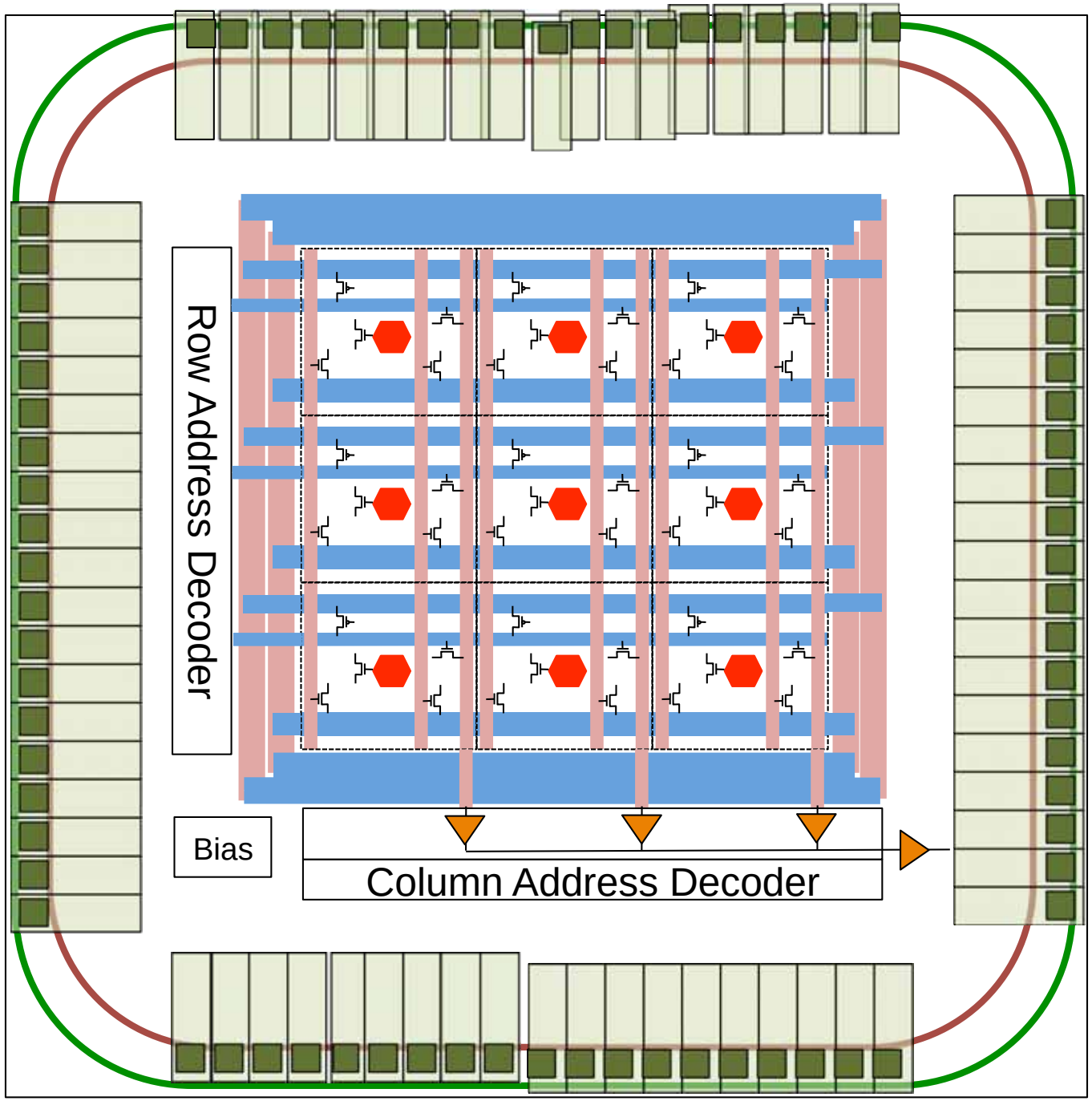
Pixel Layout例

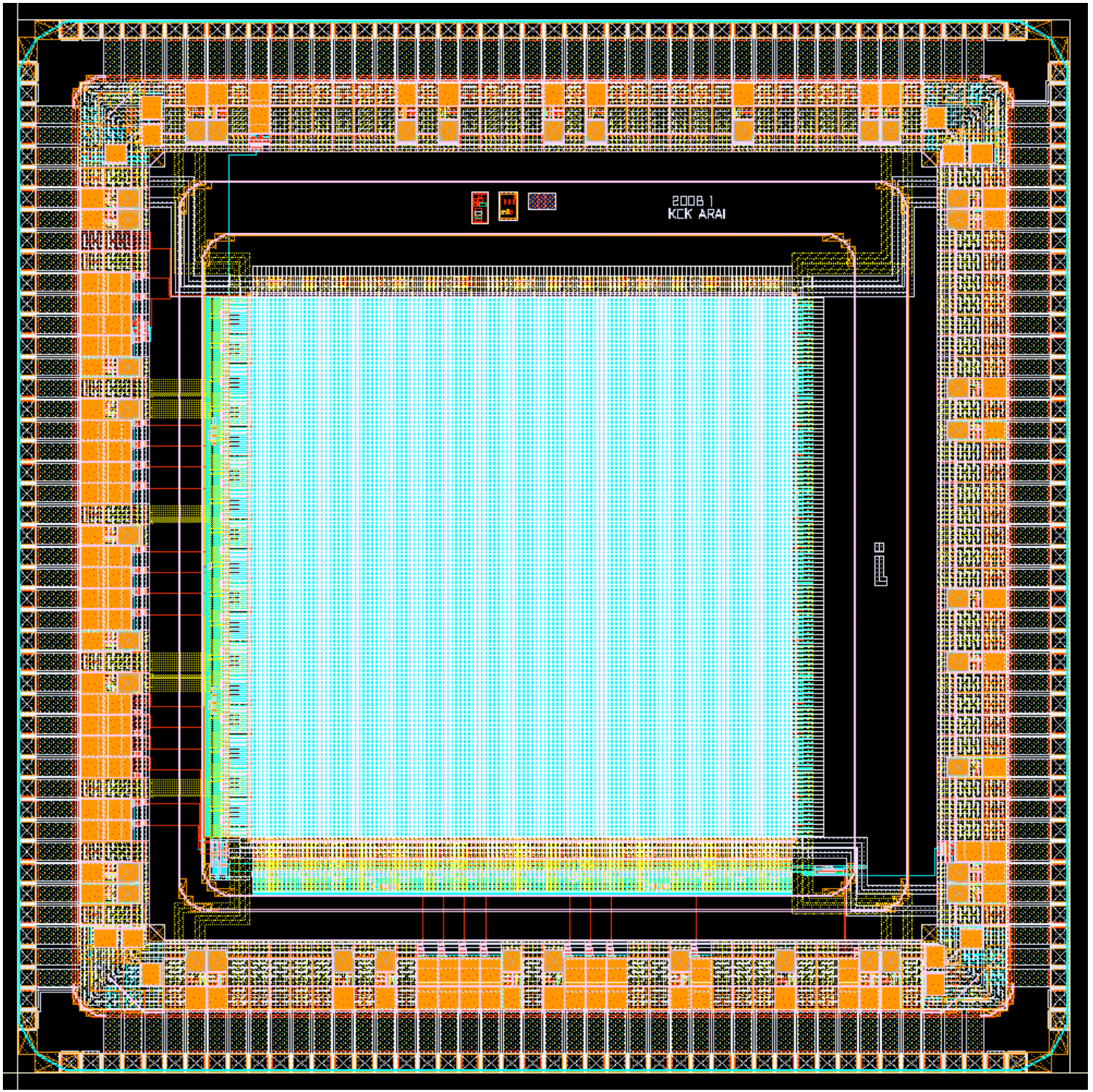



0
5
10
14.0
VDD!
READ
VDD!
VSS!
VSS!
RSTN
V_RSTN
RSTP
STORE_x
V_RSTP
STORE
RST_CDS
COL_OUT
V_RST_CDS
SHP

Pixel Layout例



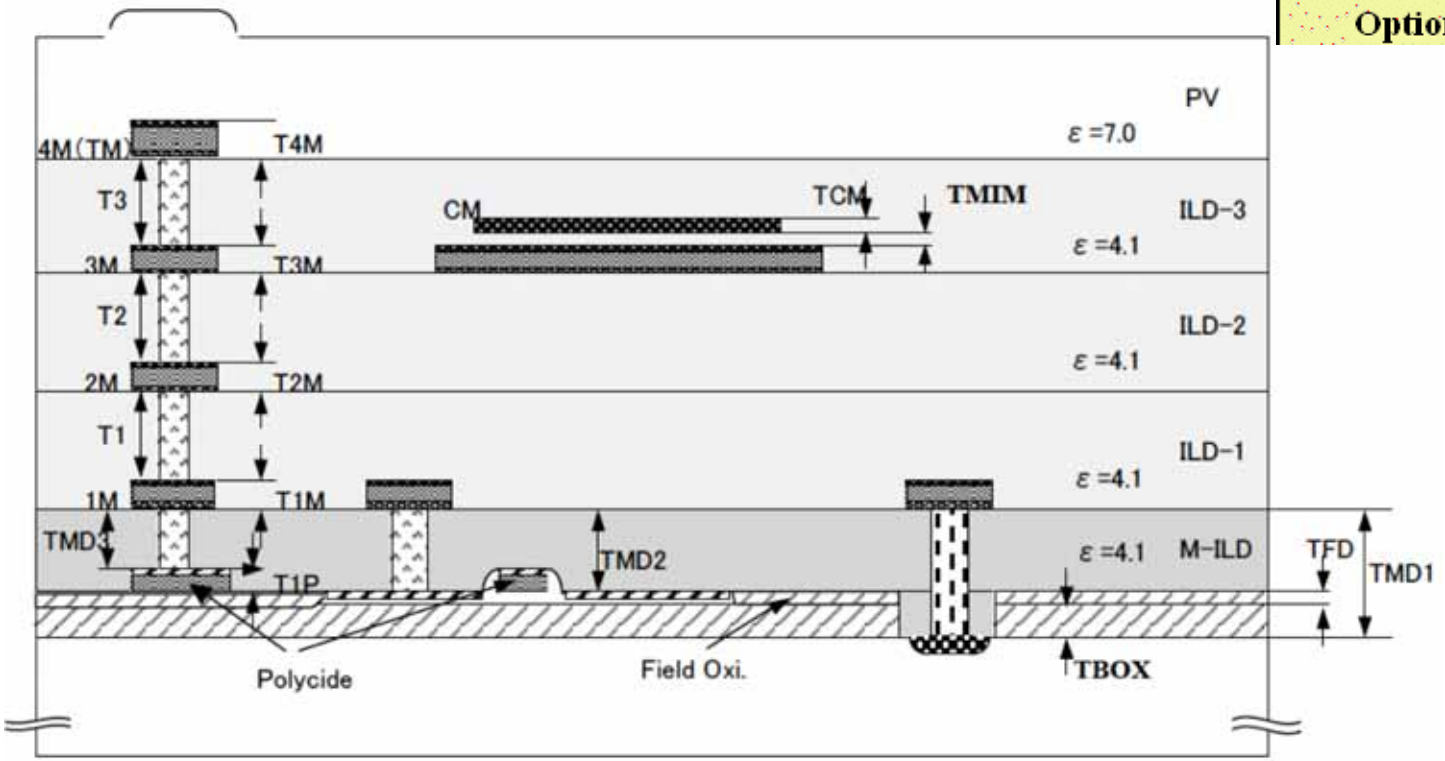

Row Address Decoder
Bias
Column Address Decoder


2008 1
KCK ARAI

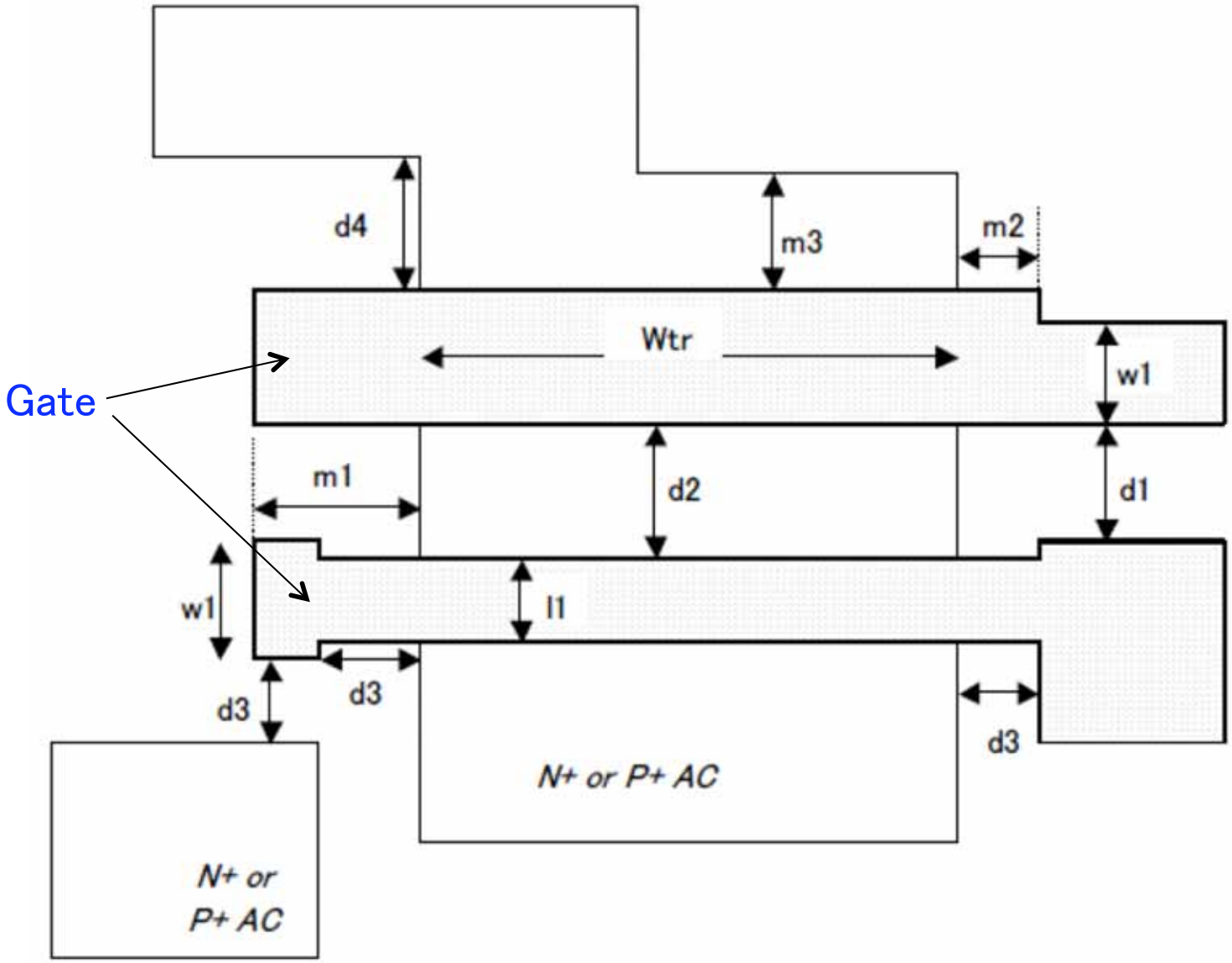
沖0.2 mm SOI CMOS Process with Sensor option

	0.20umSOI Low-Leak
· Core Vdd	1.8V
· I/O Vdd	1.8/3.3V
· Gate Length	0.2um
· Gate Oxide	4.5/7.0nm
· Core Ion N/P (uA/um)	210/-90 (@1.8V)
· Ioff	<0.1pA/um (I/O<0.1pA/um)
· Wiring Pitch	0.9um
· RF/Analog Option	MIM, Inductor Low Vt, DMOS

Layers & Contacts



Design Rule (Drawing Rule)



主なパラメータ

許容電流密度

Metal 配線	< 1 mA/μm
Contact, Via	< 0.78 mA/個

シート抵抗

シリサイド拡散、ゲート	10 Ω/sq
シリサイドなし拡散	250 Ω/sq
メタル	0.06 Ω/sq
Contact	12 Ω/個
Via	3 Ω/個
ポリ抵抗	410 Ω/sq

容量

MIM Capacitance	1 fF/μm^2
Gate 容量	8 fF/μm^2
Metal 浮遊容量	~0.05 fF/μm^2

まとめ

- SOIプロセスは耐放射線性、耐温度性等に於いて従来のバルクCMOSプロセスに比べて優れた特徴を持つ。
- SOI張合わせウエハーを使用する事により、放射線センサーと読み出し回路を一体化出来る。
- ピクセル設計は高い技術が要求されるが、複雑なロジック回路と違い、同じピクセルの繰り返しなので、フルカスタム設計が行え、全てを自分の手で設計出来る。
- 年に2回程度MPWランを行っているので、興味のある方は参加して下さい。