SiTCP による MPPC 読み出し回路の開発状況

東北大理 , KEK (A), Open-It (B)

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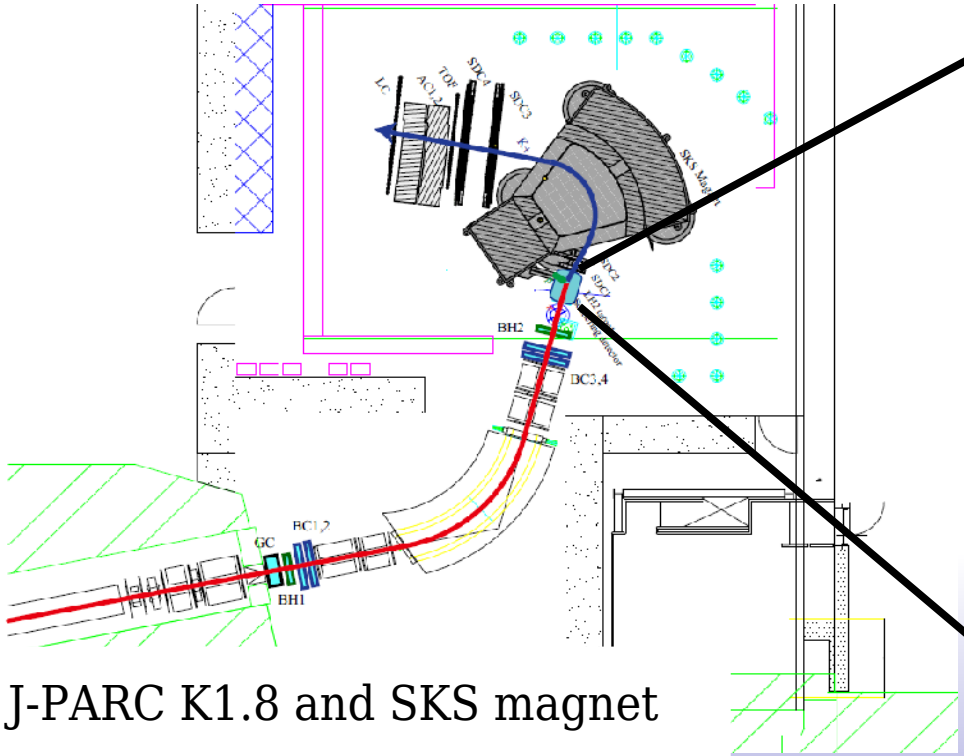
Contents

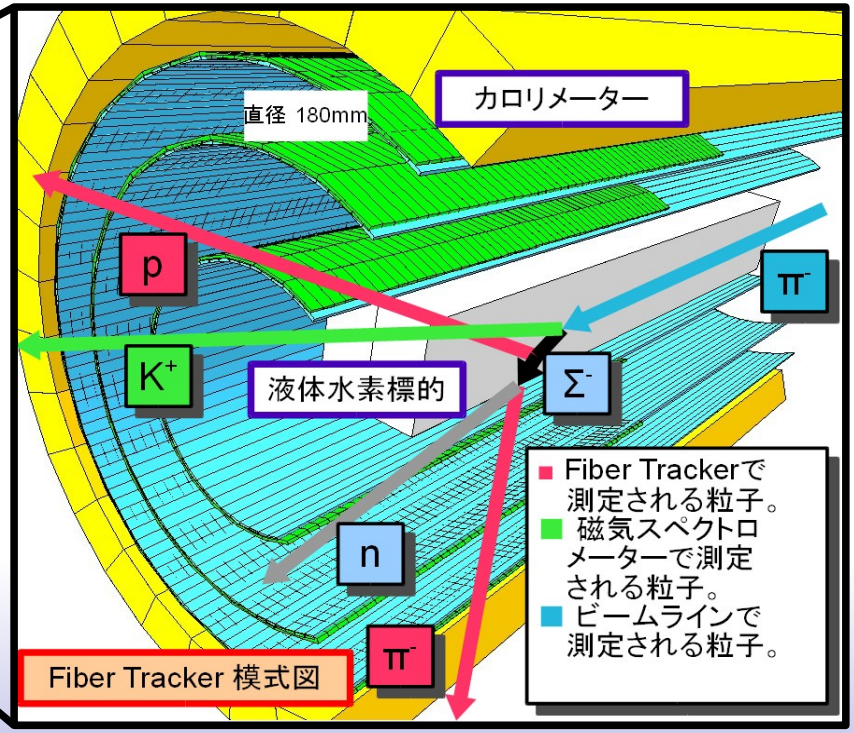
- Motivation
  - Detectors
  - Electronics
- Introduction of SPIROC
- Development of Electronics
- Summary
- 失敗談

Motivation

	Gain	Response	Magnet field	Bias voltage	Area
PPD	~10^6	Very Fast	Not Influenced	Low	Small
PMT	10^6~10^7	Very Fast	Influenced	High	Large



J-PARC K1.8 and SKS magnet



Possible to construct a very fine and small detector near by spectrometer with MPPC.

Σp scattering experiment at J-PARC

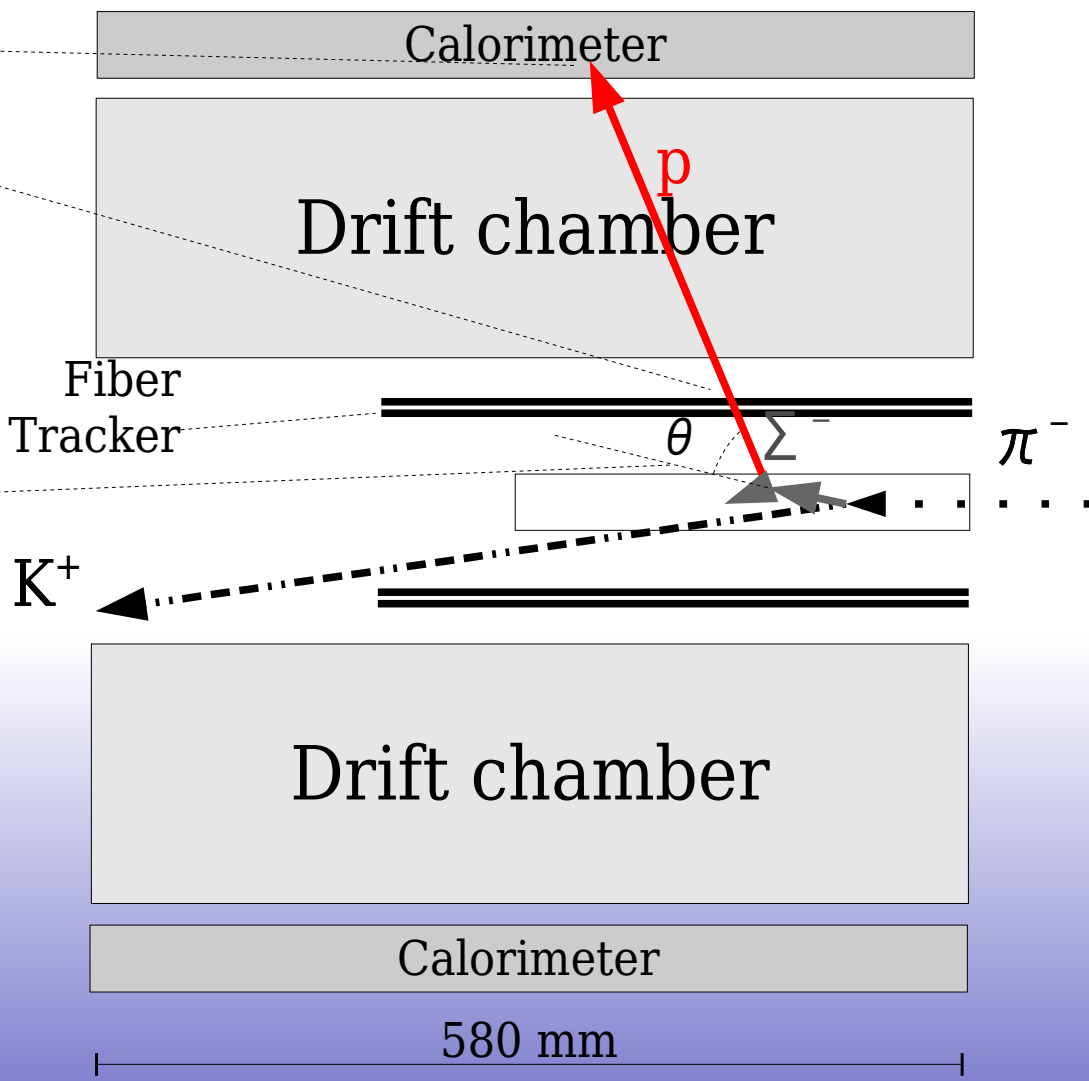
Measurement of proton

Energy at calorimeter

Energy deposit at fibers

Total energy of proton

scattering angle



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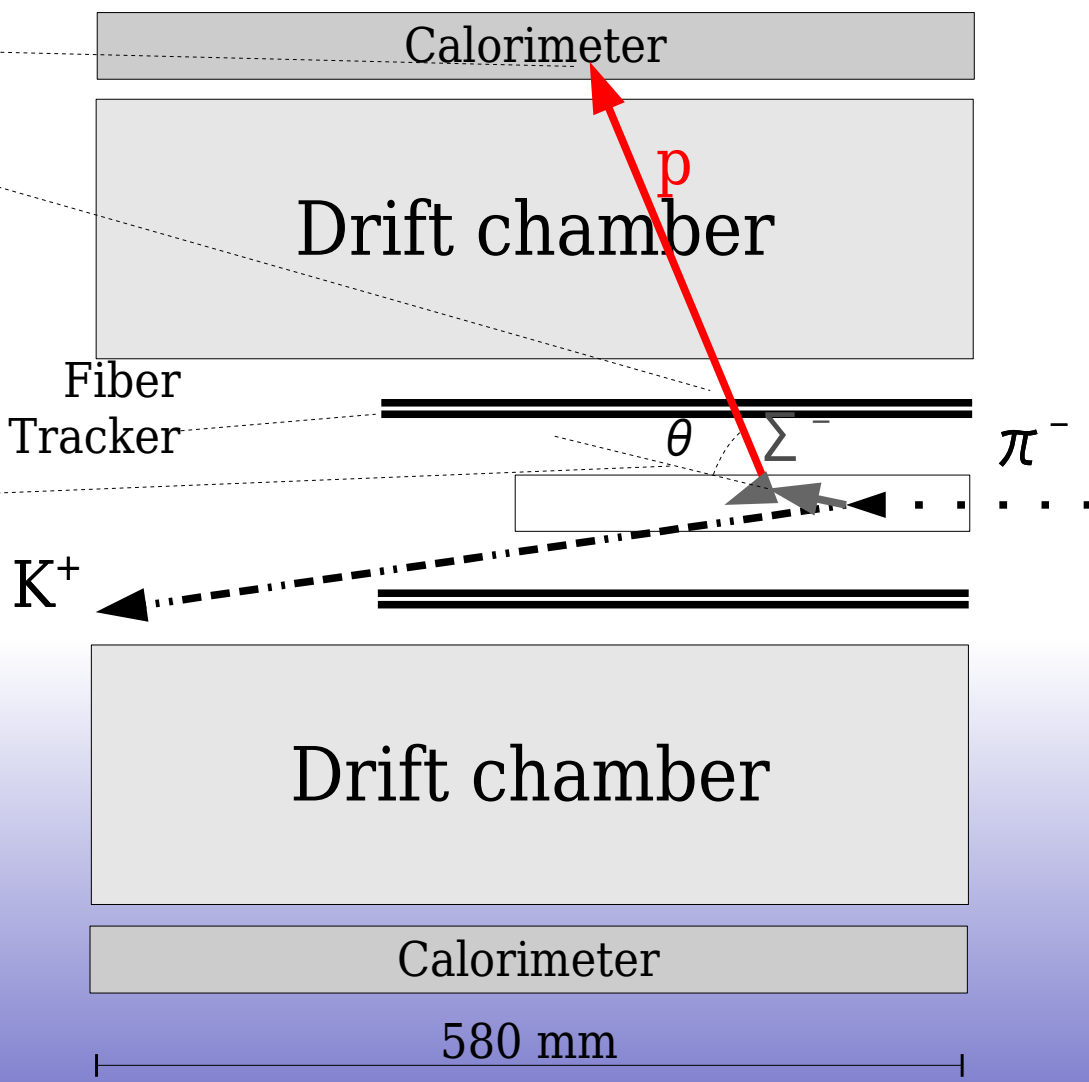
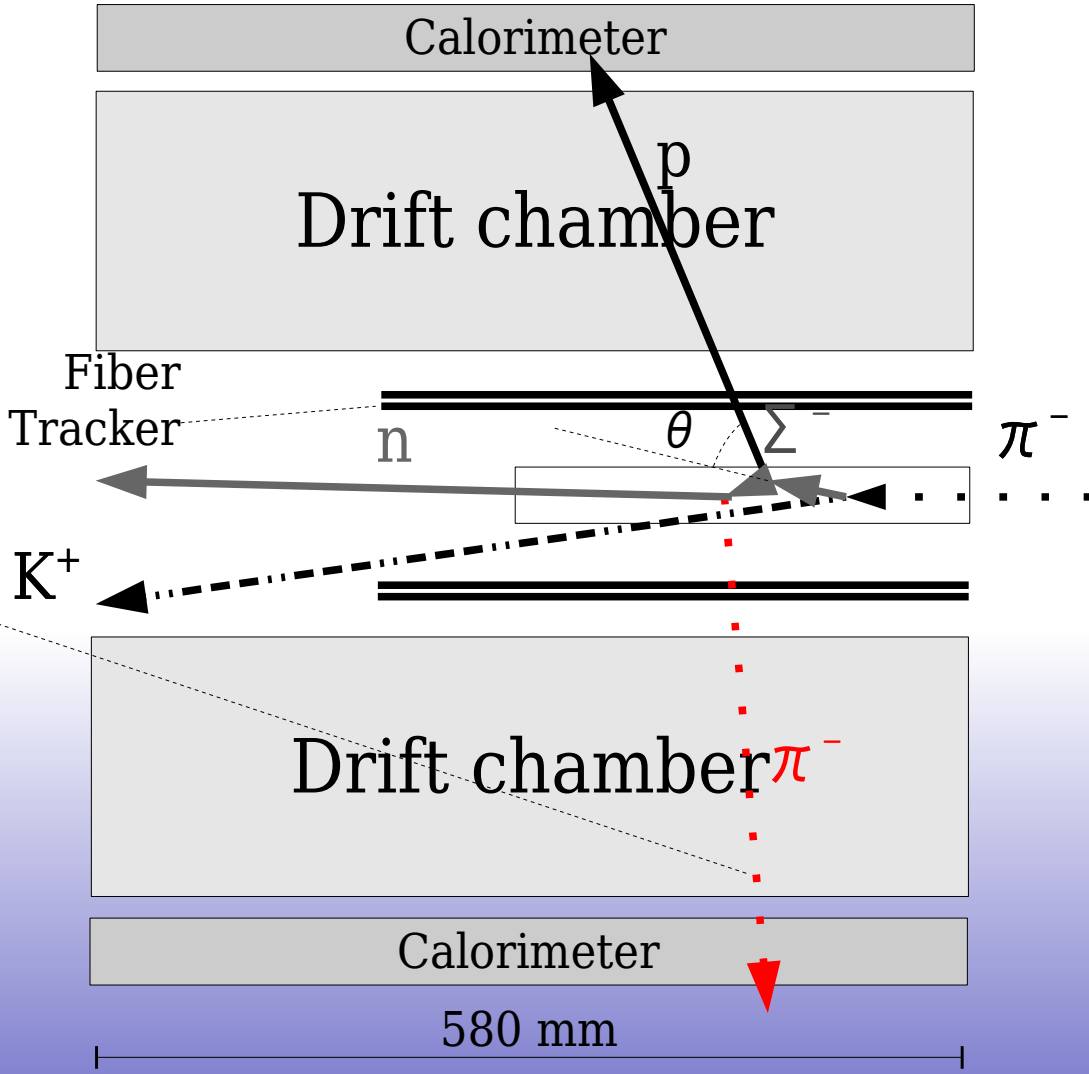


Possible to solve kinematics about Σp scattering

Σp scattering experiment at J-PARC

Measurement of proton



decay angle

Background reduction

Σp scattering experiment at J-PARC

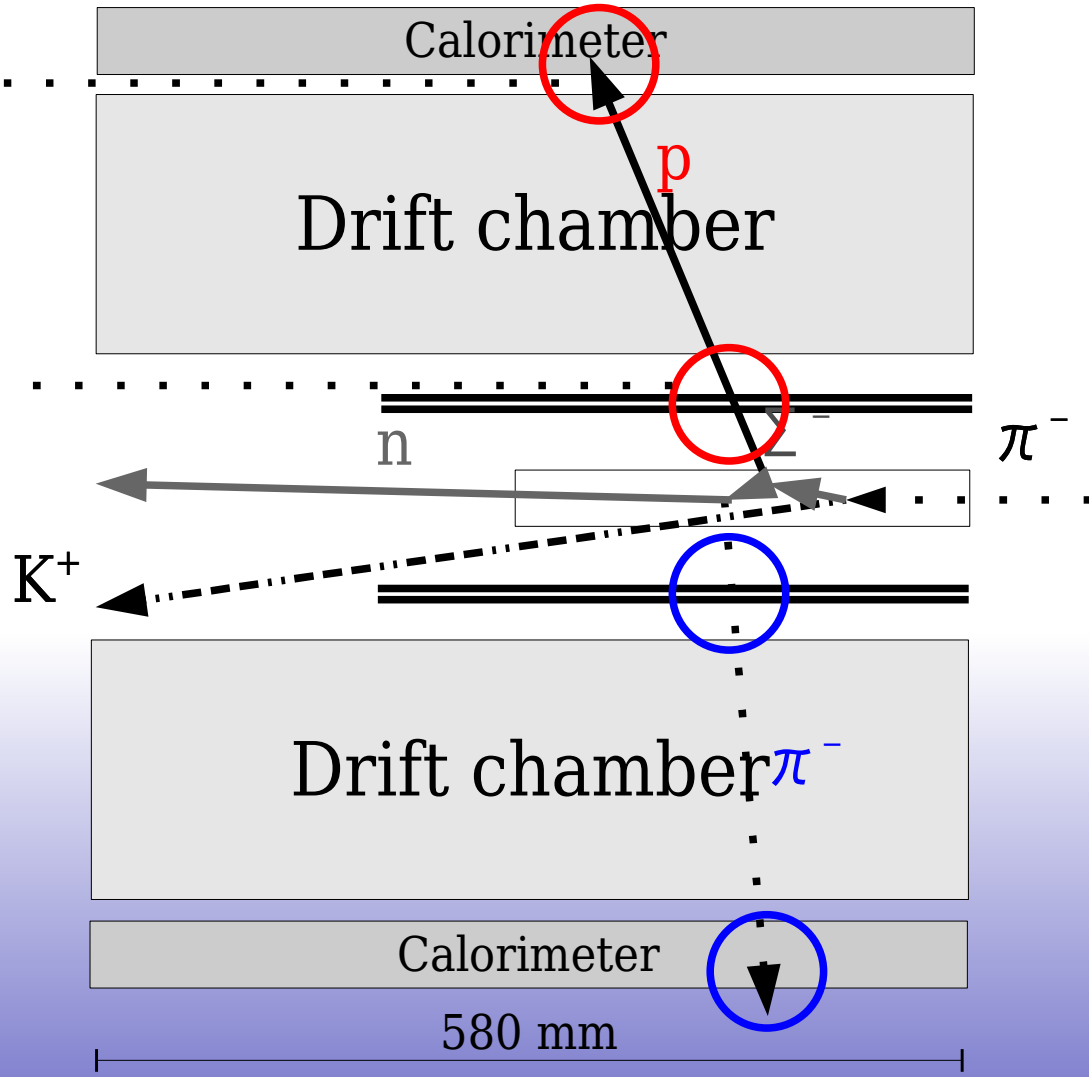
π-p sepalation *ΔE-E* method

ΔE-E : Correlation of calorimeter and fiber

Energy deposit at calorimeter

2 dimensional histogram

Energy deposit at fibers

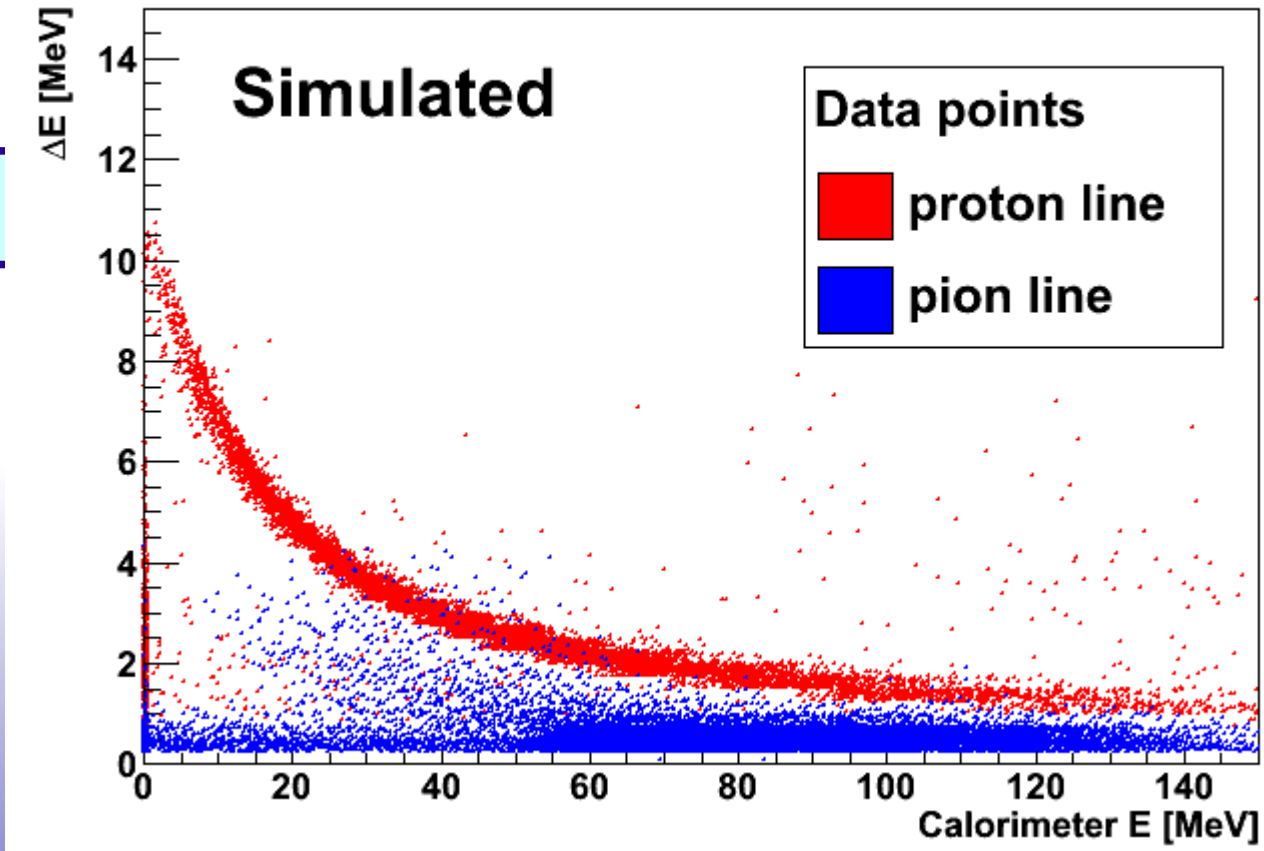


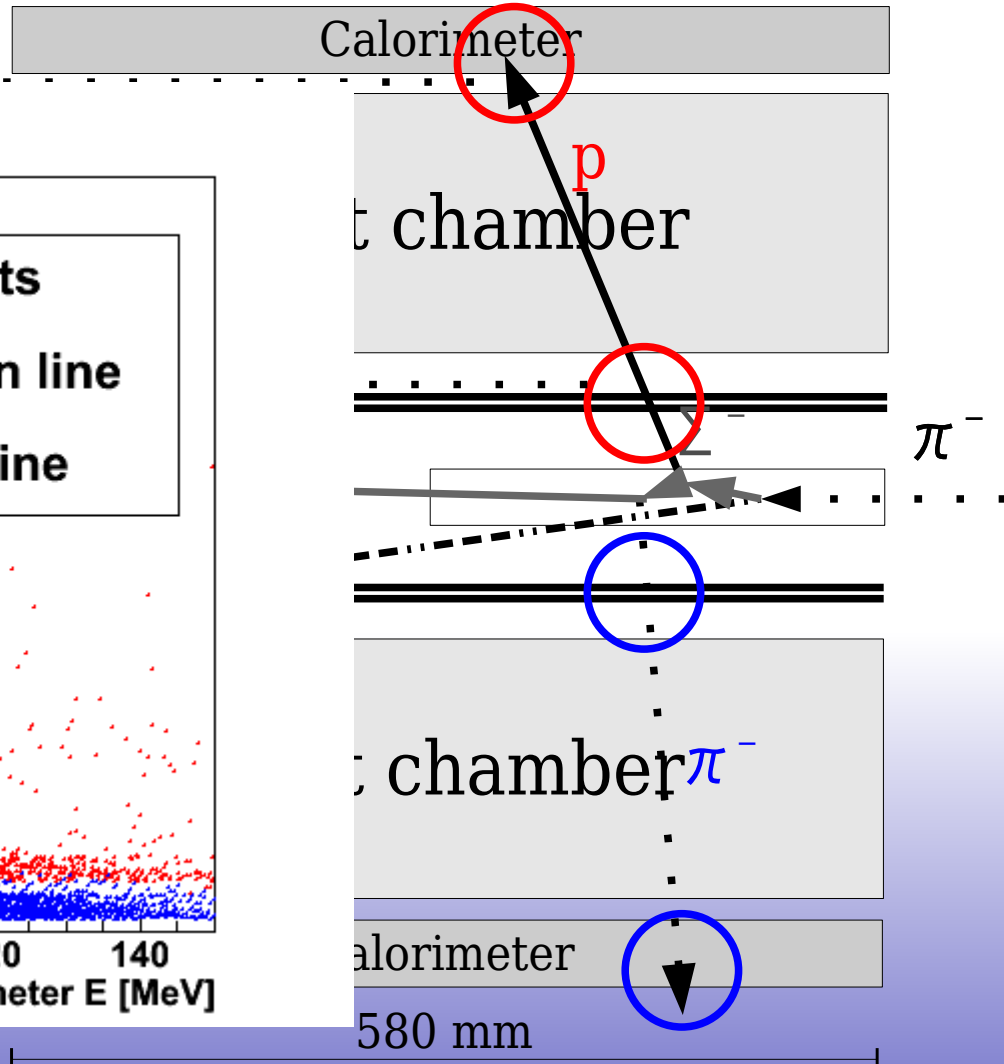
Σp scattering experiment at J-PARC

π-p sepalation *ΔE-E* method

ΔE-E : Correlation of calorimeter and fiber

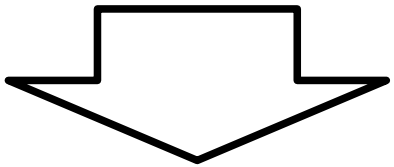
ΔE-E distribution





Motivation

There are 2000 channels MPPC
in Fiber Tracker.



Hard to readout
with existent electronics.

**Necessary to develop
a new eletronics.**

- **Multi-channels**
- **Asynchronous**
- **Easy to use**

**SPIROC chip
as a front end ASIC**

Silicon PM Integrated Read Out Chip
SPIROC

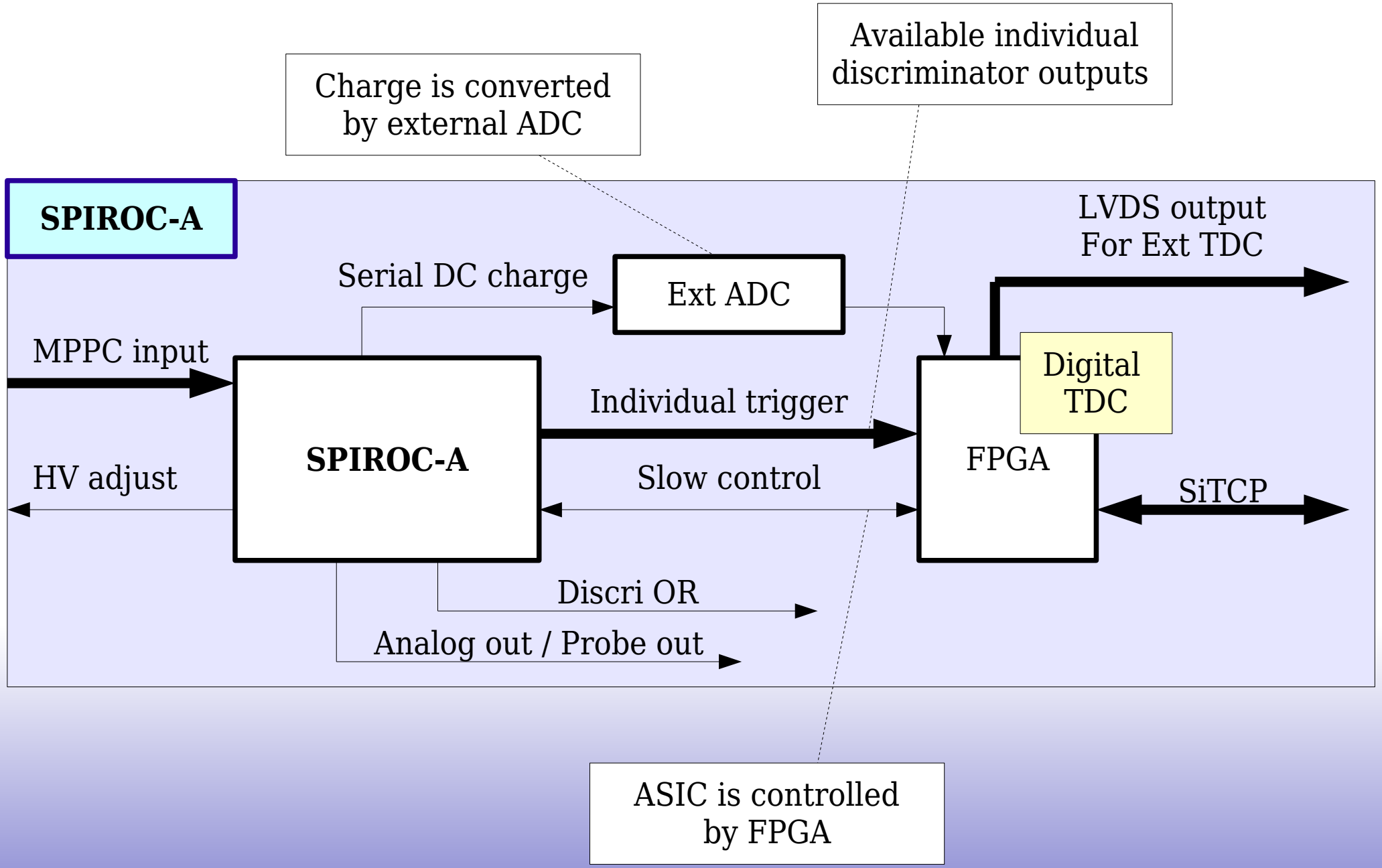
32 channels inputs
HV adjustment (4.5V 8bit)
AMP, shaper, discriminator
Variable parameters
Asynchronous analog output

TCP/Ethernet

Universal standard
High speed data transmit (~1 Gbps)

By using SiTCP
Controlled by C/C++ on Linux.

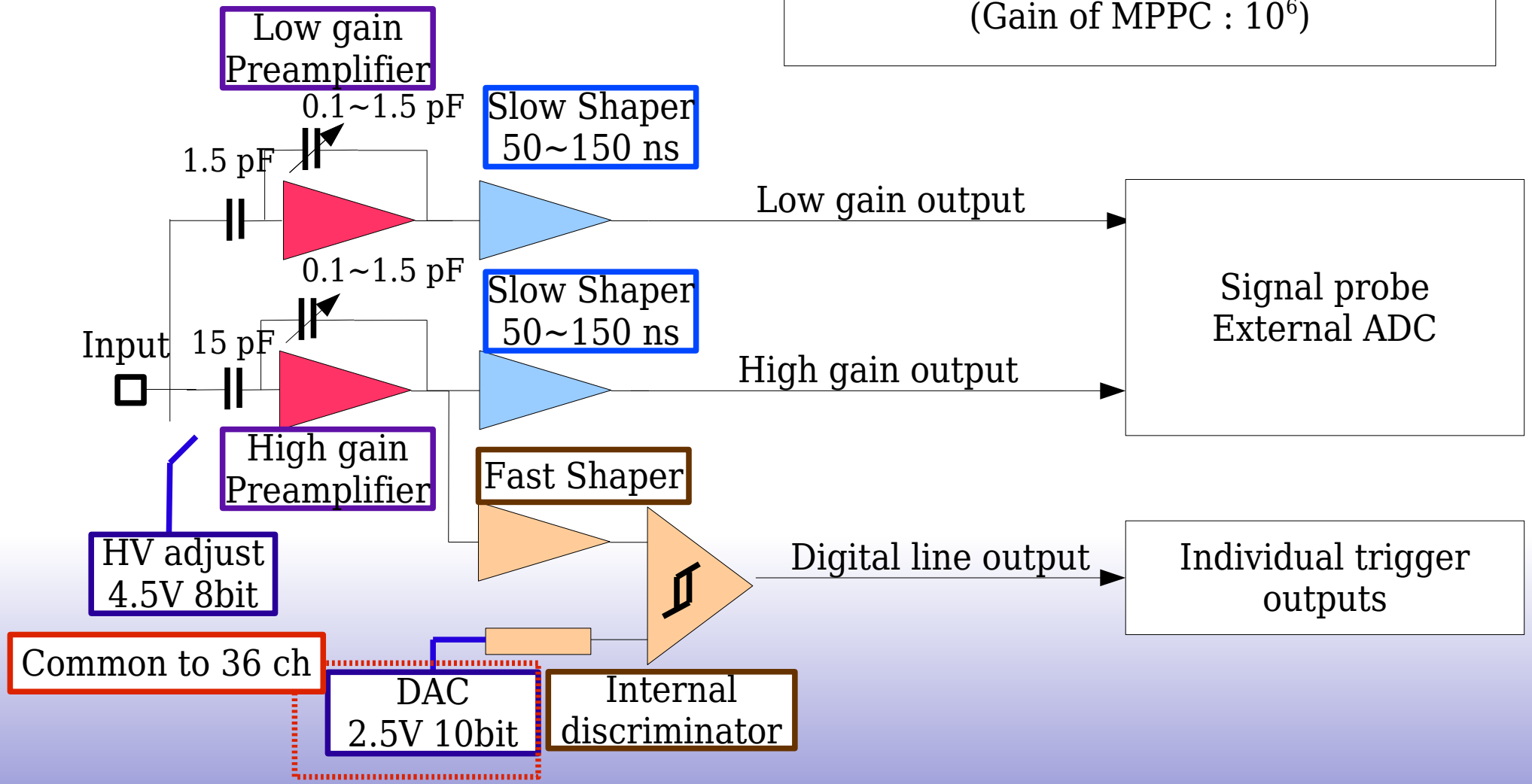
Introduction of SPIROC



Introduction of SPIROC

Schema of SPIROC analog part

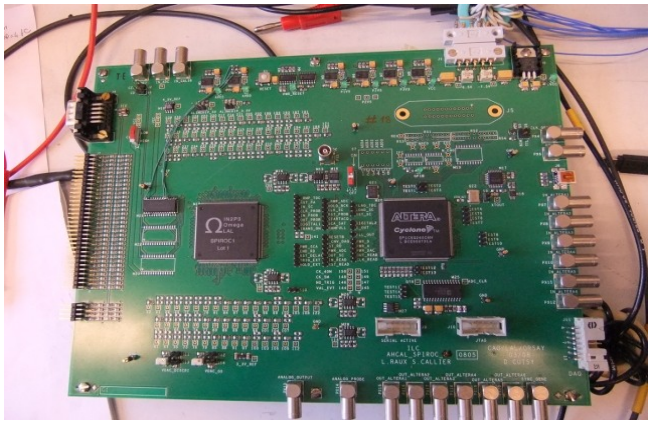
Dynamic range 160 fC ~ 320 pC
(Gain of MPPC : 10^6)



Development of Electronics

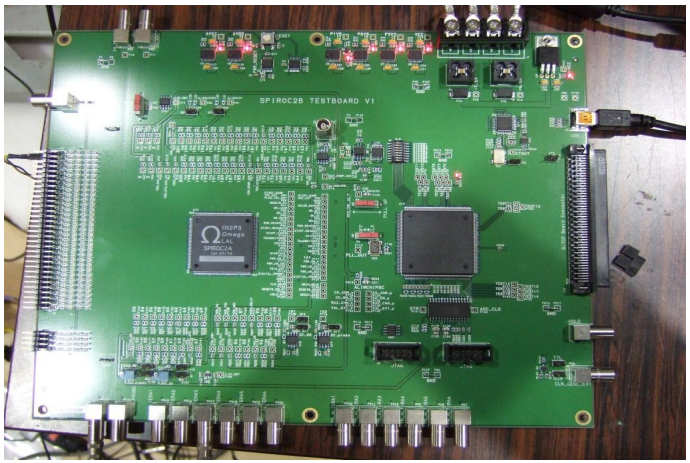
Original evaluation board (Made by LAL)

- I/F : USB
- FPGA : Altera (cyclone)
- Control software : LabView
- Signal level : LVTTL



KEK evaluation board ver.1

- I/F : USB / **SiTCP (SOY)**
- FPGA : Altera (cyclone)
- Control software : LabView / **C/C++**
- Signal level : LVTTL
- Chip : SPIROC2A



KEK evaluation board ver.2

- I/F : **SiTCP (SOY)**
- FPGA : **Xilinx (SPARTAN6)**
- Control software : **C/C++**
- Signal level : **NIM / LVDS**
- Chip : SPIROC-A

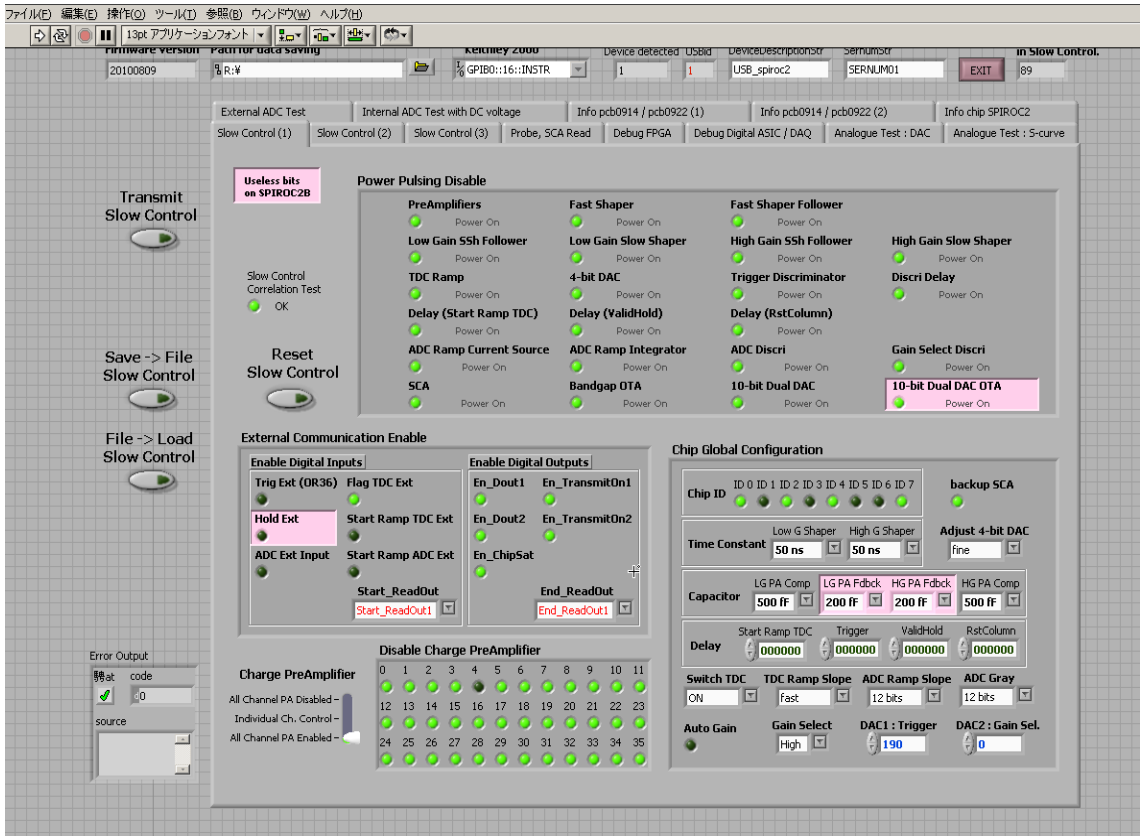
Finish
PCB layout

Development of Electronics

About original board

Front panel of LabView program.
We can change all resister with this program with GUI.

Total # of resister	60
Total # of bits	712



Development of Electronics

About original board

Front panel of LabView program.
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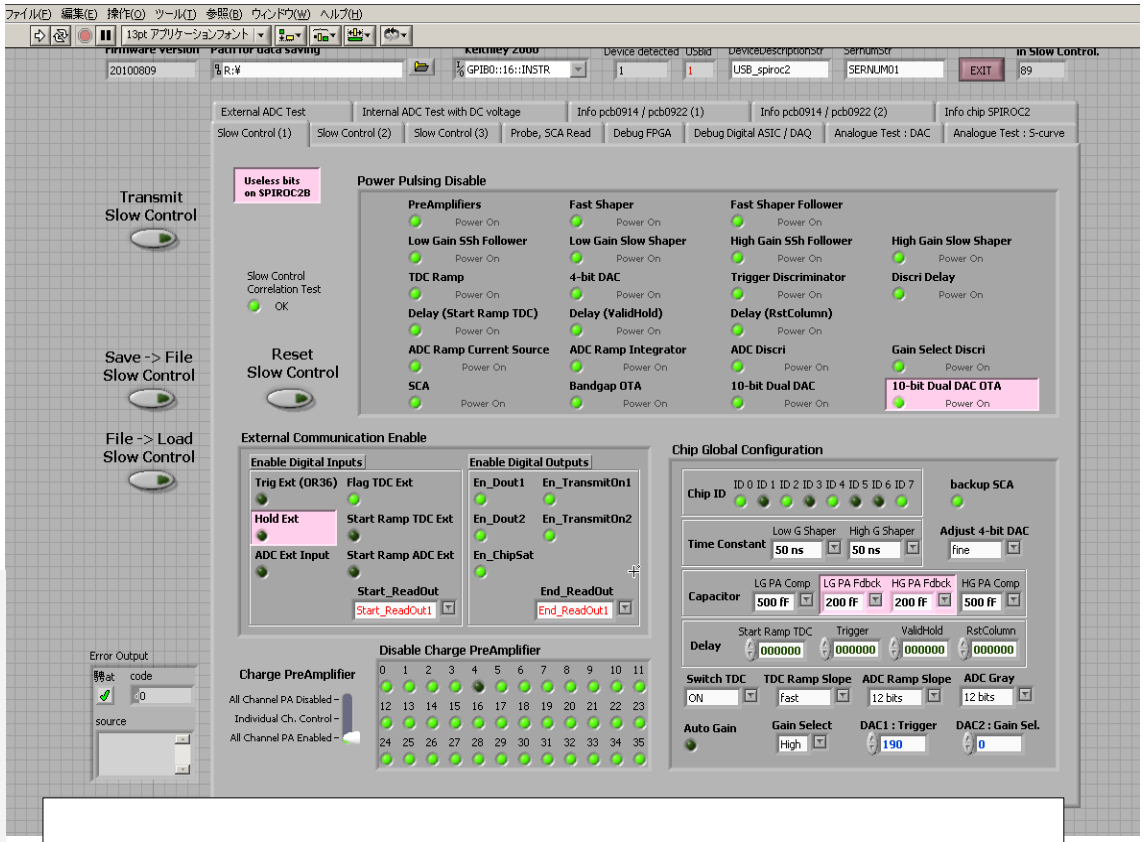
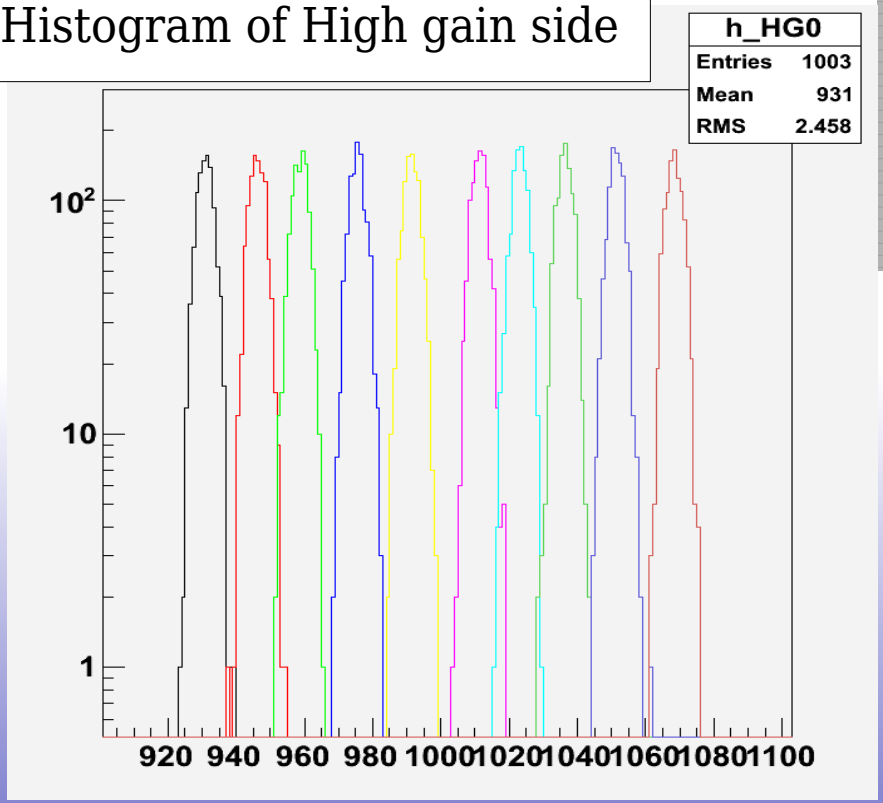
Total # of resister 60
Total # of bits 712



Histogram of High gain side



Each peak corresponds to the number of P.E.
(By using charge injection)

Development of Electronics

About KEK board ver.1

Slow control and DAQ with Ext ADC via SiTCP are implemented.

But now…

- Only text mode
- We have to know all resister behavior

  =>Front panel with GUI is needed.

Development of Electronics

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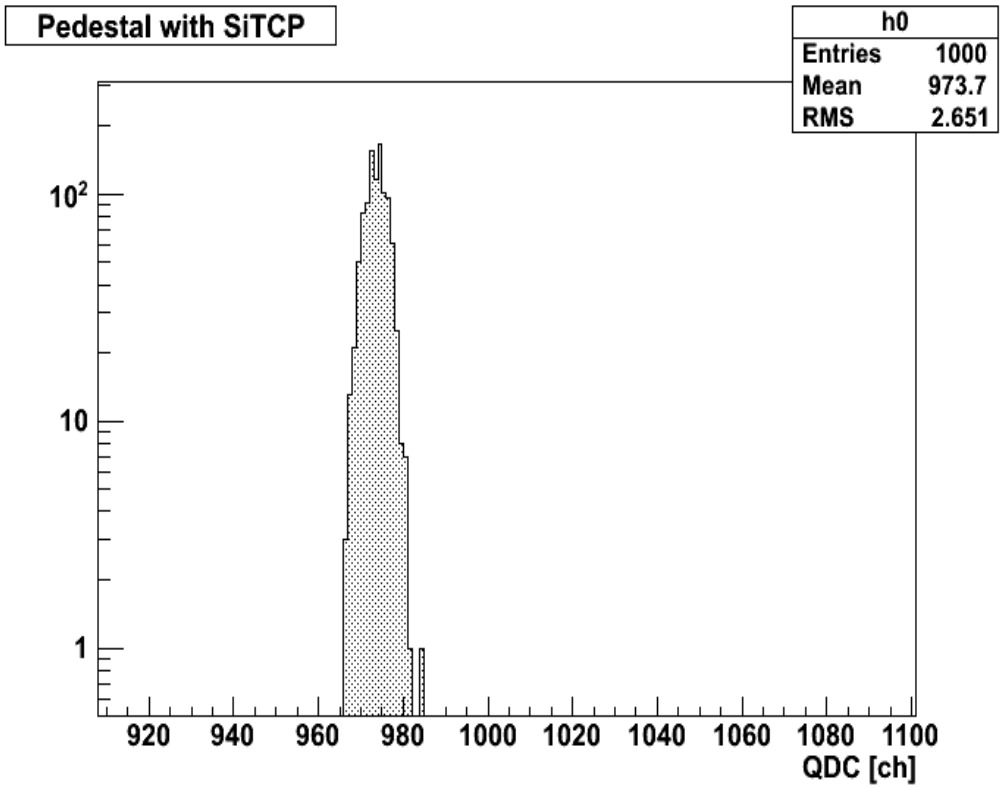


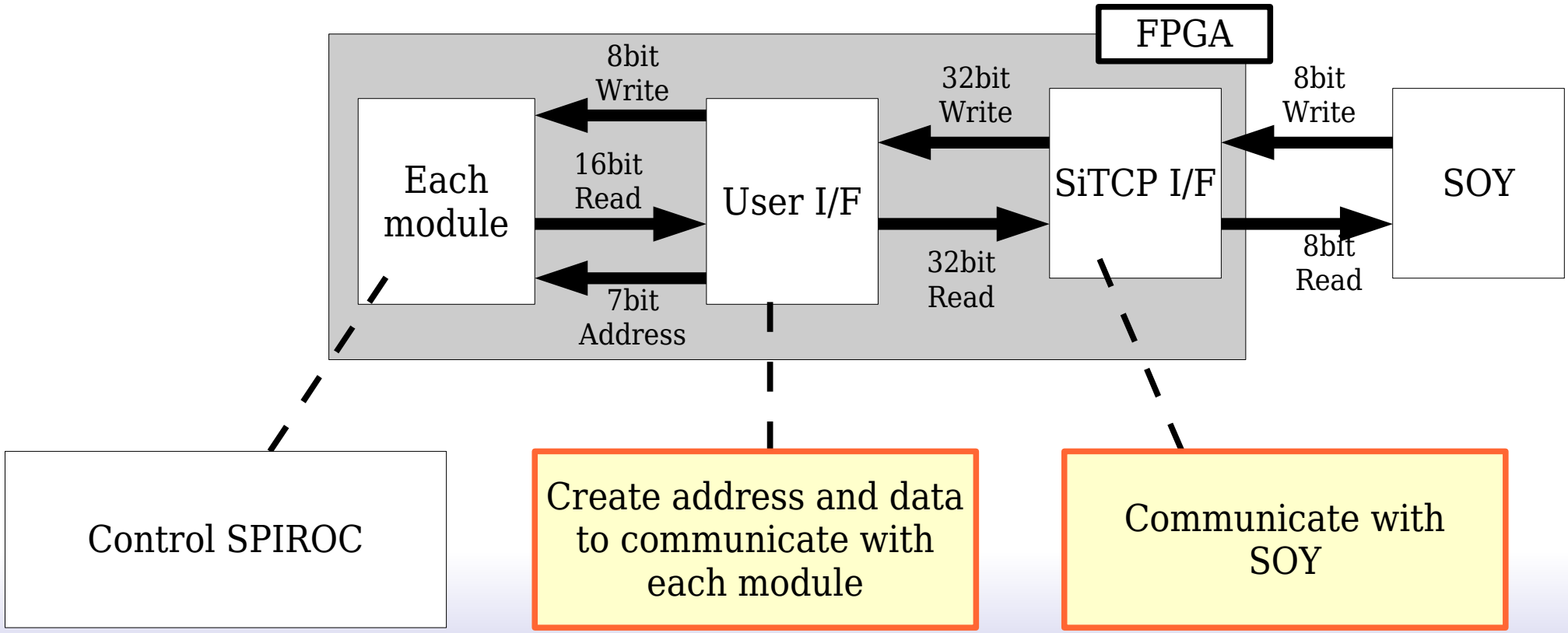
SiTCP

DAQ rate : ~250 Hz
(in Global Network)
Limited by
overhead of network funcitons
and network condition.

LabView

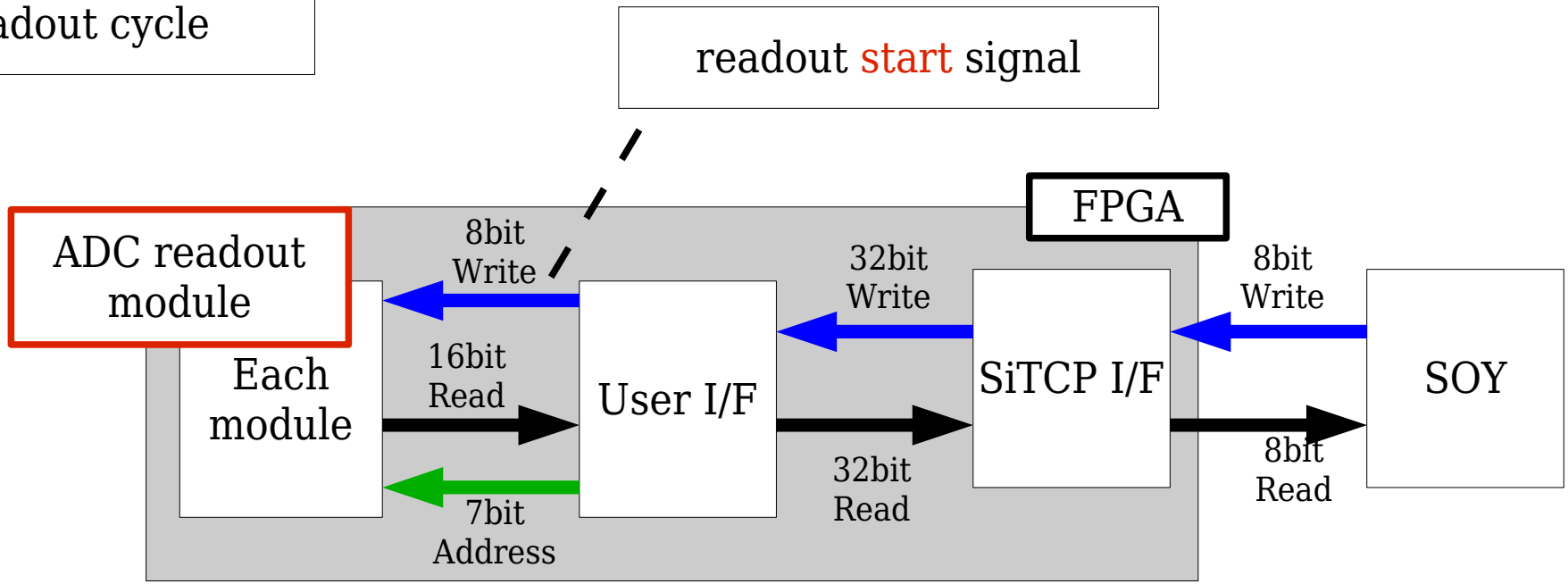
DAQ rate : ~10Hz
Limited by LabView program.

Development of Electronics

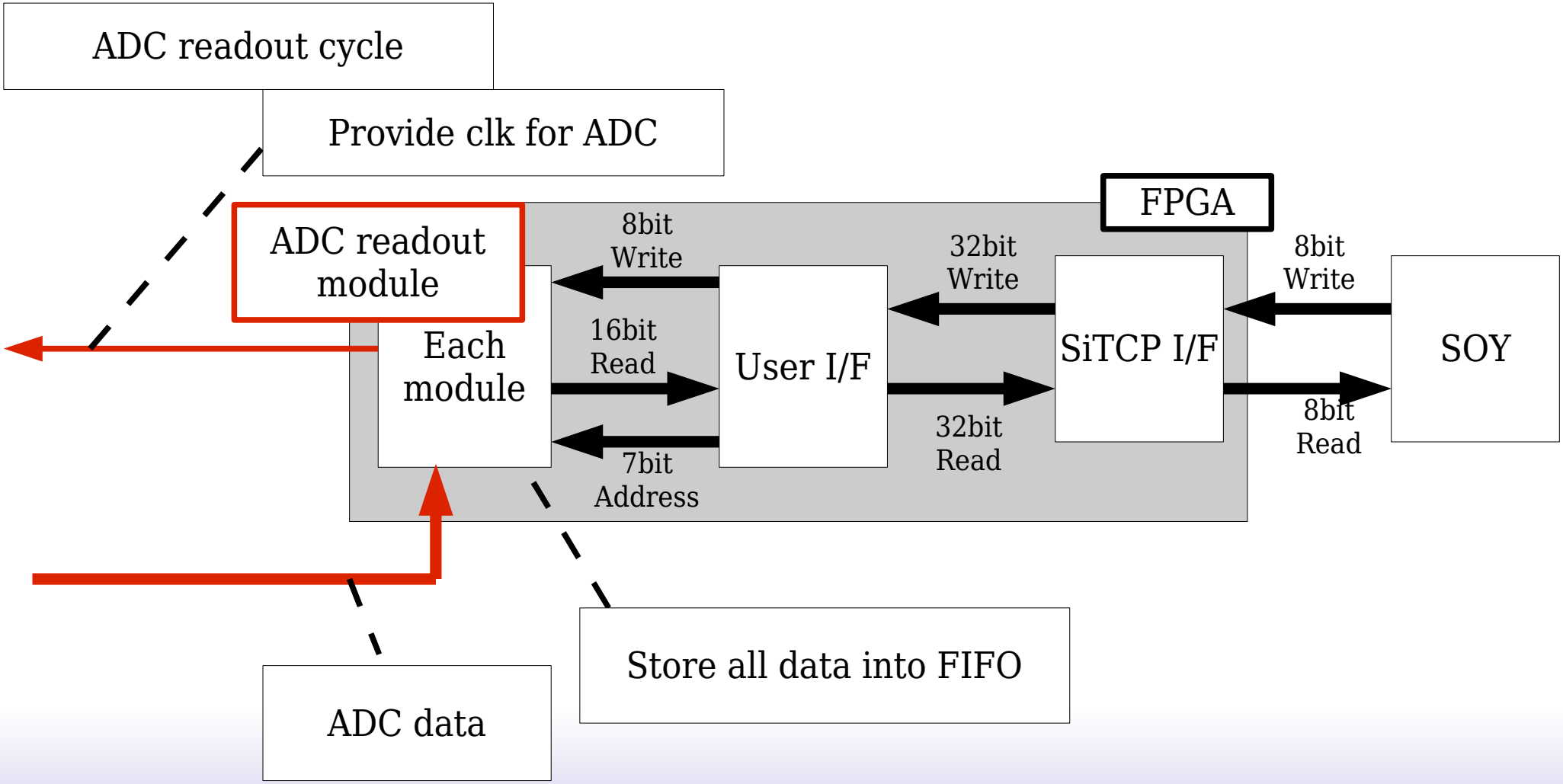


Development of Electronics

ADC readout cycle



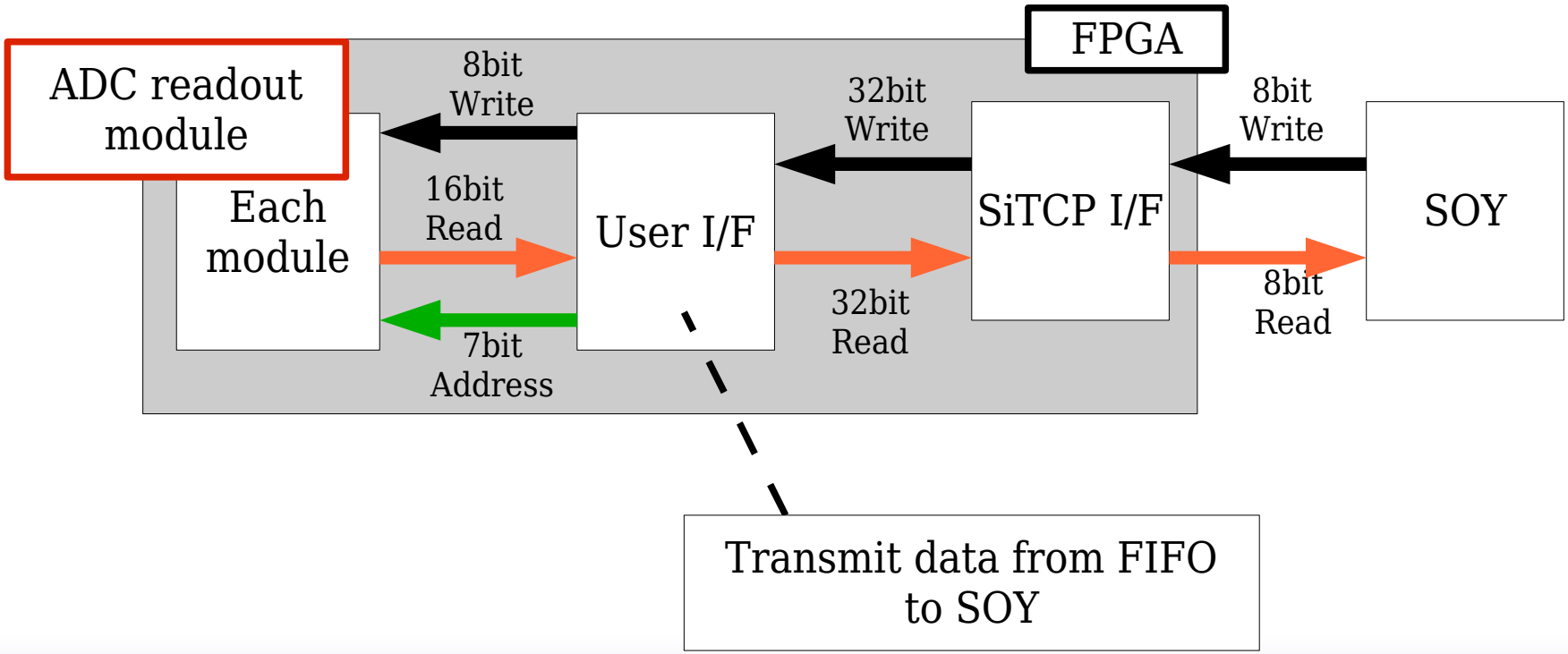
Development of Electronics



A/D conversion time : ~ 60 μs

Development of Electronics

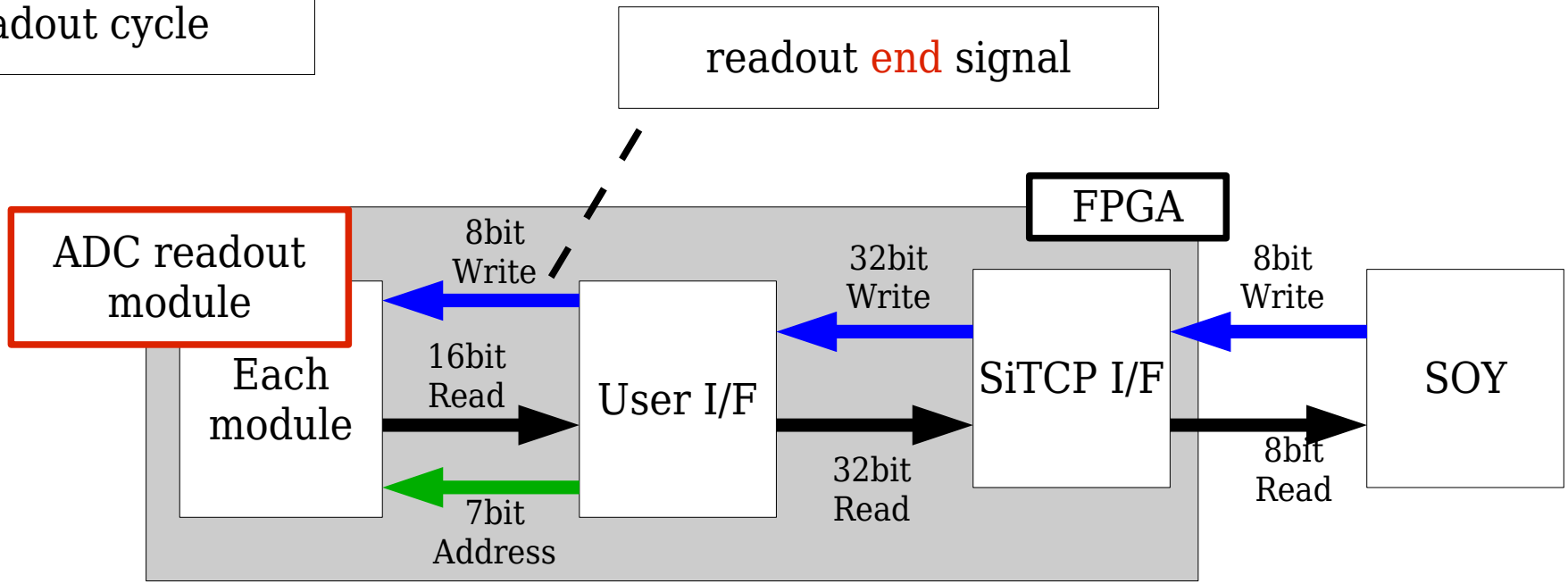
ADC readout cycle



Transmit time : 30 ~ 50 μs (Depend on network condition)

Development of Electronics

ADC readout cycle



End cycle

Performance of FPGA firmware

DAQ performance with Ext ADC

of bits : 1152 bits (32 bit x 36 channels)
Mean DAQ rate : 250 Hz
Details : A/D conversion 60 μs
+ Transmit to SOY 50 μs
+ Overhead of socket functions ～ a few **ms**

Request

Request DAQ rate : 3 kHz(Max speed of Hadron DAQ)
It's not realistic to readout all channels
⇒ pedestal suppression
After pedestal suppression :
(16bit(header) + 16bit(adc) + 16bit(tdc))x30 channels
= 1440 bits

Performance of FPGA firmware

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of bits : 1152 bits (32 bit x 36 channels)
Mean DAQ rate : 250 Hz
Details : A/D conversion 60 μs
+ Transmit to SOY 50 μs
~~+ Overhead of socket functions~~ ~ a few **ms**

Improve firmware

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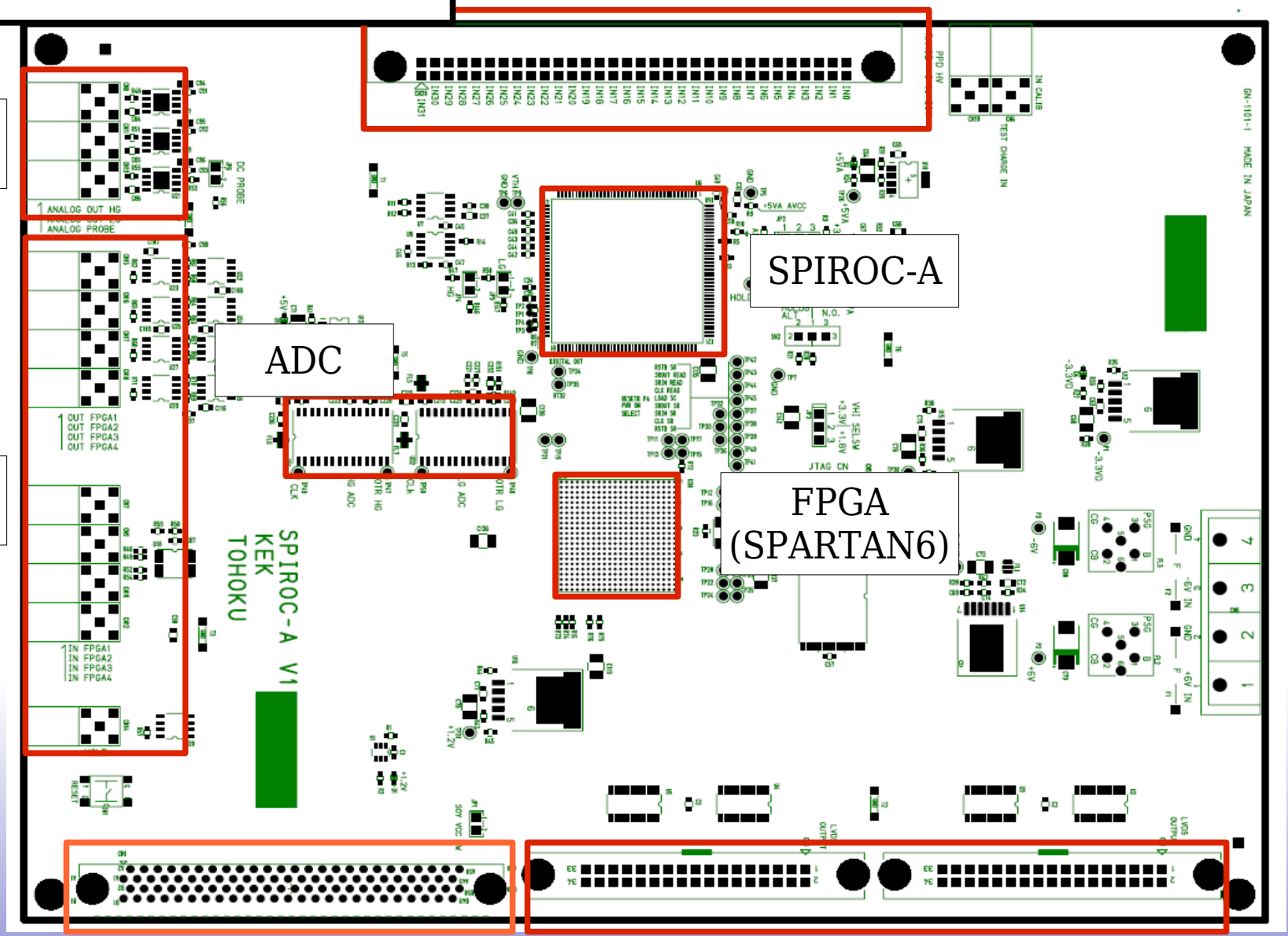
Layout of PCB

About KEK board ver.2



Layout of PCB

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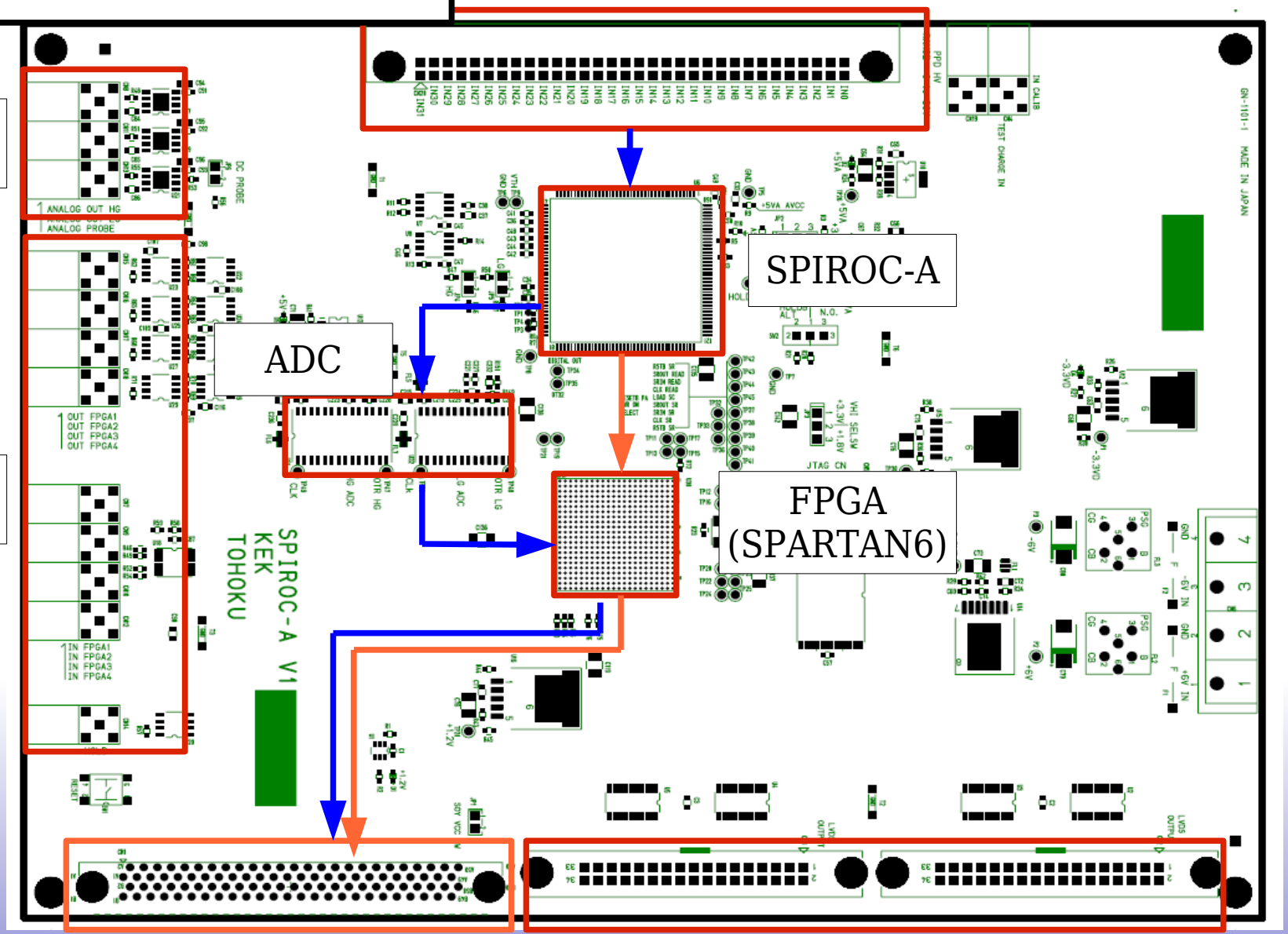

Layout of PCB

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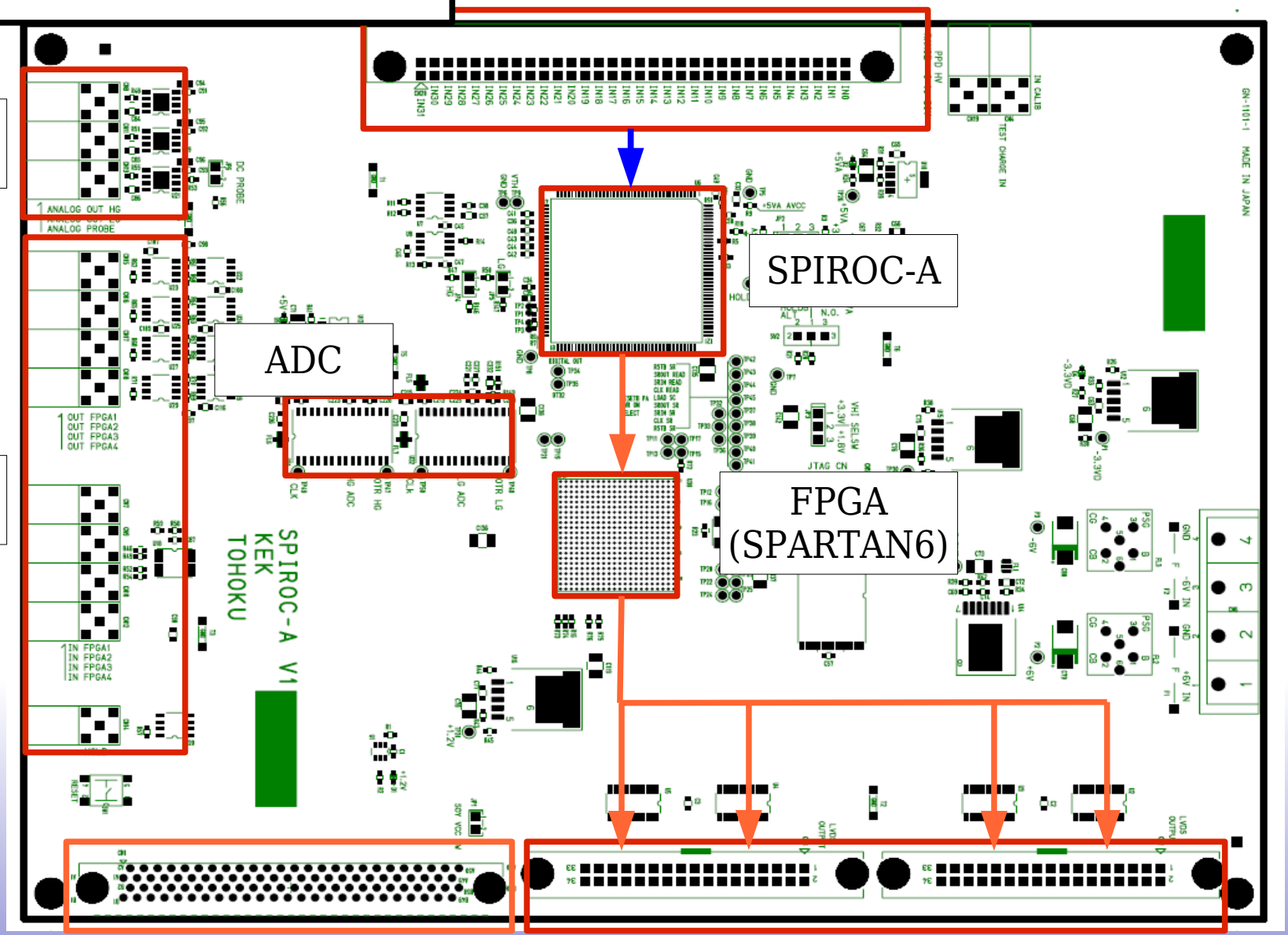

Layout of PCB

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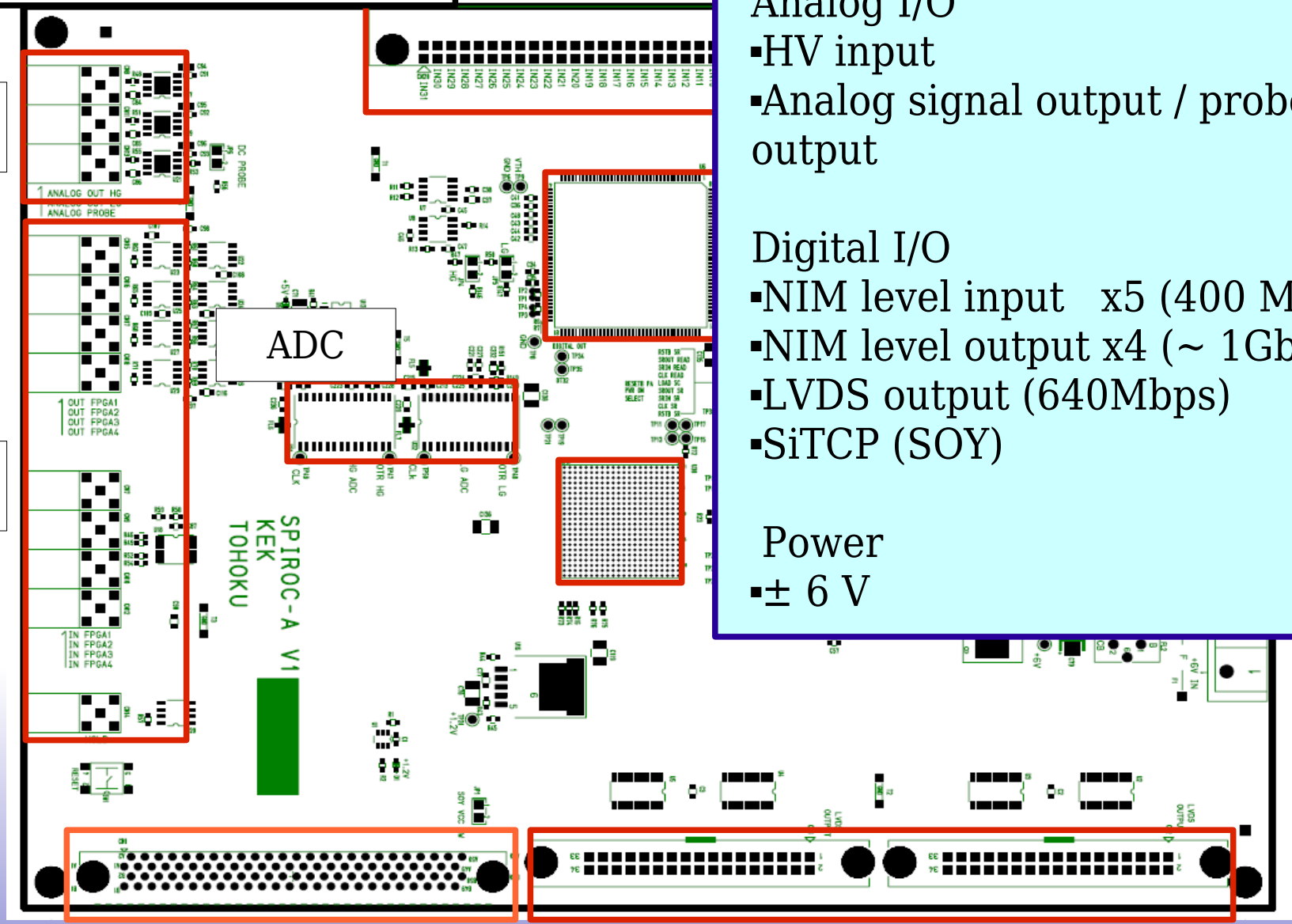


6 layers

Analog I/O
- HV input
- Analog signal output / probe output

Digital I/O
- NIM level input x5 (400 Mbps)
- NIM level output x4 (~ 1Gbps)
- LVDS output (640Mbps)
- SiTCP (SOY)

Power
- ± 6 V

Summary

- Development for multi-channels MPPC readout electronics with SPIROC and SiTCP.
- FPGA firmware to control ASIC and readout ADC
  - Improvement of firmware is necessary to achieve requested performance.
- New readout electronics is developed in Open-It.
  - Started PCB making. Debug will be started from March.

失敗談など

失敗談など

失敗談

- 回路図を描いている段階で十分な時間が取れなかった。
- 最終版の回路図でないものを GND さんに送ってしまった。
- レイアウトをしてもらっている段階で、あちらこちらから指示を出すような状況になった。
- SPIROC の入力用コンデンサの静電容量が小さい気がしてきた。
- 知識不足
  - SiTCP 、電気回路、IC の種類、配線パターンの見方等々

要望等

- 可能ならば他のプロジェクトの回路図や FPGA ロジック回路を見てみたい。

Backup

TOHOKU
UNIVERSITY

Introduction of SPIROC

What's SPIROC ?

=> **S**ilicon **P**M **I**ntegrated **R**ead **O**ut **C**hip
developed by Omega in LAL in France.

For ILC project

SPIROC2 (Original version)

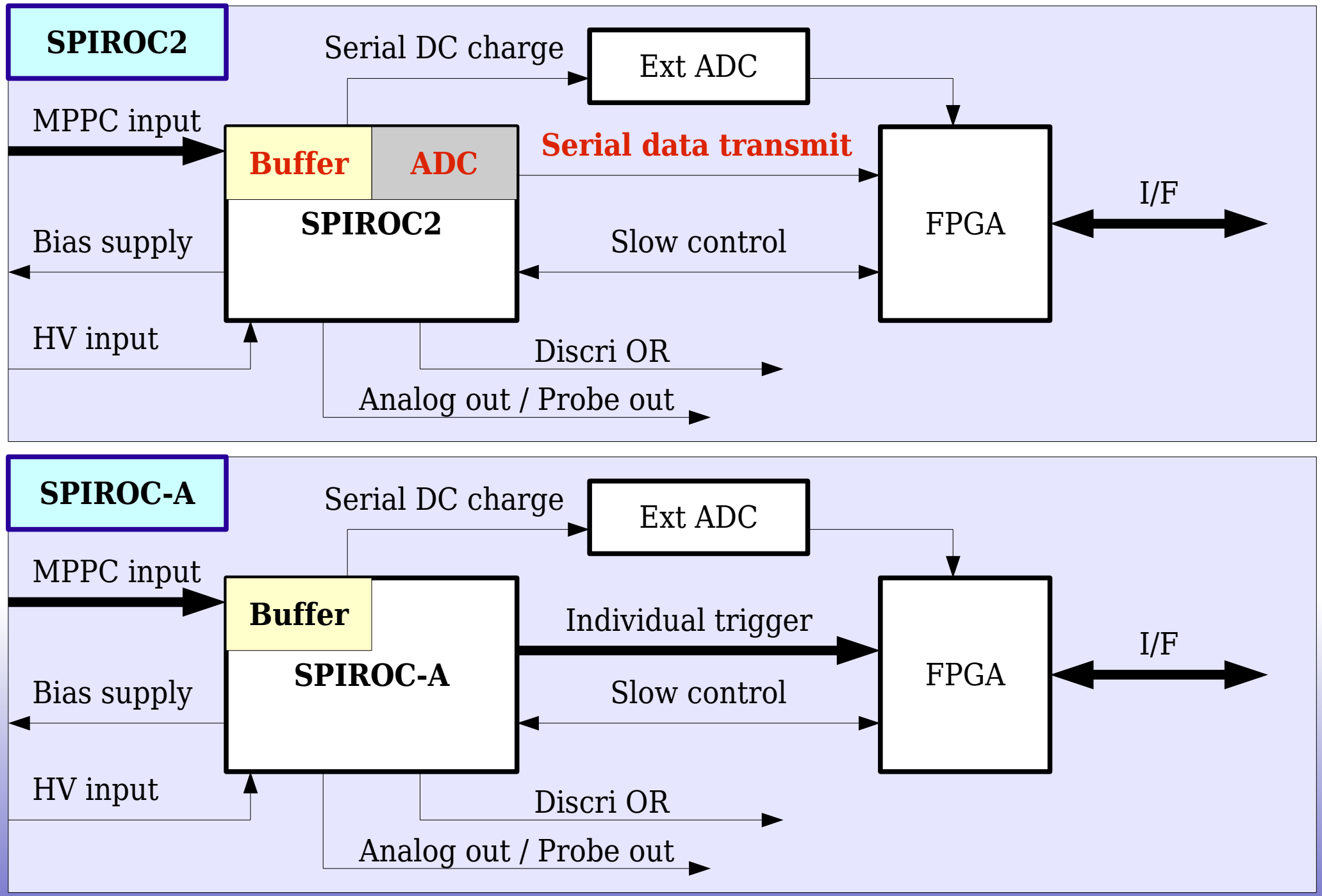
- Analog + Digital
- 36 input
- HV adjustment (4.5V 8bit)
- AMP, Shaper, Discriminator
- Analog buffer (SCA) 16 depth
- AD converter (each channel)
- Event builder
- SRAM => Serial data transmit
- Slow control

For balloon exp.

SPIROC-A (Derivative version)

- Analog only
- **32 input**
- HV adjustment (4.5V or 2.5 V 8bit)
- AMP, Shaper, Discriminator
- Analog buffer **1** depth
- **No AD converter**
- **Individual trigger output**
- Slow control

Introduction of SPIROC



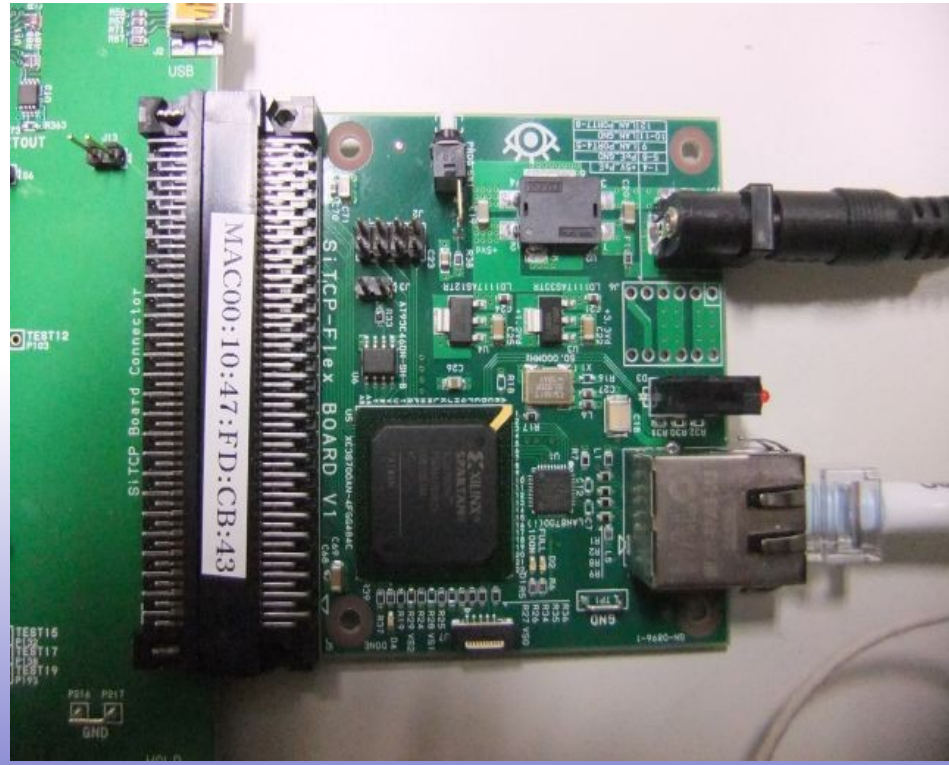
Development of Electronics

What's SiTCP ?

=> TCP/IP which is implemented with hardware (without software)

SOY is a product of Bee beans technology.
We can use SiTCP easily by using SOY.

Protocol type	: TCP and UDP
Band width	: Up to 100Mbps
Low frequency clock	: 25 MHz



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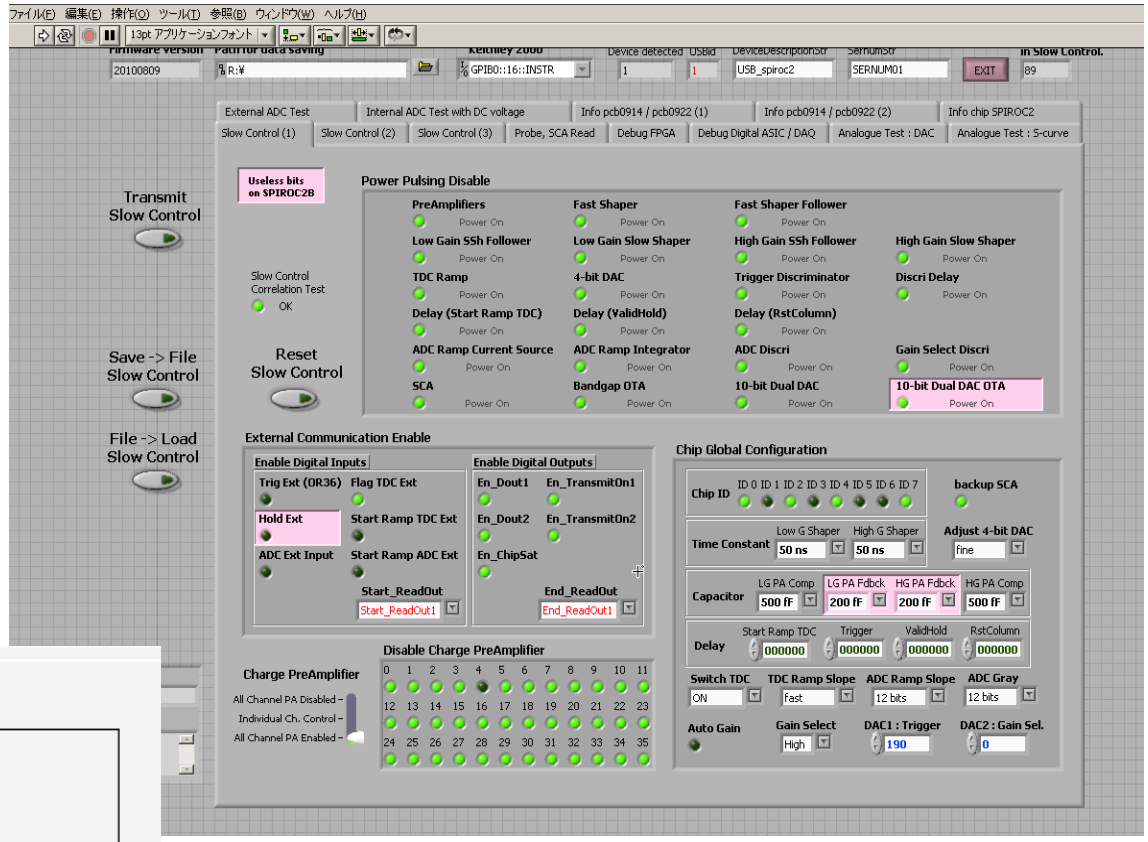
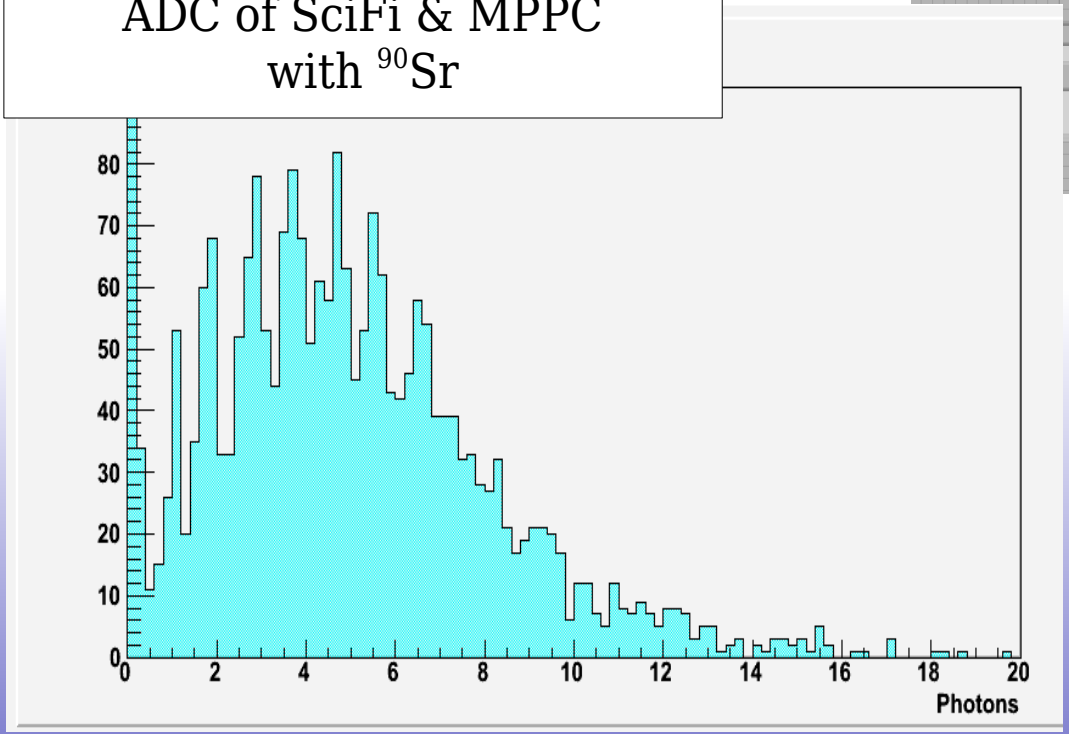


ADC of SciFi & MPPC with ^{90}Sr

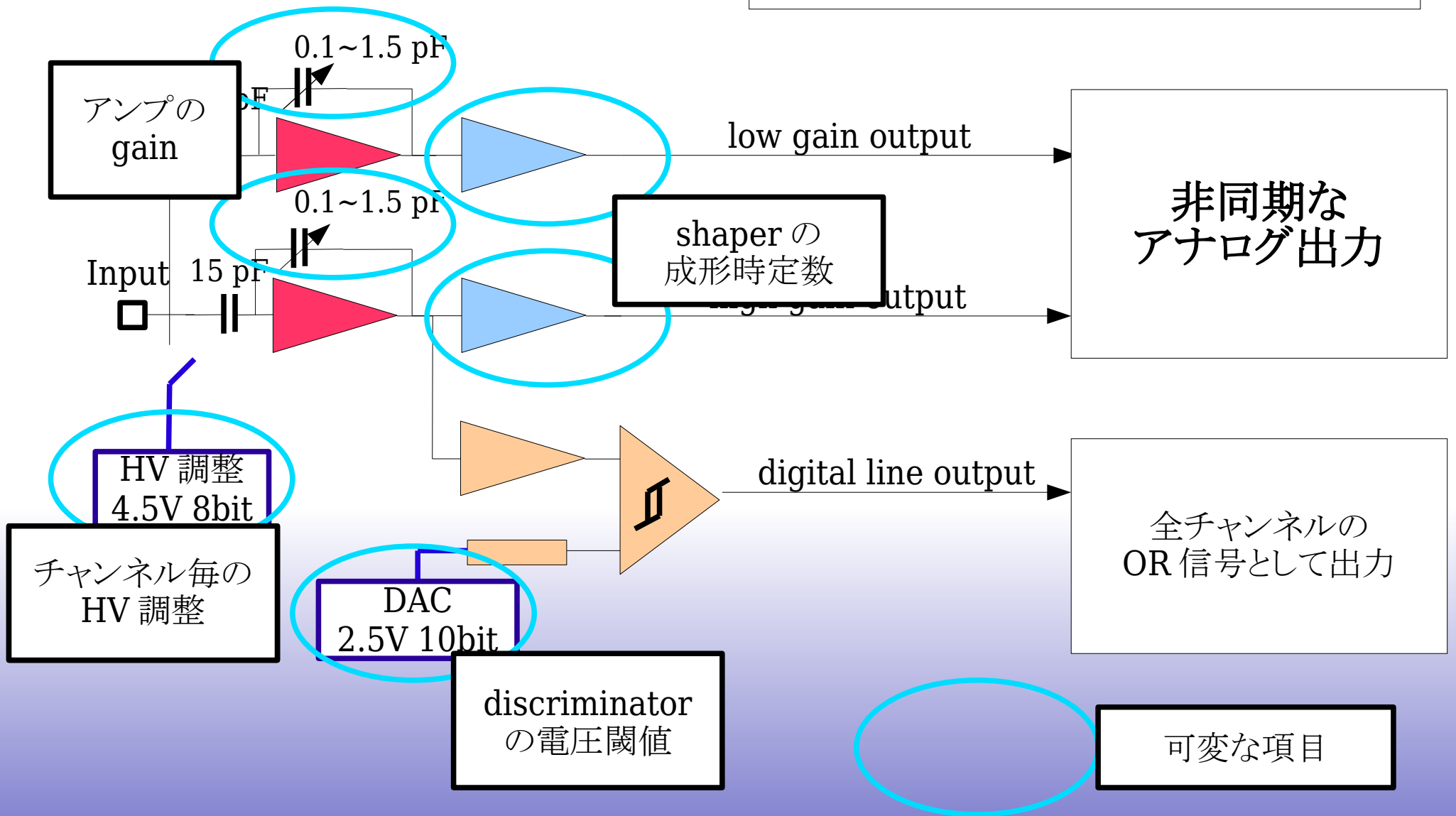


ADC spectrum of ^{90}Sr
SciFi (1mm x 1mm) & MPPC (11-50C)

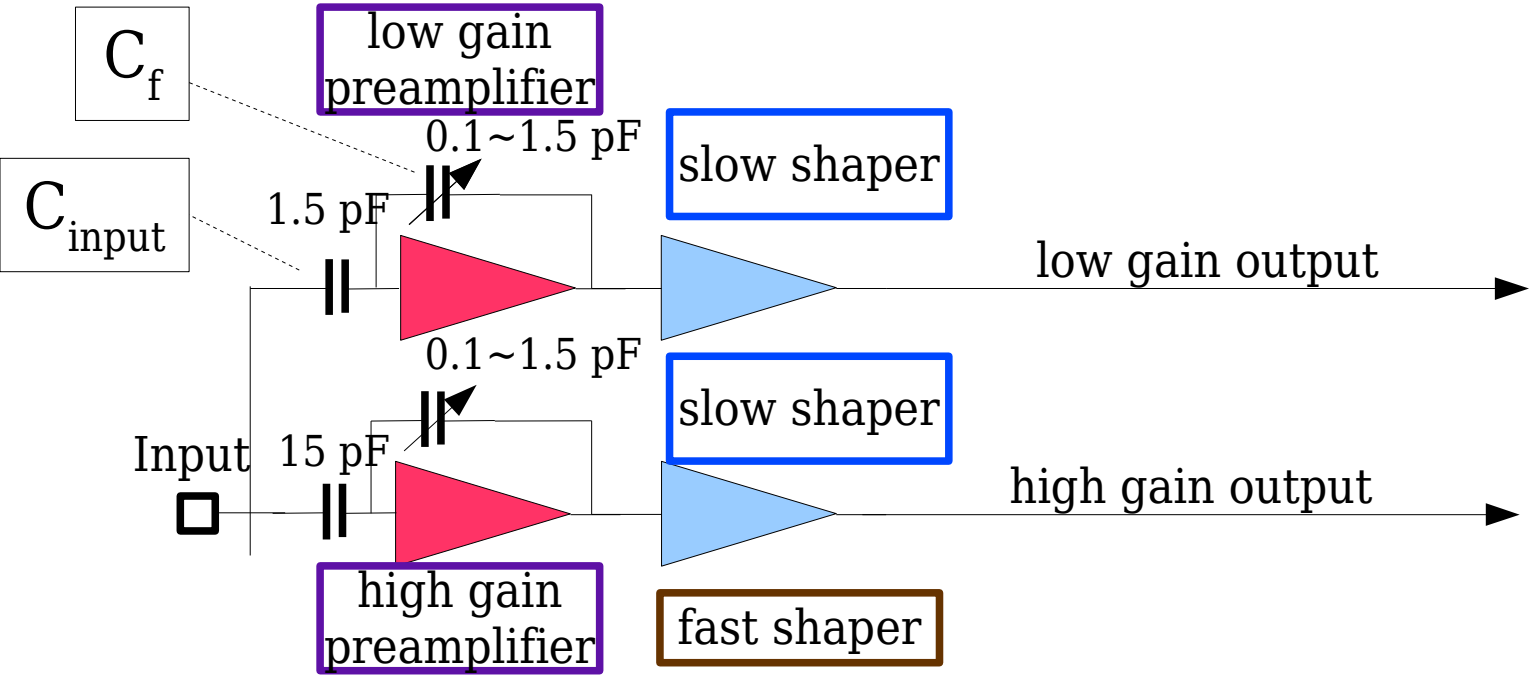
フロントエンド ASIC SPIROC

SPIROC チップのアナログ部分

ダイナミックレンジ 160 fC ~ 320 pC
(gain of MPPC : 10^6)



フロントエンド ASIC SPIROC



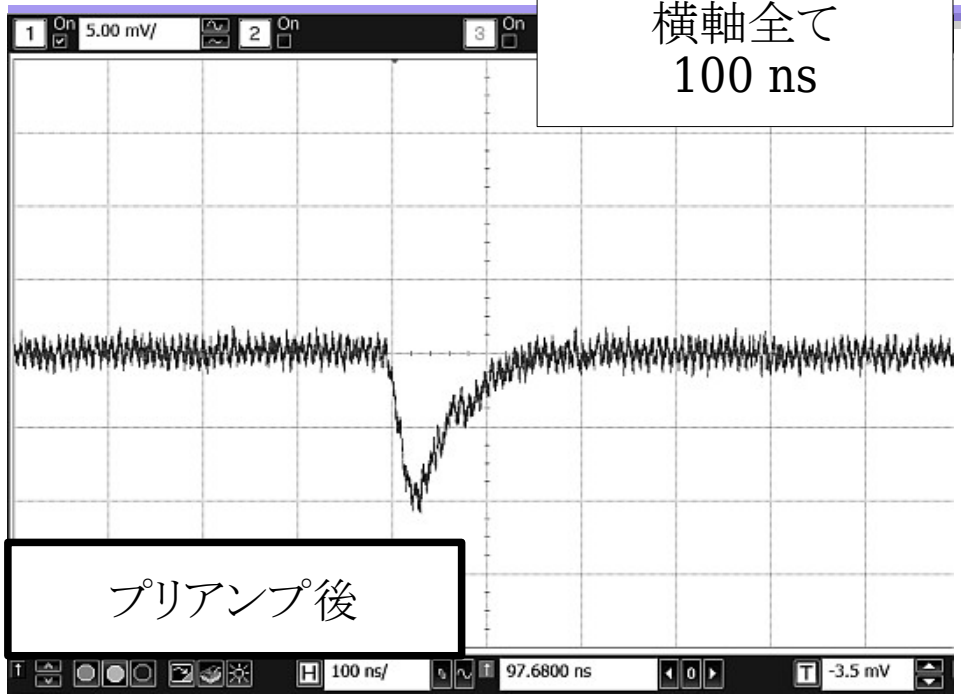
プリアンプの gain は以下の式に従う

$$\frac{V_{input}}{V_{out}} = \frac{C_f}{C_{input}}$$

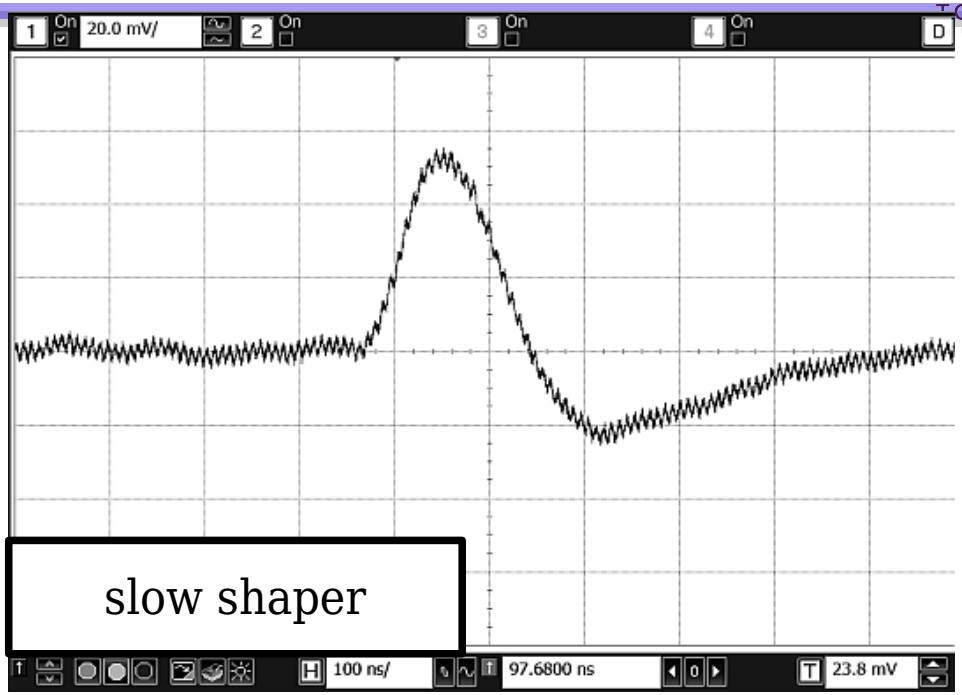
Hign gain 10 – 100 倍
Low gain 1 - 10 倍

最終 (slow shaper 後) gain　　: 11 mV/1 p.e(160 fC)

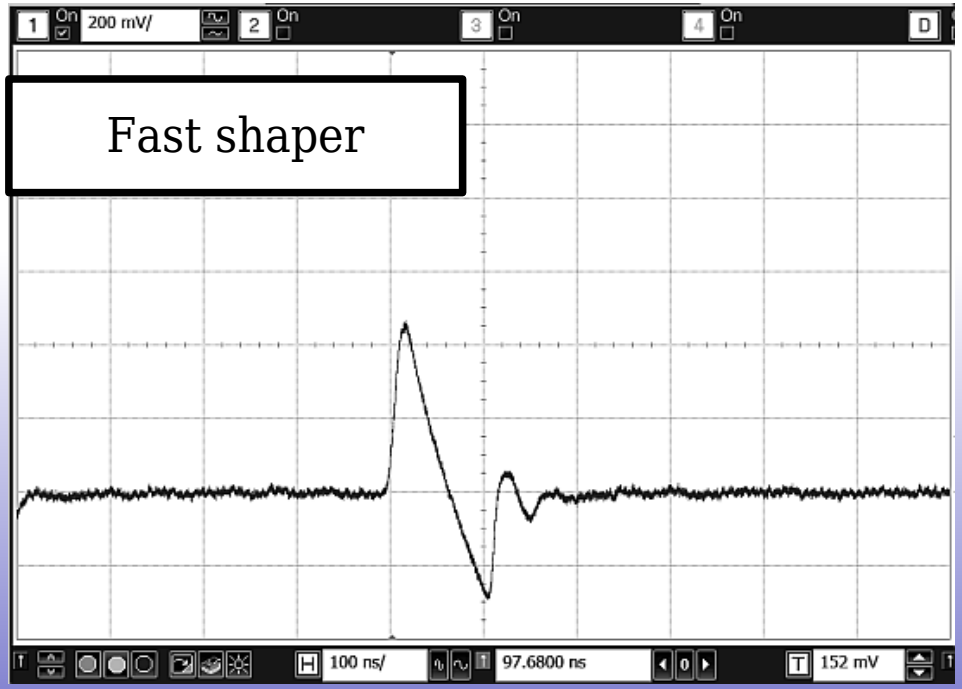
横軸全て
100 ns



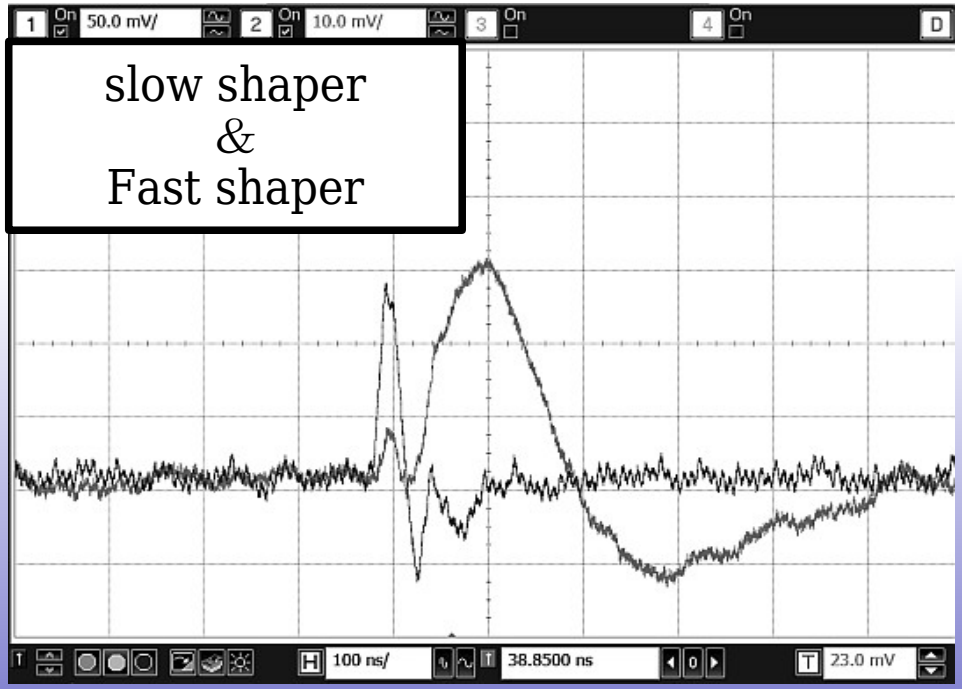
プリアンプ後



slow shaper

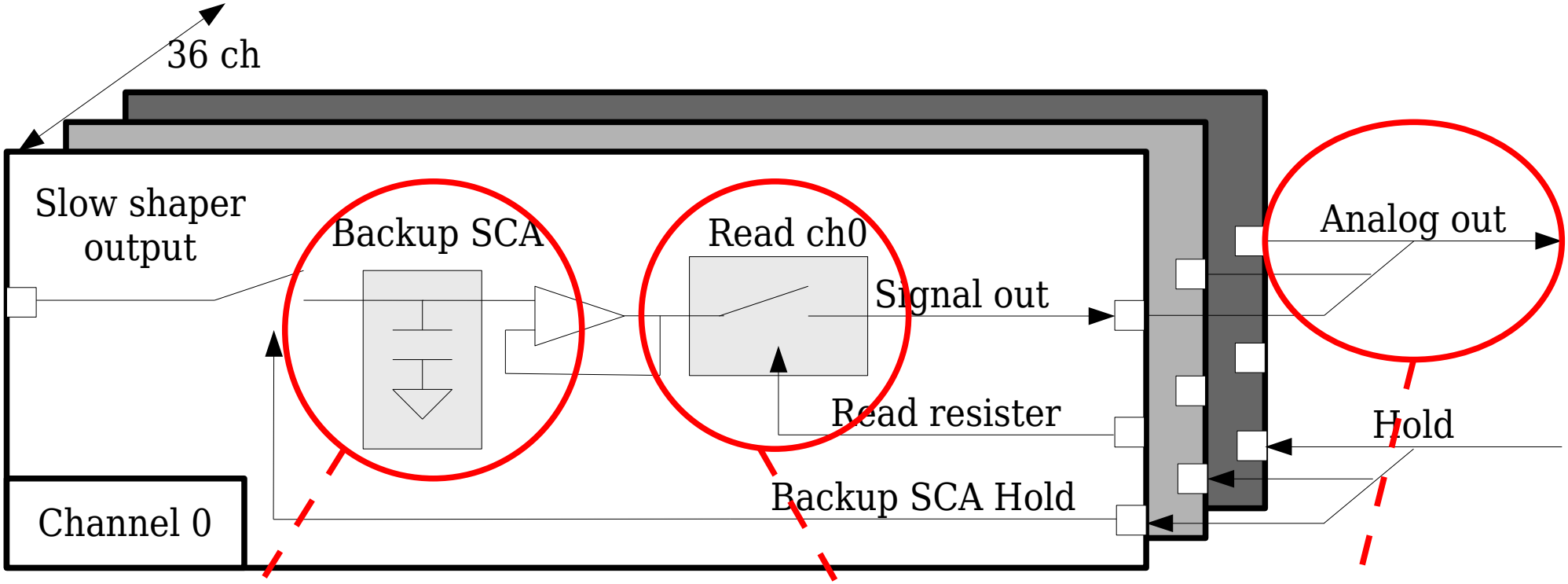


Fast shaper



slow shaper
&
Fast shaper

読み出しエレキ 読み出し方法



アナログ波形の波高情報を
電圧としてコンデンサに保存

どのチャンネルの電圧を
出力するか選択する

一つの ADC で順番に
全てのチャンネルの電圧を
A/D 変換する