Silizium Labor Bonn

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高集積化フロントエンドのトレンド

~CMOSピクセル・放射線耐性~

University of Bonn

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Outline

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✓ Introduction (自己紹介)

✓ ハイブリッドピクセル検出器 (HEP Tracker)

- Pixels@LHC

✓ (セミ) モノリシックピクセル検出器

- DEPFET
- Depleted MAPS

✓ テクノロジーのトレンド

- Smaller feature-size (TSMC 65 nm CMOS)

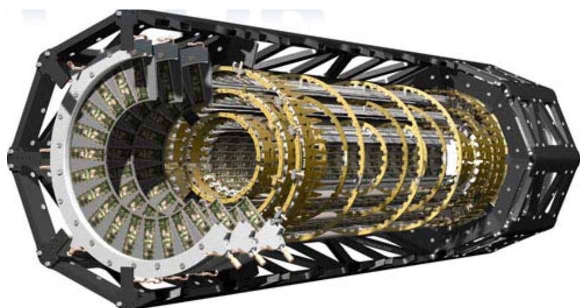
etc…

nn大学における研究状況

Group Prof. Norbert Wermes

高エネルギー実験用のfront-end ASIC及び
ピクセル検出器の開発で中心的な役割

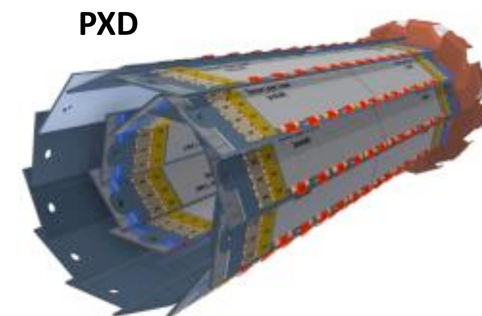
ATLAS



- FE-I3, FE-I4 chip design
- Hybrid pixel detector, bump
- IBL module production
- Diamond detector
- 3D sensor, TSV technology

Belle II

- DHP chip design
- PXD module testing
- DEPFET sensor testing



Borrowed from home page

ASIC design

Our group is developing full custom chips since 1994. Up to now, more than 40 designs have been submitted and successfully tested. They vary from simple transistor test structures to full readout chips for silicon strip and pixel detectors. At the moment, we are working on 8 workstations with the CADENCE software using different CMOS technologies. Further down this page lists the designs starting with the most recent submissions.

アナログfront-endデザインを中心となって進めている

ハイブリッドピクセル検出器

+ good S/N←fully depleted
+ fast R/O→~ns time stamp
- radiation length→ 3.5% x/X0
- spatial resolution→~10 µm
- bump bonding

LHCにおけるピクセル検出器の現状

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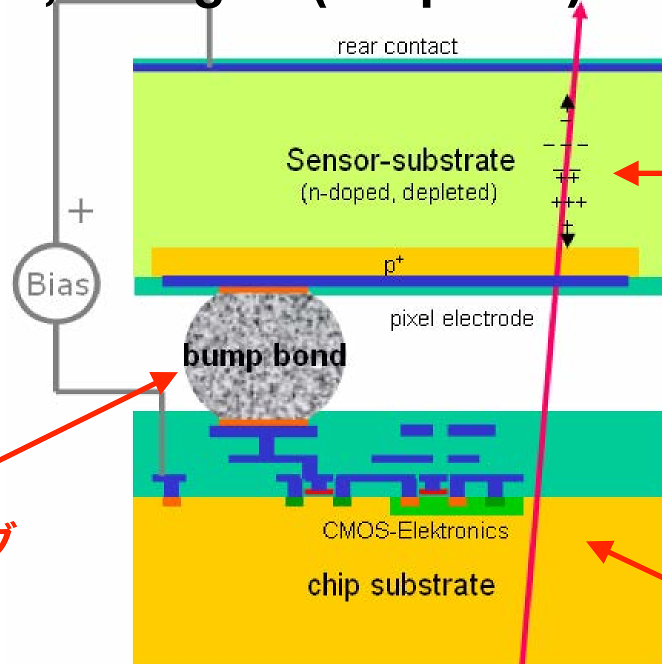
ハイブリッドピクセル検出器 (state of the art)

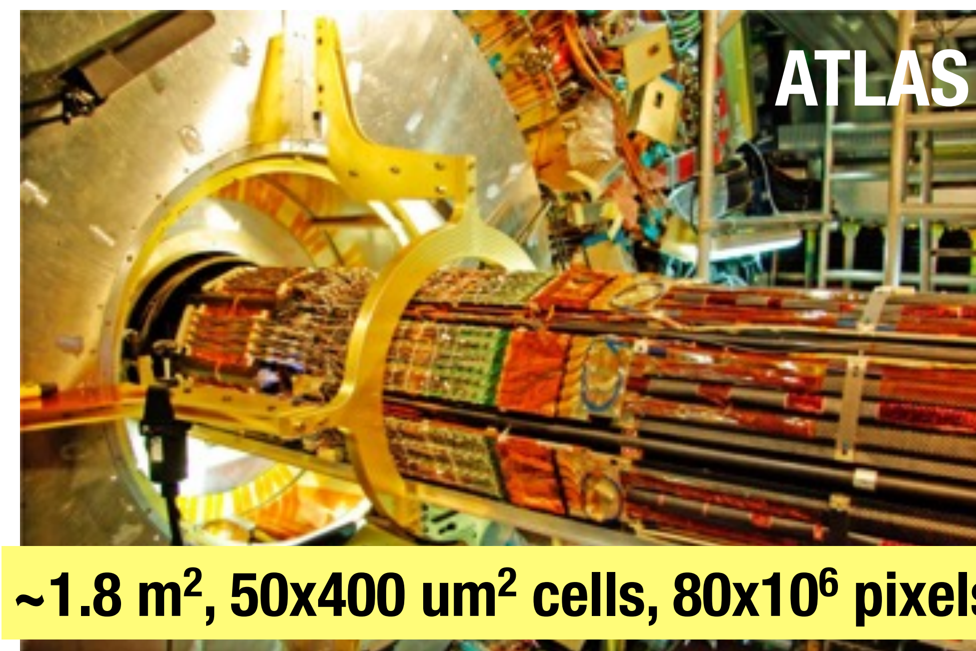
sensorとASICは別プロセス
first use in 1992, OmegaD (10^3 pixels)



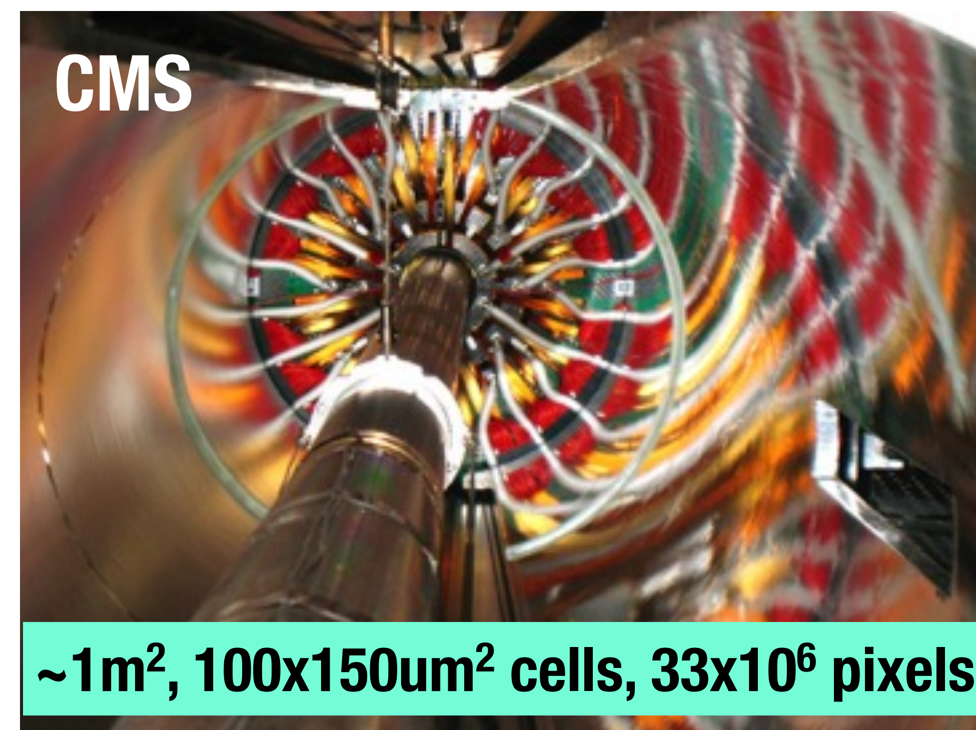
シリコンピクセル検出器

フリップチップ
バンプボンディング

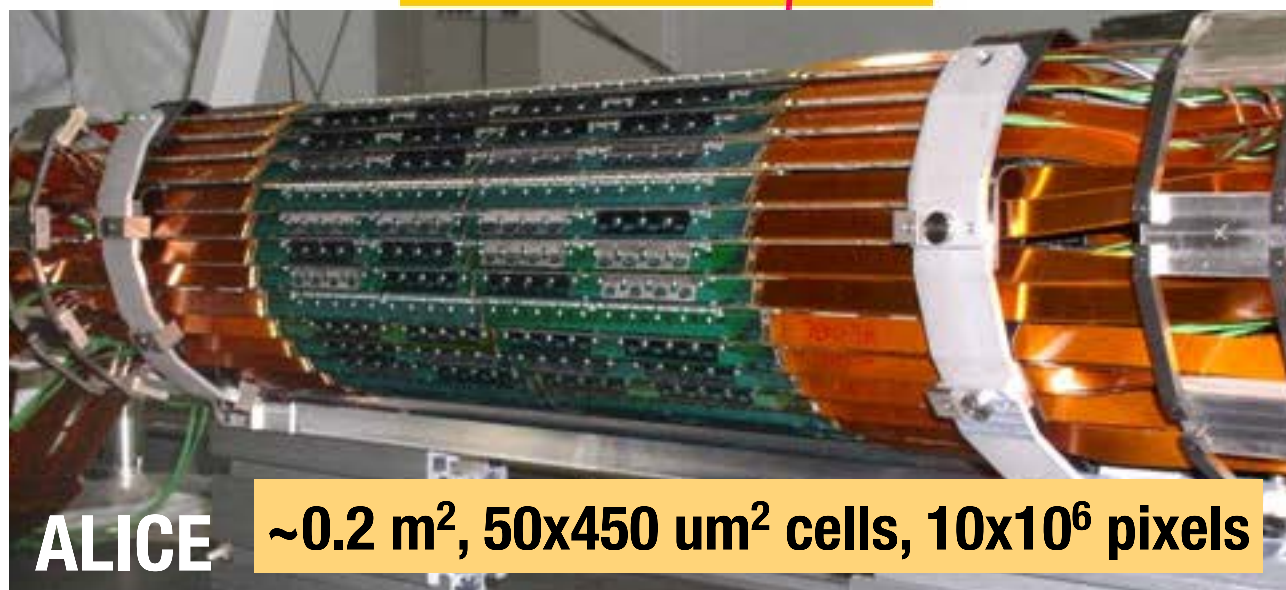
フロントエンドASIC



~1.8 m^2, 50x400 um^2 cells, 80x10^6 pixels



~1m^2, 100x150um^2 cells, 33x10^6 pixels



~0.2 m^2, 50x450 um^2 cells, 10x10^6 pixels

全実験でInnermost layerにハイブリッドピクセルを使用

ATLASシリコンピクセル検出器

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ATLAS Pixel Module

HV hole
HV guard ring
Type0 connector
MCC
barrel pigtail
decoupling capacitors
flex
NTC
sensor
FEs
NTC
flex
MCC
barrel pigtail
glue
TMT
sensor
FEs
bump bonds
dimensions: ~ 2 x 6.3 cm²
weight: ~ 2.2 g

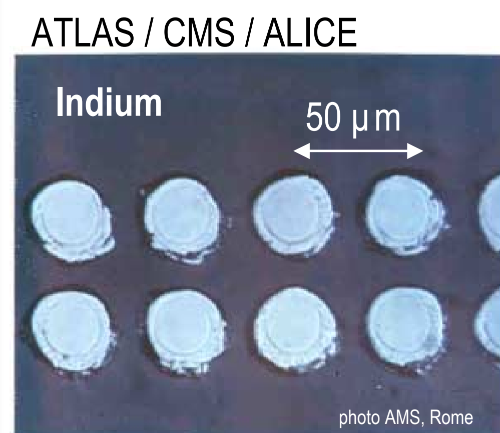
Siセンサー

- ✓50 × 400 um^2, 250 um thickness
- ✓n+ pixel on n- material
- ✓rad-hard ($10^{15} n_{eq}$, 80 Mrad)
- ✓p- after irrad. (can be operated partially depleted)

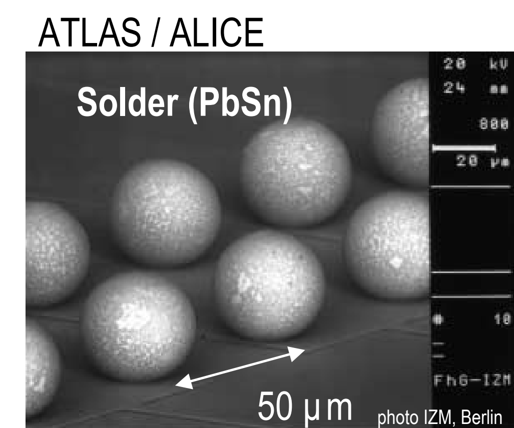
ハイブリッドプロセス

- ✓PbSn or In bumping (wafer scale)
- ✓IC wafers thinned after bumping to ~180 um

ATLAS / CMS / ALICE



ATLAS / ALICE



ハイブリッドピクセルの読み出し原理

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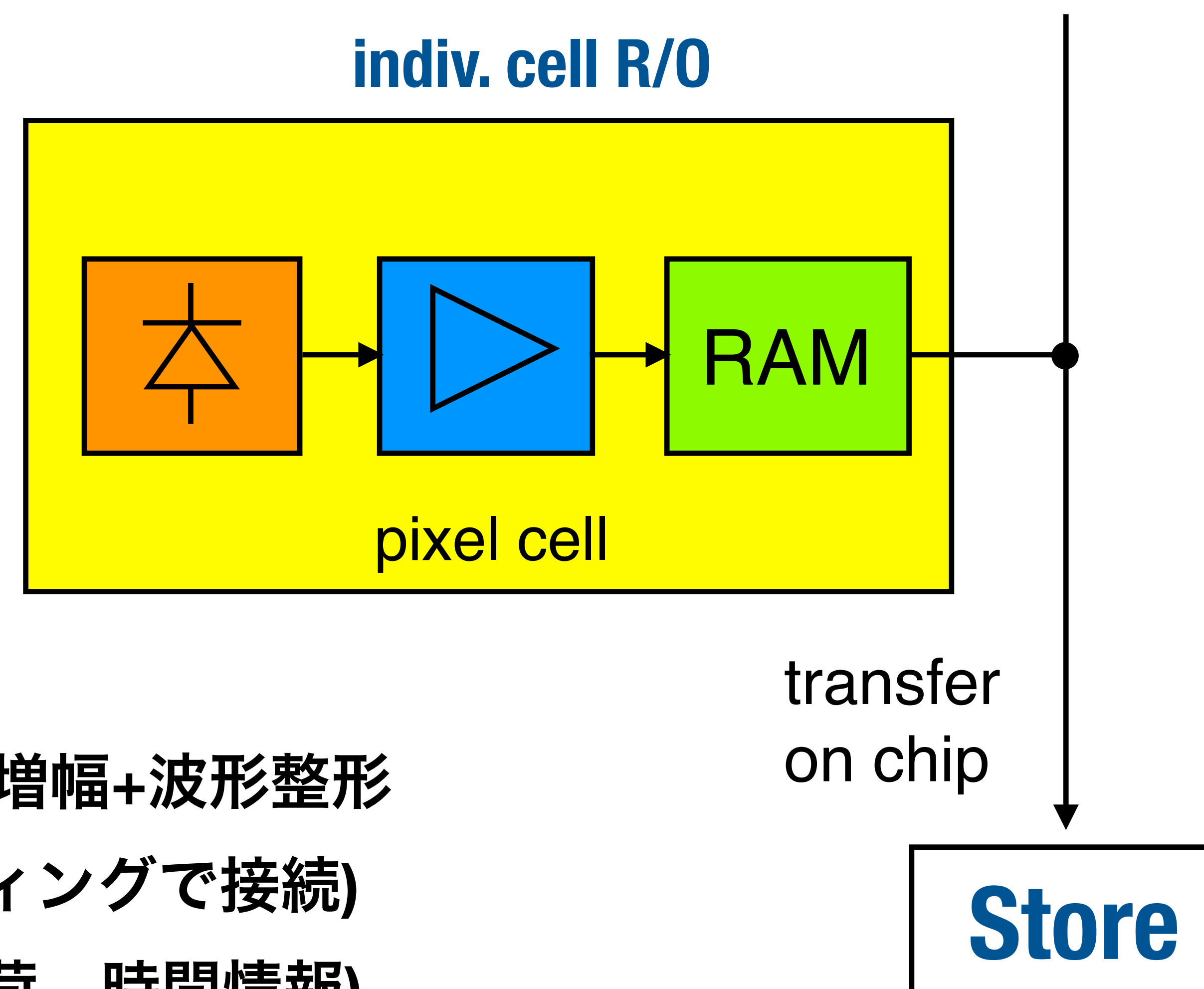
センサーで電荷生成→フロントエンドASICで信号処理

各BX time間のヒット信号を保持 (dig./ana.)
トリガー同期のヒットピクセル読み出し



- アドレス
- 電荷 (ToT)
- 時間情報

✓PNダイオード→Q_{signal}
✓センサーに最適化したFront-end ASICで信号増幅+波形整形
(ピクセル電極と読み出し回路をバンプボンディングで接続)
✓各ピクセルのヒット情報を保持(アドレス、電荷、時間情報)
✓End of Columnロジック(トリガー待機)
✓カラム読み出し

ATLASフロントエンドASIC: FE-I3

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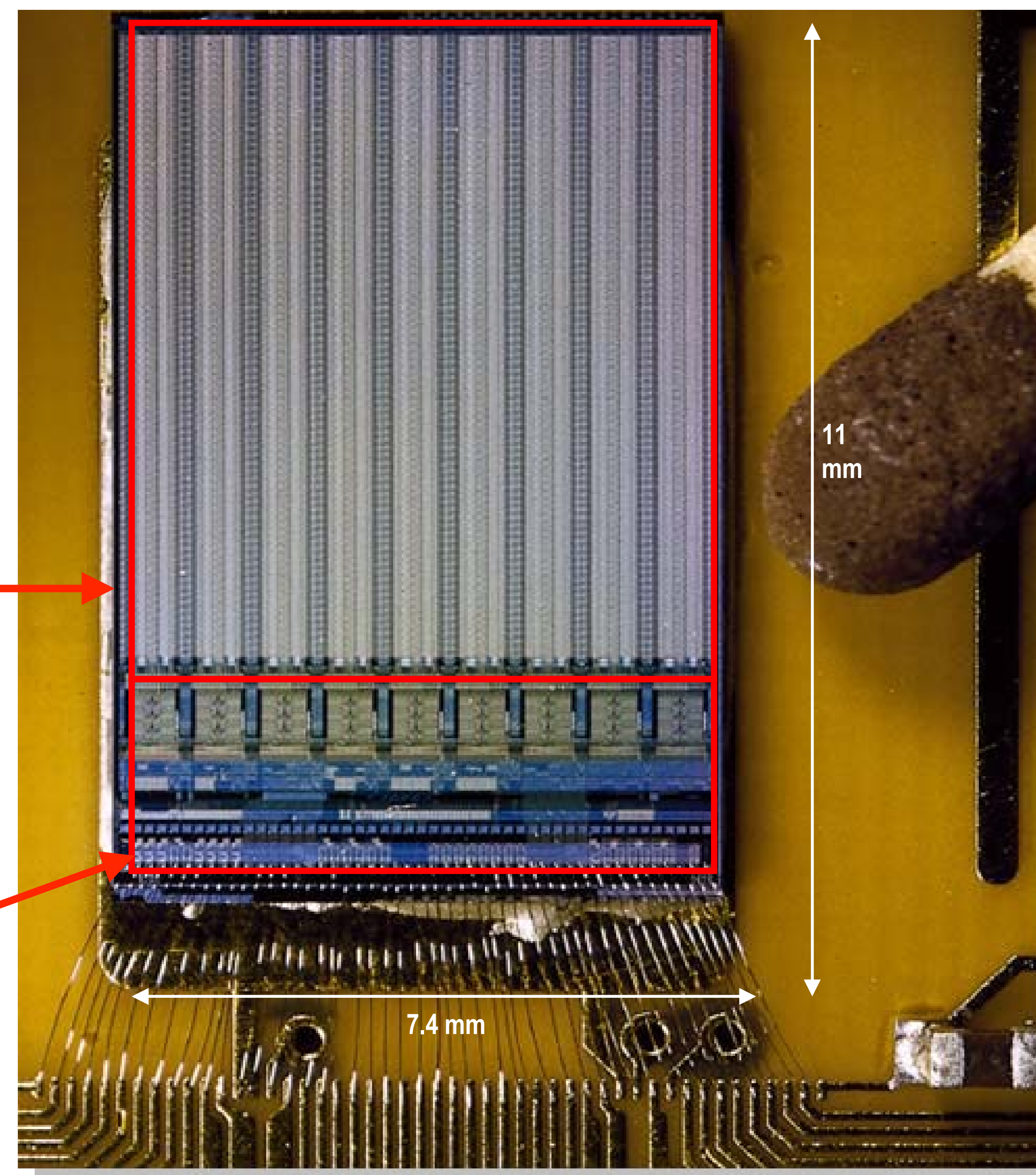
複数のプロセスで試作(DMILL, BiCMOS)

- ✓0.25 μm CMOSプロセス
- ✓80 Mrad, 10^{15} n_{eq}/cm^2

Pixel cell

- ✓ピクセルサイズ: 50×400 μm^2
- ✓18 column × 160 rows = 2880 cells
- ✓各ピクセルにCSA, zero-suppression
- ✓低消費電力: ~50 μW/pix
- ✓低雑音: ~250 e-
- ✓閾値のばらつき: ~70e- (after tuning)



End of columnロジック

- ✓40 MHz clockでタイムスタンプ
- ✓データバッファリング(2.5 μs trigger latency)
- ✓ヒットセレクション

IBL(Insertable B-Layer)

Innermost layerに4層目を追加(nearest BX layer)

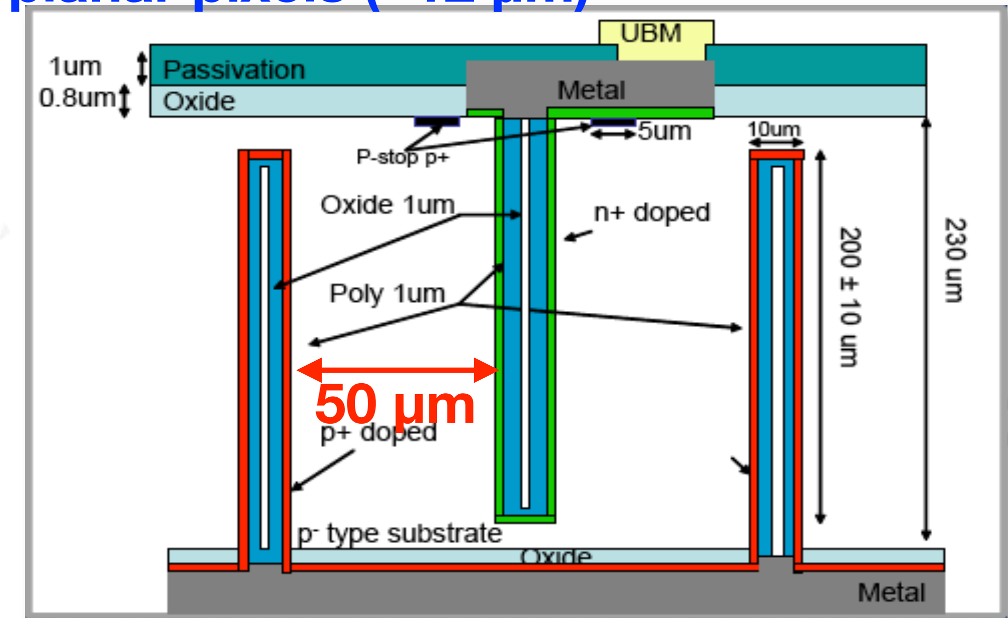
2種類のセンサーを採用

200µm from pixel to dicing strip
~200+250 µm inactive edge

Planar s	(n-in-n)	(n-in-p)
200 µm t		
inactive edg (minimize		
low Q gener → low thres		30V)
cheaper and		able for

500µm long pixels

$V_{depl.}$~10V, spatial resolution as for planar pixels (~12 µm)



Stanford, SINTEF(Oslo), IRST(Trieste), CNM(Barcelona)

フロントエ

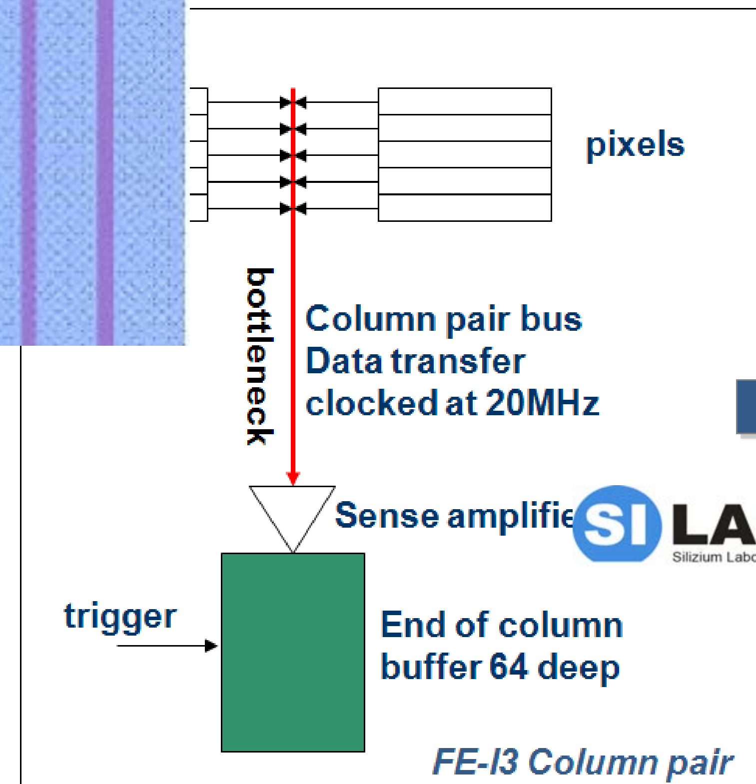
✓250 nm
✓ピクセル

→50×250 µm²

✓データ ...60 Mb/s

✓ローカルバッファを採用

✓(Serial powering)



SI LAB
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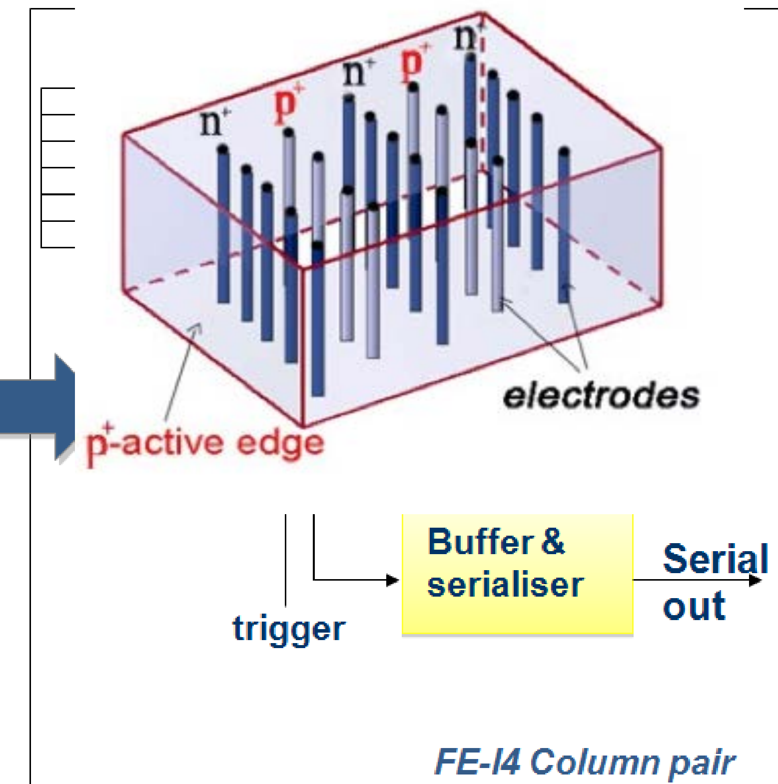

フロントエンドアーキテクチャ(ATLAS)

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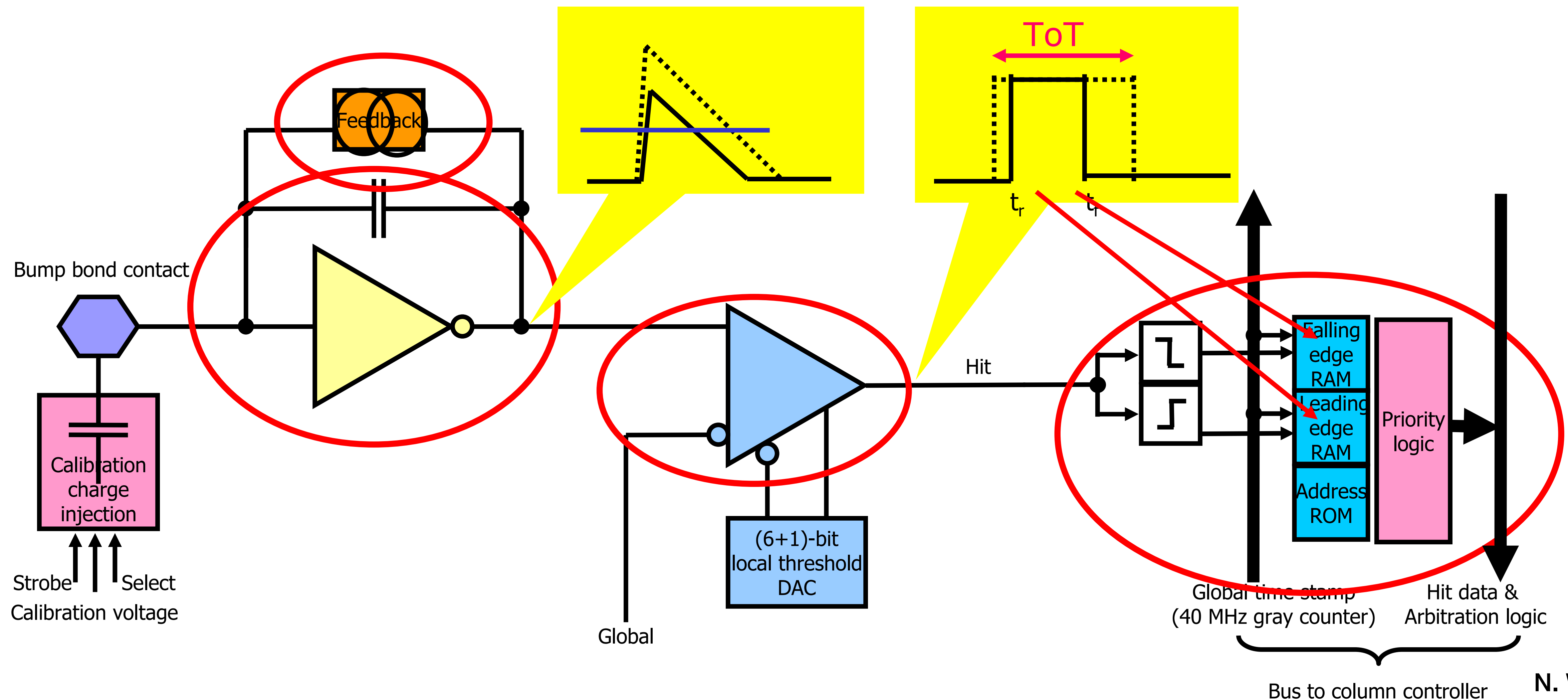
"ATLASはデジタル, CMSはアナログ"アーキテクチャ



✓Integration of signal charge by charge sensitive amplifier
✓Pulse shaping with constant current feedback
✓Hit detection by comparator
✓~5 bit analog info. via "time over threshold" (small time walk with small Q)
✓storage of address and time stamps in RAM at the periphery

フロントエンドアーキテクチャ(CMS)

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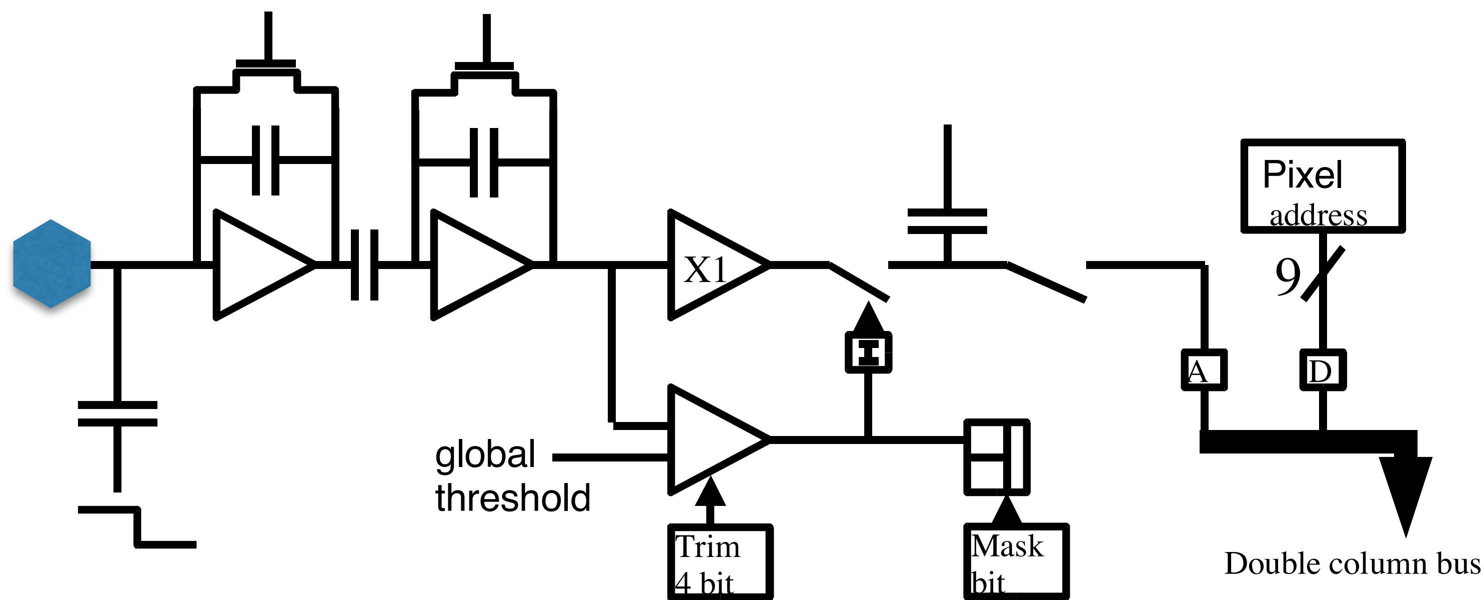
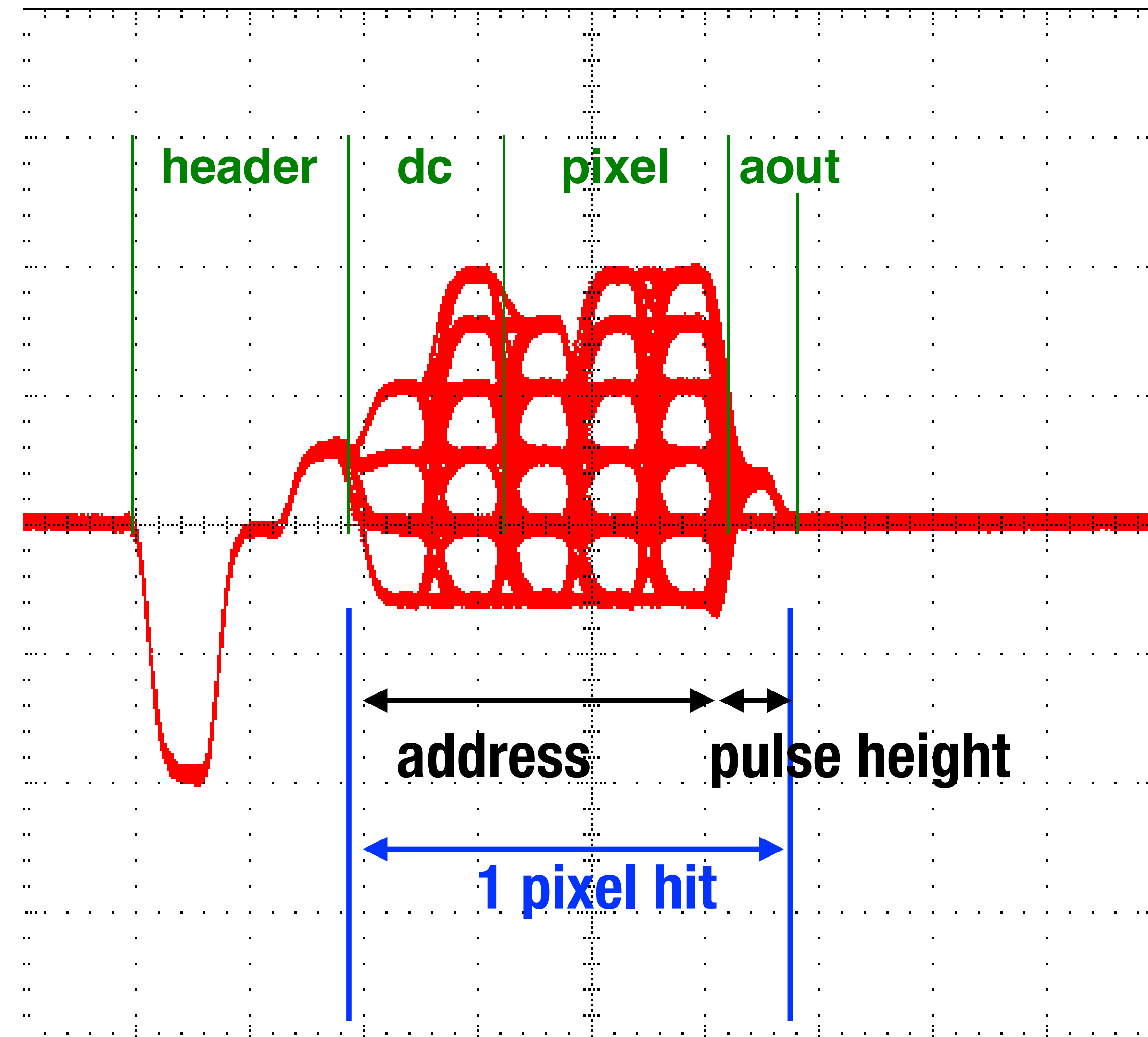
アナログブロック





- ✓0.25 µm CMOS
- ✓pixel size: 100 × 150 µm^2
- ✓CSA, Shaper, Sample/hold, comparator
- ✓251 fets per pix
- ✓52 × 80 = 4160 pixels

- ✓5 clock cycleで11ビットのアドレス情報をエンコード(6 levels)
- ✓1 clock cycleでアナログ波高値

放射線によるピクセル検出器への影響

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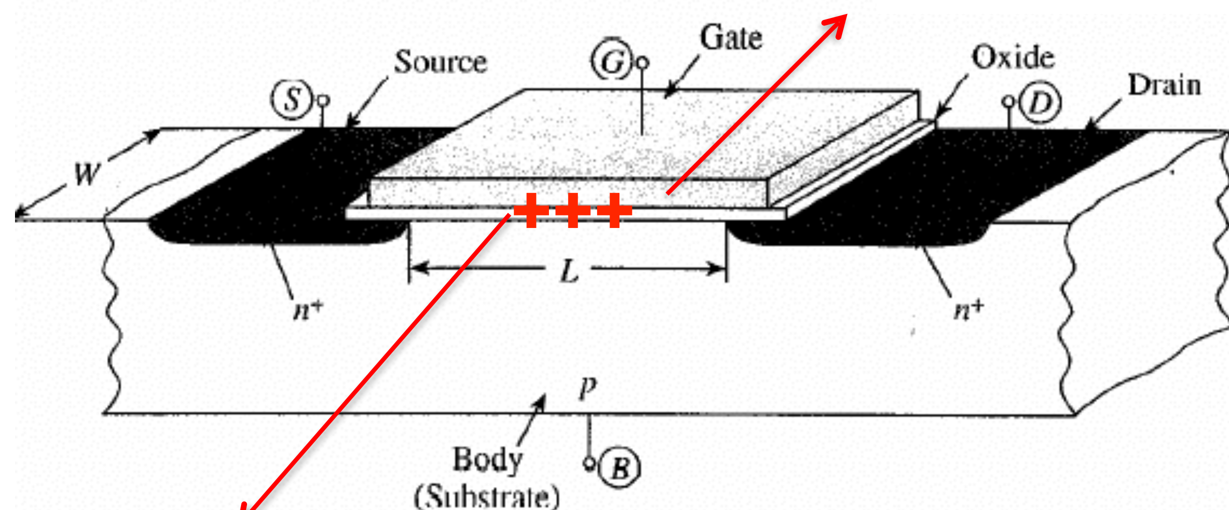
FEへの影響

✓ゲート酸化膜への電荷蓄積



✓界面トラップ (Si-SiO2)

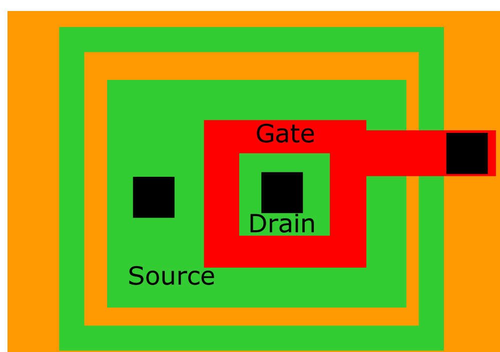
✓STI

トランジスタのV_{th} shift (good in DSM,

d_{ox}<10 nm but larger gate leak),

leakage current→ELT

SEU (ビット反転)→DICE SRAM



センサーへの影響

バルクダメージ(NIEL)

✓change of doping concentration

→"type inversion"

✓leakage current →noise, power

✓チャージトラップ →signal

サーフィスダメージ(IEL)

✓界面トラップ, SiO2への電荷蓄積

→breakdown behavior

- Material Engineering-New Materials (work concluded)
  - Silicon Carbide (SiC), Gallium Nitride (GaN)

diamond

- Device Engineering (New Detector Designs)
  - p-type silicon detectors (n-in-p)
  - thin detectors
  - 3D detectors
  - Simulation of highly irradiated detectors
  - Semi 3D detectors and Stripixels

Pixels@HL-LHC

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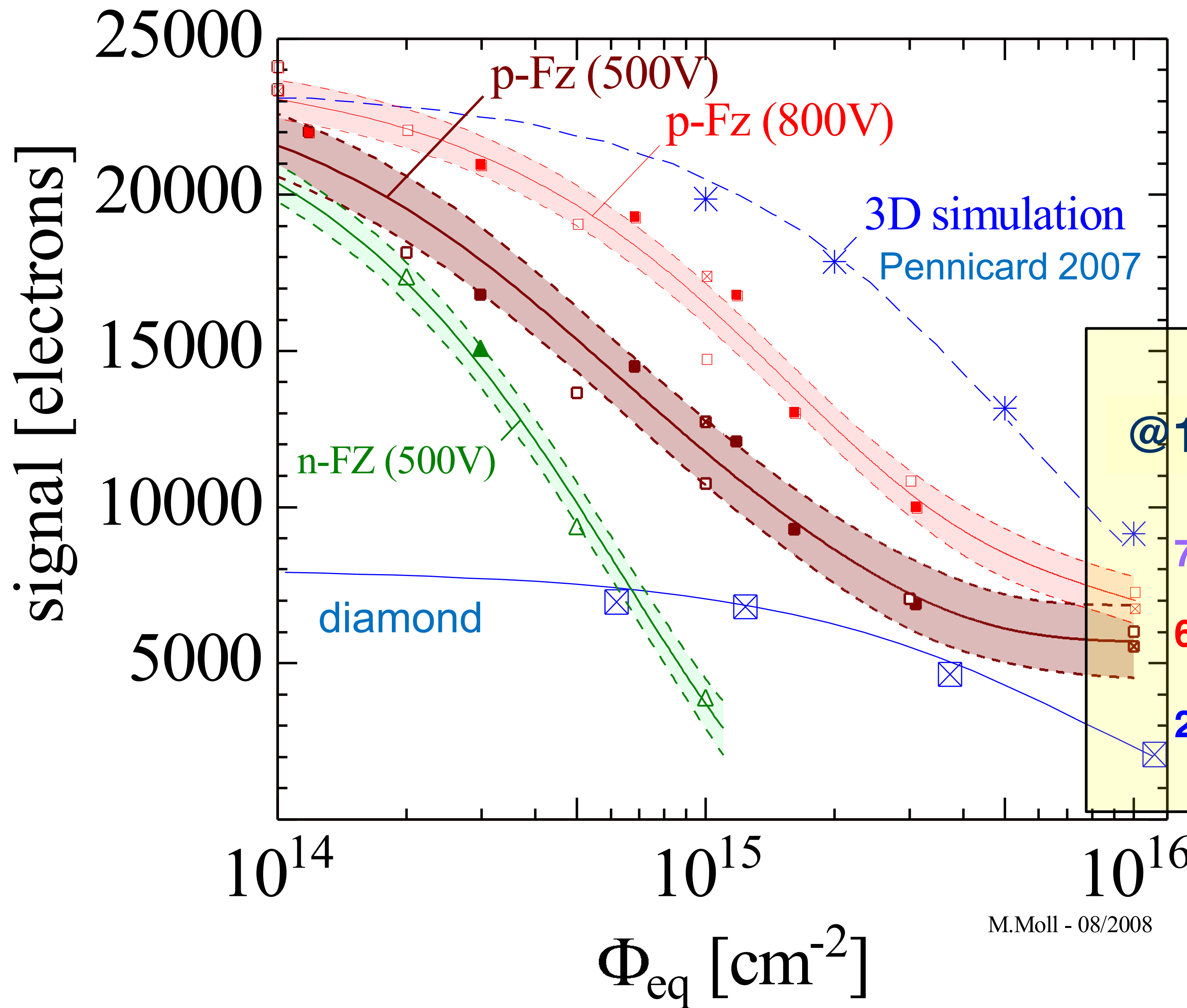
trend: n+ on n → n+ on p (FZ or MCZ)



FZ Silicon Strip Sensors

Data from Gianluigi Casse et al. (Liverpool) presented on VERTEX 2008

- n-in-p (FZ), 300µm, 500V, 23GeV p
- n-in-p (FZ), 300µm, 500V, neutrons
- n-in-p (FZ), 300µm, 500V, 26MeV p
- n-in-p (FZ), 300µm, 800V, 23GeV p
- n-in-p (FZ), 300µm, 800V, neutrons
- n-in-p (FZ), 300µm, 800V, 26MeV p
- p-in-n (FZ), 300µm, 500V, 23GeV p
- p-in-n (FZ), 300µm, 500V, neutrons
- Double-sided 3D, 250 µm, simulation! [1]
- Diamond (pCVD), 500 µm [2] (RD42 data!)

3D Si simulation
p – FZ planar Si
diamond
↓
ATLAS DBM

N.Wermes

note: n_{eq} (Si) normalization (correct for diamond?) & diamond better in S/N terms

(セミ) モノリシックピクセル検出器

+ no bump bonding
+ very thin (50-75 μm)→~0.2% x/X0
+ small pixel size (20-50 μm)→~1μm resolution
+ low power→less cooling
- radiation hardness
- R/O speed

モノリシックピクセルの読み出し原理

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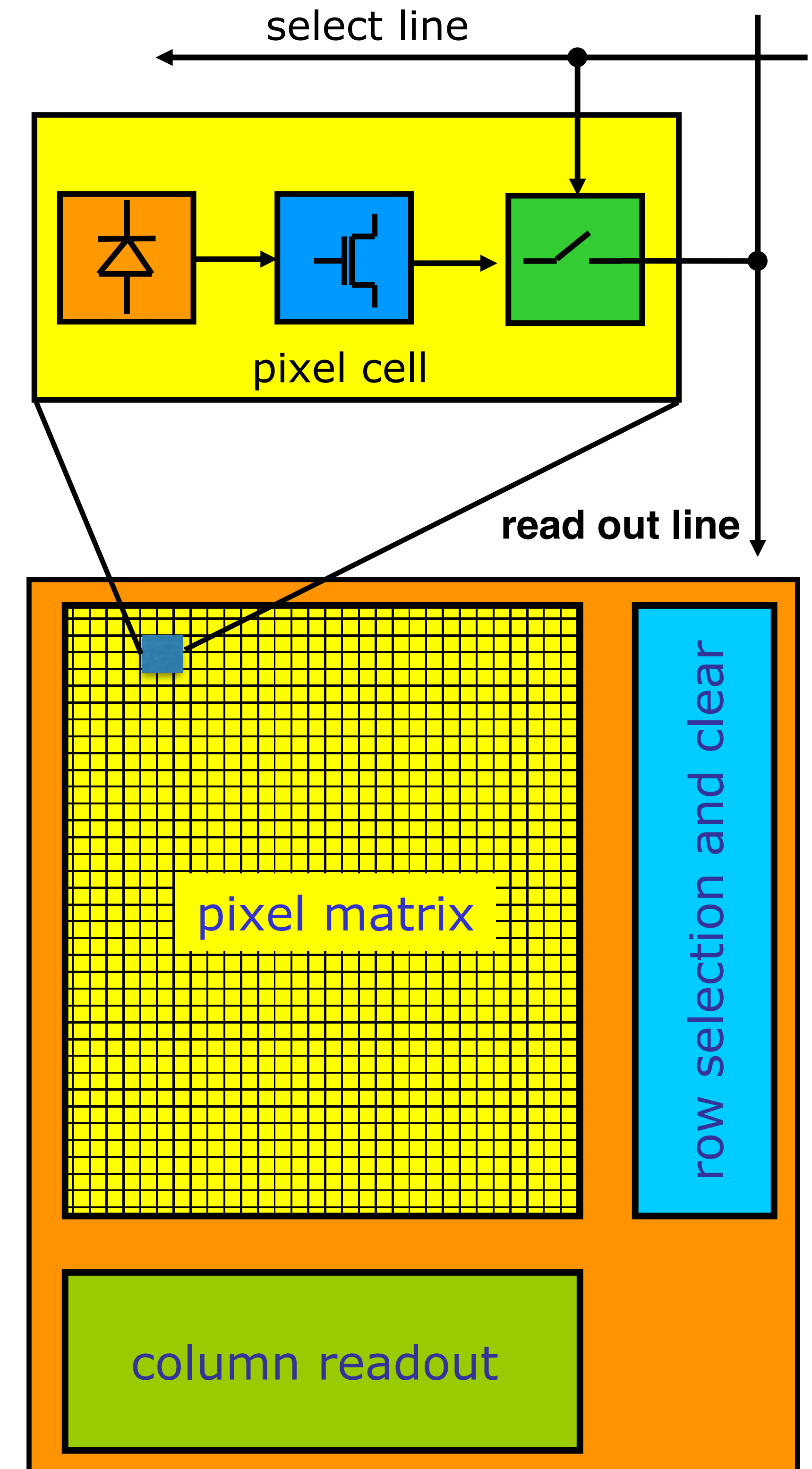
電荷生成と信号処理に共通のSi-sub.を用いる

- ✓PNダイオード→Q_{signal}
- ✓sense node (transistor gate)
- ✓rowセレクト(row-wise selection)
- ✓column読み出し(column-wise R/O)
- ✓select/resetスイッチ



CMOS active pixels (MAPS)

- ✓電荷収集と駆動+信号処理回路が同じ基盤上に配置

DEPFET pixels (セミモノリシック)

- ✓初段FETを完全空乏化したバルク上に配置
- ✓駆動+信号処理のASICはマトリックスの側面に配置

DEPFETピクセル検出器

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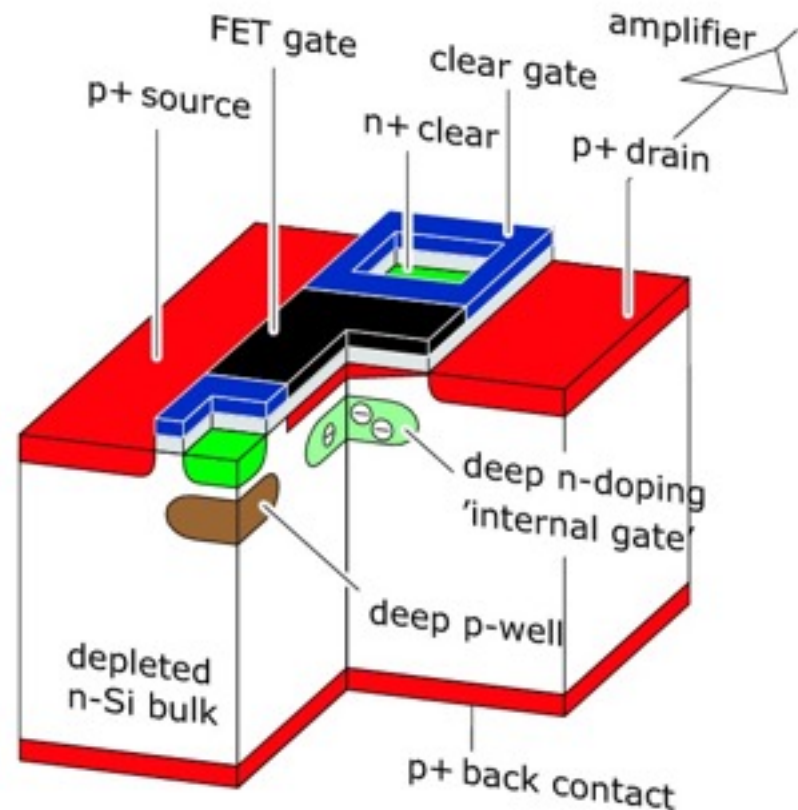

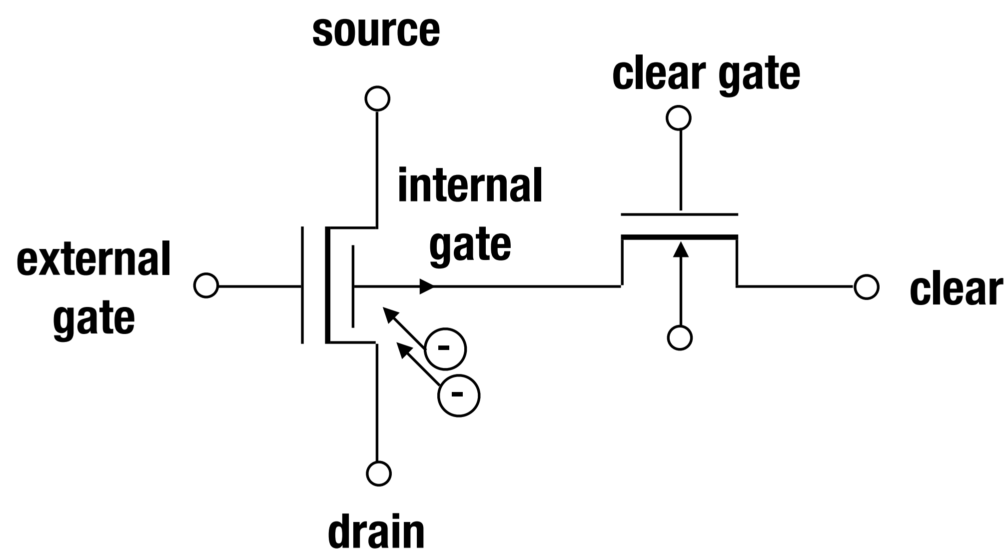

✓初段FETにPMOS (完全空乏化したバルク上に配置)

- ピクセルサイズ：小
- driftによる電荷収集(fast collection, large signal)

✓Internal gate (IG): n-implant, potential min. for e^-

✓IGに蓄積された電荷に応じてドレイン電流が変化

- low C_{det} + amp.→低雑音

✓蓄積電荷をパンチスルー効果によって除去

- 余分なresetが必要(non-commercial process)

✓FETは電荷収集時はOFF

- 低消費電力

✓電流信号をフロントエンドASICで処理

- マトリックス駆動用ASIC+信号処理ASIC (CDS)が必須

>10 yrs R&D　Collaboration: Aachen, Bonn, Heidelberg, MPI Munich, Karlsruhe, Plaque, Valencia

電圧読み出し vs. 電流読み出し

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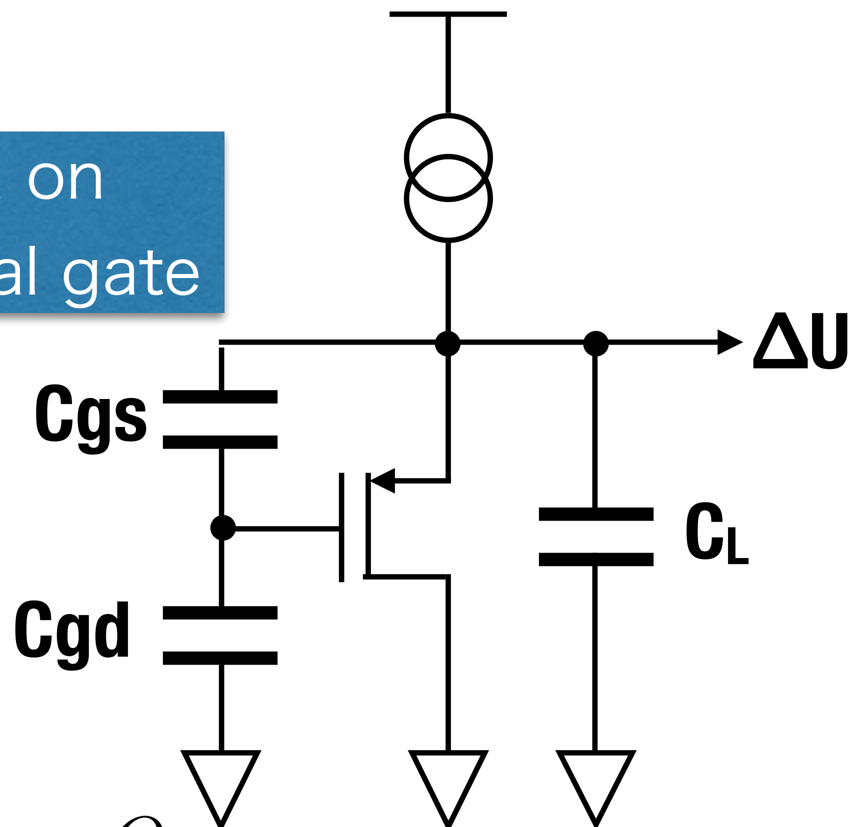
電圧読み出し(ソース)



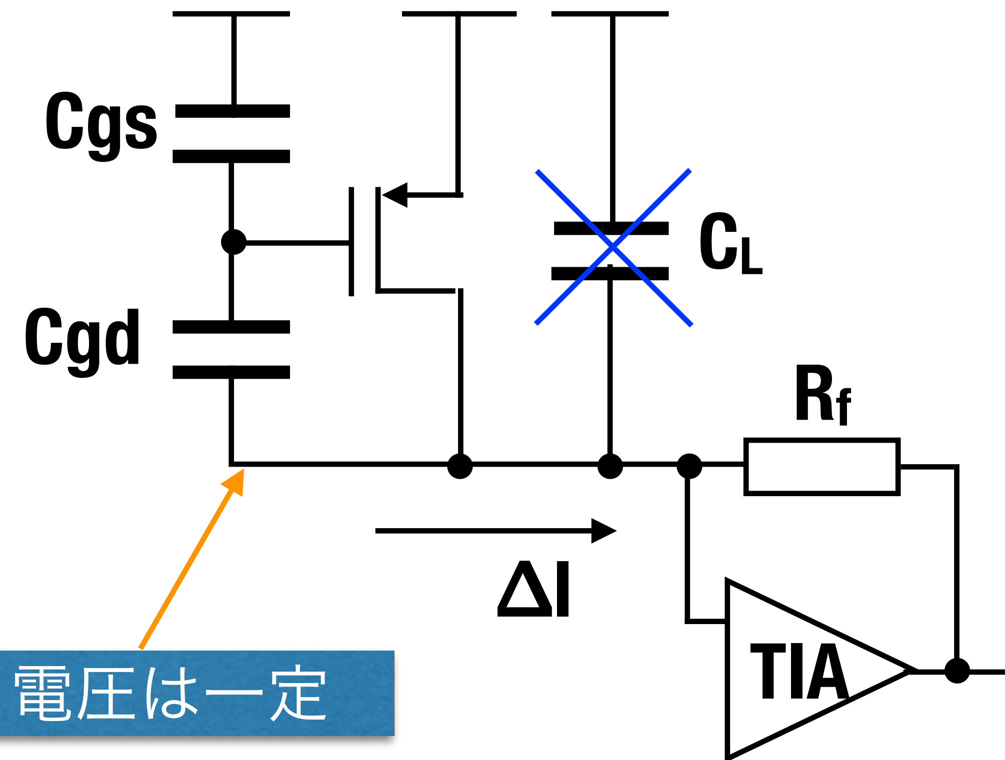
$$\Delta U \sim \frac{Q_{\rm in}}{C_{\rm g}}$$

$$\tau = 2.2 \times \frac{C_{\rm L} \cdot (1 + C_{\rm gs}/C_{\rm gd})}{g_{\rm m}} \sim \mu {\rm s}$$

✓Cgs, Cgdはゲインとスピードのトレードオフ

✓C_Lが立ち上がり時間に影響

電流読み出し(ドレイン)



$$\Delta I \sim \frac{Q_{\rm in}}{C_{\rm gd} + C_{\rm gs}} \times g_{\rm m} \qquad \tau = \text{very small}$$

✓ドレイン電圧が一定なので高速読み出しが可能

(virtual ground, R_{drain}とgate settling timeでリミット)

Belle II用Depfetは電流読み出しを採用

DEPFETフロントエンドASIC (Belle II)

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マトリックスの駆動/読み出しに3種類のASICを用いる

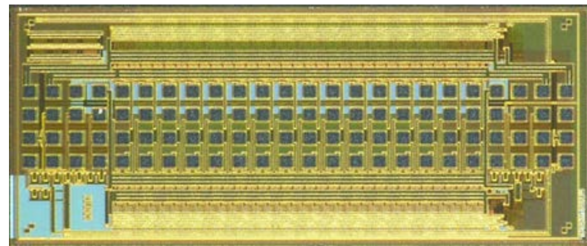
- センサー部の厚さは75 μm, 周辺部は450 μm @MPP
- ASICはセンサーサブストレートにバンプボンド
- 10 Mrad (5 yr)

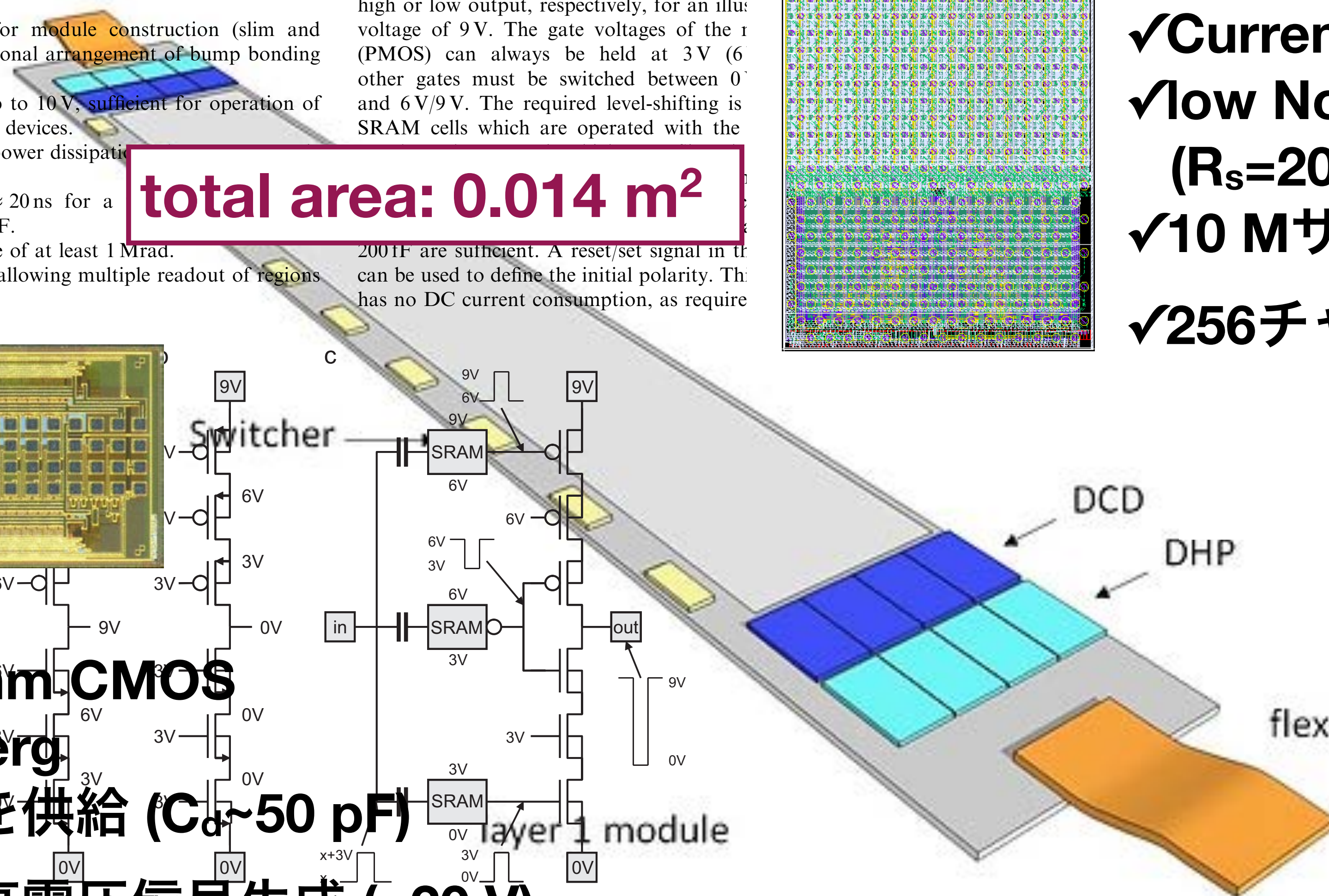
DCD-B

- ✓UMC 180 nm CMOS
- ✓Univ. Heidelberg
- ✓Current Receiv. (TIA)+ ADC
- ✓low Noise & fast settling (R_s=200Ω, C_d=50 pF)
- ✓10 Mサンプル/s
- ✓256チャンネル

total area: 0.014 m²

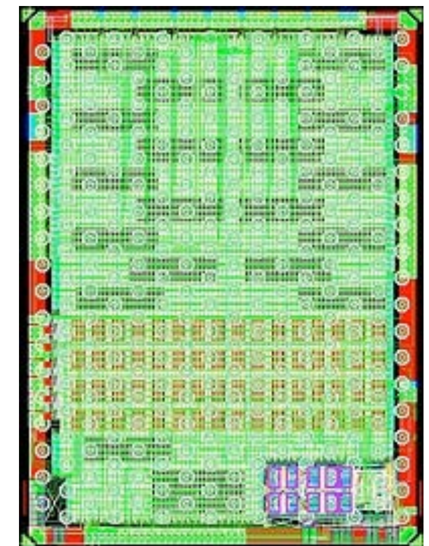
SWITCHER-B





- ✓AMS HV 180 nm CMOS
- ✓Univ. Heidelberg
- ✓速い駆動信号を供給 (C_d~50 pF)
- ✓信号クリア用高電圧信号生成 (~20 V)

DHPT



- ✓TSMC 65 nm CMOS
- ✓Univ. Bonn
- ✓SW, DCDへのクロック供給
- ✓Zero-Suppression
- ✓G-bitデータリンク

Design review in Oct. 2014→final submission in 2015!

MAPS-epi テクノロジー

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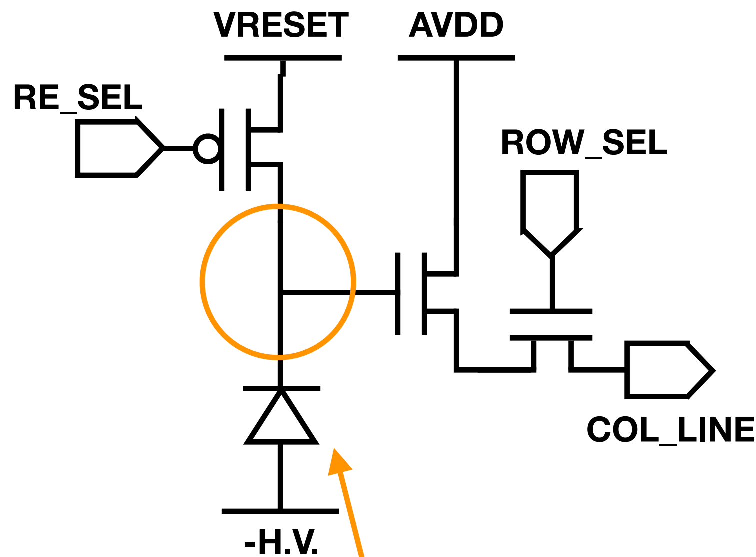
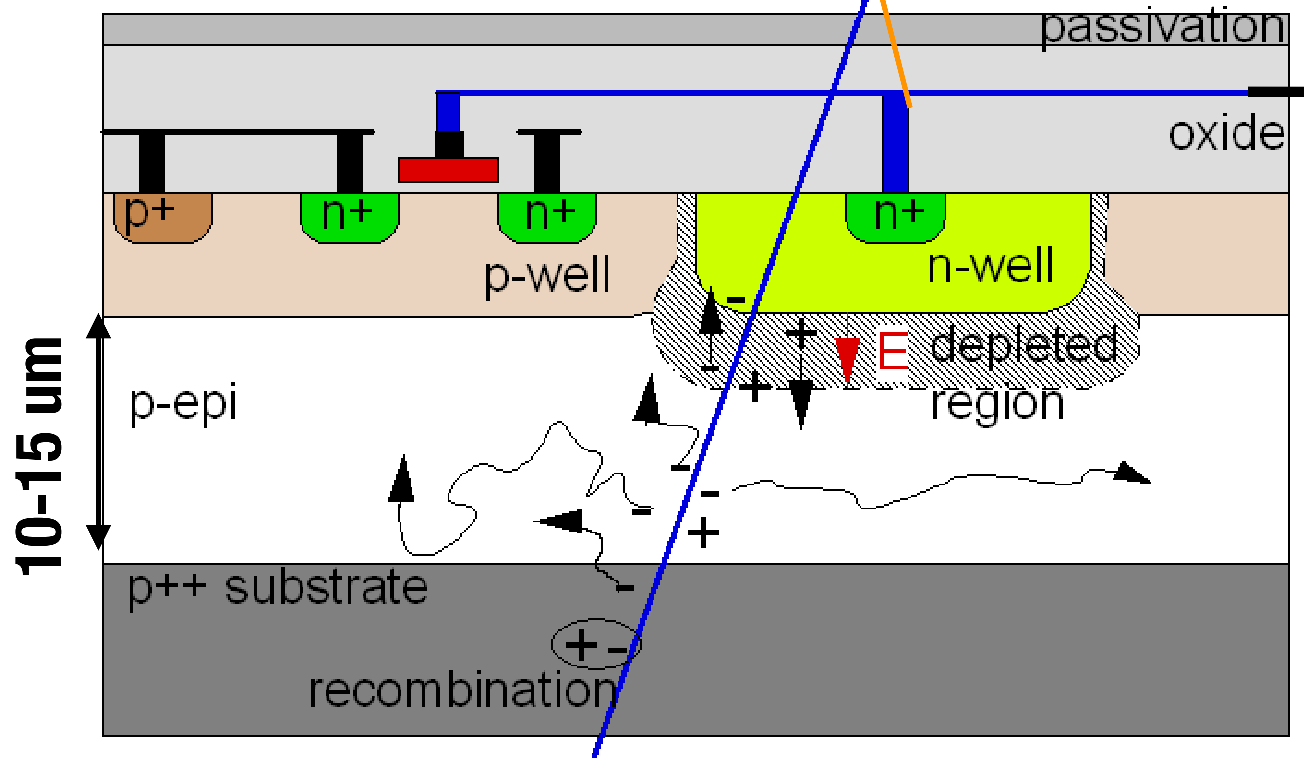
“スタンダード3T”



✓eliminate: base levels, 1/f noise, fixed patter noise
✓do this either offline-> slow or on-chip R&D



✓センサーと読み出しを同じSiウェハーに形成

- commercial CMOSプロセス(安価)

✓low-dopedエピタキシャル層で電荷生成

(10-15 um, e.g., AMS 0.35 μm)

- MIP signal < 1000 e-→低雑音読み出しが課題

✓拡散による電荷収集(~100 ns)

(p-well, sub.による散乱、n-well/epiで収集)

→信号が複数ピクセルに分布

✓NMOSのみをエレキに使用

(n-well/epiがcollection node)

✓小ピクセルサイズ (20-30umピッチ)

→spatial resolution < 2 um

✓Large detector→19.4x17.4 mm^2 (1 Mpix)

MAPS-epi テクノロジーの現状(@STAR)

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初のMAPSベースのtracker (Strasburg+LBNL, >15 yrs R&D)

2004-2006
First MAPS prototypes for the STAR PXL detector

2008
Full size sensor with digital readout

2011-2012
Final sensor for the PXL detector

Complementary detector readout

Sensing elements → *analog signals* → ADC → *digital* → CDS → *Digital signals* → Data sparsification → DAQ

Preamplifier + CDS → *analog* → ADC

column level discr. and 0-suppr.

sensor generations

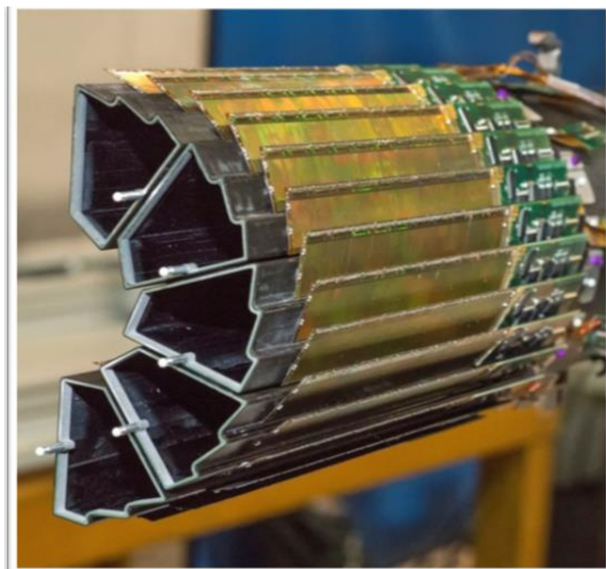
1st — *4 ms integration time*

2nd — *640 μs integration time*

3rd — *< 200 μs integration time*

C. Hu-Guo

Courtesy of M. Szelezniak, HICforFAIR Workshop 2014



MIMOSA28

- ✓ ピクセルサイズ: 20.7 × 20.7 μm², 厚さ: 50 μm
- ✓ 400 sensors, 356 Mpixels, ~0.15 m²
- ✓ 20 to 90 krad/yr
- ✓ 2×10^{11} to 10^{12} n_{eq}/cm^2
- ✓ 室温で動作
- ✓ 積分時間: 185 μs

最近のMAPS開発の現状

trend: epi→high-R sub., CMOS electronics

Signal charge & time resolution

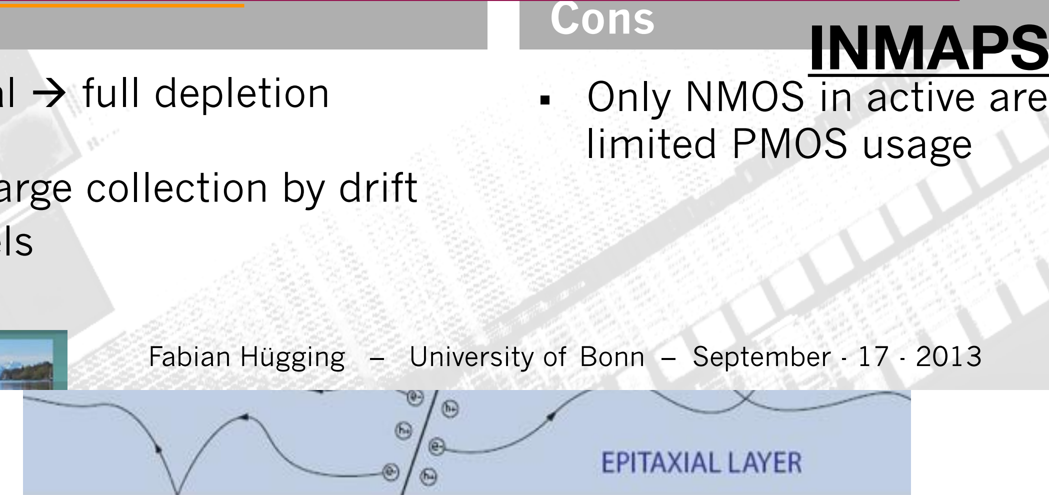
		Charge collection by drift		
		No	Yes	
		Epi-layer or bulk CMOS	High voltage technology	High resistive substrate
Full CMOS in pixel area	Yes	"INMAPS"		D-MAPS
	No	Std. MAPS	HV-MAPS	"LePIX"

In-pixel signal processing ↑

Leading institutes: Heidelberg, Bonn, CPPM, Strasburg

P N N N N P
PW
Deep Nwell
Deep Nwell
60-300um
particle track
P-substrate
<-10

extended deep-Nwell collecting electrode
(STM 130 nm triple well cmos)
complete signal processing chain
Pavia, Bergamo, Pisa: V. Re, G. Rizzo et al.



INMAPS

epi with deep p-well (RAL, UBirmingham…)
quadrupel well 0.18 um CMOS
to shield the n-wells that contains PMOMS
deep-p cannot be made too small

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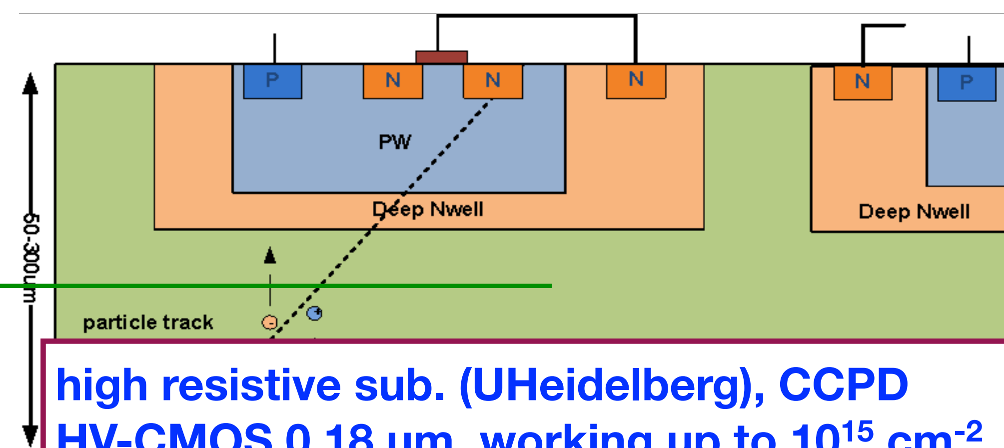
HV-MAPS



high resistive sub. (UHeidelberg), CCPD
HV-CMOS 0.18 μm, working up to 10^{15} cm^{-2}

MAPS-SOIテクノロジー(OKI/Rapis)

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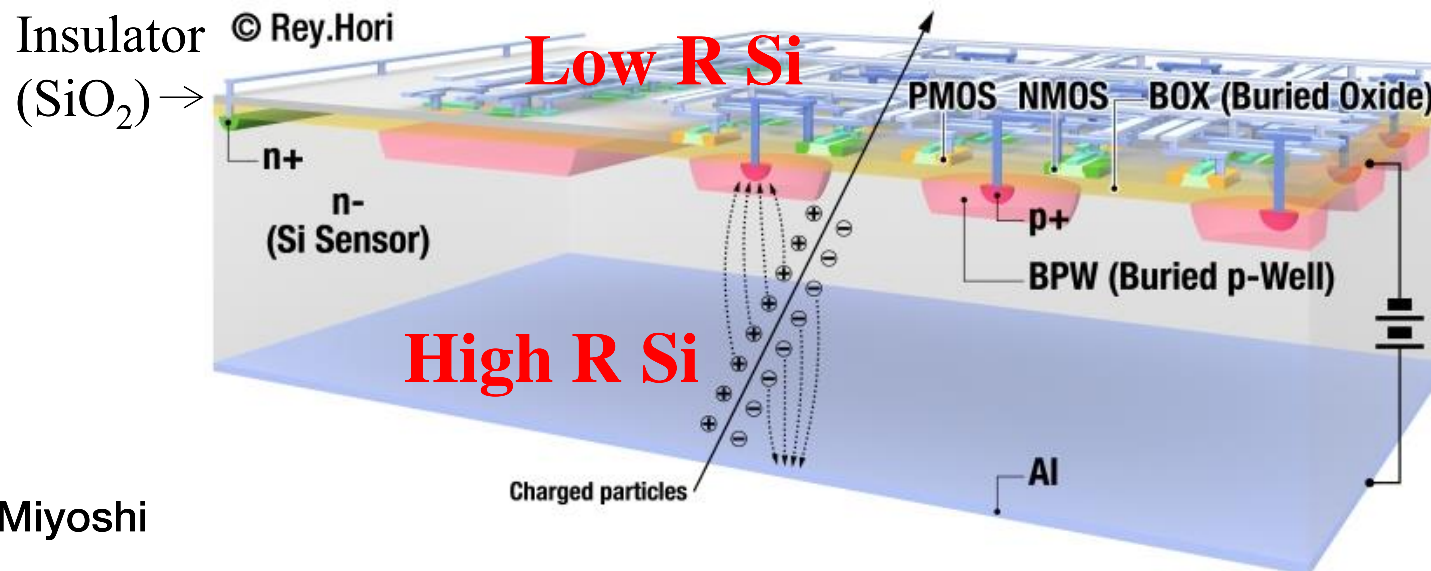
✓ハンドルウェハーをセンサーに使用
✓読み出しをBOX層の上に配置

→本当の意味でのモノリシックピクセル...



borrowed from Miyoshi-san, TWEPP-2014

Targets
High-Energy Physics
X-ray astronomy
Material science
Non-Destructive inspection
Medical application

The features of SOI monolithic pixel sensor

- No mechanical bump bonding. Fabricated with semiconductor process only
- Fully depleted (thick & thin) sensing region
  with low sense node capacitance (~10 fF@17 µm pixel) → high sensor gain
- SOI-CMOS; Analog and digital circuit can be closer → smaller pixel size
- Wide temperature range (1-570K)
- Low single event cross section
- Technology based on industry standards; cost benefit

✓センサー/エレキのカップリング
→charge injection from CMOS swing
✓BOX層への正電荷蓄積によるVthシフト

back bias effect →PD...

MAPS-SOIテクノロジー@BONN

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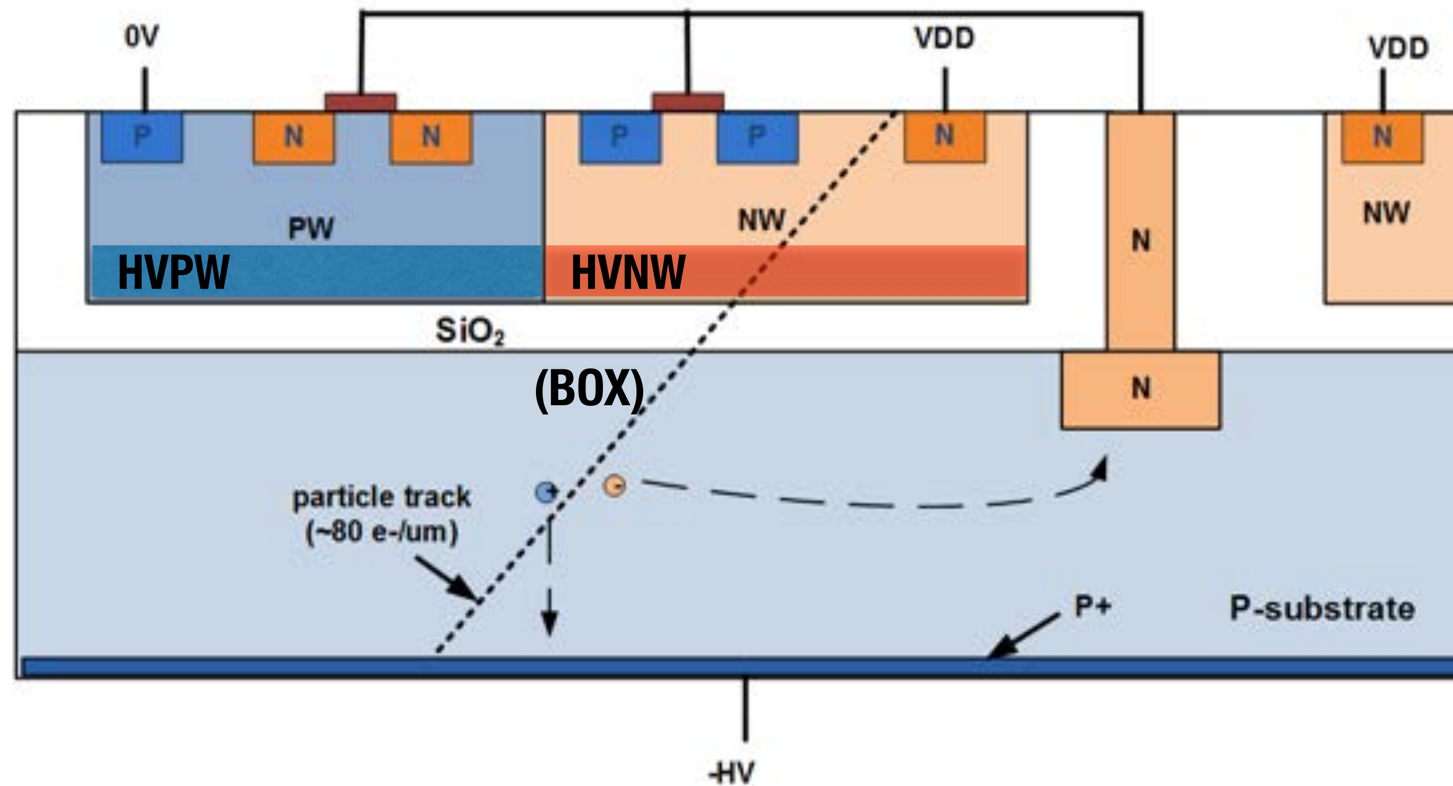
XFAB 180 nm HV SOI CMOSプロセス



Feature size: 180 nm
Supply rail: 1.8 V
p-type bulk, 4 metal layers
Resistivity: ~100 Ω cm
High voltage: ~several 100 V

Thickness:
gate oxide: 4.1 nm
BOX: 1 μm
Chip: 300 μm
Distance from Gate to BOX: 3 μm

- ✓ BOX isolates electronics part from the sensor part
- ✓ full depletion possible → fast & high signals $d \sim \sqrt{\rho \cdot V}$
- ✓ full CMOS electronics (CSA, shaper etc. if needed)
- ✓ theoretically rad-hard (less SEU) + separated with HV-layers

No BOX effects to FETs, sensor optimization is necessary, e.g., I_{leak}

HEPに要求される放射線耐性

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Innermost pixel layer　**higher lumi. & radiation→smaller pixel**

	BX time	Particle rate	Fluence	Ion. dose
	ns	MHz/cm^2	n_{eq}/cm^2 per lifetime*	kGy per lifetime
LHC(10^{34}cm^{-2}s^{-1})	25	100	10^{15}	790
HL-LHC(10^{35}cm^{-2}s^{-1})	25	1000	>10^{16}	5000
SuperBF(10^{35}cm^{-2}s^{-1})	2	40	~3×10^{12}	100
ILC(10^{34}cm^{-2}s^{-1})	350	25	10^{12}	4
RHIC(8×10^{27}cm^{-2}s^{-1})	110	0.38	1.5×10^{13}	8

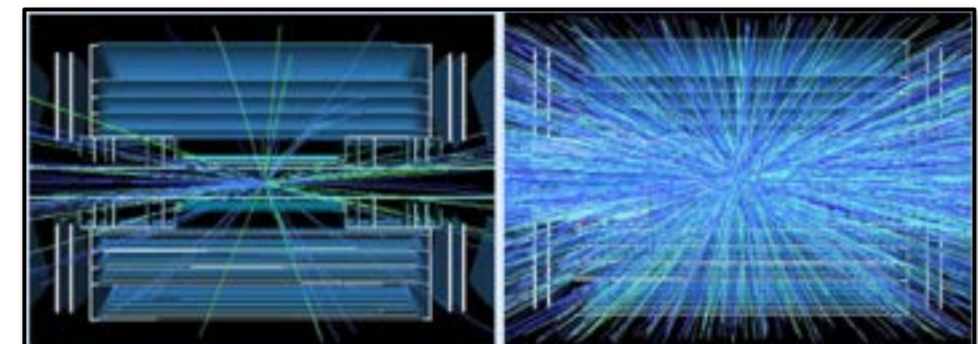
*lifetime: LHC, HL-LHC for 7yrs, ILC for 10 yrs, others for 5 yrs

モノリシックピクセル

- ✓lower rates 😨
- ✓lower radiation 😨
- ✓less power 😃
- ✓less material 😃
- ✓smaller pixel 😃

ハイブリッドピクセル

- ✓higher rates 😃
- ✓higher radiation 😃
- ✓more power 😨
- ✓more material 😨
- ✓bigger pixel 😨



テクノロジーのトレンド

- ✓ 3D integration
- ✓ CCPD (Charge Coupled Pixel Detector)
- ✓ 65 nm CMOS

3D Integration

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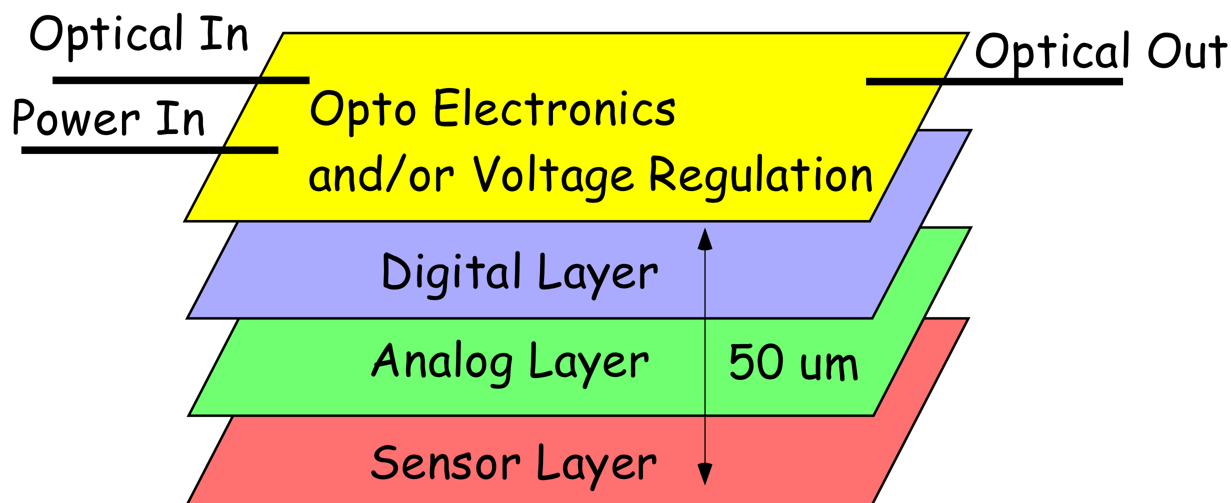
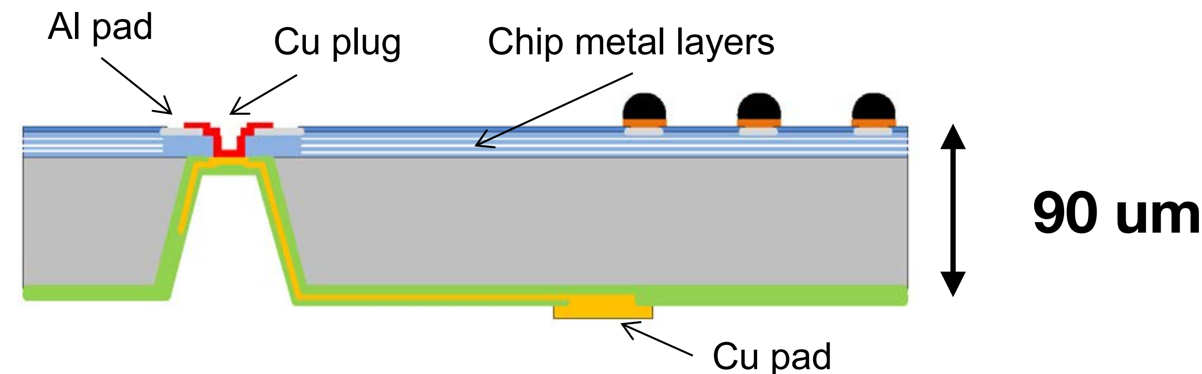
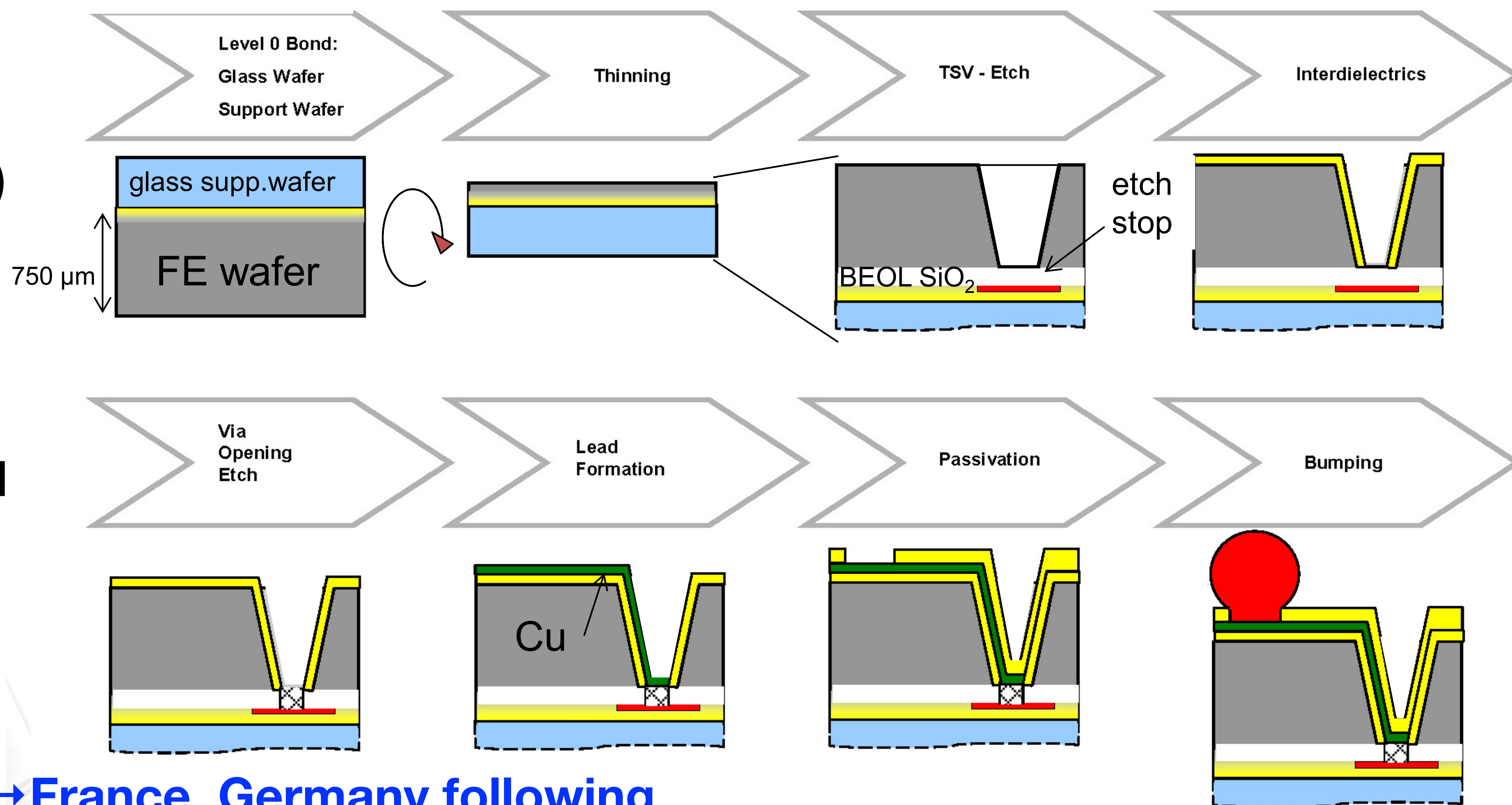
Detector physicists' dream…



Tapered Side Wall TSV (Through Silicon Via)
@IZM, Berlin





- ✓チップを積層(analog, digital)
- ✓各layerで異なるTechnologyを使用可能 (BiCMOS, SiGe, opto)
- ✓reduced R, L, and C→speed
- ✓reduced interconnect power, x-talk
- ✓reduce pixel size

first initiative from Fermilab→France, Germany following…

    need more time…

Capacitive Coupled Pixel Detector (CCPD)

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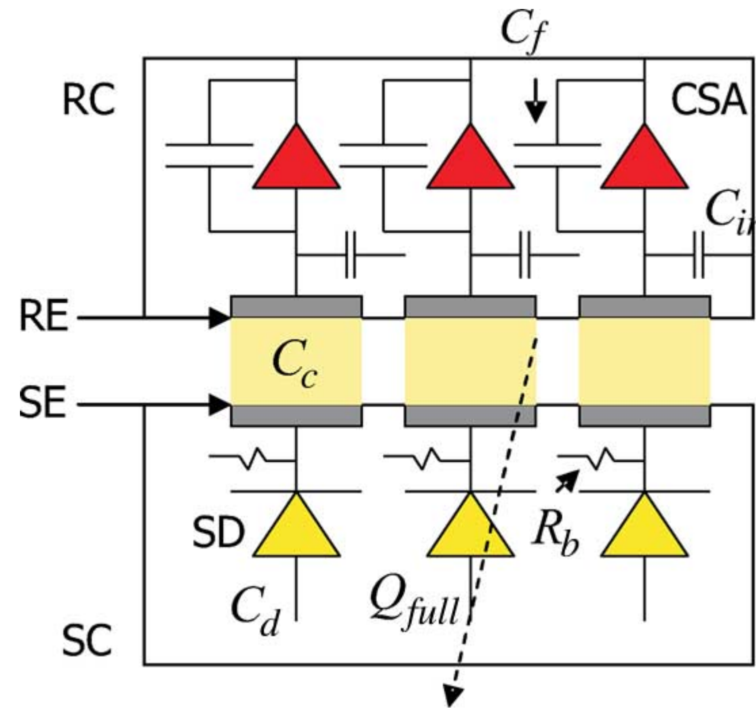
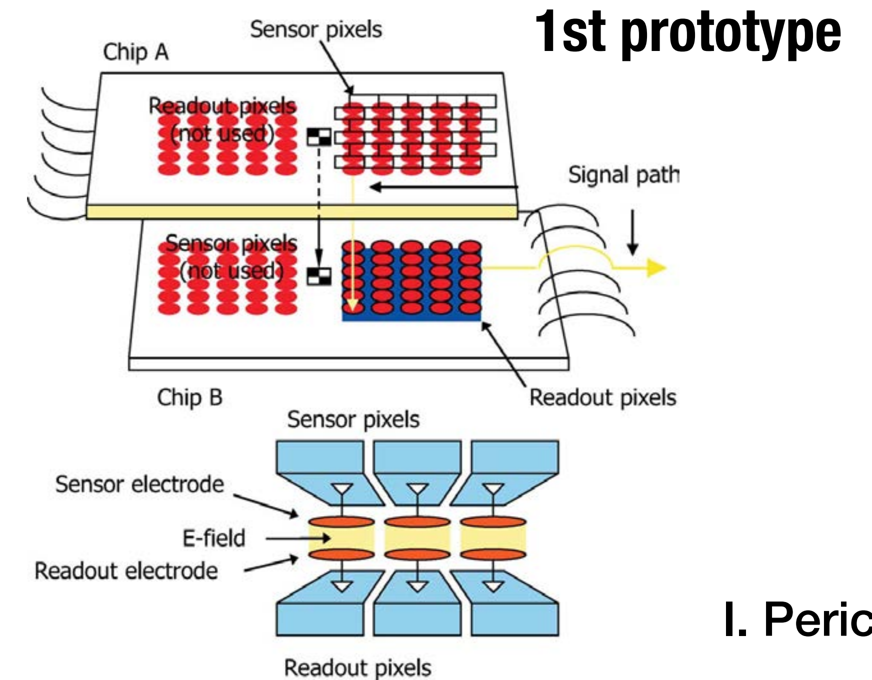
bumpless hybrid approach

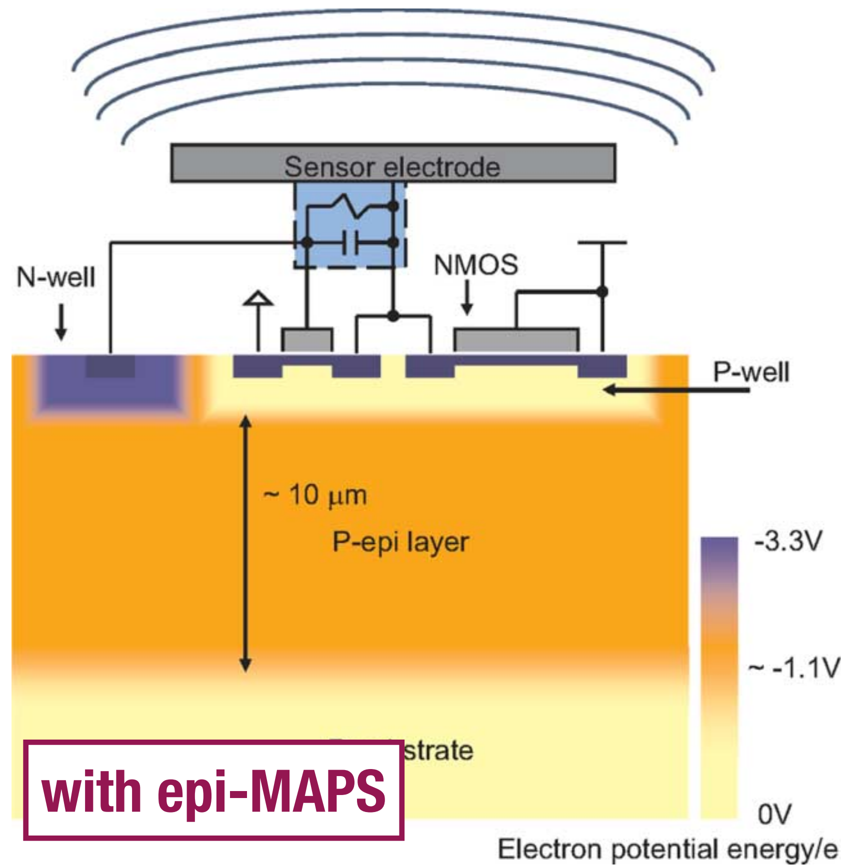
- ✓"in-house"
- ✓non-conducting glue

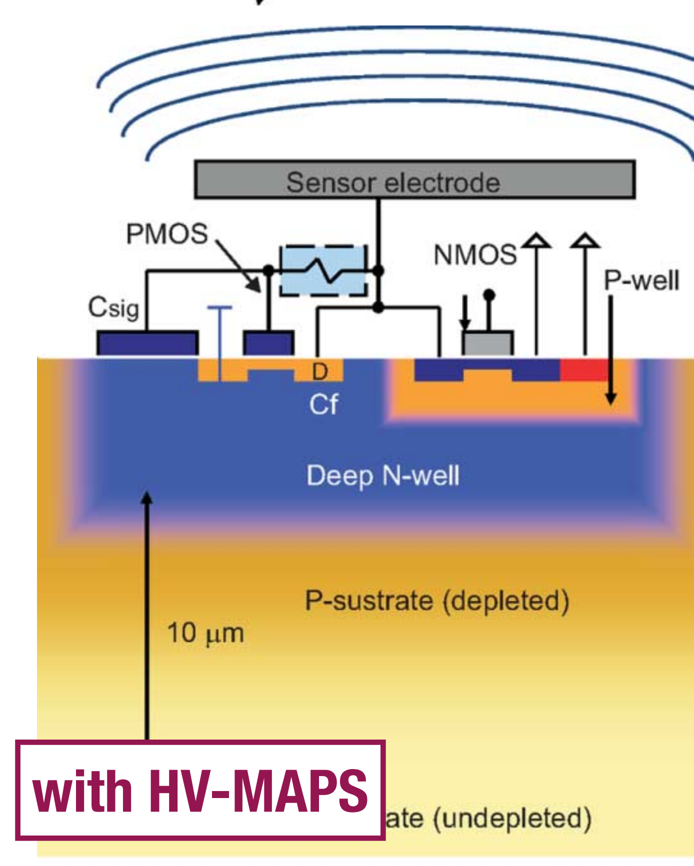


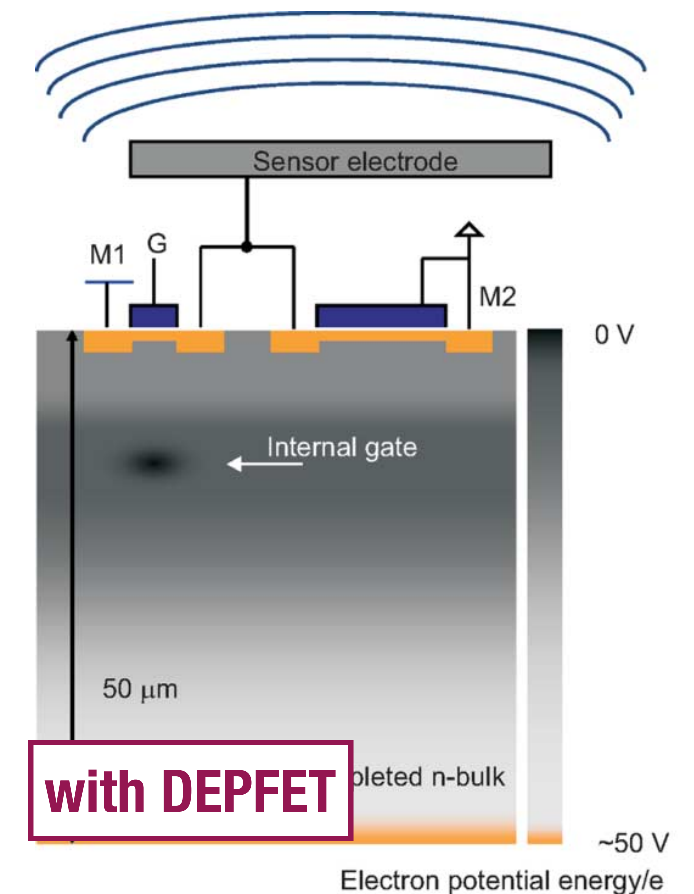
1st prototype



I. Peric







HEPとCMOSテクノロジー

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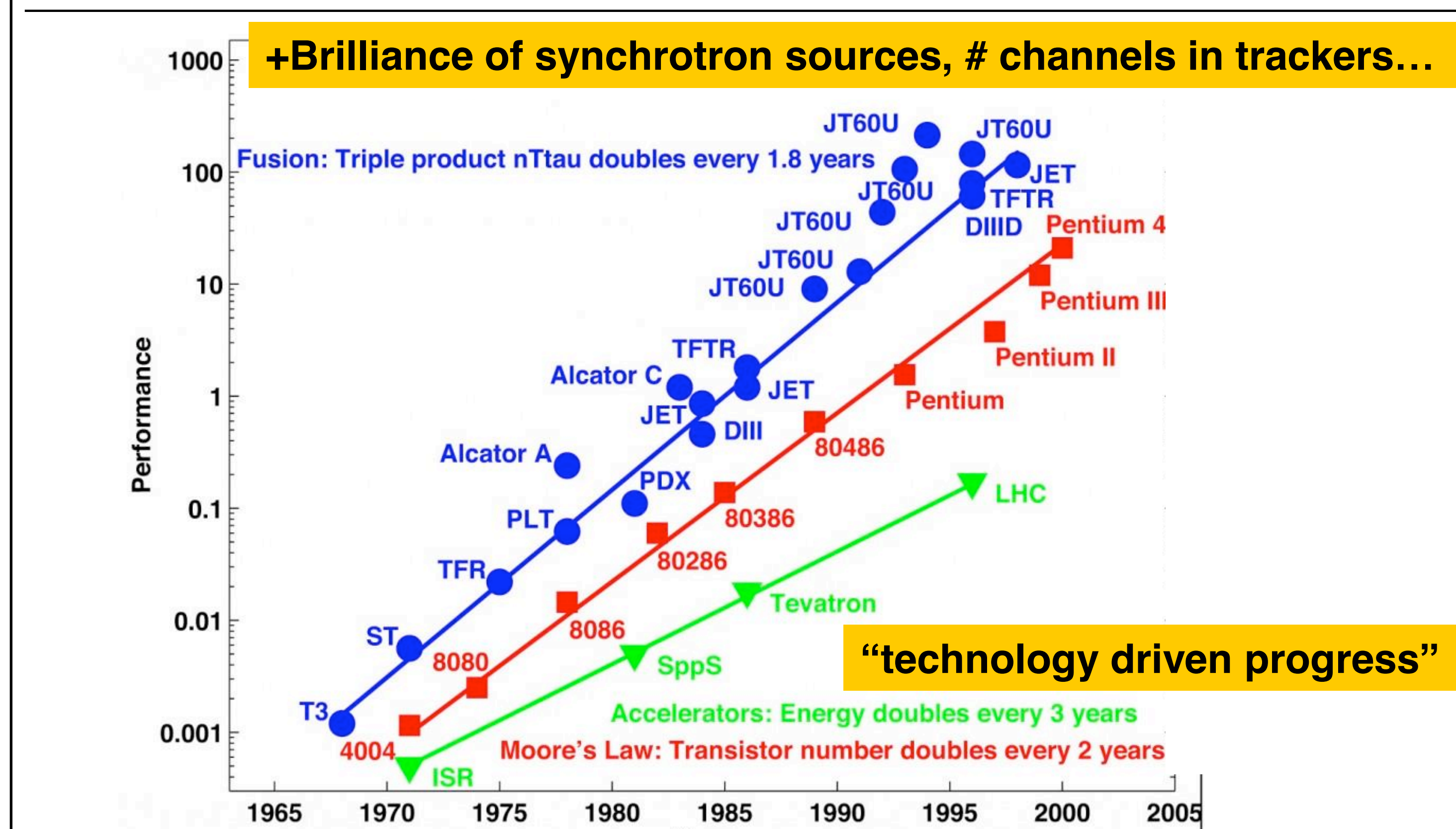
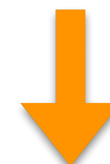
Moore’s Law – chips, accelerators, fusion…



HEPでの要求

- ✓小ピクセル化
- ✓低消費電力
- ✓高速信号処理
- ✓more “intelligence” in each pixel
- ✓放射線耐性

65-nm CMOSが主流になりつつある

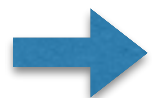


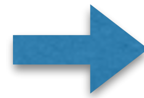
開発における課題

- ✓Expensive…
- ✓低電源(😨アナログデザイン)
- ✓ゲート漏れ電流(tunneling)
- ✓デザインルール増(EGT not arrowed)
- ✓デザインの複雑化

(RD53: ATLAS, CMSのpixel FE)

UNIVERSITY OF TWENTE.





250 nm technology	130 nm technology	65 nm technology
pixel size 400 × 50 μm²	pixel size 250 × 50 μm²	pixel size 125 × 25 μm²
3.5 mil. transistors	80 mil. transistors	~ 500 mil. transistors

フロントエンドへの応用@BONN

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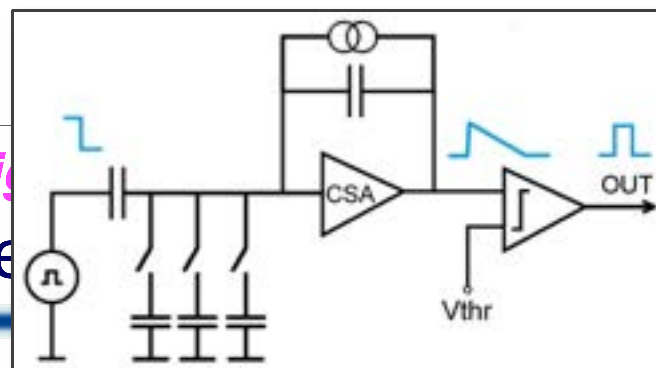
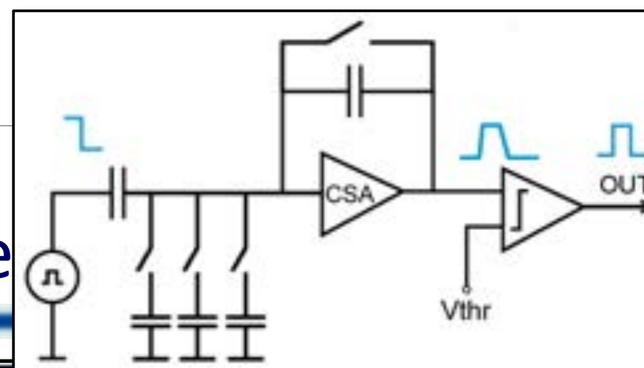
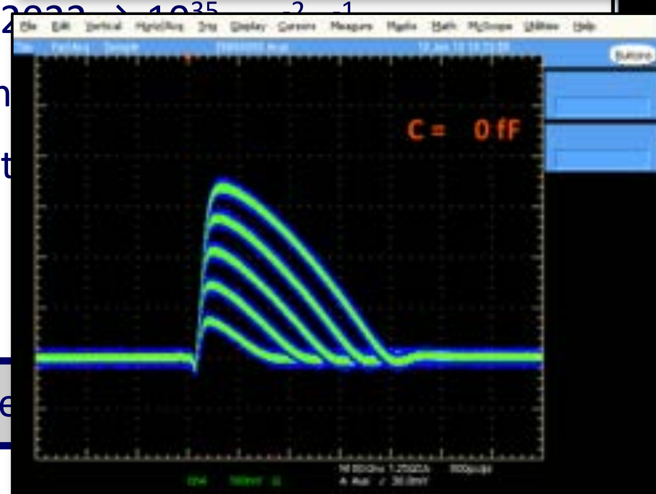
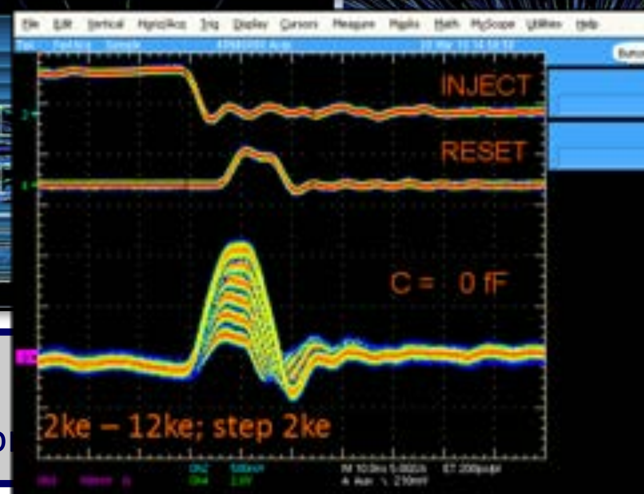
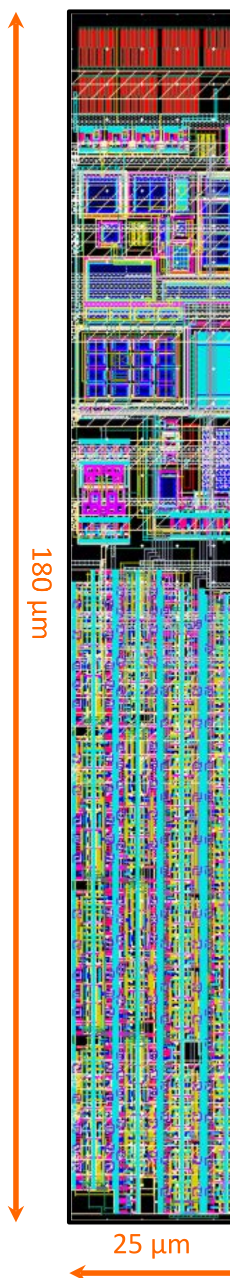
M. Havranek











FE-T65-1 – single pixel

- CSA+comparator
- TDAC
- 8 bit counter
- config. register
- mask, HitOr

	FE-I4	FE-T65-1
Technology	130 nm	65 nm
Pixel size	250 × 50 µm^2	180 × 25 µm^2
Dimensions of analog part	156 × 50 µm^2	59 × 25 µm^2
Charge sensitive amplifier	2 stages	1 stage
Comparator	continuous	continuous /dynamic
Analog power consumption	21.9 µW / pixel	10.6 µW (18 µW) / pixel
Analog power density	1.75 mW / mm^2	2.36 mW / mm^2 (4 mW / mm^2)

not final design…

✔FE-I4と同性能

✔ピクセル面積1/4

超低消費電力ADCデザイン

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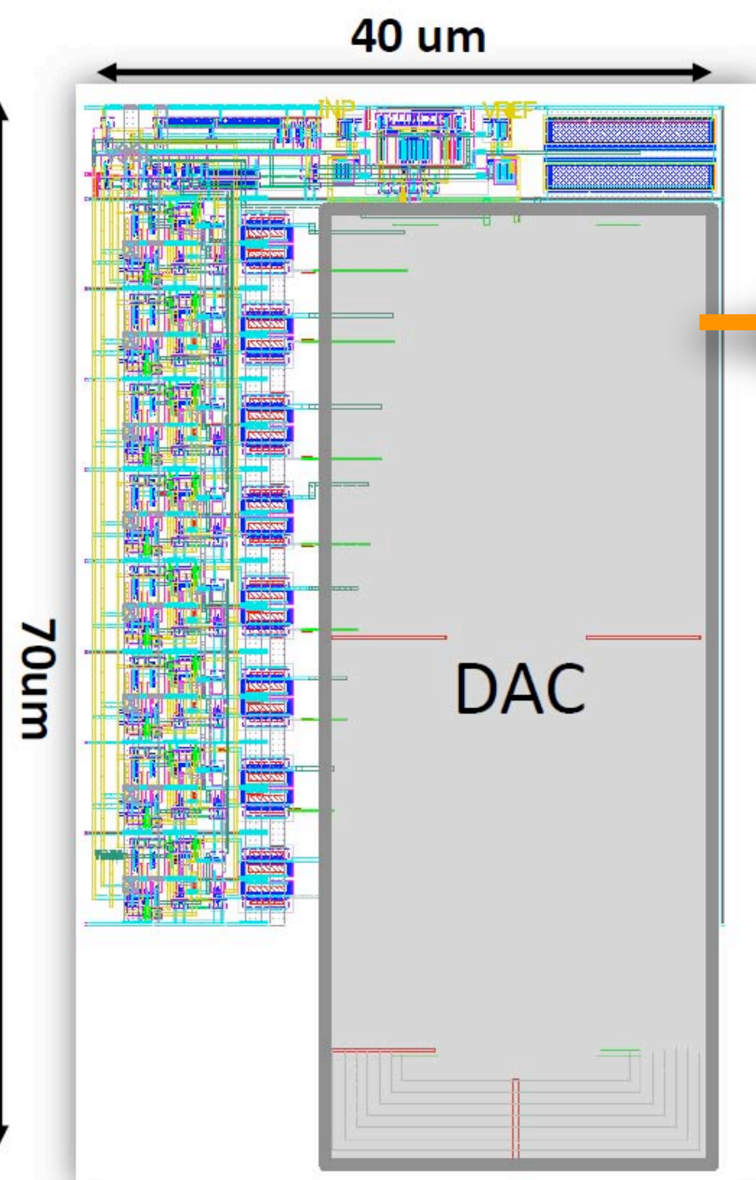
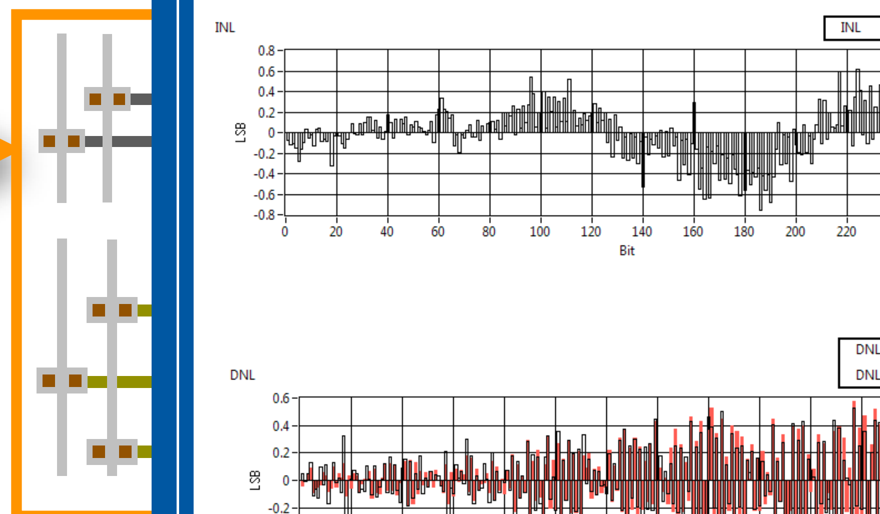
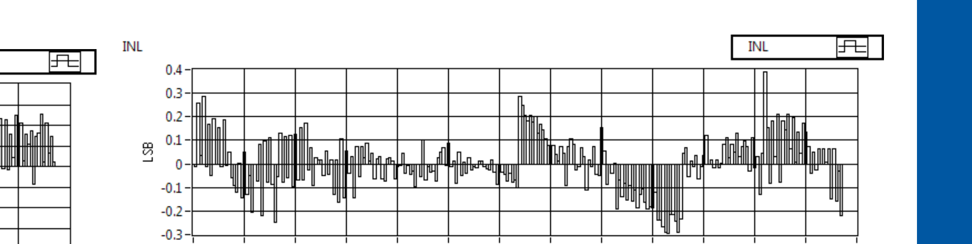
Conventional ADCs are pow

→SC circuit + dynamic com





BEST ASYNCHRNOUS ADC – 12.5MS/s



10

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3D integration, MAPS, photon counting…

65 nmプロセスの放射線耐性

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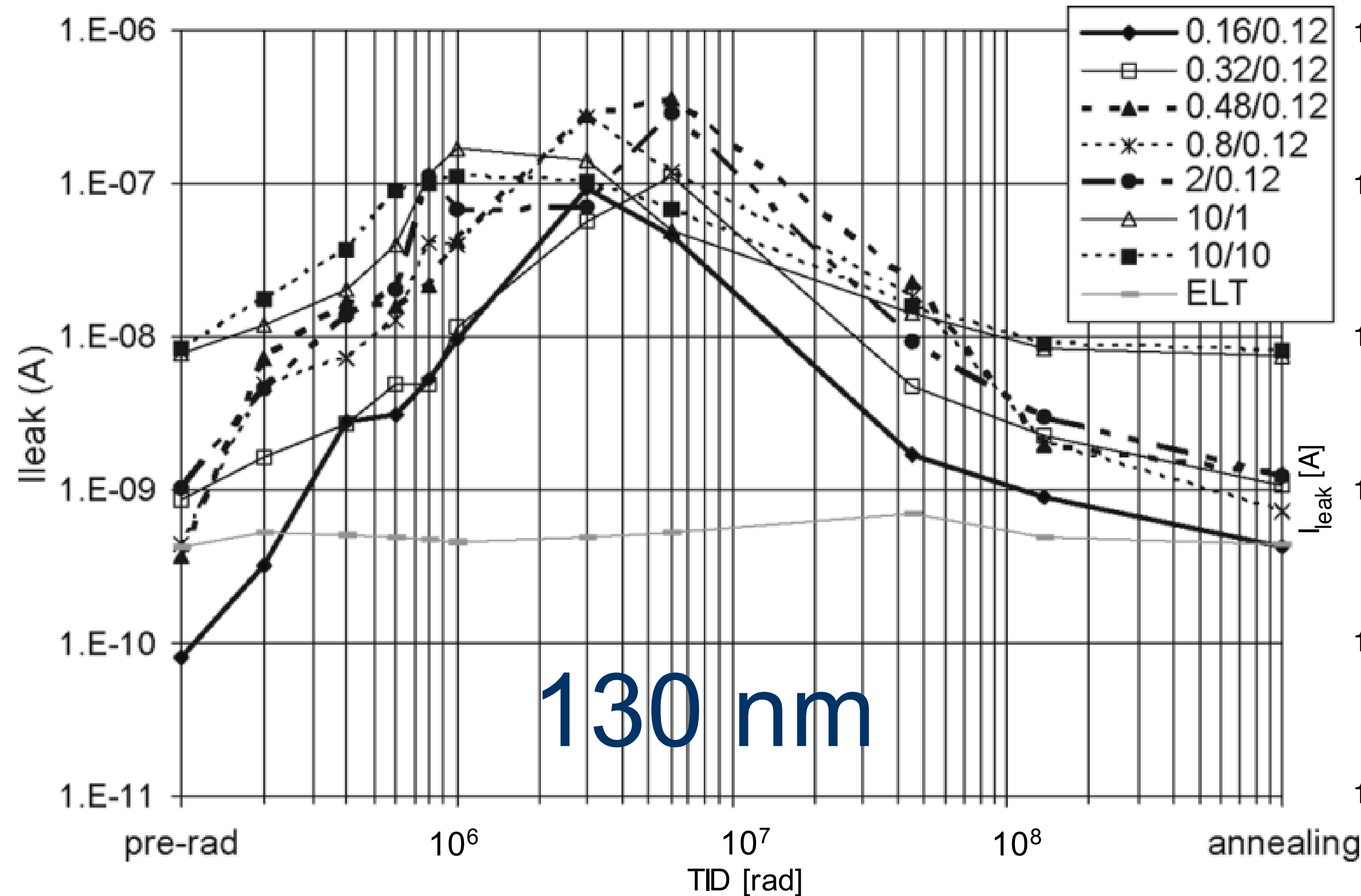
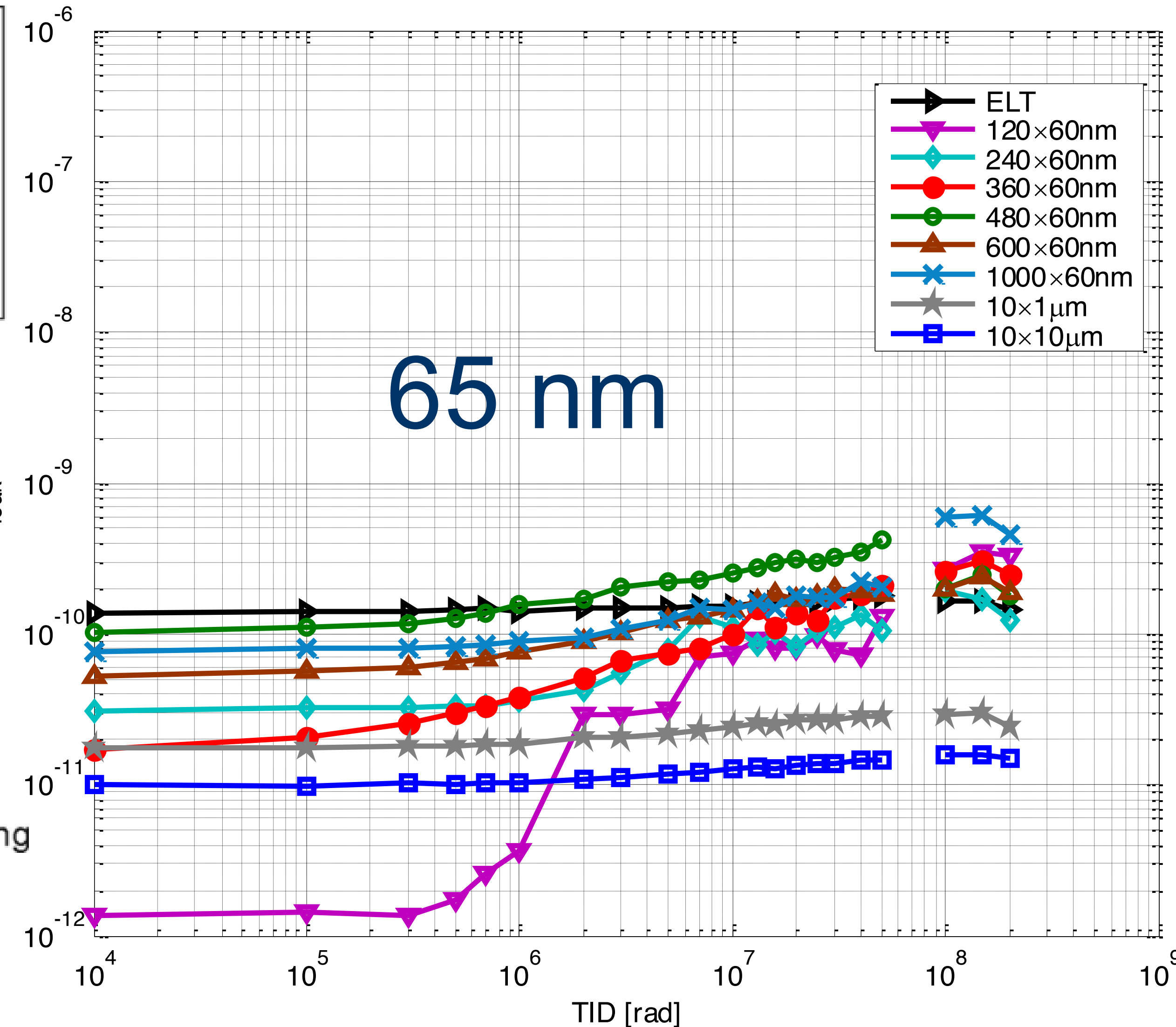
borrowed from CERN group



F.Faccio et al., "*Radiation-induced edge effects in deep submicron CMOS transistors*", IEEE Tr. Nucl. Sci. 2005

core NMOS, leakage current



✓a rebound effect is visible in 130 nm
✓all 130 nm devices are peaking at ~100 nA
✓small W devices increase I_{leak} by 2 orders of magnitude
✓I_{leak} is ~1 nA@136 Mrad

lower V_{th} shift than 130 nm (core FET)

Conclusions

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ハイブリッドピクセル

needs heavy R&D on sensor materials, ICs and modules, 3D integ.

✓state of art, 技術的には成熟

✓sensorとエレキを別々に選べる

✓rad-hard OK

✓production yieldの問題, アセンブリーが大変, 複雑なオペレーション(many modules)

✓比較的高価 (50-100 EUR/cm^2)←innermost layerならOK

✓smaller pixel →50 x 50 um^2 with smaller feature-sized technology (65 nm CMOS)

モノリシックピクセル

needs heavy R&D on full CMOS integration, radiation tolerance

✓技術的にはこれから(rad-hard, sensor propertyはprocess optionに依存)

✓大面積を安価に実現できる可能性(commercial CMOS, no bump, <10 EUR/cm^2)

✓3D integrationが実現できればより高速かつ、intelligentなpixel検出器が可能

✓Monolithic for ILC; MAPS, DEPFET, new tech. like SOI pix, a-Si:H pixels

Next challenge

✓HL-LHC radiation tolerance up to $10^{16} n_{eq}/cm^2$→新しいセンサー (diamond, 3D)

✓light weight→less power, new cooling, new mechanism

✓data band width: 40MHz→GHz