ATLAS 実験アップグレード用
シリコン検出器試験用DAQの開発

計測システム研究会@RCNP

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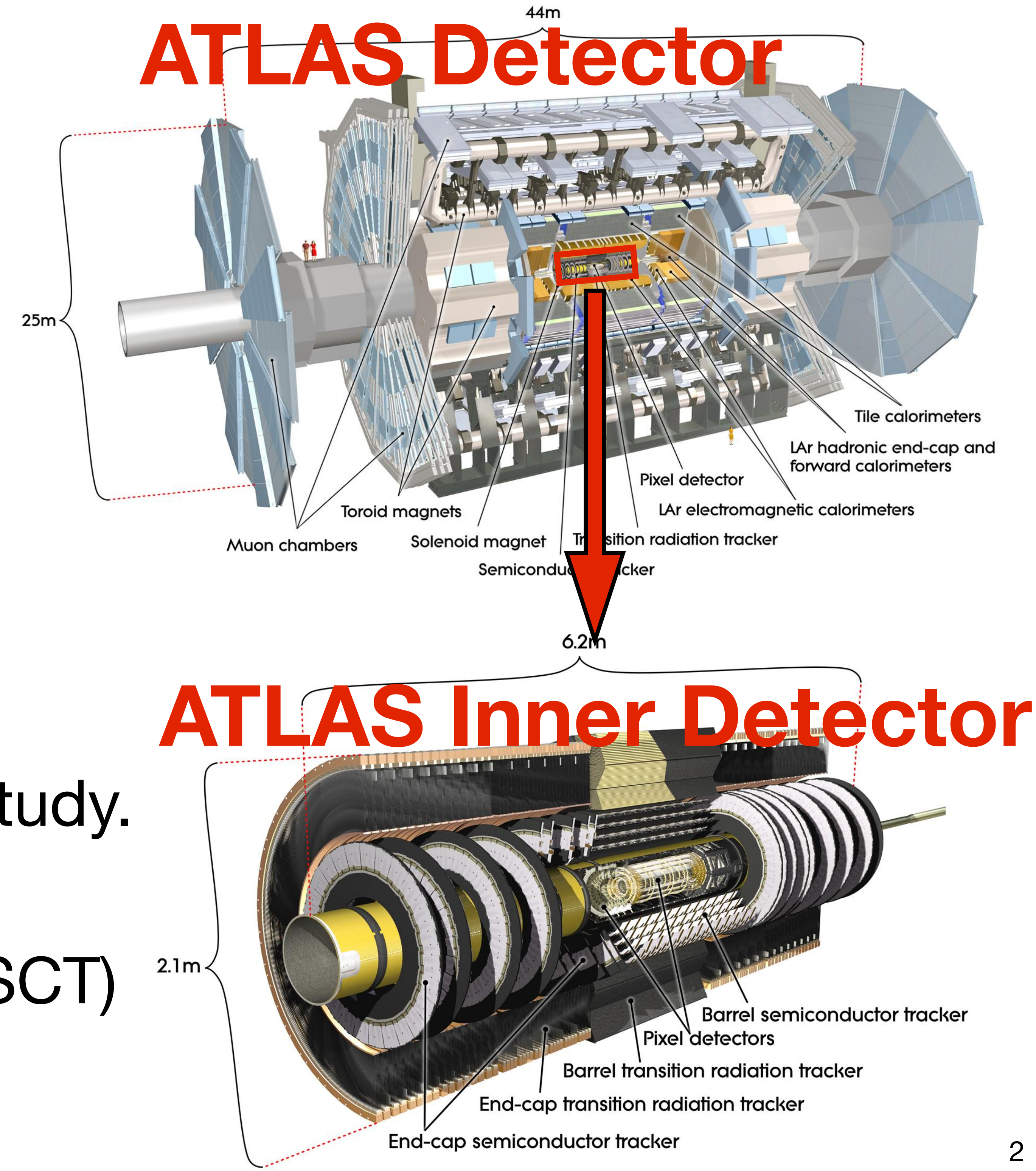
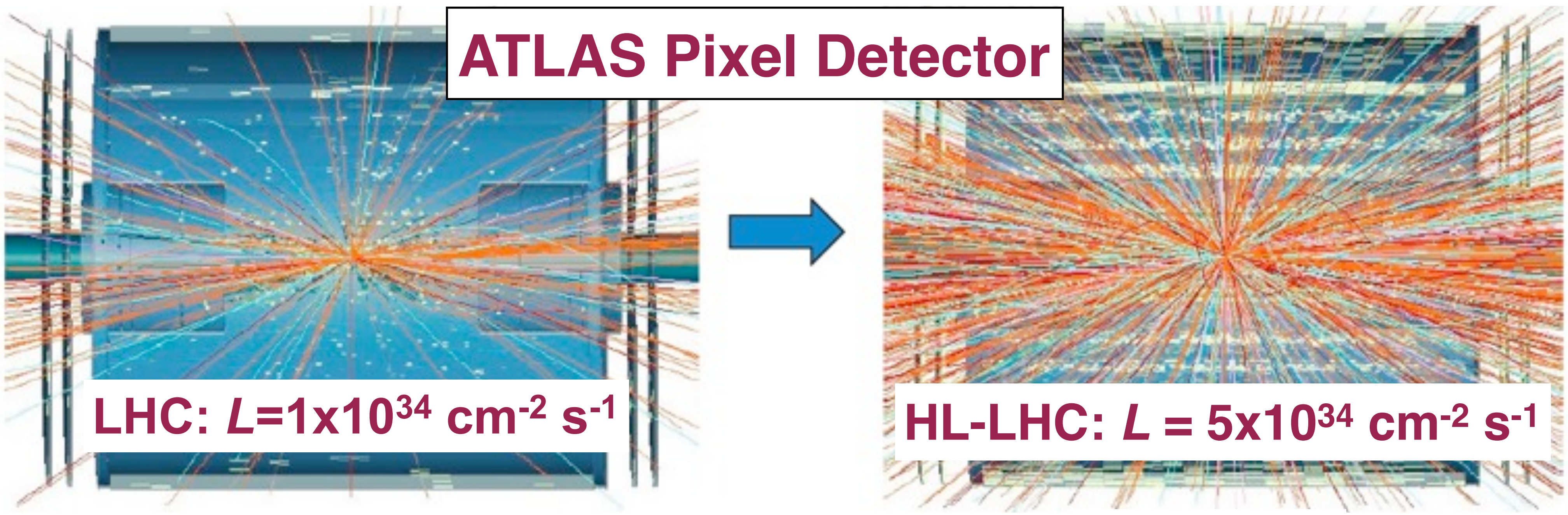
Introduction

- Inner detector in ATLAS
  - ➡Purpose :
    - Particle tracking
    - Vertexing
  - ➡Provides very important information for "all" reconstructed object.



- ATLAS-Japan group is involved in silicon detector study.
  - ➡Pixel detector
  - ➡SemiConductor Tracker (SCT)

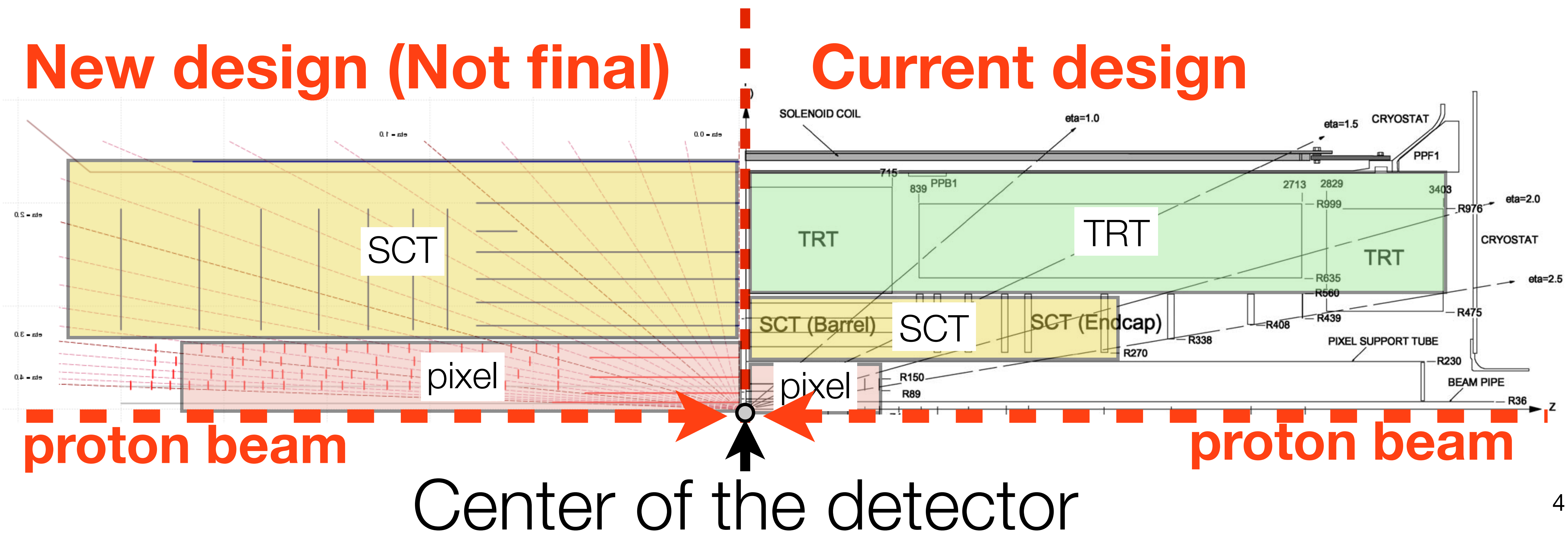
Inner detector in HL-LHC



- Many problems to use the current design.
  - ➡Intolerable radiation damage
    - Fluence of ~10^{16} n_{eq}/cm^2
  - ➡Unacceptable occupancy
    - 23 → 140 *pp* collisions in one bunch crossing.
- **Completely new design is under study for the upgrade.**

Overview of the upgraded detector

- Full silicon tracker.
  - ➡To have high granularity/fast responding detector.
- Larger detector acceptance.
  - ➡Extend up to |η|<4.0.
- Many studies are ongoing.
  - ➡Detector R&D, layout, support structure, cooling etc...



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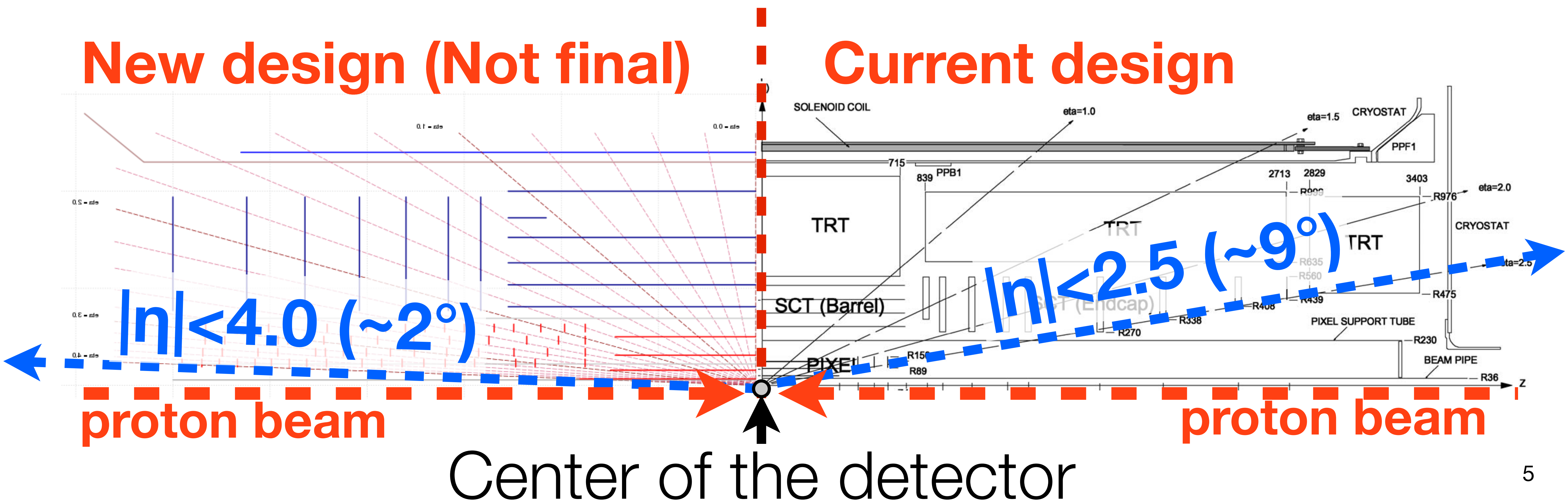

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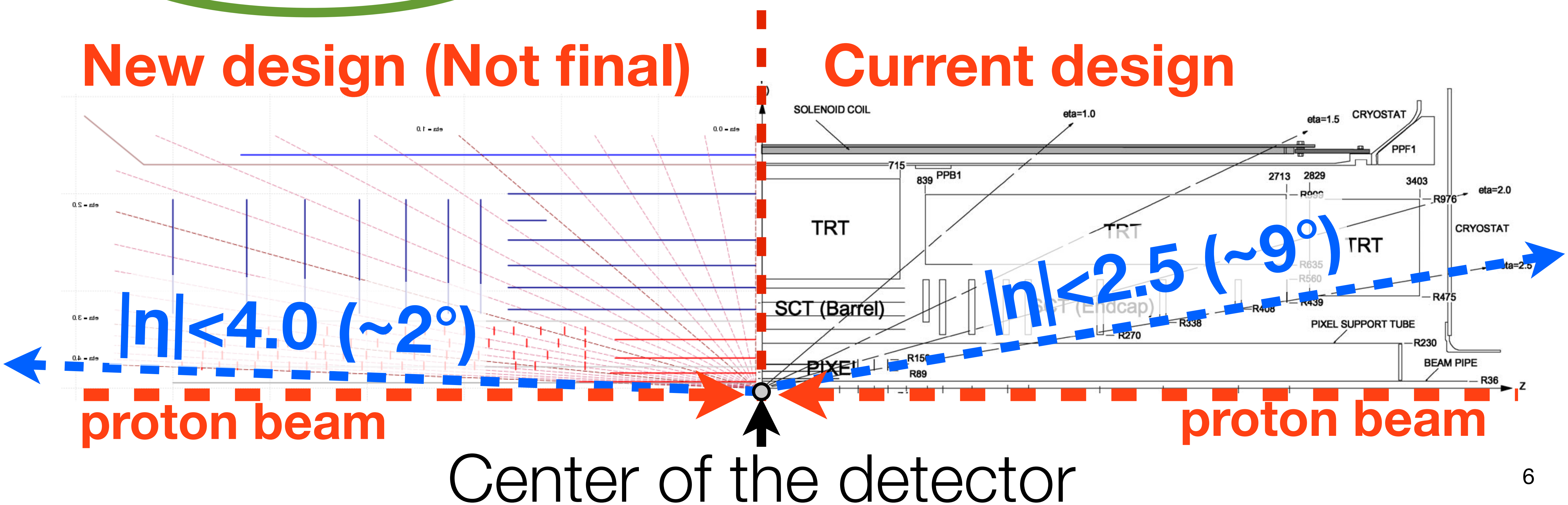
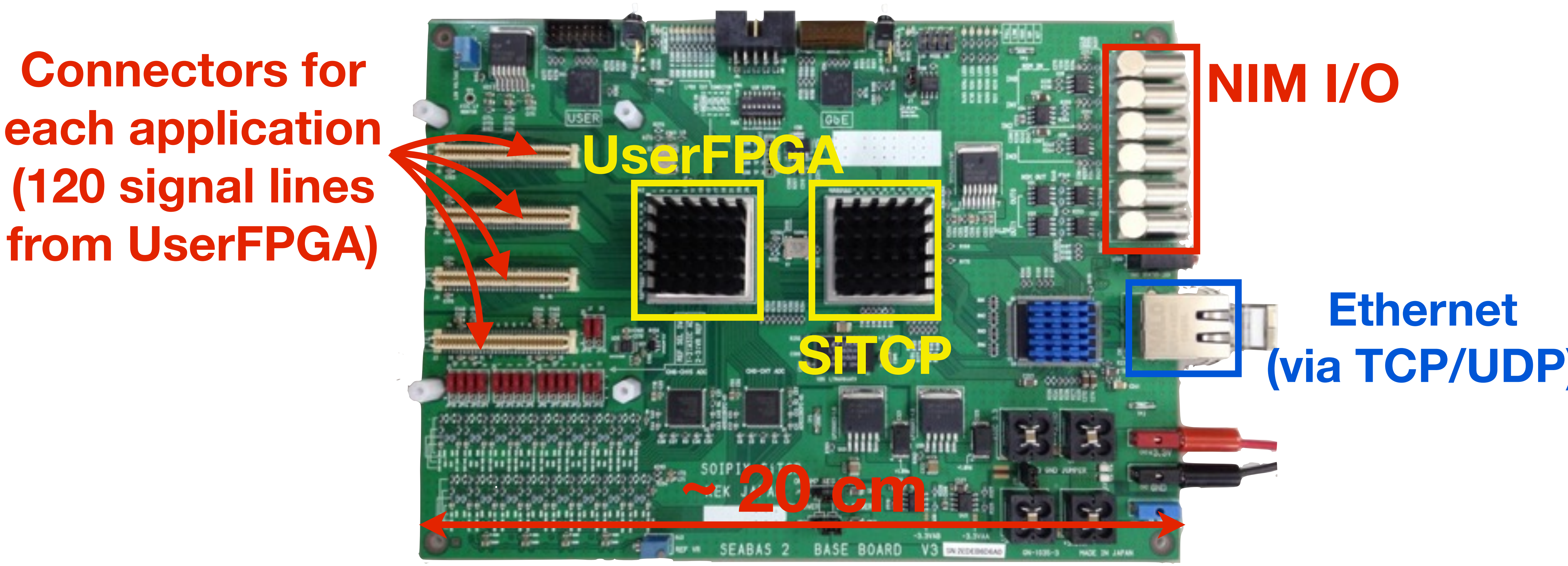
Japanese group is working mainly on this part.



Introduction of the SEABAS board

- SEABAS2: general purpose DAQ board with SiTCP.
  - ➡SiTCP: network processor to communicate with PC.
    Maximum data rate: 1 Gbps.
  - ➡FPGA for each user application.
  - ➡4×NIM_IN, 2×NIM_OUT (trigger, busy etc...).
  - ➡16ch×ADC and 4ch×DAC



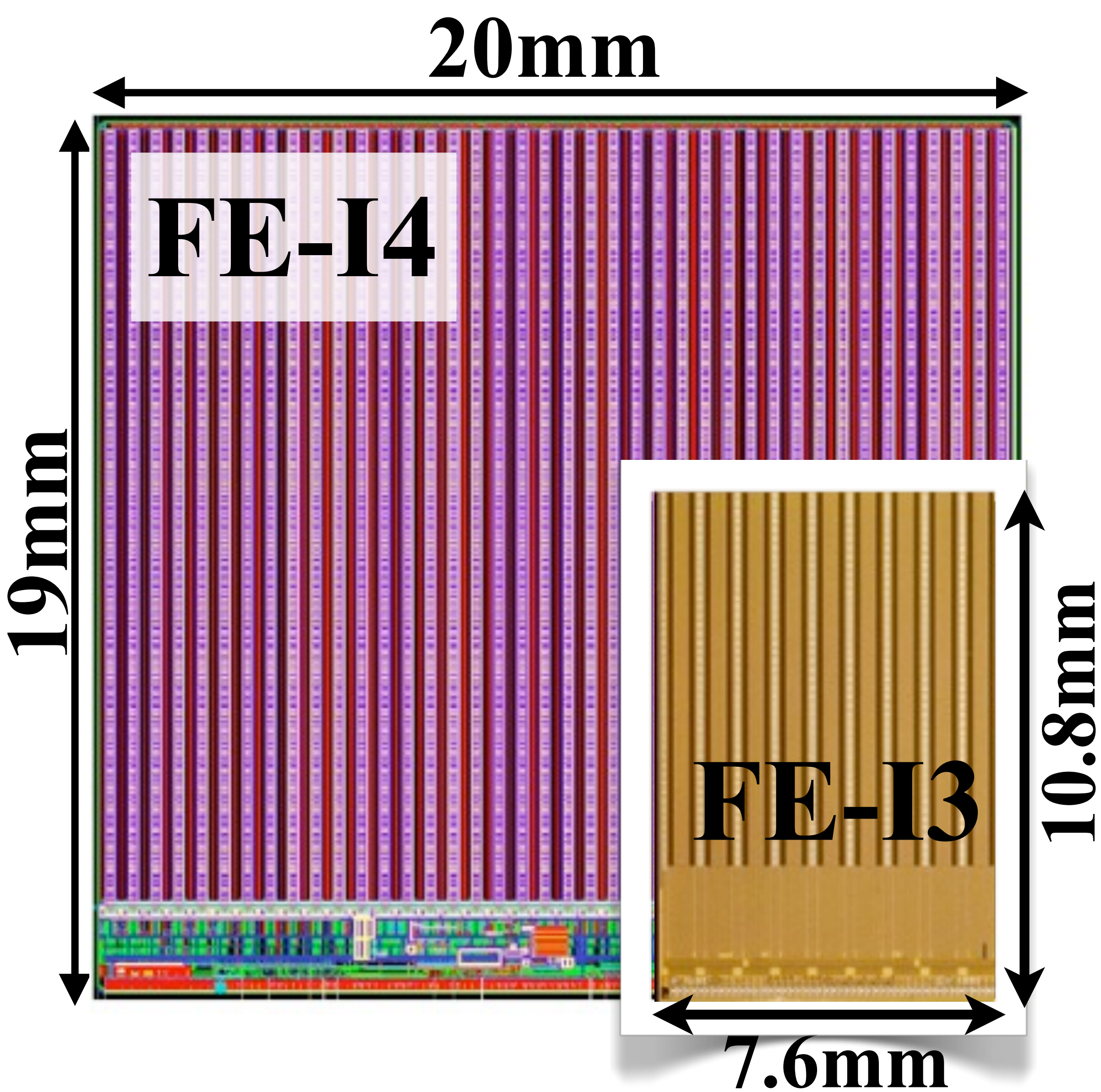
Advantage to use SEABAS

- “Compact” and “versatile” DAQ system.
  - ➡Compact :
    - Don’t need large crates just for testing prototypes...
      - ✓E.g. NIM, CAMAC, VME, ATCA etc...
    - Portable system is preferable.
      - ✓We have to transport the system for the testbeam.
  - ➡Versatile :
    - Have to test new features of the prototype quickly.

SEABAS is one of the good solution !!
- enough data transfer speed.
-enough I/O ports.

Upgrade of the pixel detector

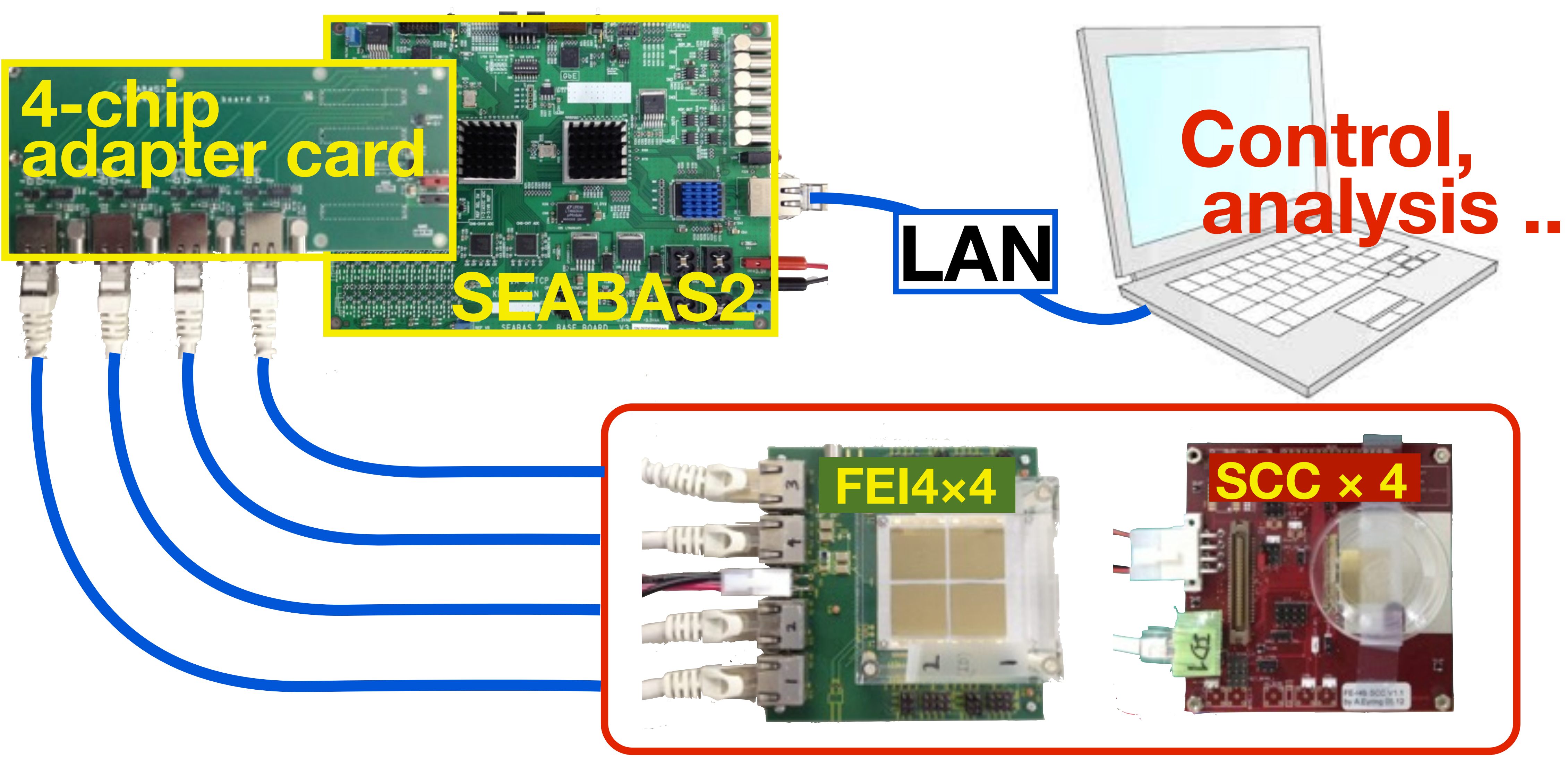
- Readout ASIC: FE-I3 → FE-I4.
  - ➡Smaller pixel size, faster readout speed.
    - To cope with higher hit rate.



	FE-I3	FE-I4
Pixel array	18×160	80×336
Pixel size (um^2)	50×400	50×250
Data rate (Mb/s)	40	160
CMOS process (nm)	250	130

FEI4-SEABAS2 DAQ system

- Can readout up to four FEI4s
  ➡MUX can be used to readout two FEI4s.



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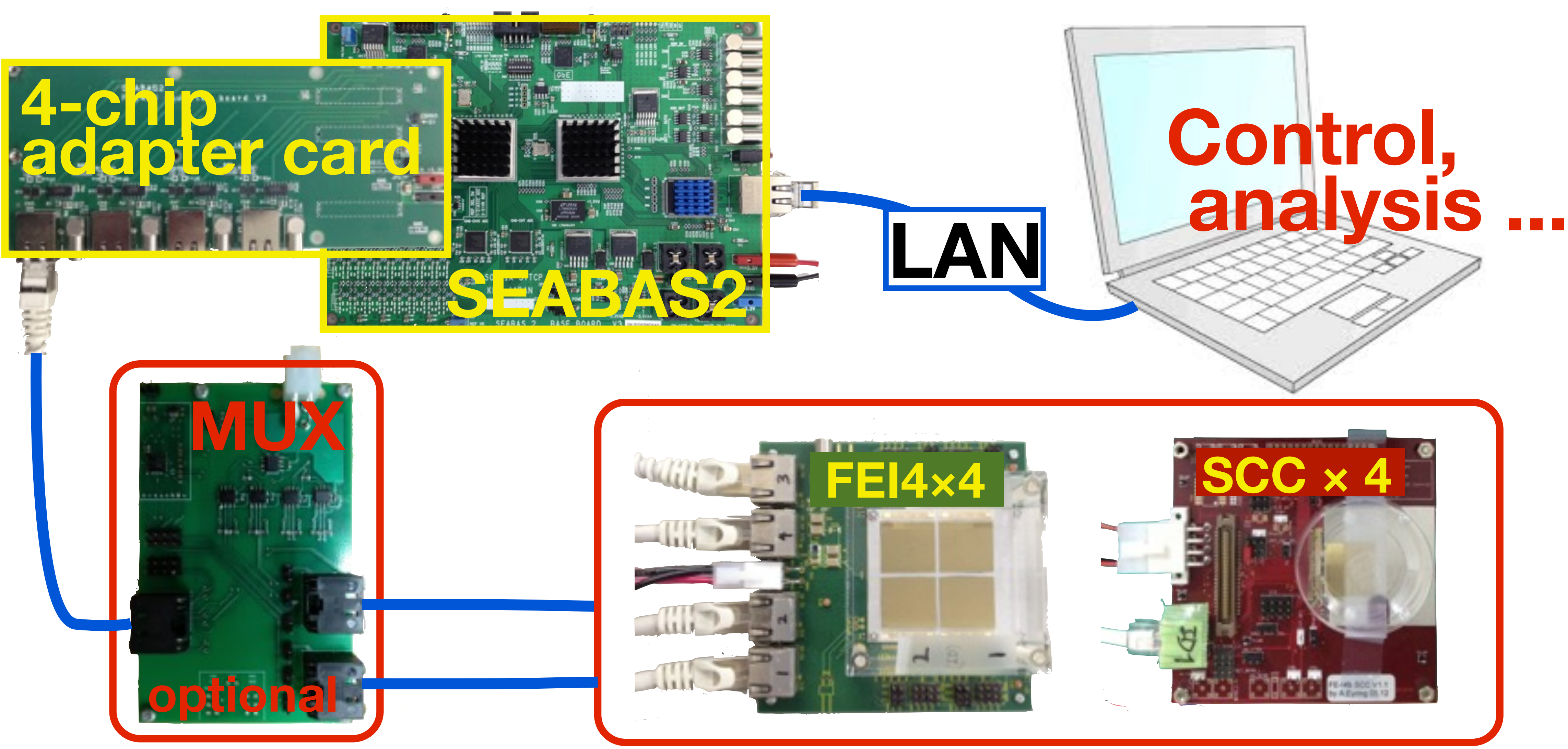
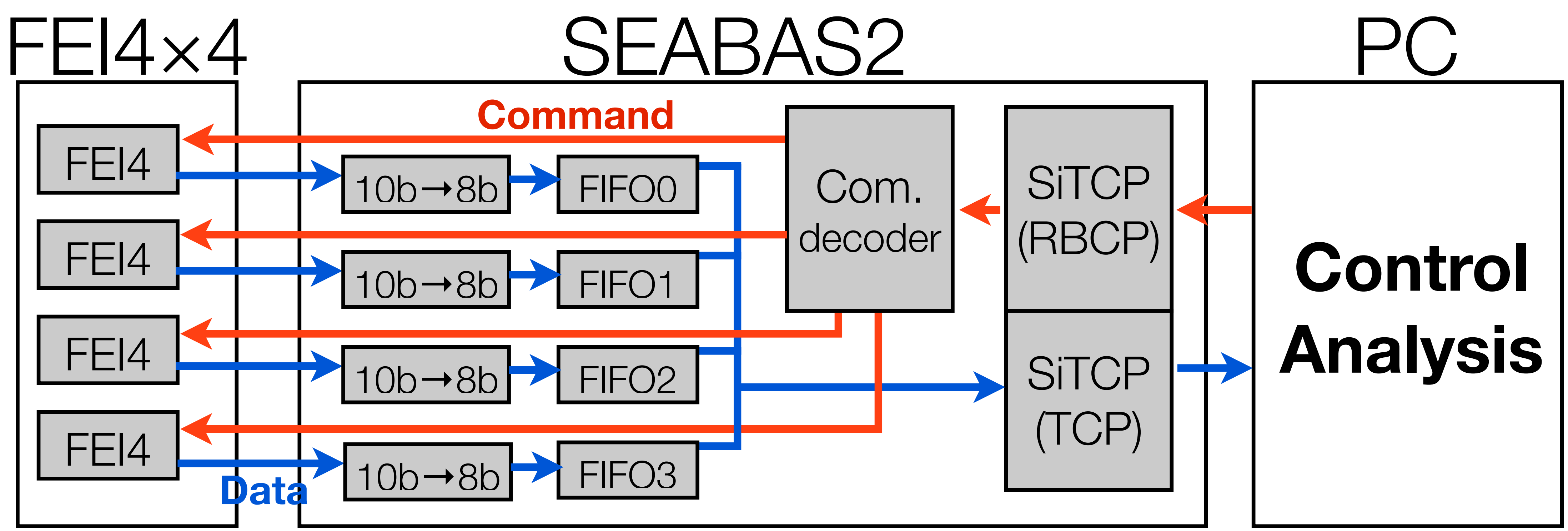
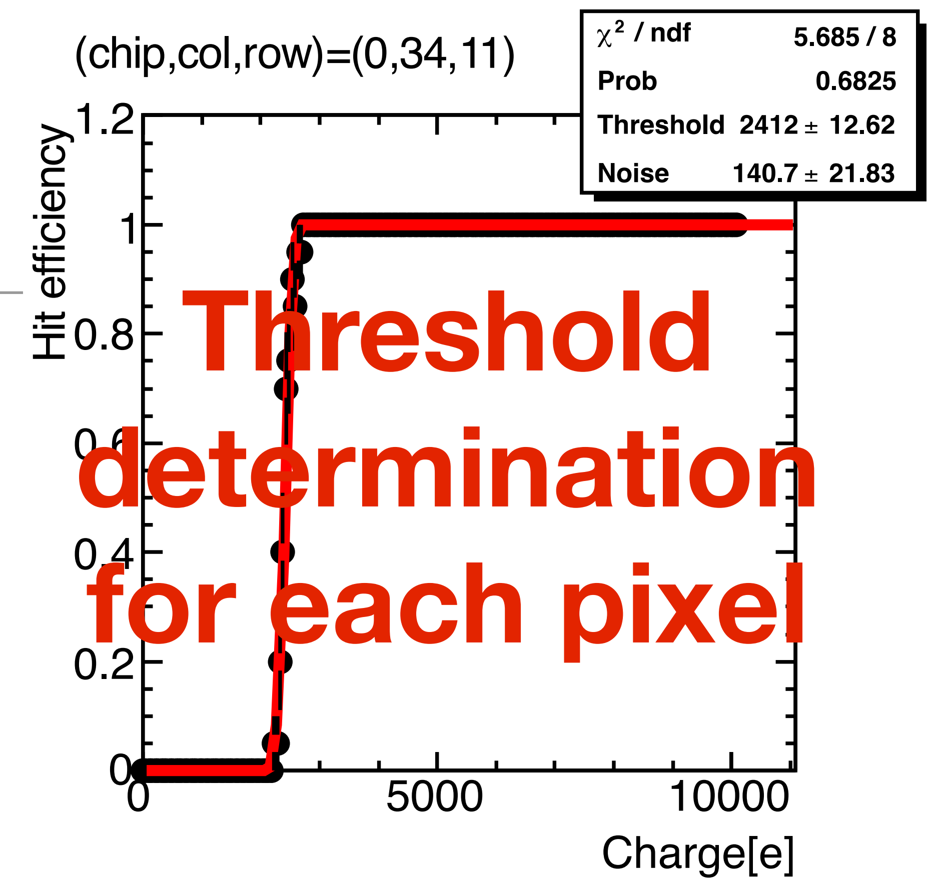


Firmware design

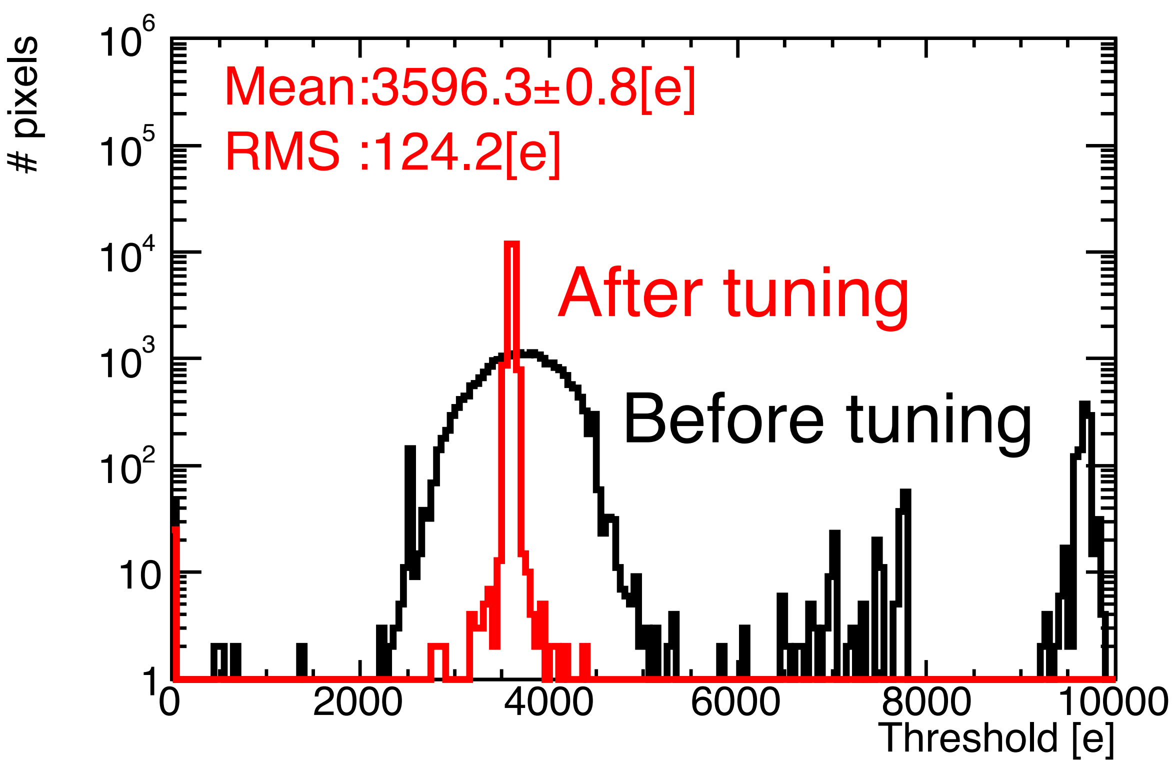
- To make flexible DAQ system
  - ➡Only provide the interface for <u>ten FEI4 commands</u>.
    - e.g. LV1Trigger, CalibrationPulse, WrRegister etc...
  - ➡All meaningful data from FEI4s are sent to PC.
- All operation can be done by software coding.
  - ➡Relatively easy for non-DAQ expert to test new things.

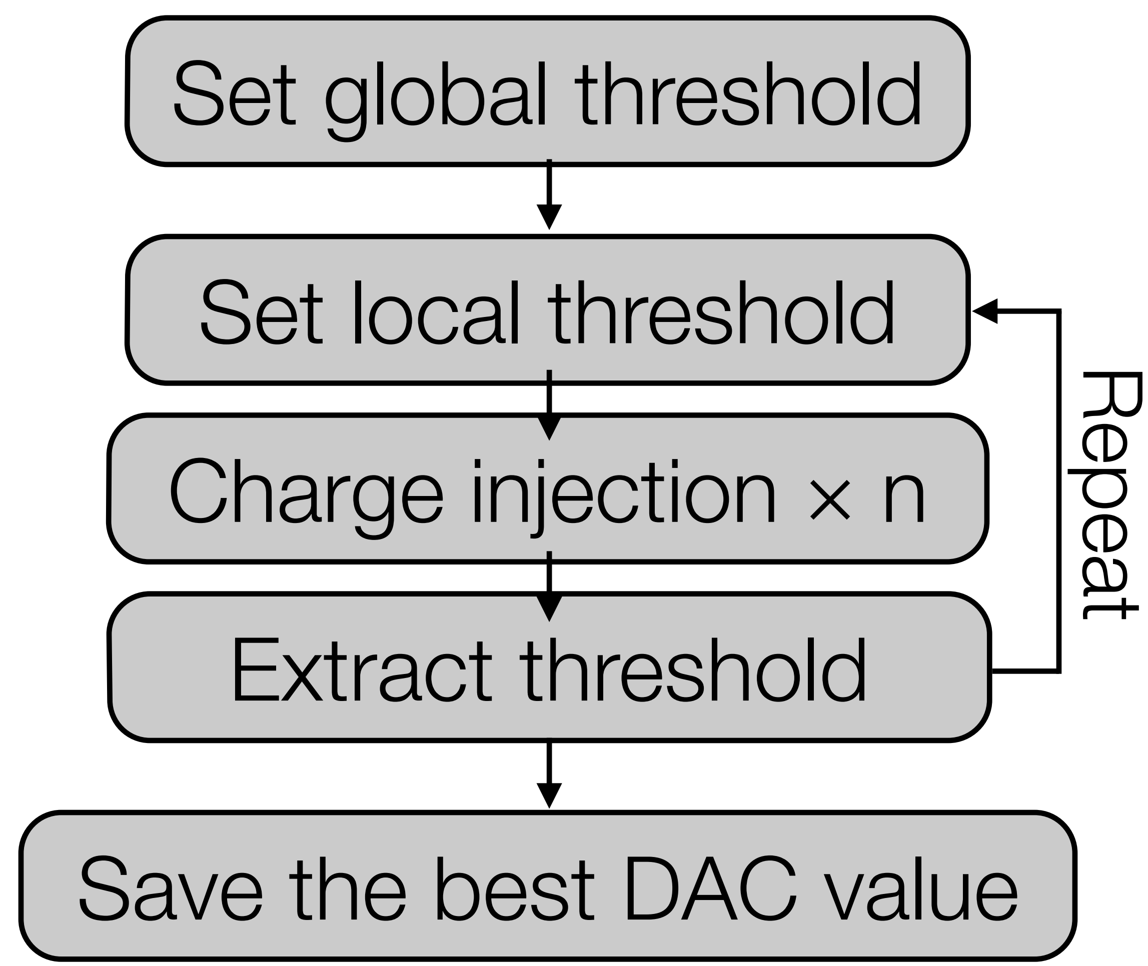


Example: threshold tuning



- To set same threshold among pixels.
  ➡Good example of the operation
  - Needs global configuration.
  - Needs pixel local configuration.
  - Charge injection
  - etc...

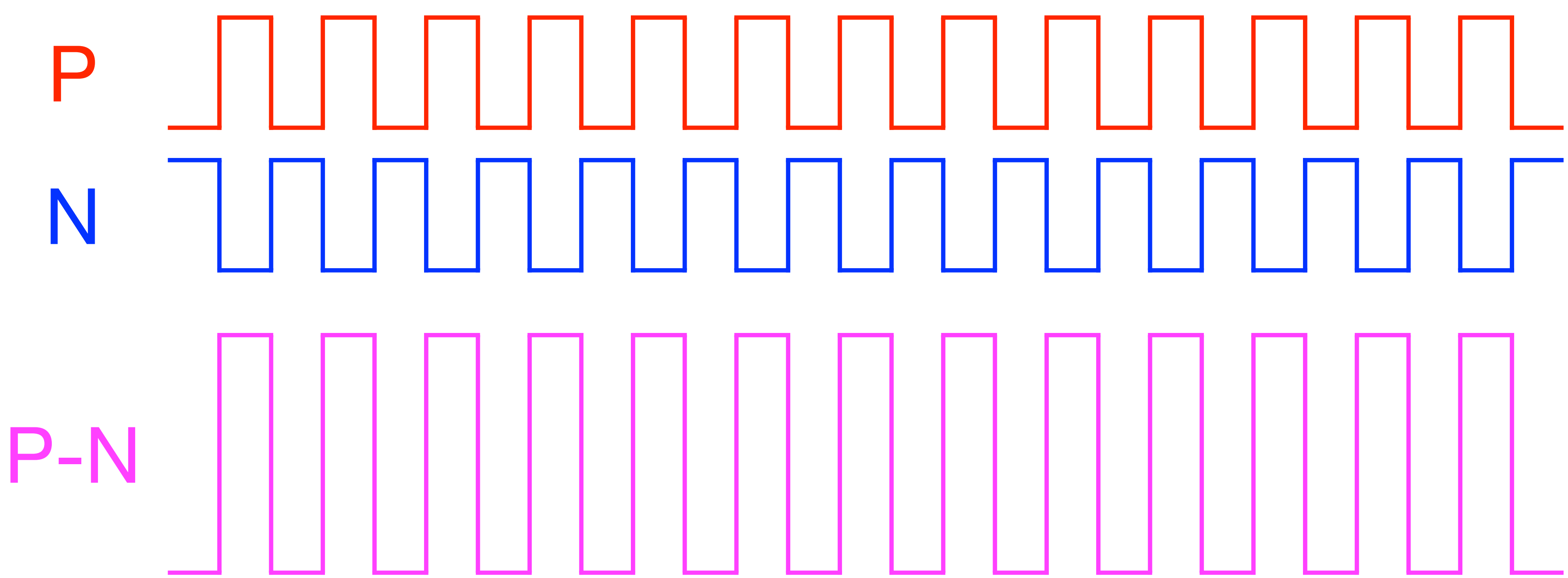




Problems & Solusions

Differential Signaling

- FEI4 Interface: “Custom” SLVS
  - ➡ SLVS? → Scalable Low Voltage Signaling
    - ✓ Derived standard of LVDS (differensial signal standard).
- Differential signaling
  - ➡ Suit for long distance signal transmission.



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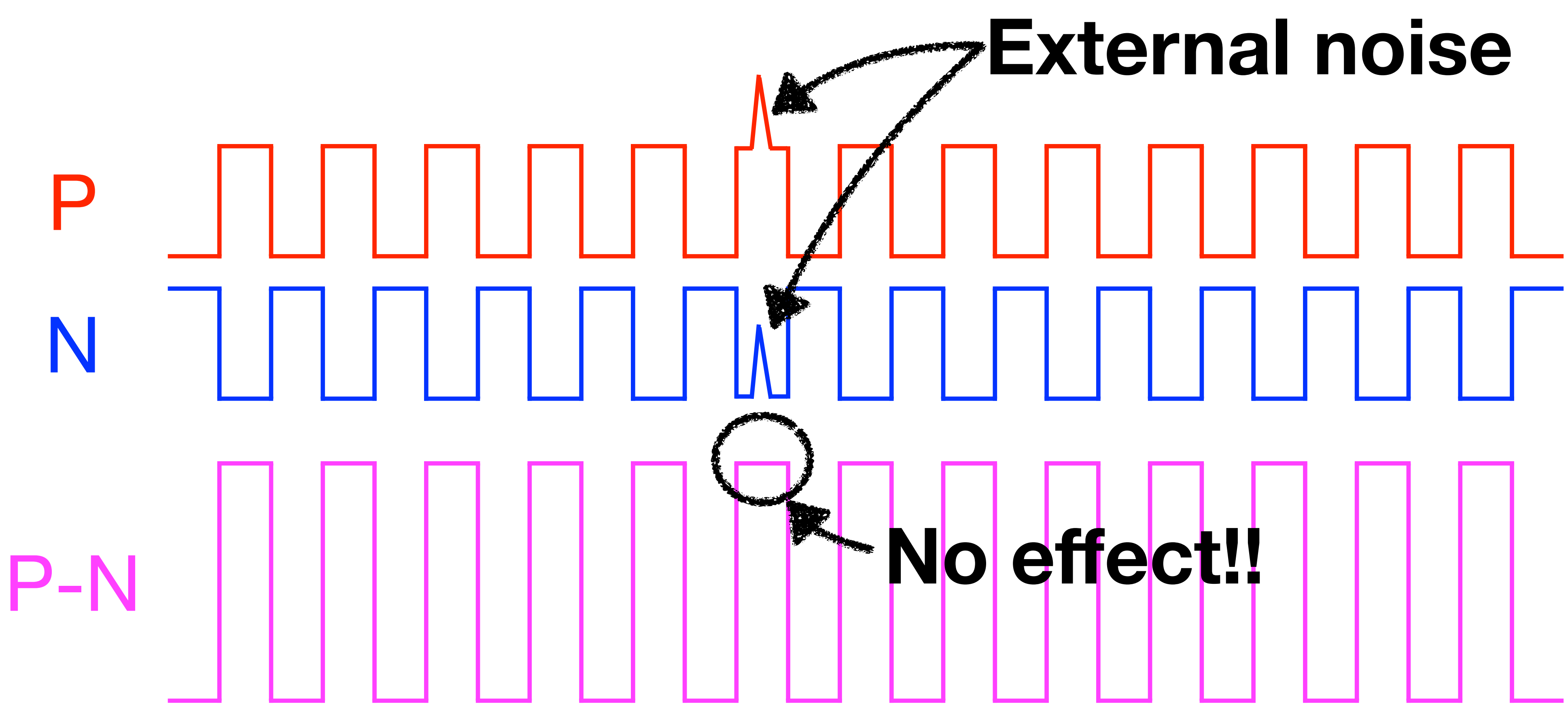

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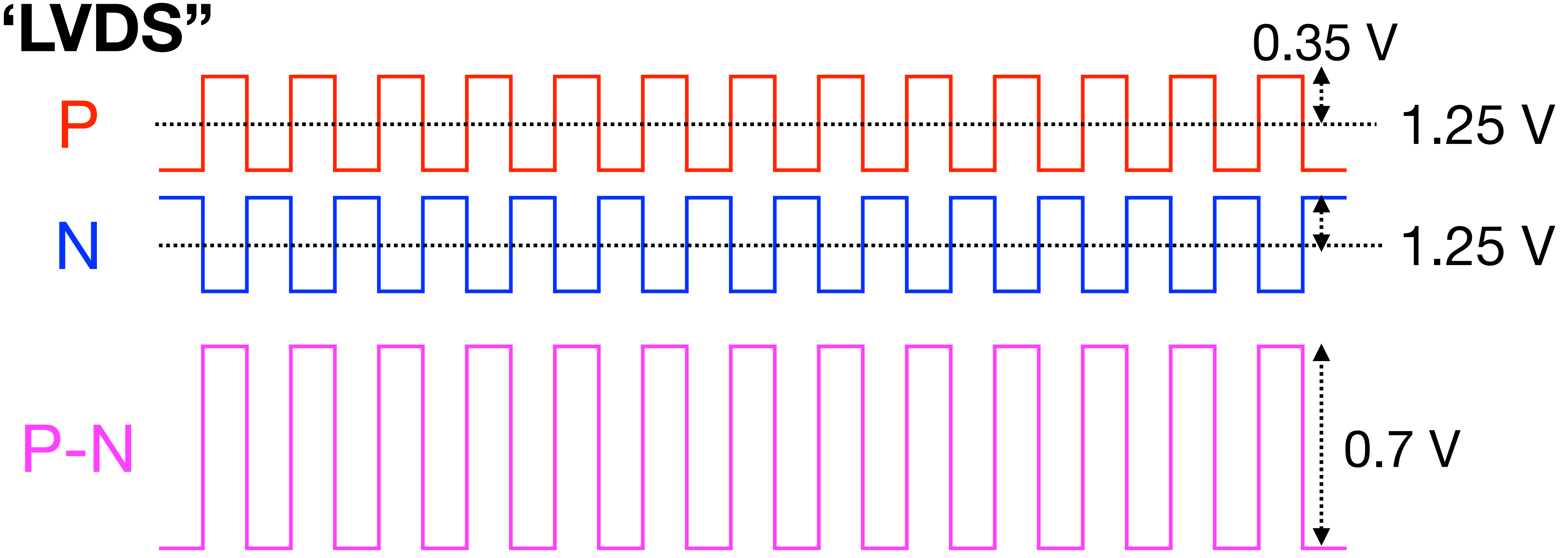
“LVDS”



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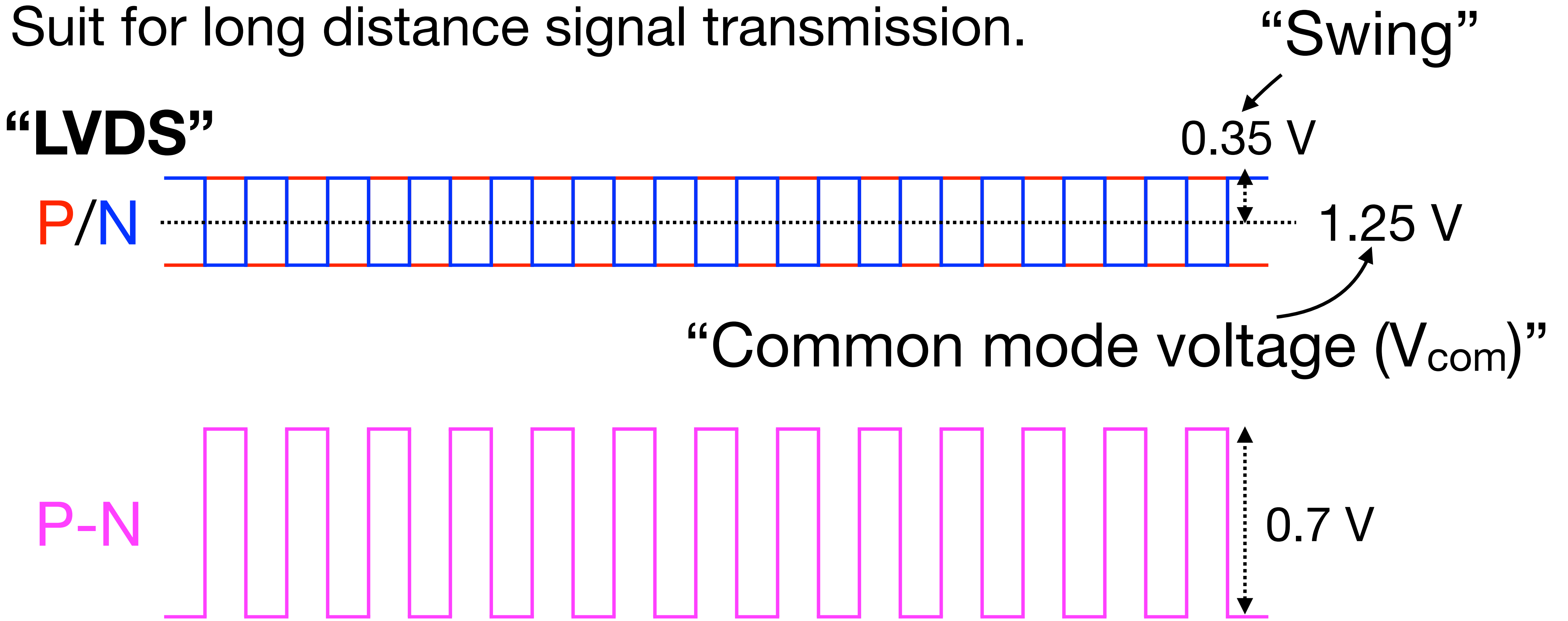

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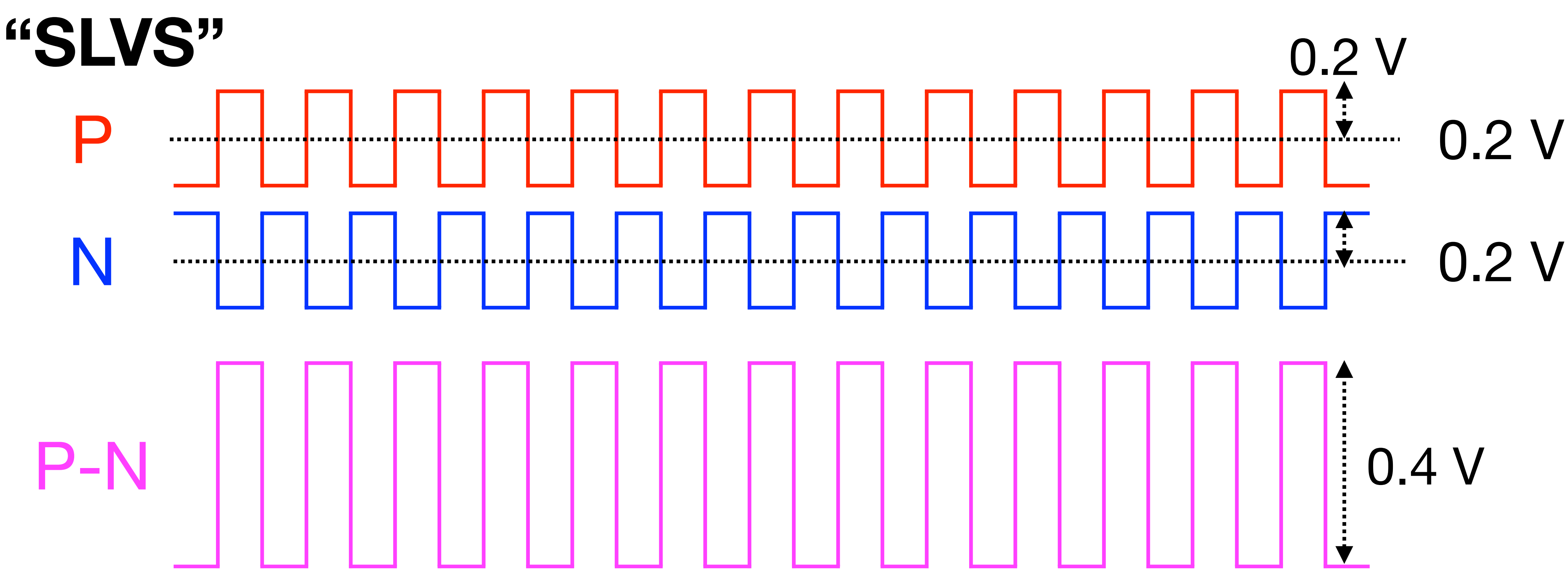

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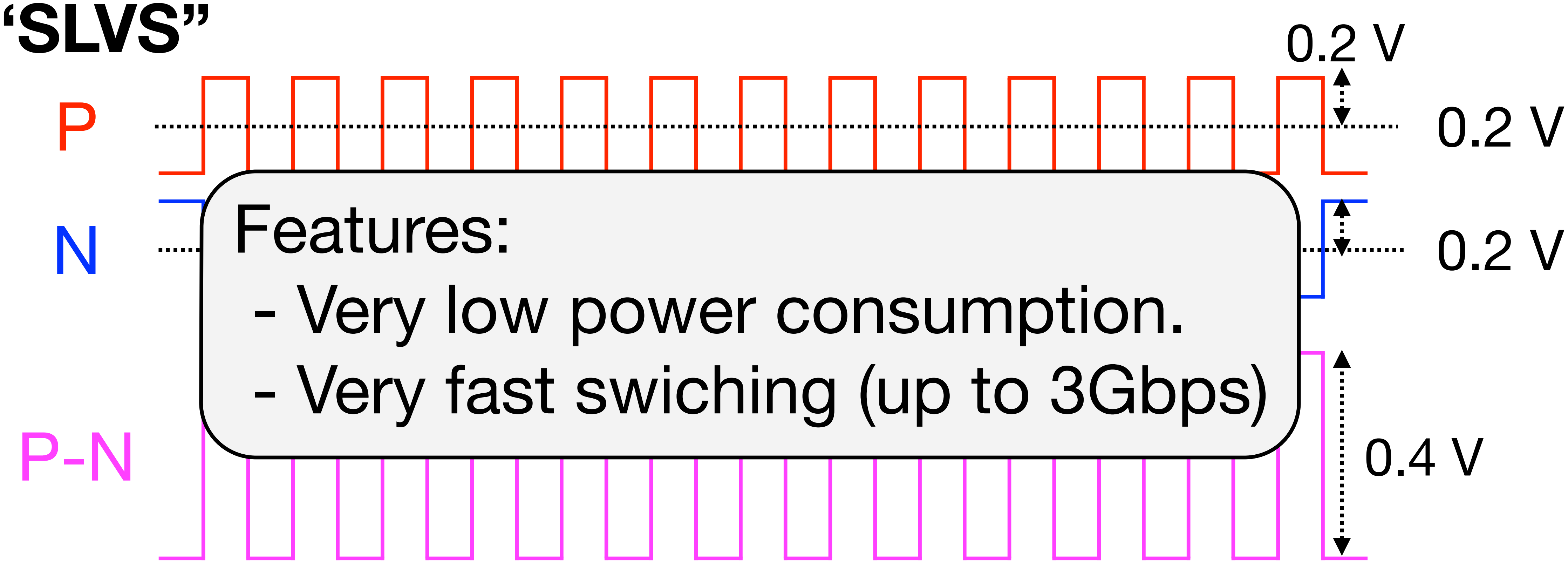
“SLVS”



Features:
- Very low power consumption.
- Very fast swiching (up to 3Gbps)

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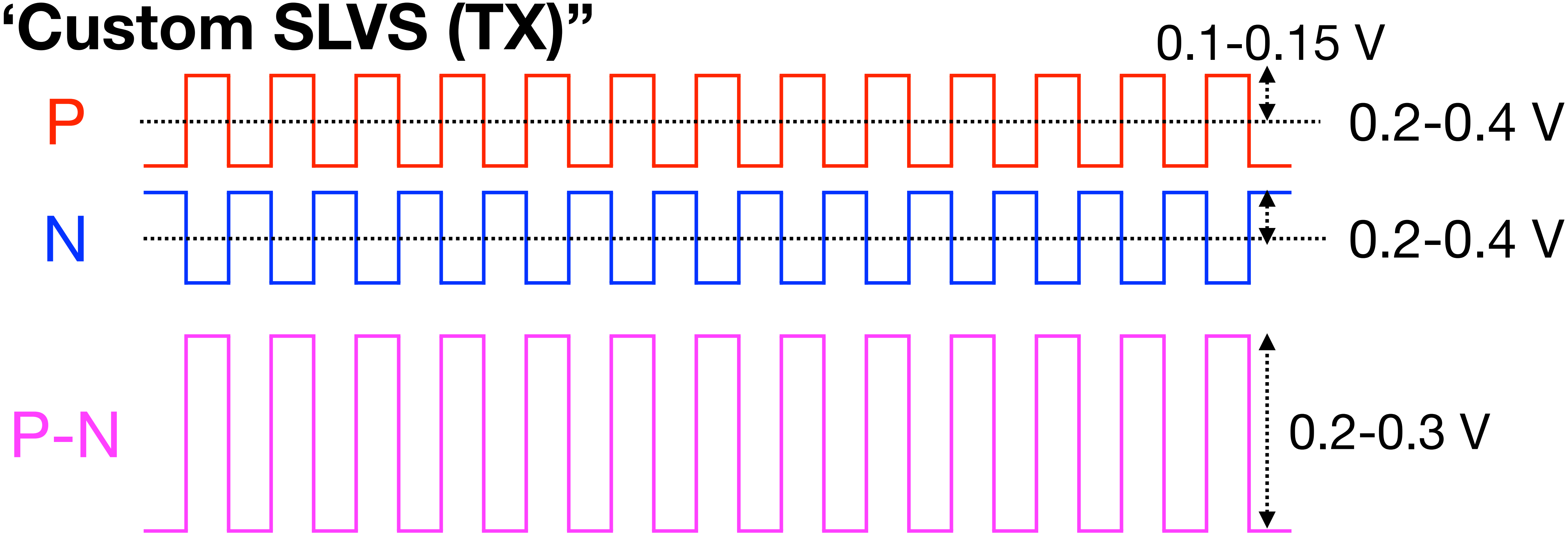
“Custom SLVS (TX)”



Differential Signaling

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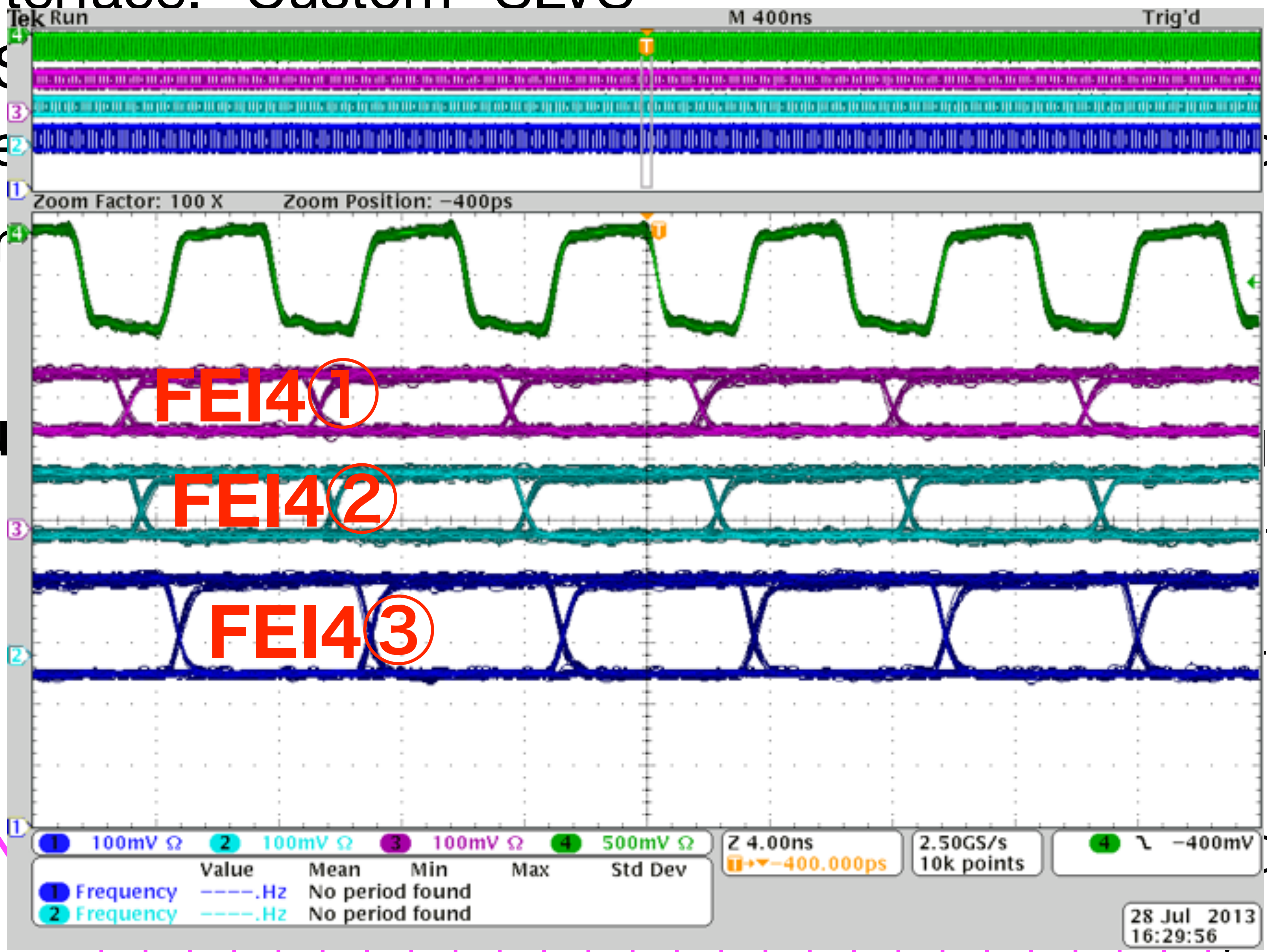
  - ➡ SLVS
    - ✓ De … dard).
- Differen
  - ➡ Suit

“Cu … 5 V

P … 0.2-0.4 V

N … 0.2-0.4 V

P-N … .2-0.3 V



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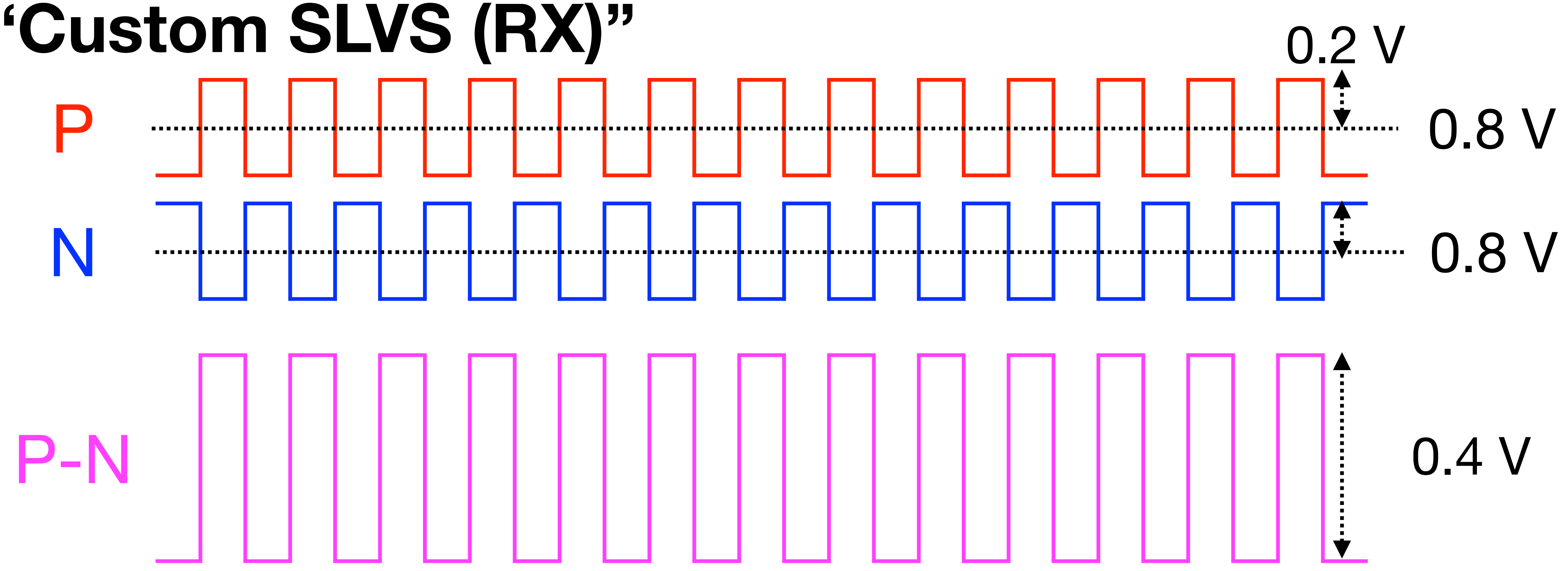
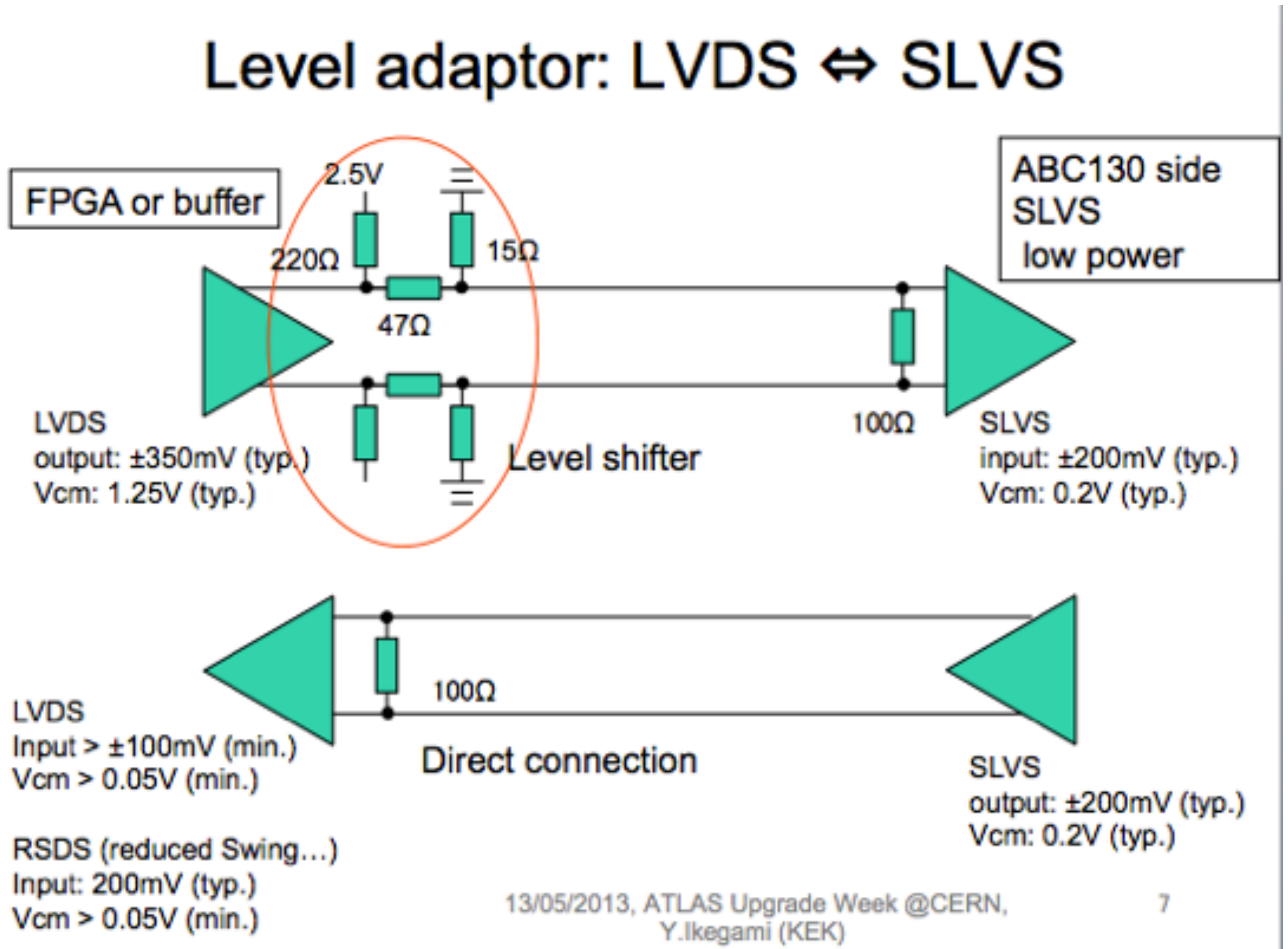
“Custom SLVS (RX)”



How to use SLVS with FPGA?

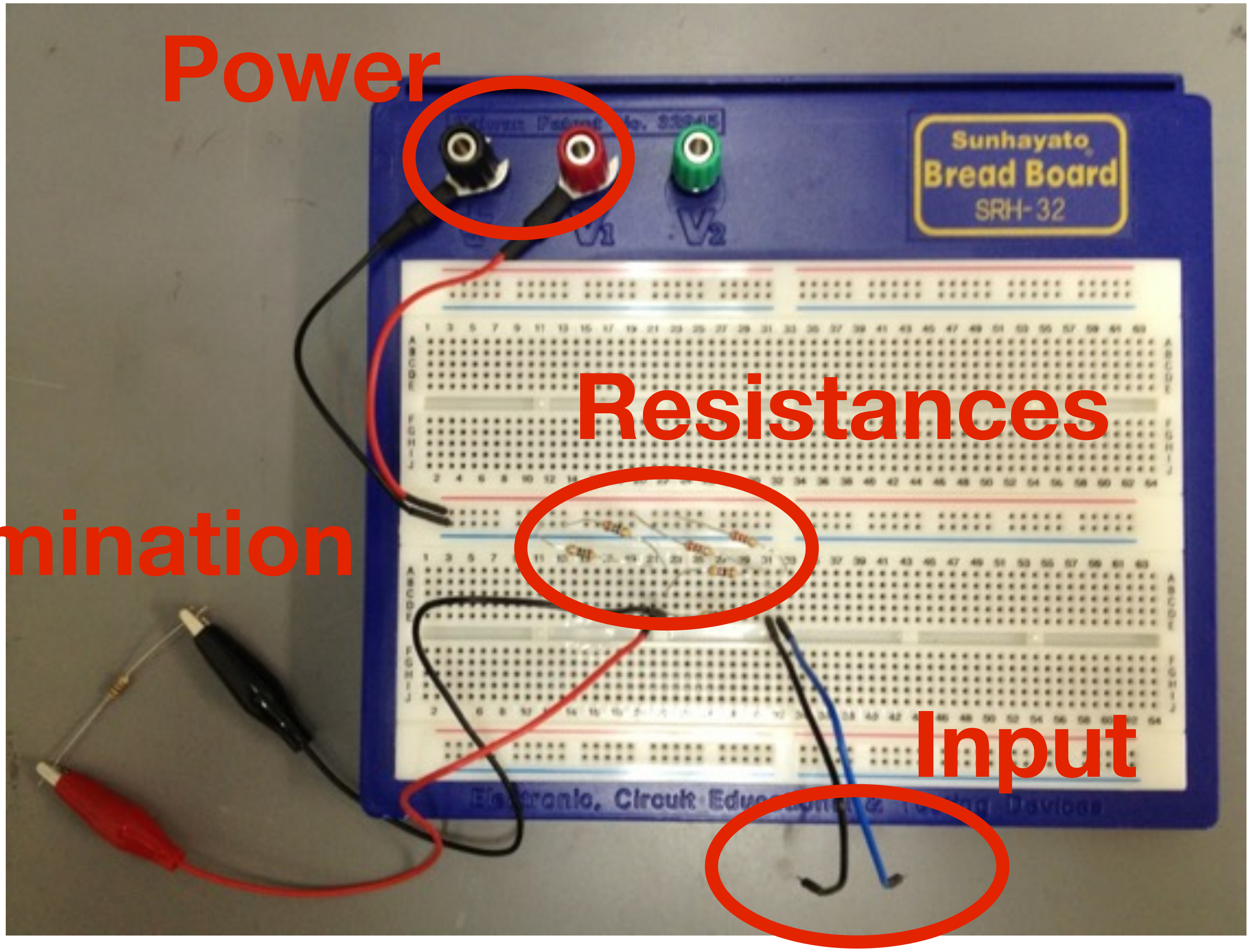
- No SLVS support by Virtex-5.
- Needed to prepare a level adaptor.
  ➡ Ref.: http://ednjapan.com/edn/articles/1109/20/news120.html



Slides from Y. Ikegami

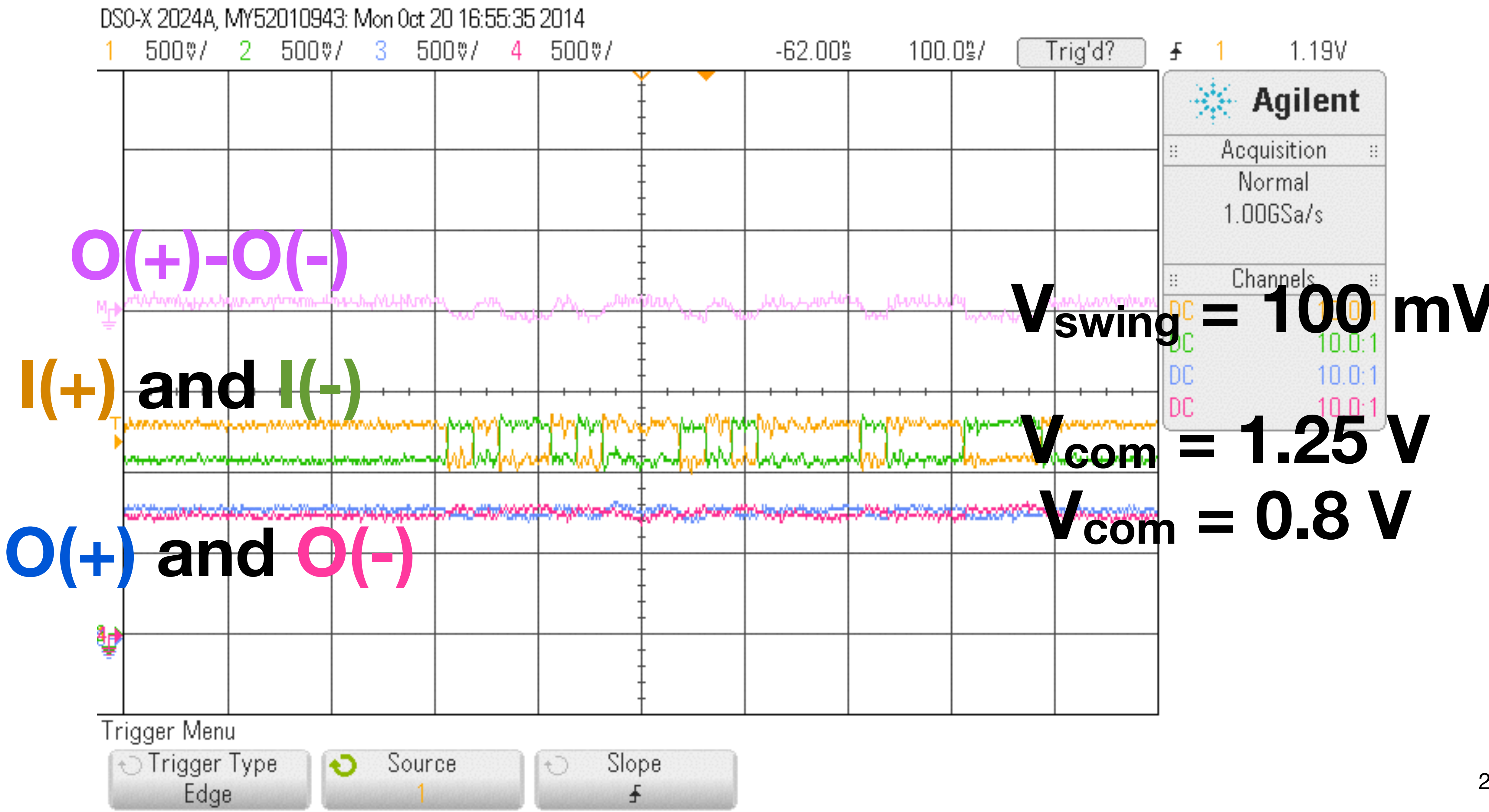
Test with the proposed design

- Functionality test with a bread board.



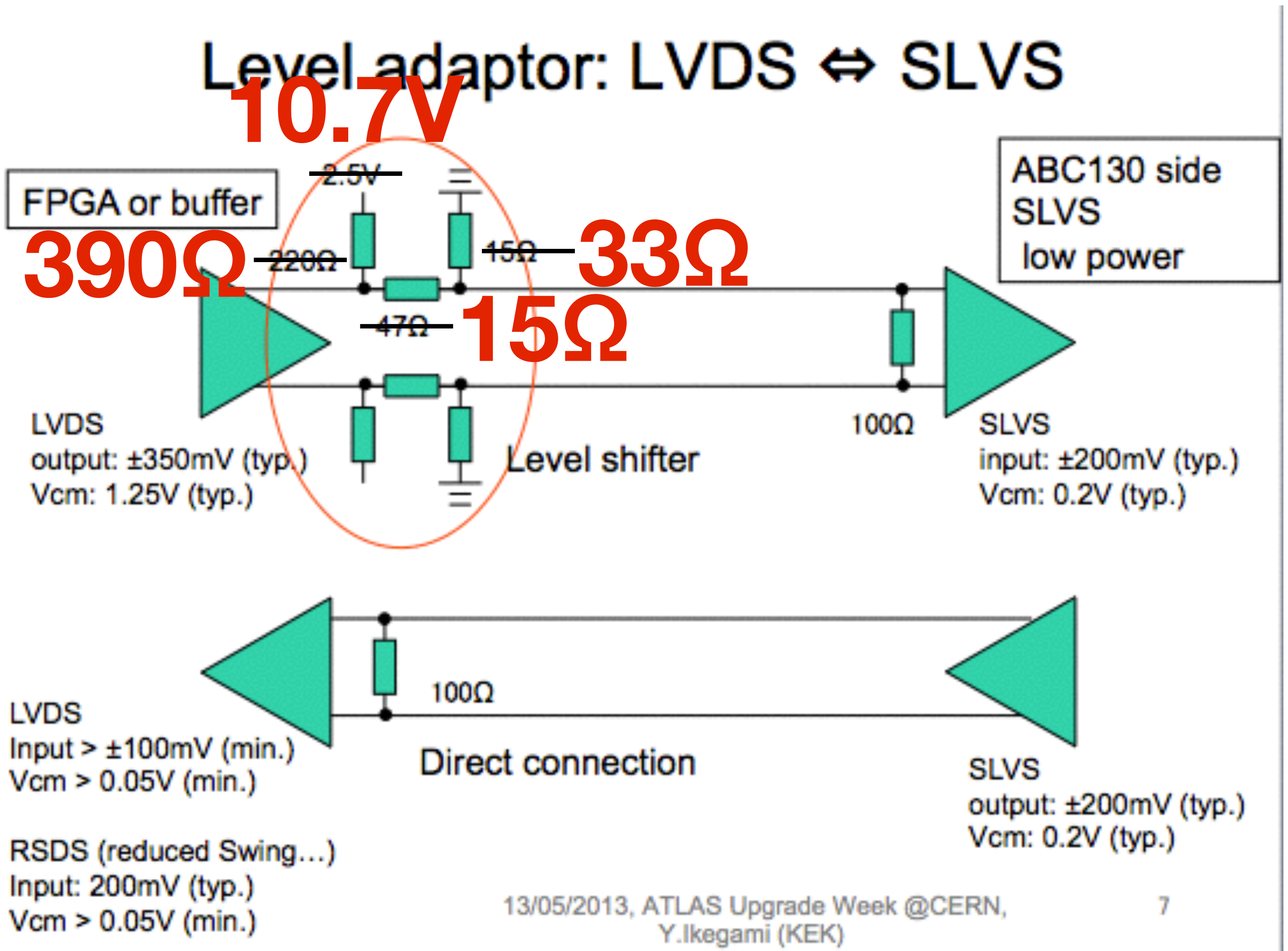
Result①

- I could adjust V_{com} to be 0.8 V.
  - ➡But swing seems to be too small (Diff. signal looks unclear).



Changing the resistances

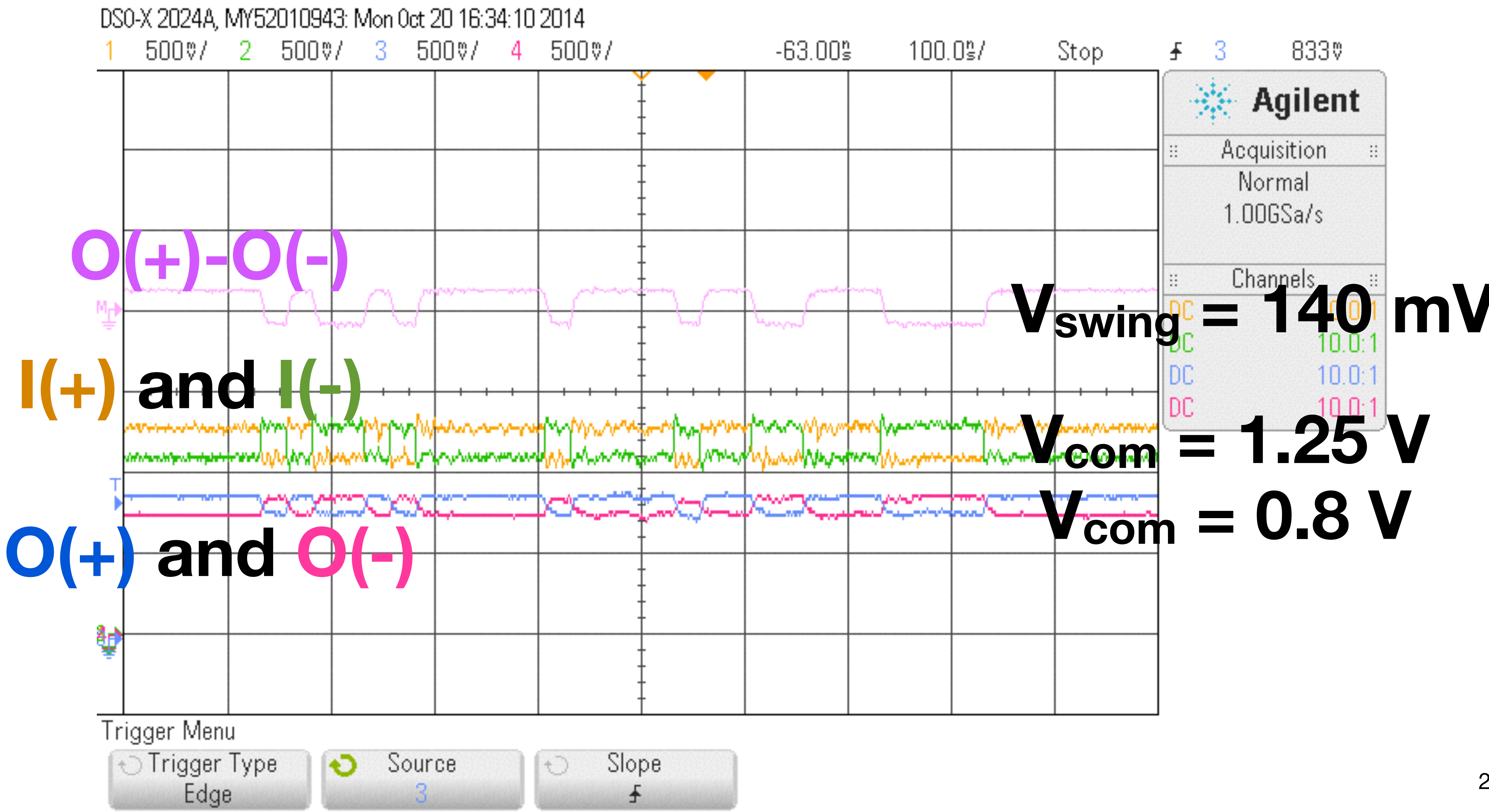
- Picked-up values are determined by trial and error.



Slides from Y. Ikegami

Result②

- V_{com} adjusted as 0.8 V.
  ➡Much clear High/Low separation.



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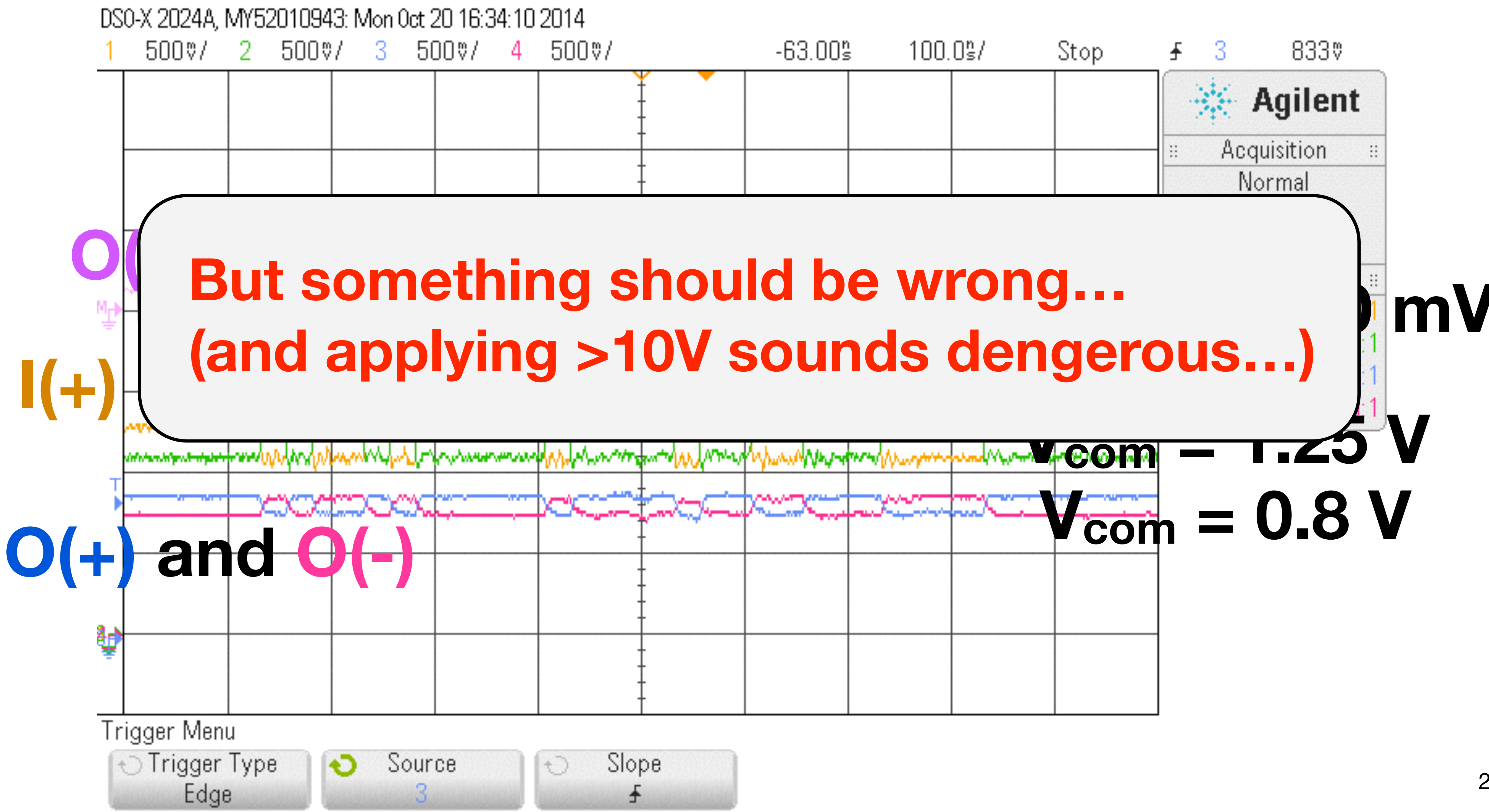
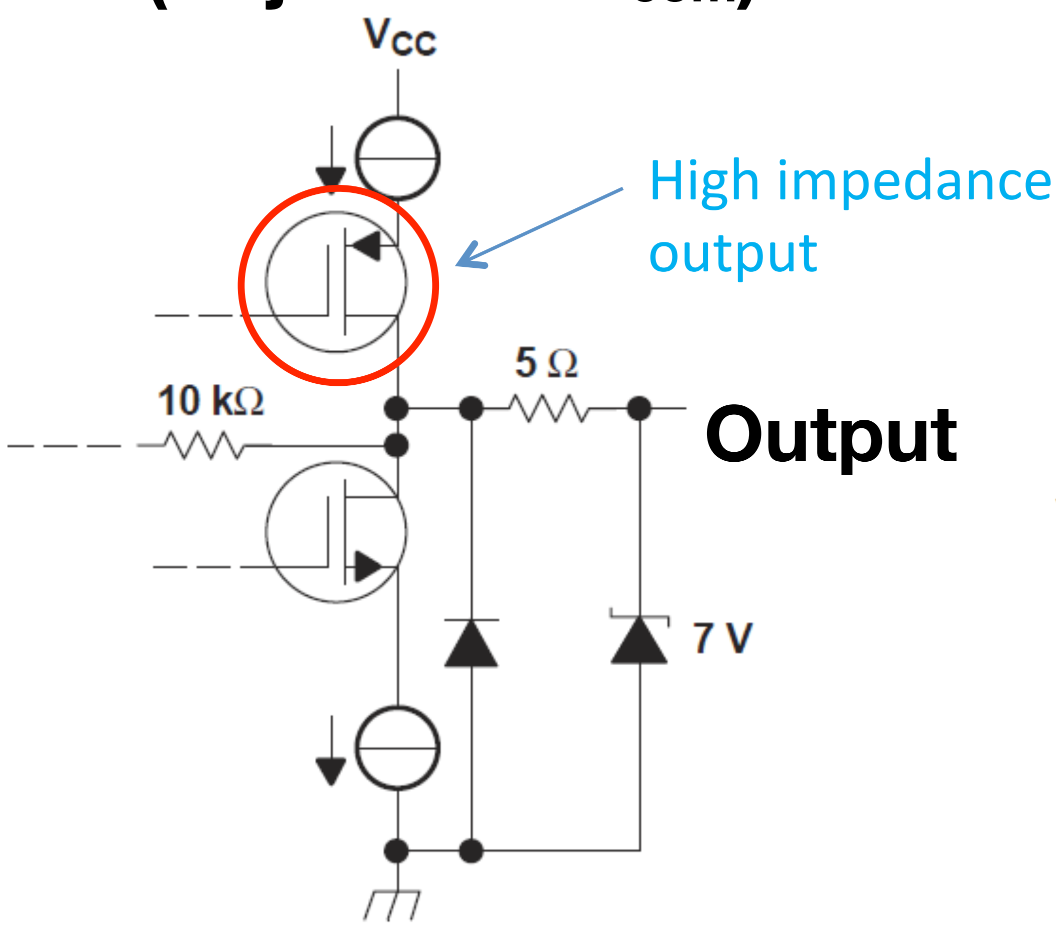


But something should be wrong…
(and applying >10V sounds dengerous…)

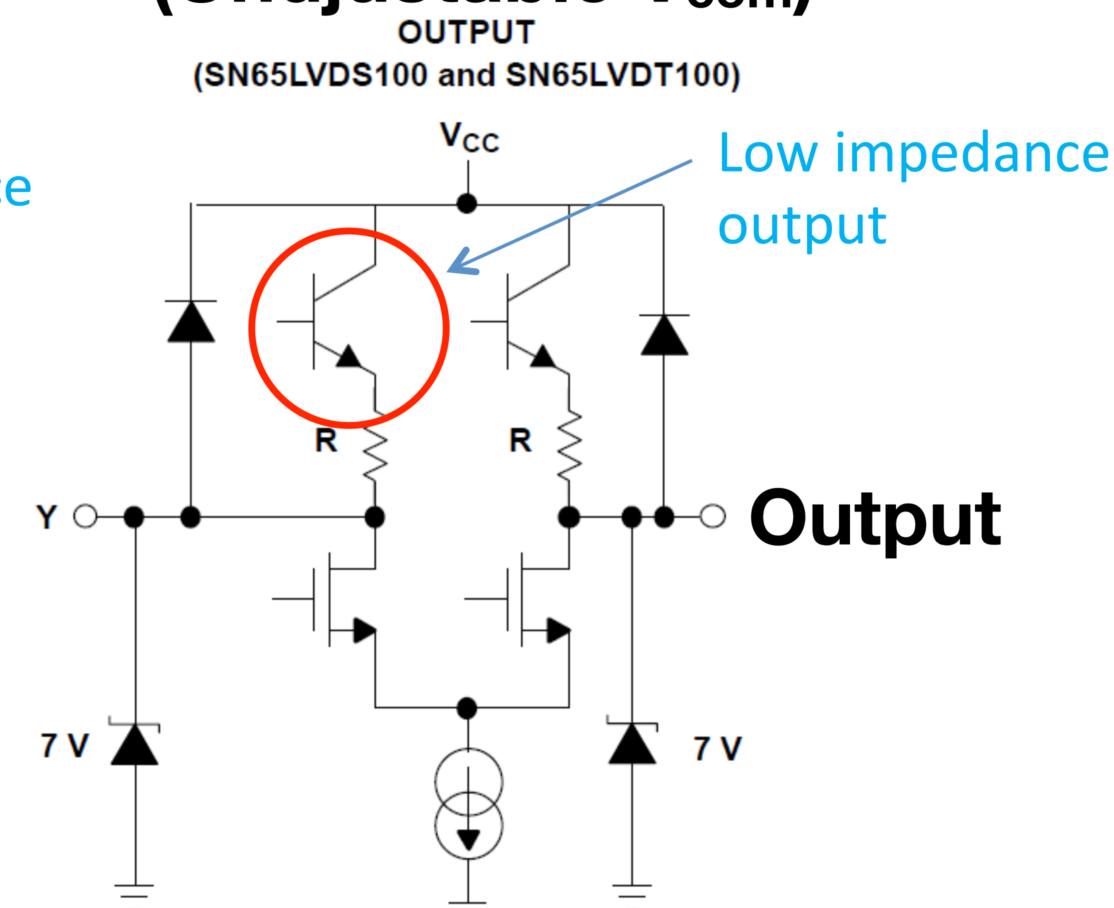
Level shifter

- The problem apparently comes from buffer circuits.

sn65lvds051d (Adjustable V_{com})



sn65lvdt100dgk (Undjustable V_{com})

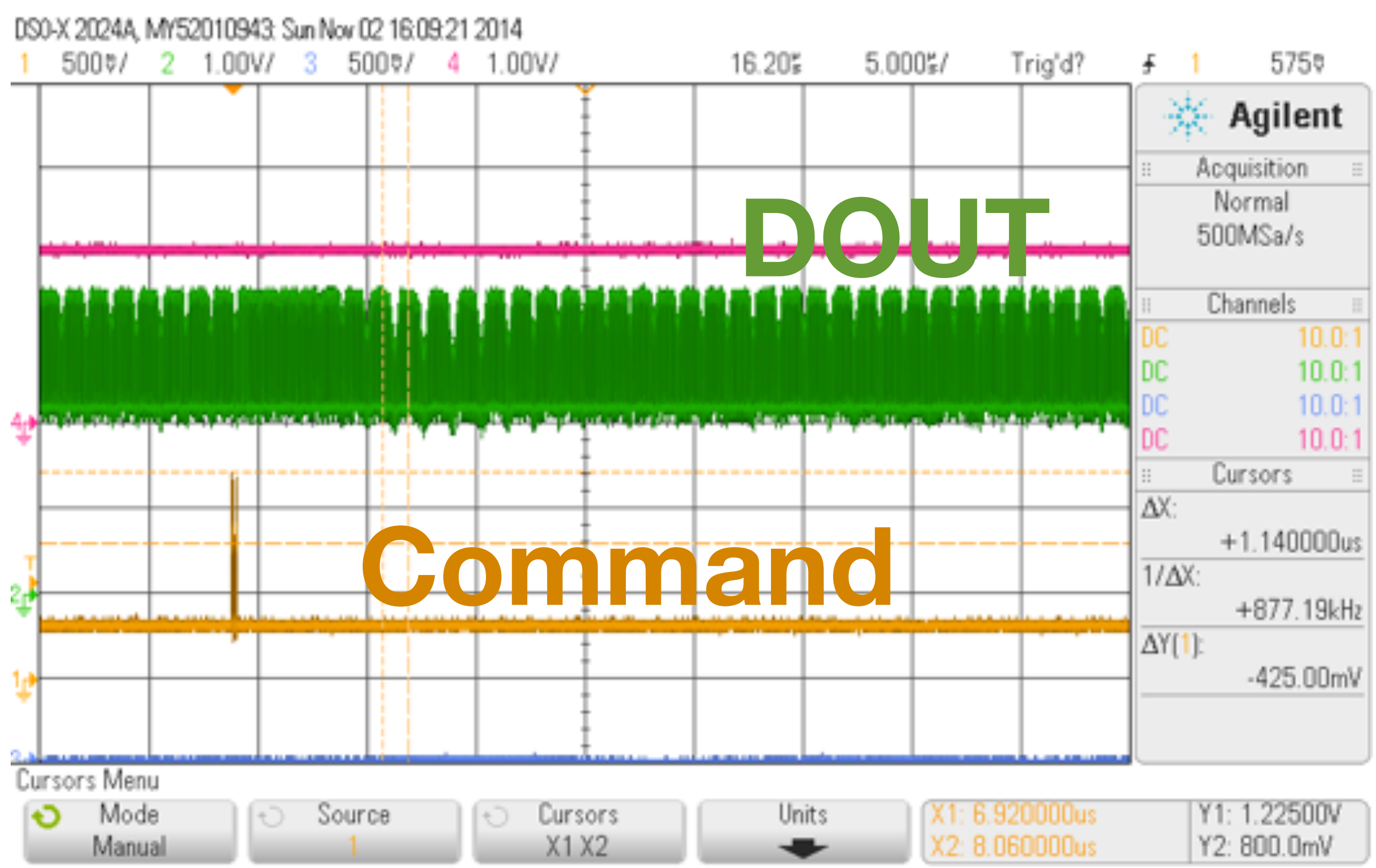


Picture from Y. Ikegami

Lesson: check equivalent circuit for ASIC when encountering problem…

Final (tentative) solution

- Succeeded to lowering the common level of the diff. signal.
  - ➡Output signals with the “HT_25” standard.
    - HyperTransport: V_{com} ~ 600 mV, V_{swing} ~ 400 mV.
- Another problem arised…: periodical “dips” on output data from FEI4.
  - ➡Disappear when $V_{digital}$>1.3 V (←Nominal value=1.2 V).
  - ➡Caused by larger V_{swing} than SLVS?



ISERDES

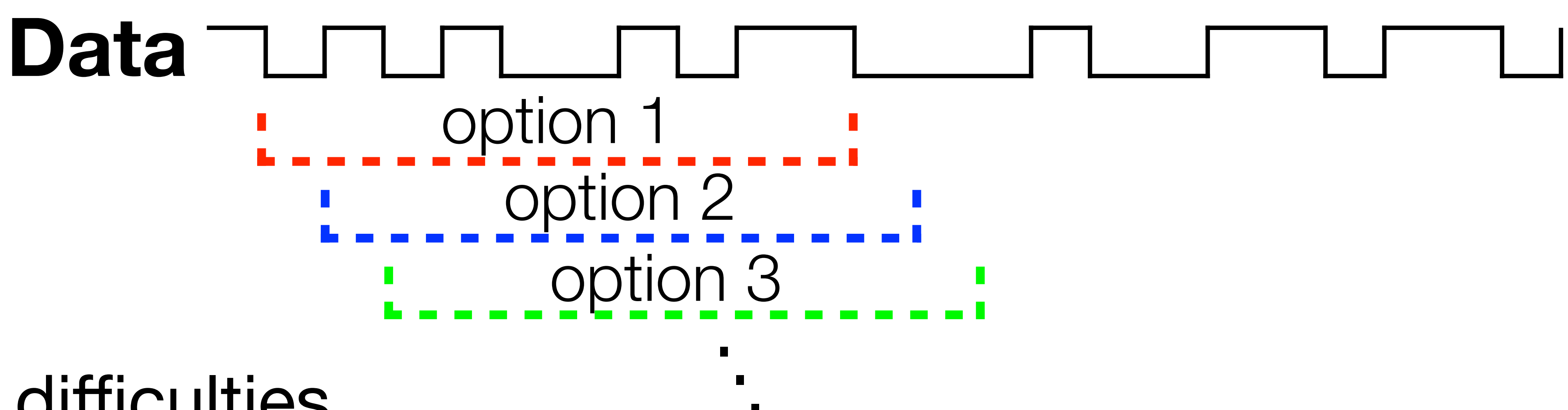
Firmware problem

- Compilation succeeds but sometimes the firmware don’t work.
  - ➡Even though we don’t change anything (e.g. only adding a comment line.).
  - ➡Working ISE project might not work at other sites (LBL etc..).
  - ➡This suggests there might be a timing issue in FPGA.
    - Caused by a delay of signal routing etc...

- To get rid of the timing problem inside FPGA completely.
  - ➡Adopting built-in deserializer (160 MHz --> 16 MHz).
  - ➡Could get easier to design the firmware in terms of timing.
    - Used to use 480 MHz to deserialize 160 MHz data stream.
    - Timing margin gets larger by a factor 30.

Built-in deserializer

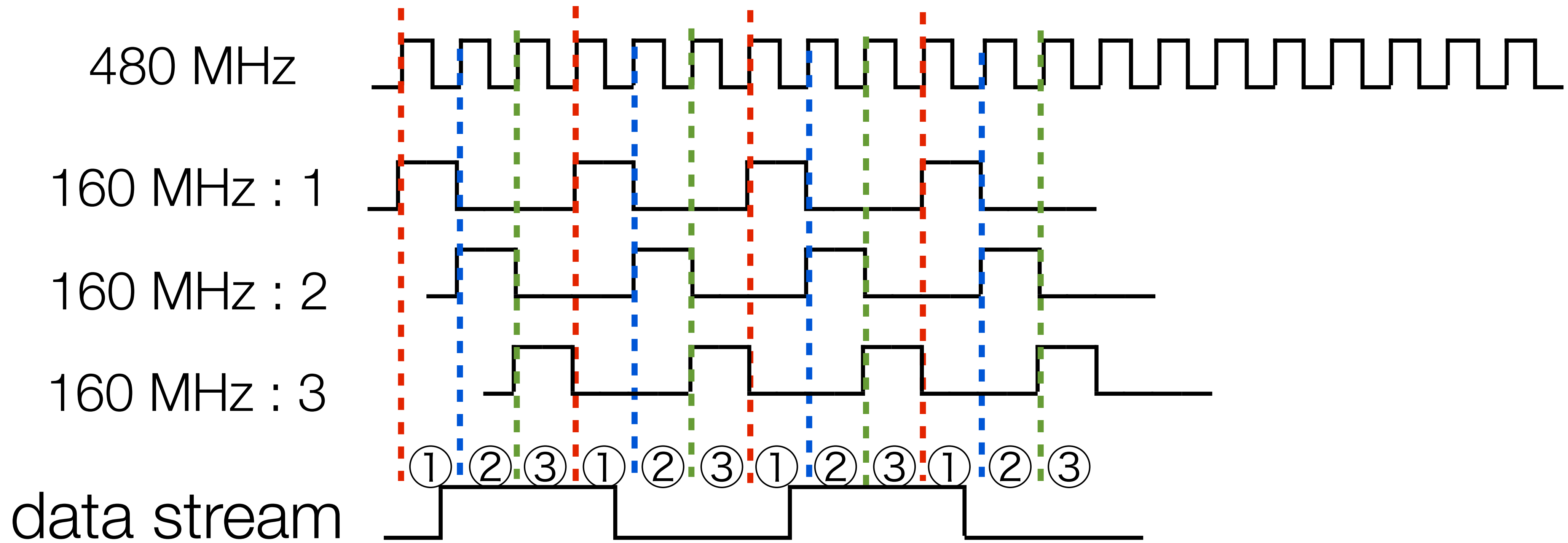
- ISERDES (Input SERializer/DESerializer) + IDELAY + BITSLIP
  - ➡ISERDES: Fast deserializer up to 644 MHz
    (1:10 parallelize is possible for Virtex5)
  - ➡IDELAY: Precise signal delay
    (Range : (0-63)×76 ps ~ 4.8 ns)
  - ➡BITSLIP: Word alignment function



- Some difficulties…
  - ➡Training bit pattern: 20 bits long.
  - ➡Serial data speed: 160 MHz (i.e. 1CLK=6.25ns)

Data clock alignment

- Old : choose the best clock by finding data edges
  by triple over-sampling.

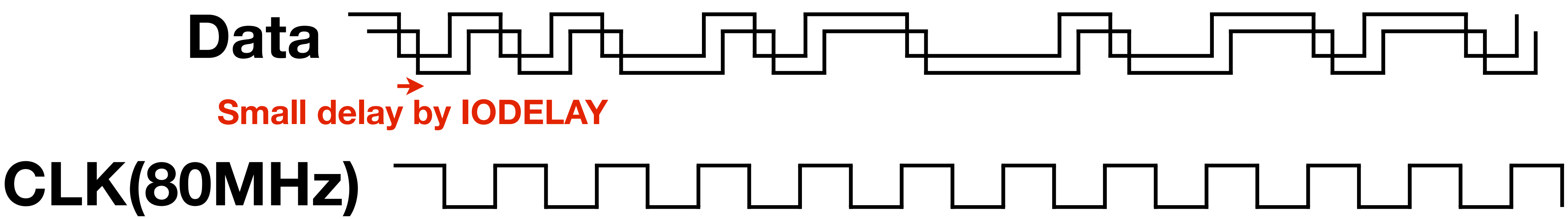


➡Problem :

- Clock is selected depending on the data timing.
- Gated clock is generated → Worsen the clock quality.

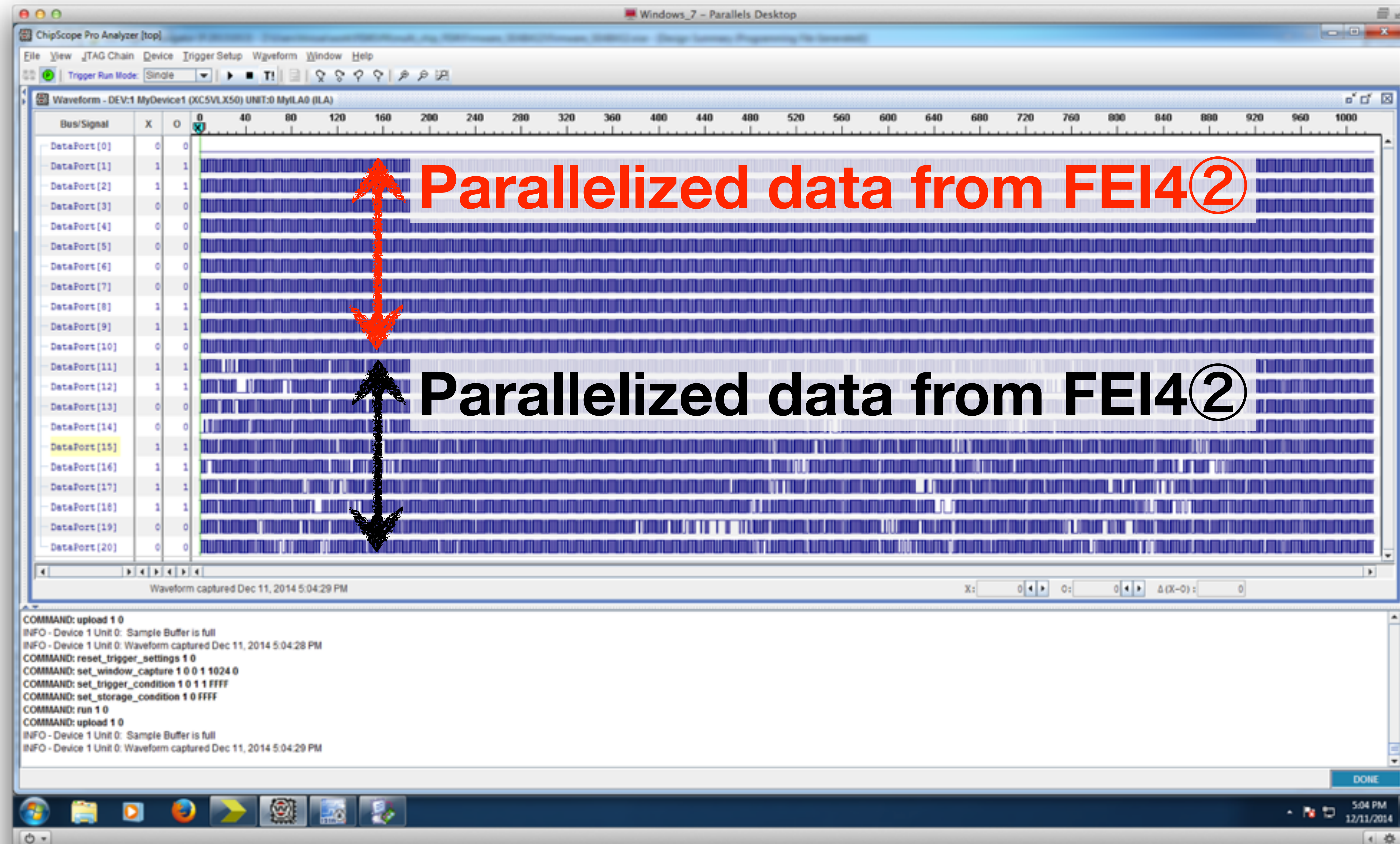
Data clock alignment

- New : finding the best “delay” to the input data.



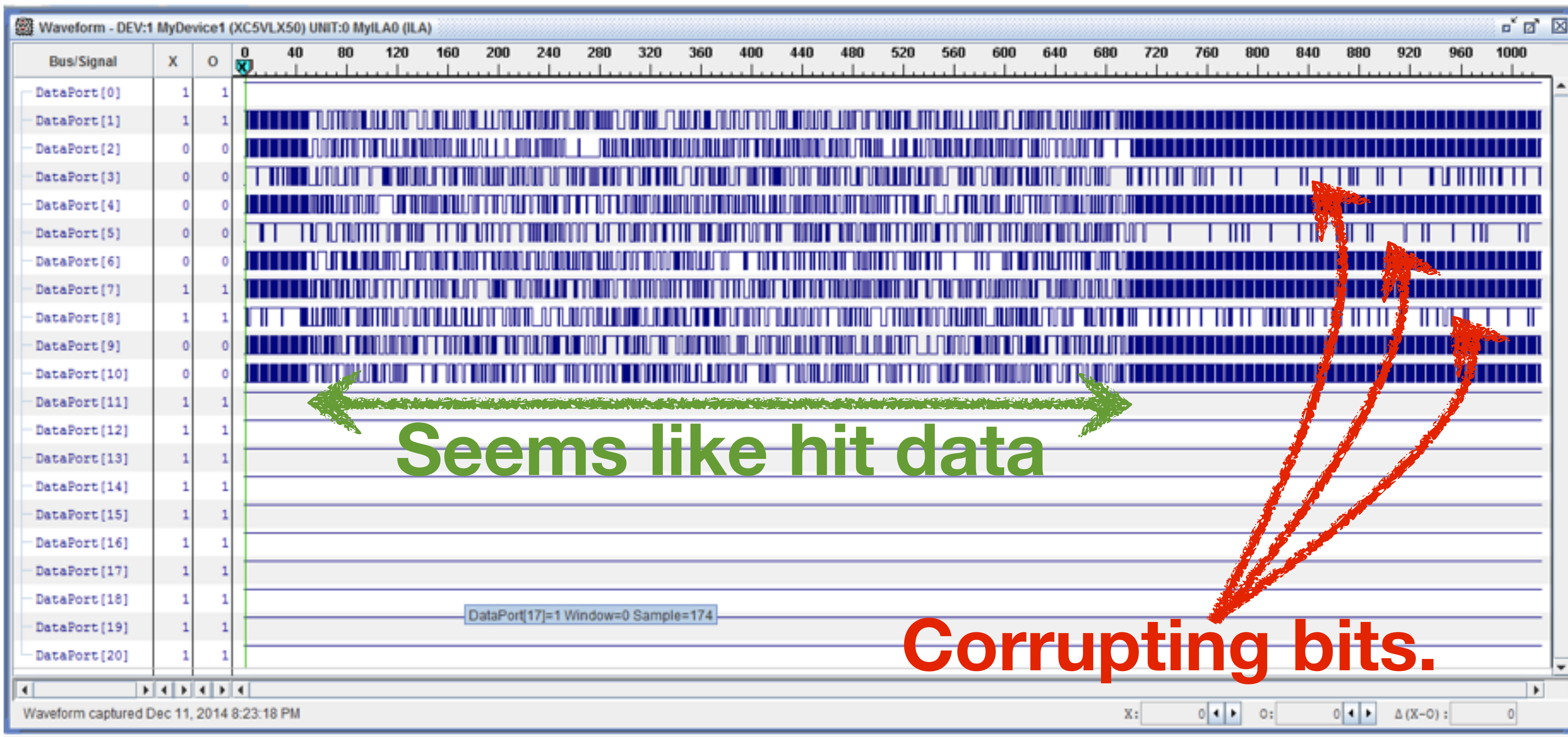
- Advantage :
  ➡No gated clock.
  ➡Slower clock frequency (480 MHz --> 80 MHz).
  - Note : Data is now extracted by DDR.
  ➡**“Timing won’t be change by the compilation environment.”**
  - Using registers in the particular IOB.

Periodical noise (?)



Hit data with some corruptions

- FEI4 successfully returns data, but some bits keep corrupting.

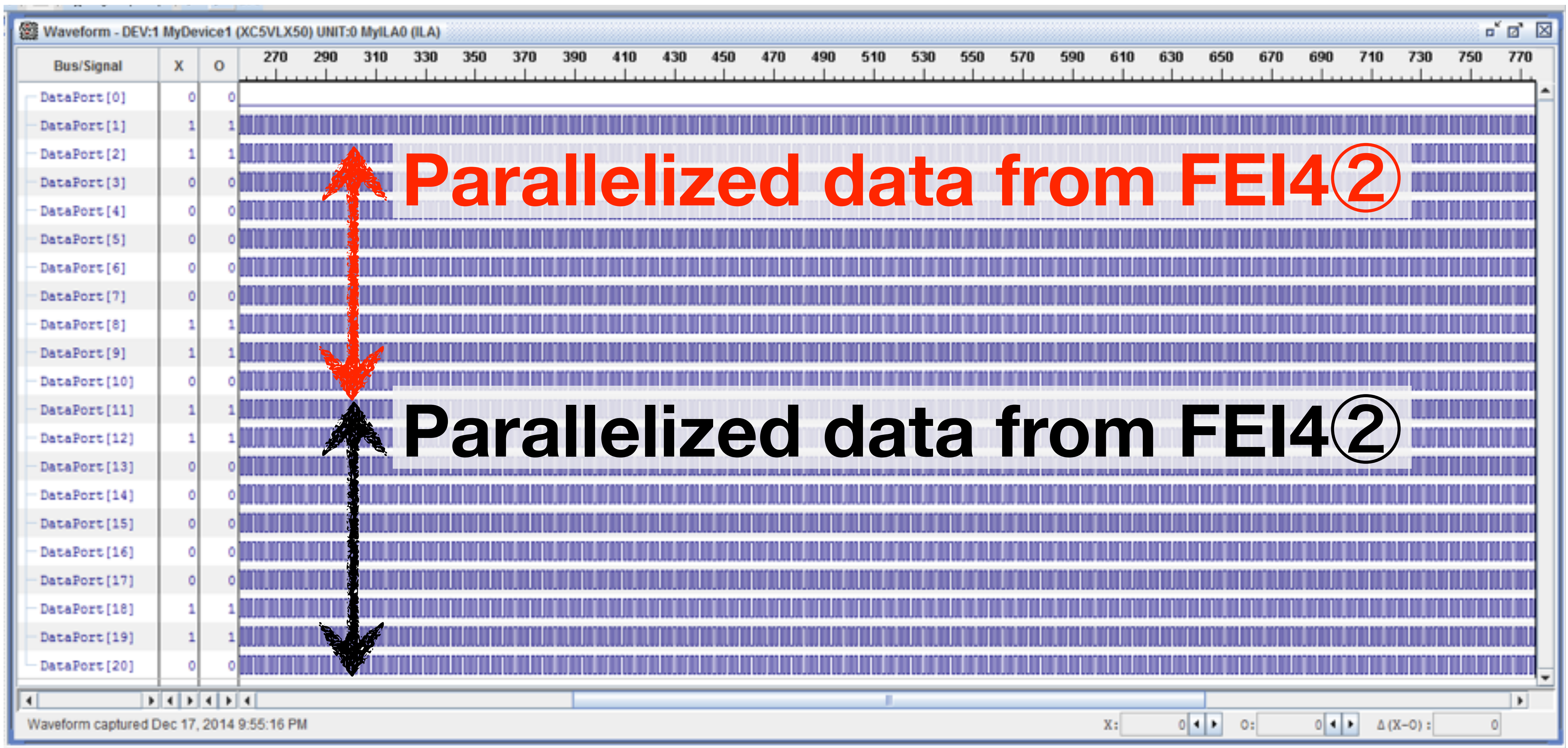


Finally found the reason of corruption

- The SERDES circuit for Chip0 in the SEABAS2 which I used seems to be broken.
  - ➡Data corruption happens only for Chip0.
    - If the corruption is due to the timing, it should happens among chips randomly.
  - ➡Perfectly works on the other SEABAS2 board.
    - Could reproduce the problem by testing several times.
  - ➡Without SERDES, firmware seems to work.

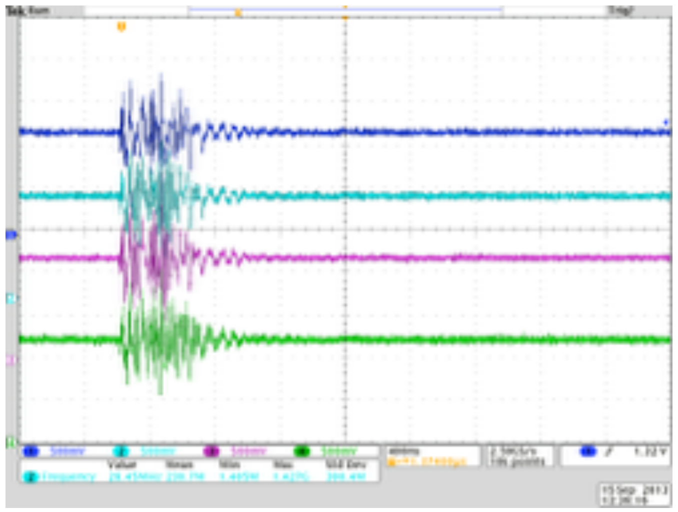
- Lesson:
  - ➡It’s rare case, but sometimes unexpected behavior isn’t caused by my bug!!

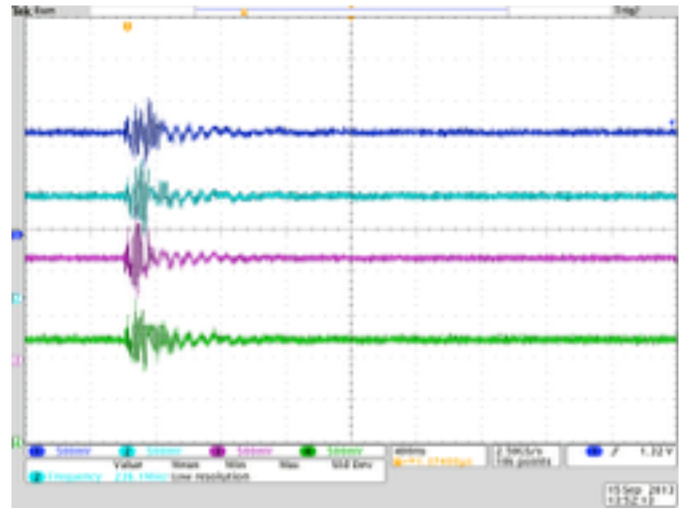
Perfect data extraction

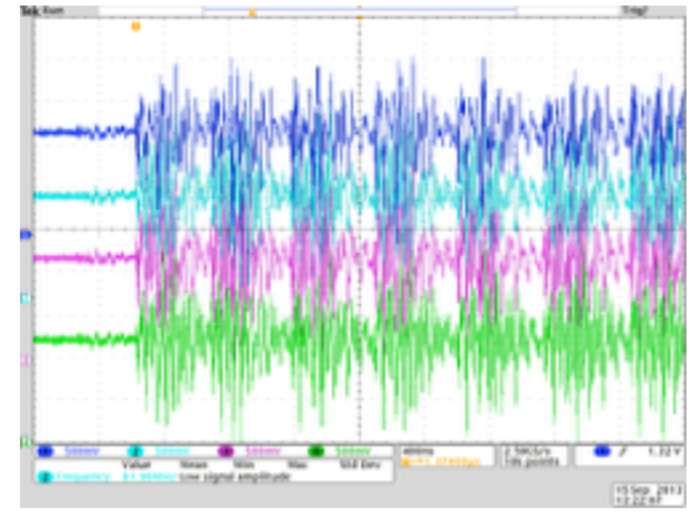


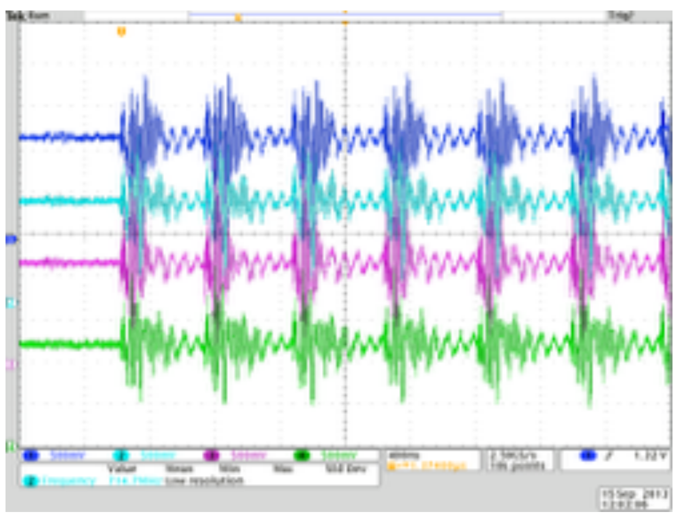
Weird noise on SEABAS

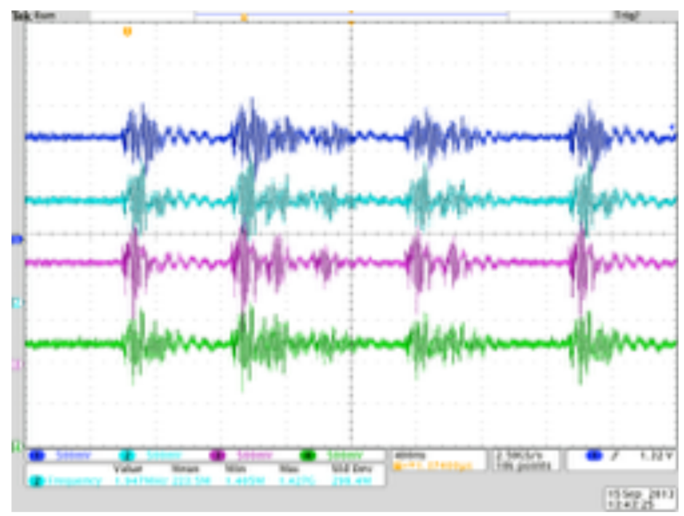
Example of the noise

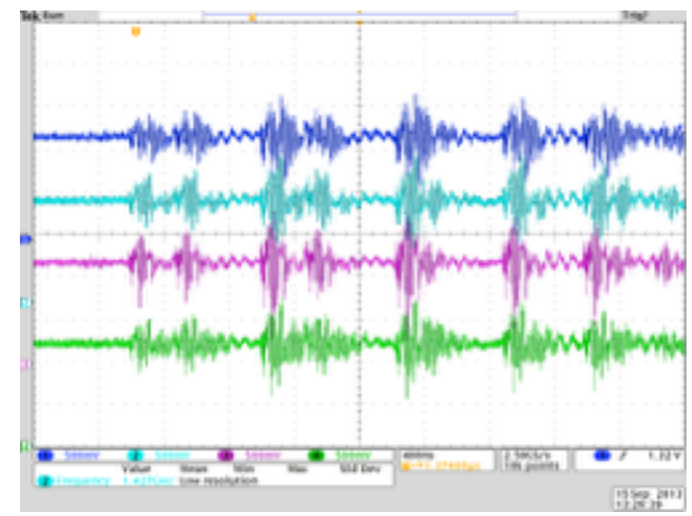


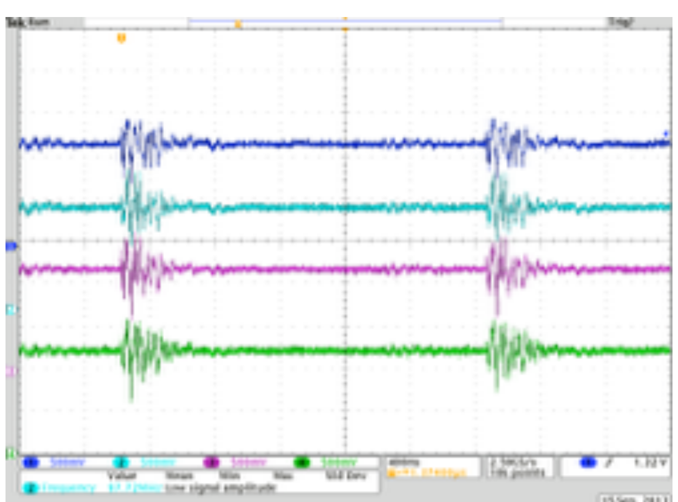










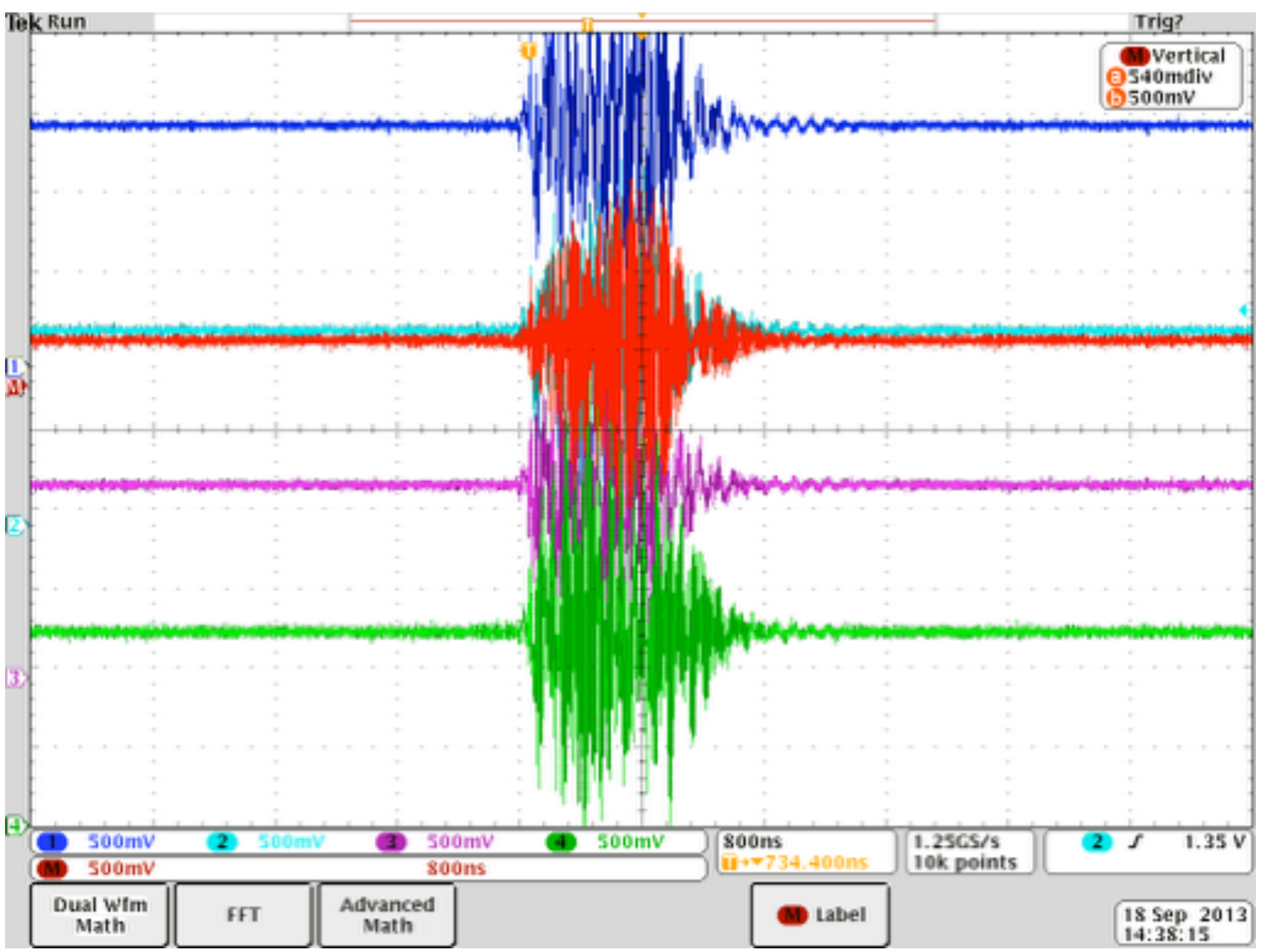


Frequency is not always the same.
Amplitude is also not the same.
Duration varies for each time.

Still existing on differential signals

➡Existing even after taking difference.

- Even though negative side have a similar noise at the same time...
- Noise can exceed the LVDS threshold.



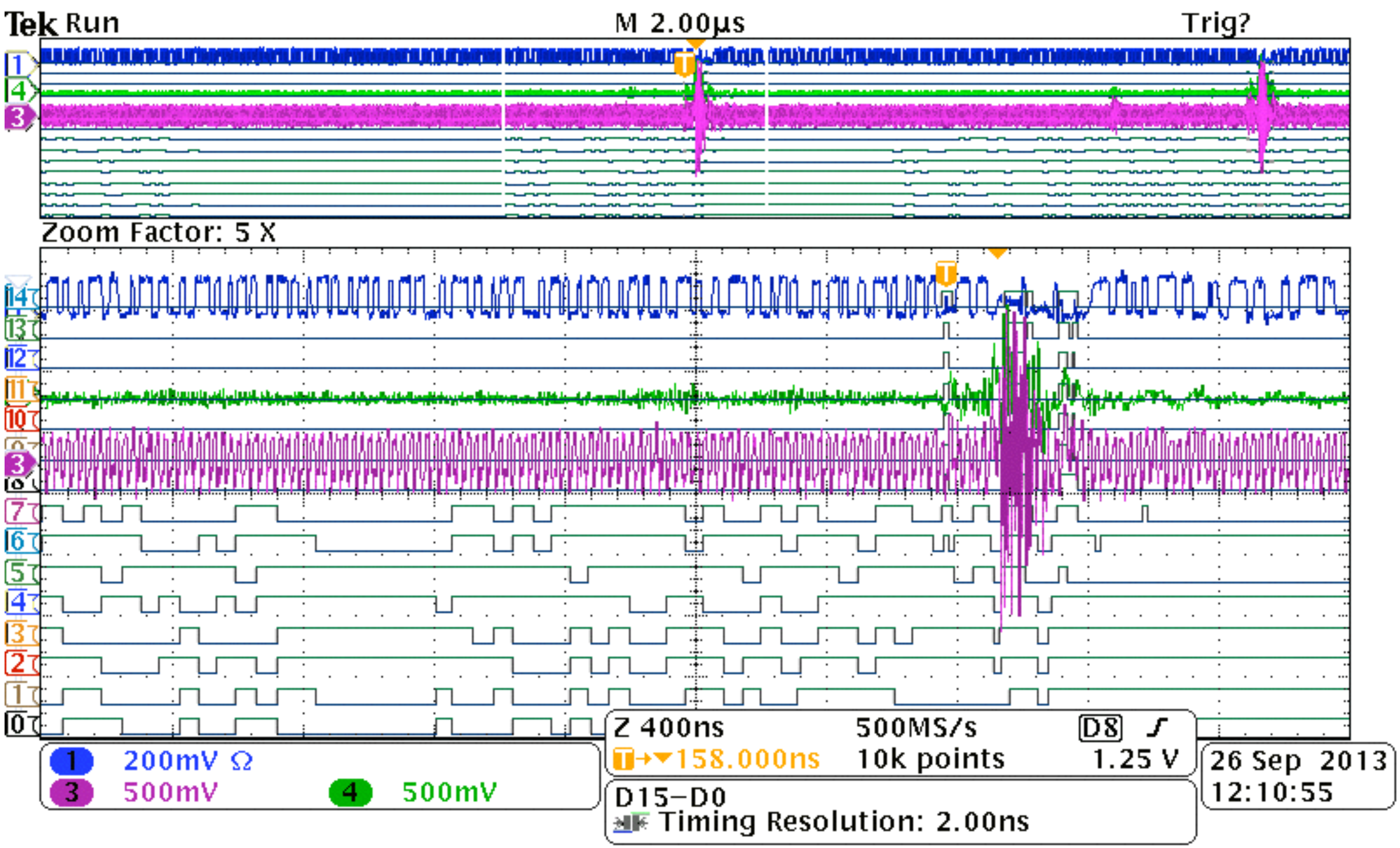
Positive side

Negative side

Diff(P-N)

The noise appears for all the signal lines

- ch1 : DOUT, ch2 : COMMAND, ch3 : REFCLK



Chair makes the noise.

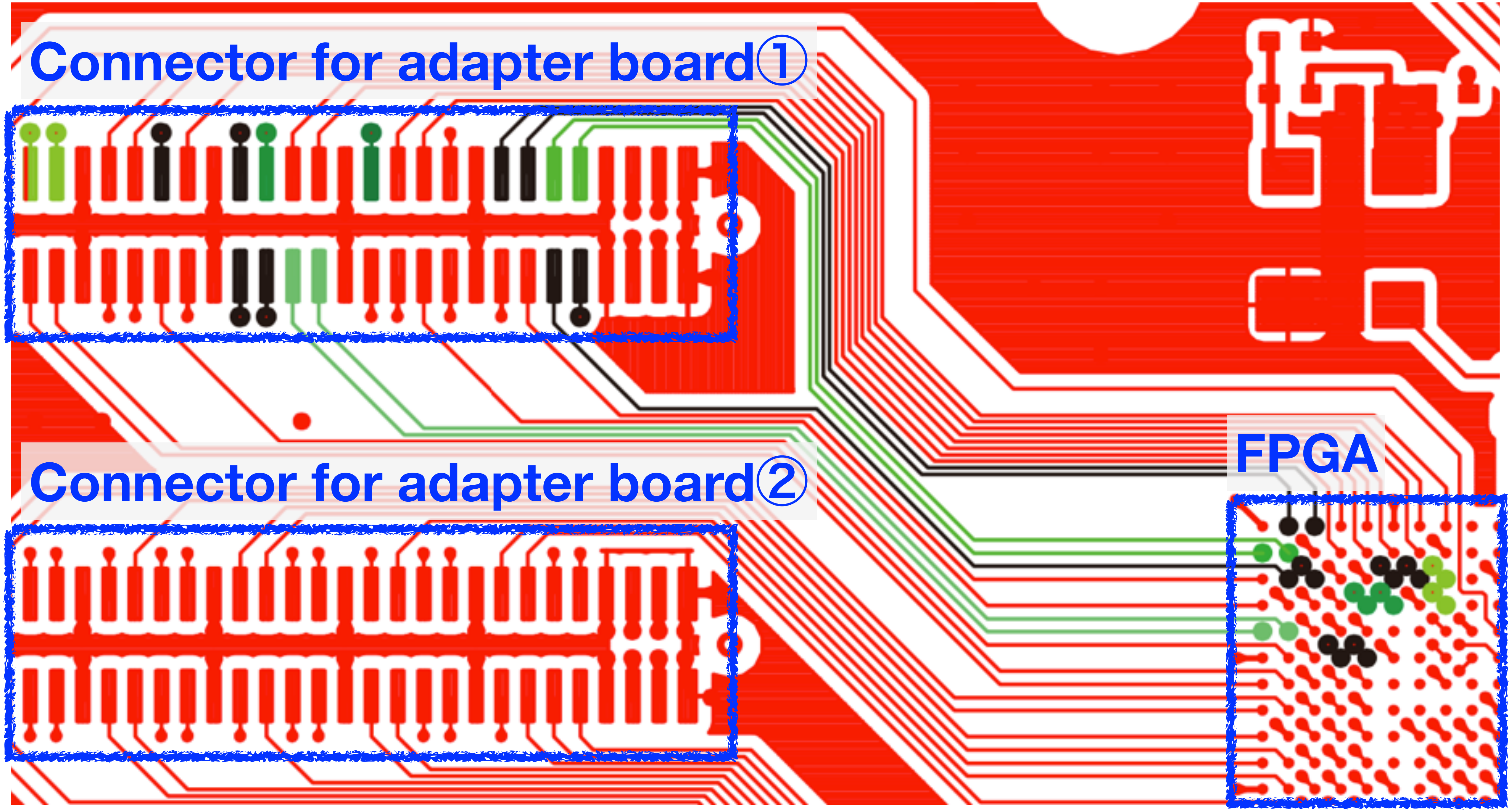
- There are two types of chairs in the lab.
  - ➡ Maybe, chair on the right makes ESD.
    - Can easily reproduce the noise by moving chairs.
  - ➡ No anti-ESD items in our lab except,,,
    - Wrist strap, anti-ESD mat on desks (×Floor, ×Dry air).

ESD CAUTION

- Have to take the “funny” sticker seriously.
  (Looks like just a joke though...)

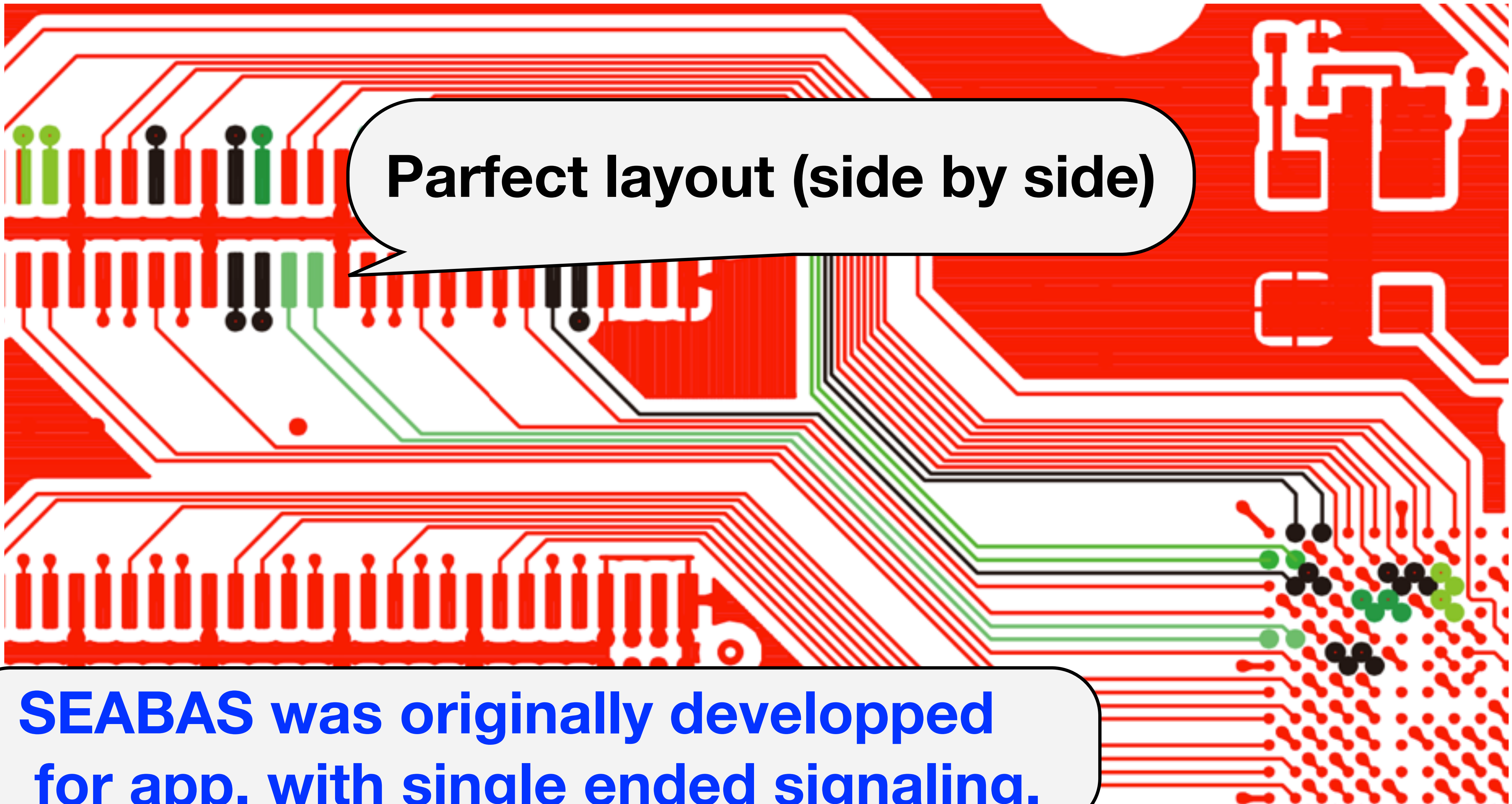
Indirect causes

- Displaced differential signal pairs.



Indirect causes

- Displaced differential signal pairs.

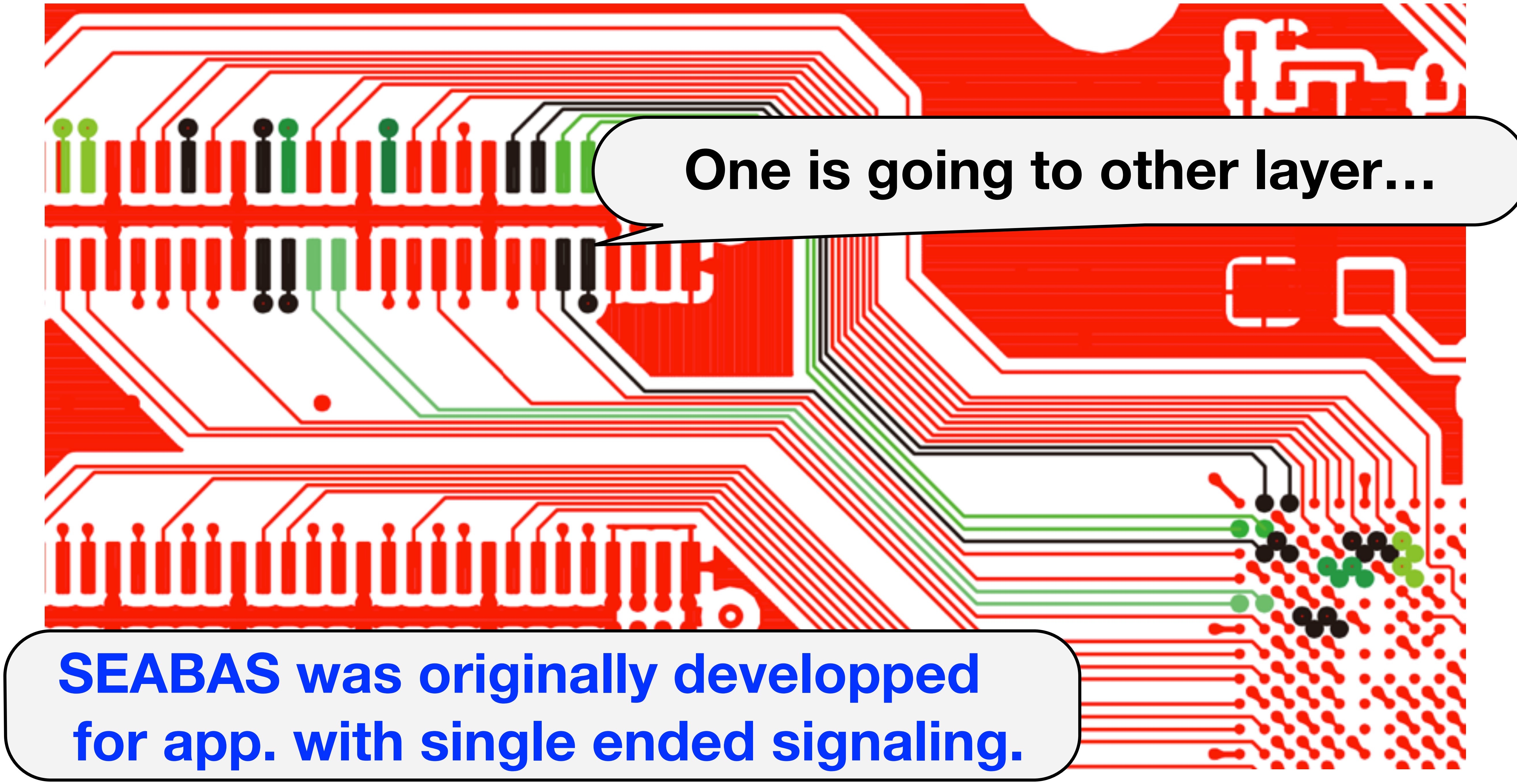


Parfect layout (side by side)

SEABAS was originally developped for app. with single ended signaling.

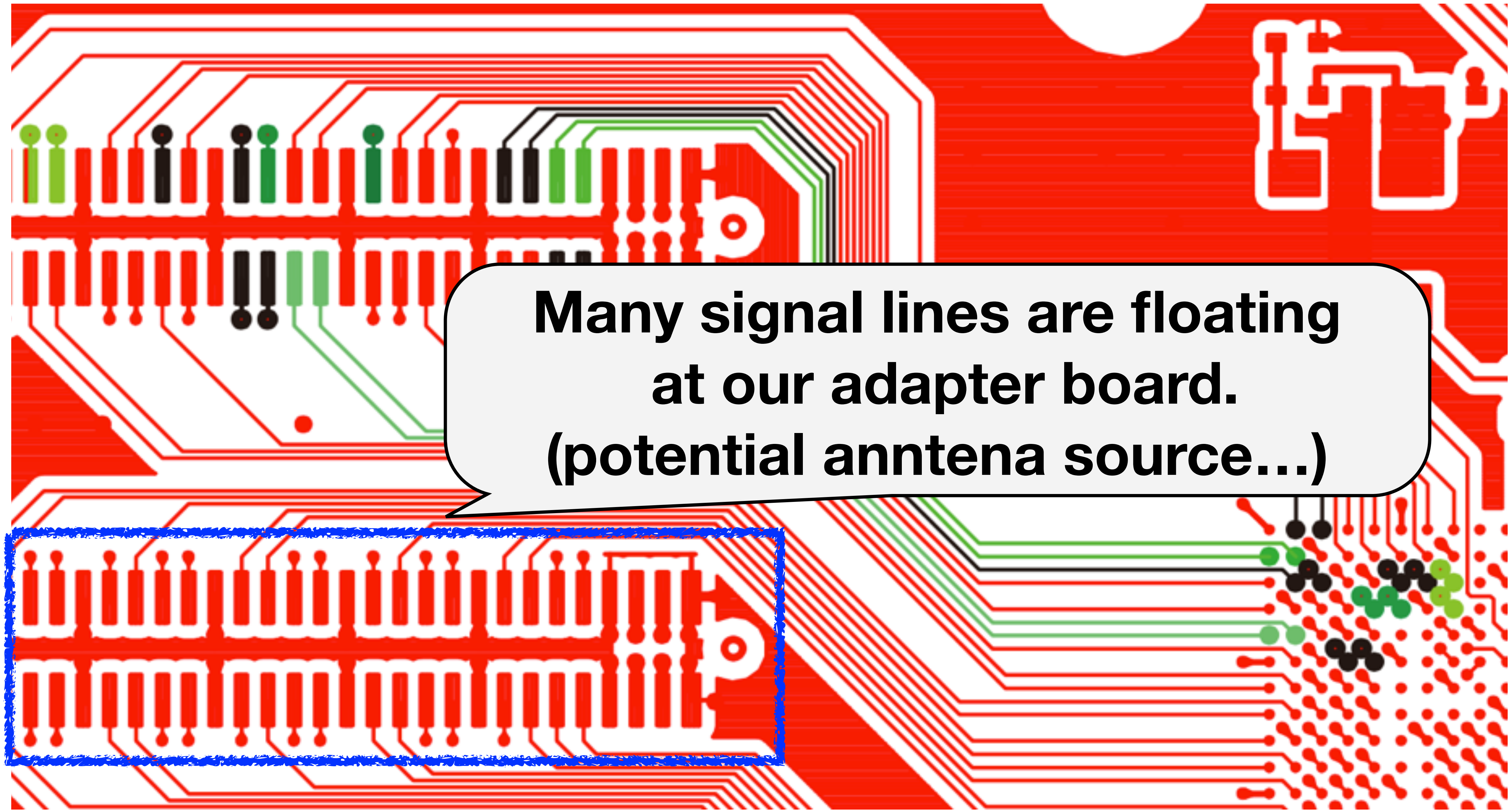
Indirect causes

- Displaced differential signal pairs.



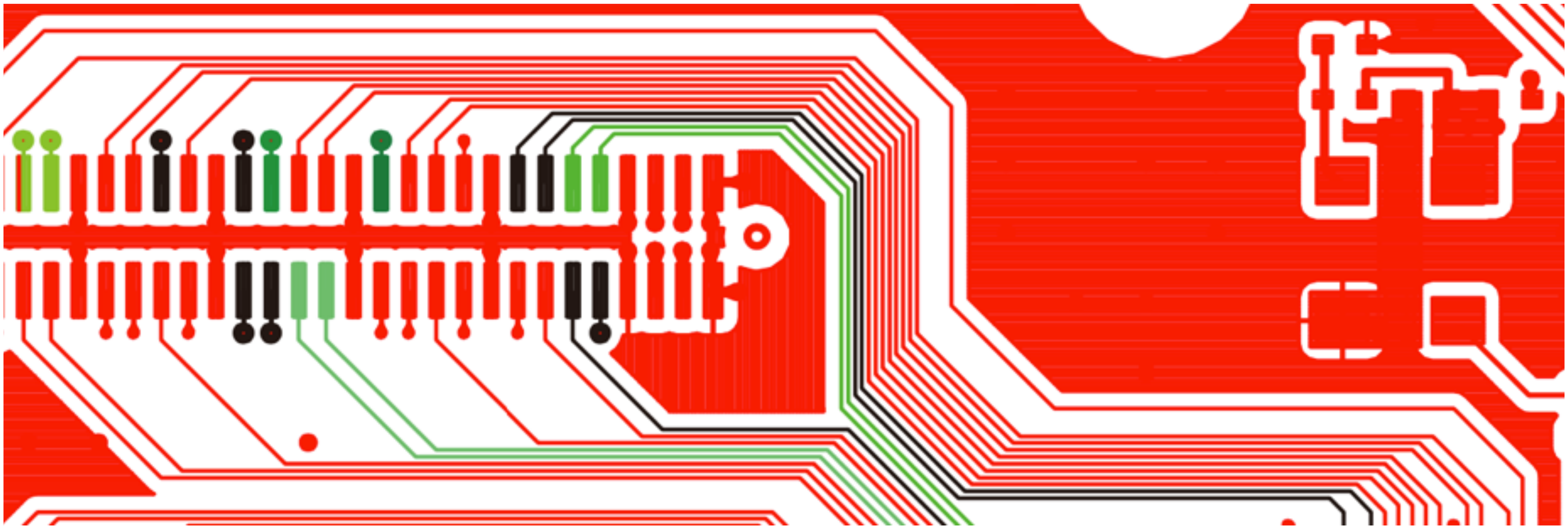
Indirect causes

- Floating signal lines



Indirect causes

- Floating signal lines



- For next generation SEABAS (and daughter boards)
  - ➡ Optimal signal line layout for differential signals.
  - ➡ Prevent user’s connectors to be an anntena.

Conclusions

- Presented development of DAQ system for testing the ATLAS upgraded pixel.
  - ➡ Basically it's working after experiencing many troubles.
- Also presented some problems which could happen for other projects and our solutions.
  - ➡ Hope to have useful comments from experienced developpers.
  - ➡ Hope this talk helps all future developments.
- I think this workshop is very good place to share this sort of things (Obviously not suit for JPS meeting).

Other systems