J-PARC二次ビームライン 高強度化に向けたFront-end electronicsの開発状況

KISHIMOTO LAB., OSAKA UNIV.
RYOTARO HONDA

- Self-Introduction
- Overview of DAQ system in K1.1 beam line
- Developed electronics
  - DRS4QDC
  - VME-EASIROC
  - Hadron Universal Logic module
- Summary

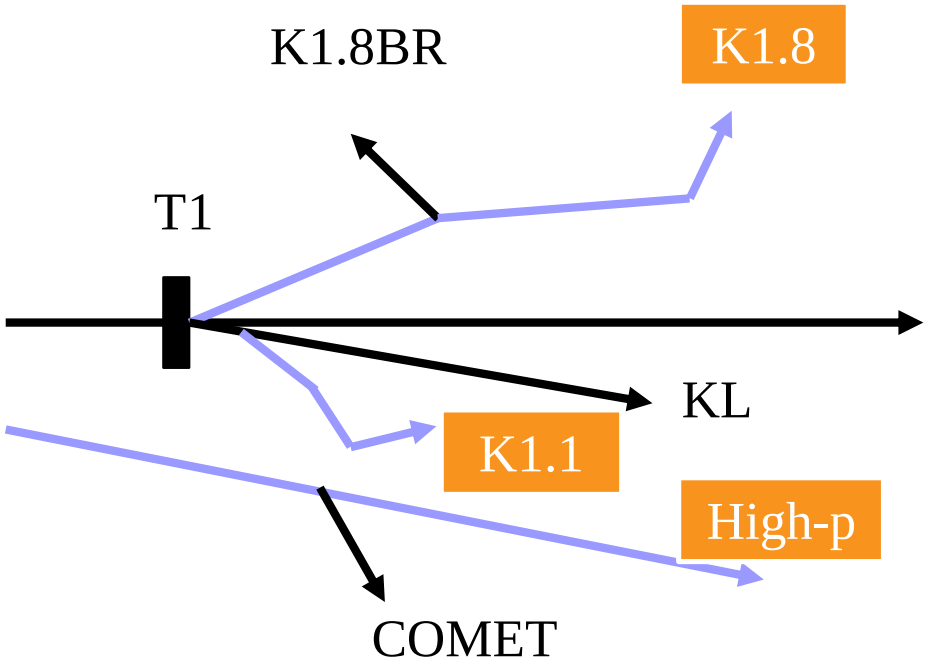
Self-Introduction

Ryotaro Honda （本多良太郎）
Strange nuclear physics, Hadron physics in J-PARC
Tohoku U. (Ph.D) → Osaka U. (PostDoc)

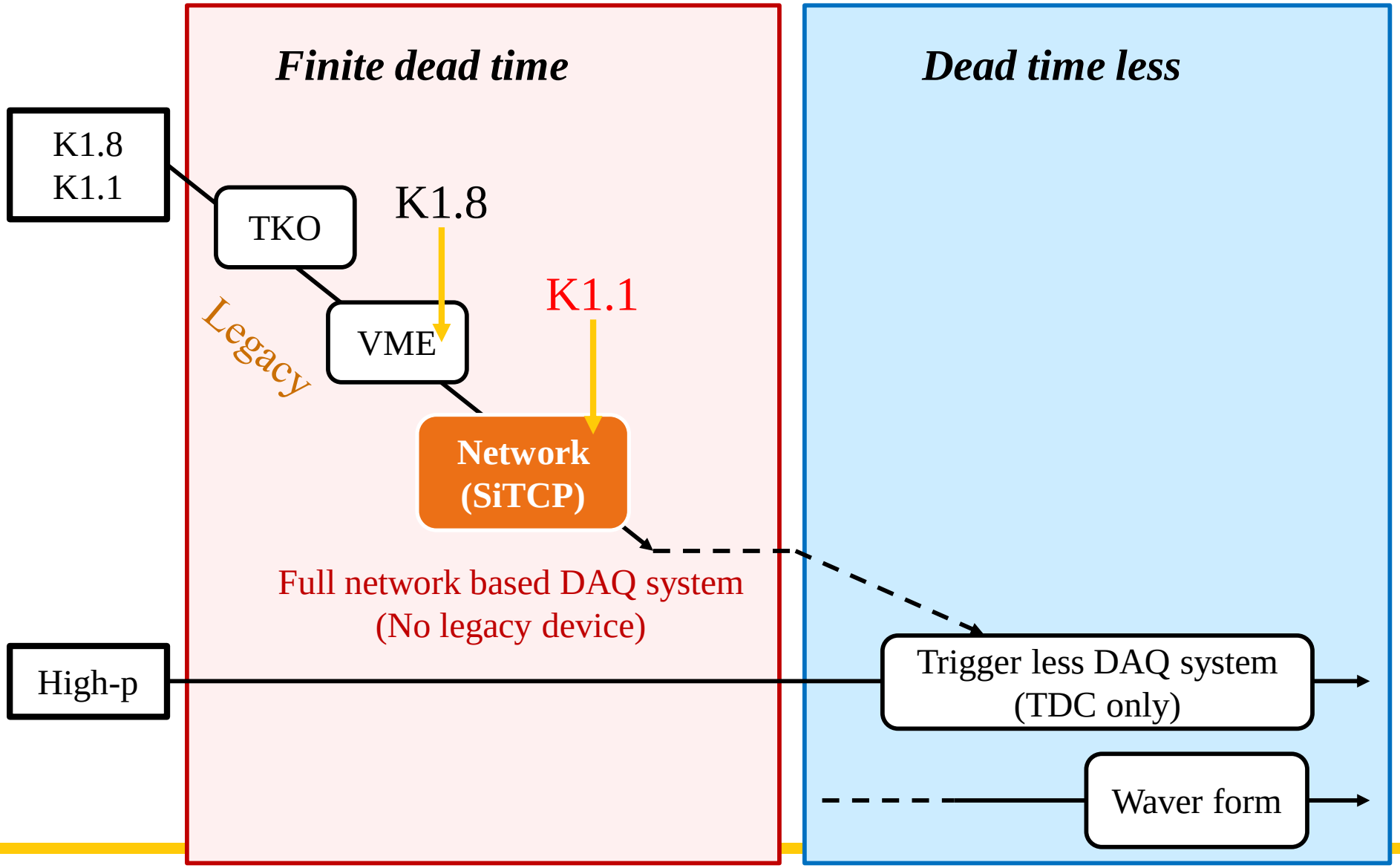
DAQ developer in K1.8/K1.1/ High-p beamline
Especially, for the hardware development.

- Circuit schema
- PCB design
- FPGA firmware
- (Software)

J-PARC Hadron facility

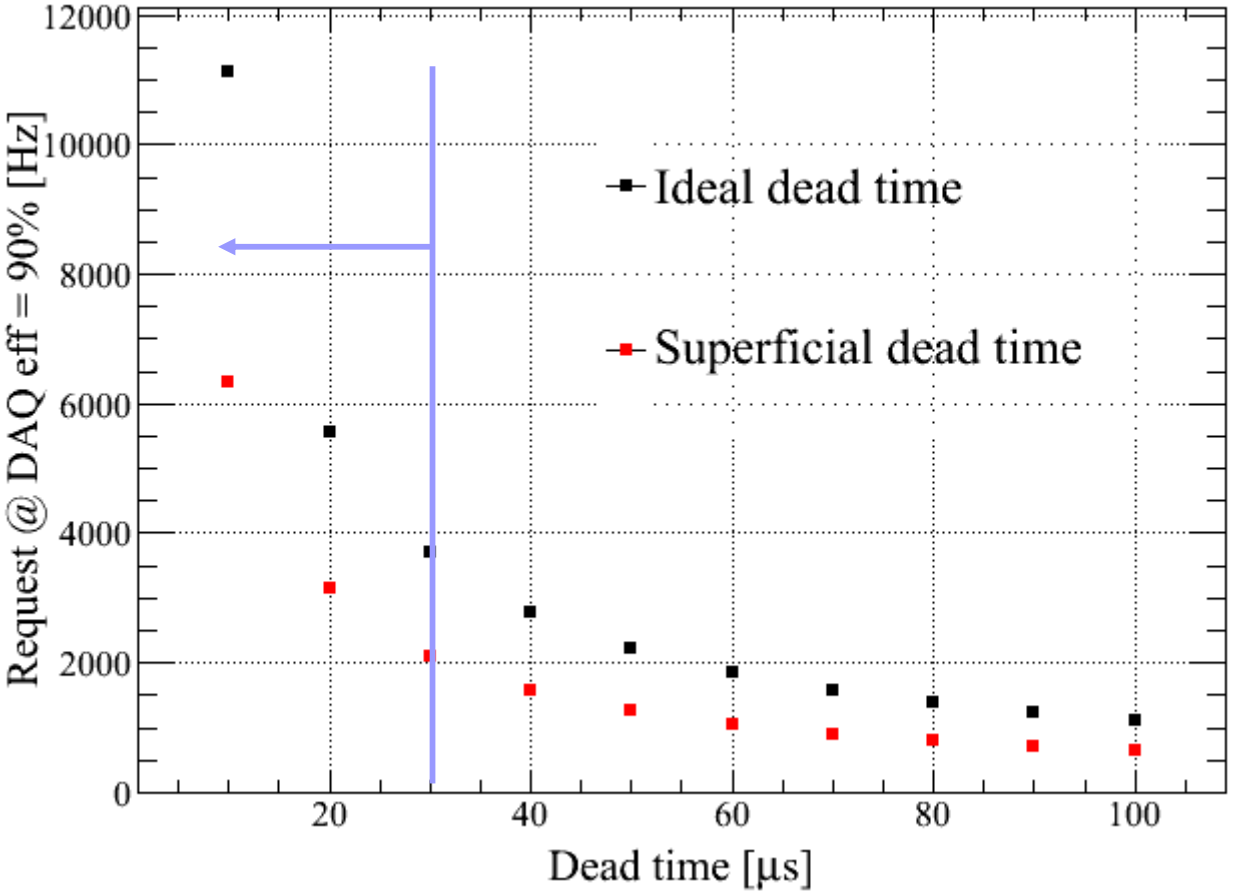


Dead time and generation of DAQ system



Dead time & DAQ eff.

Relation between the dead time and trigger rate
when DAQ eff. can achieve 90%



Less than 30us of dead time is recommended
by considering the future beam intensity of SX.

Detector setup in K1.1 (E63)

Timing (trigger) counters
- BH1
- BH2
- TOF wall
- SFV

Plastic scintillator

PID counters
- BAC1,2
- SAC1,3
- SP0
- SMF (LC)

Aerogel Cherenkov

Plastic scintillator

Lucite Cherenkov

Tracking detector
- BFT
- BC1,2
- SDC1,2,3,4

Scintillation fiber tracker

MWPC

MWDC

γ-ray detectors
- Hyperball-J

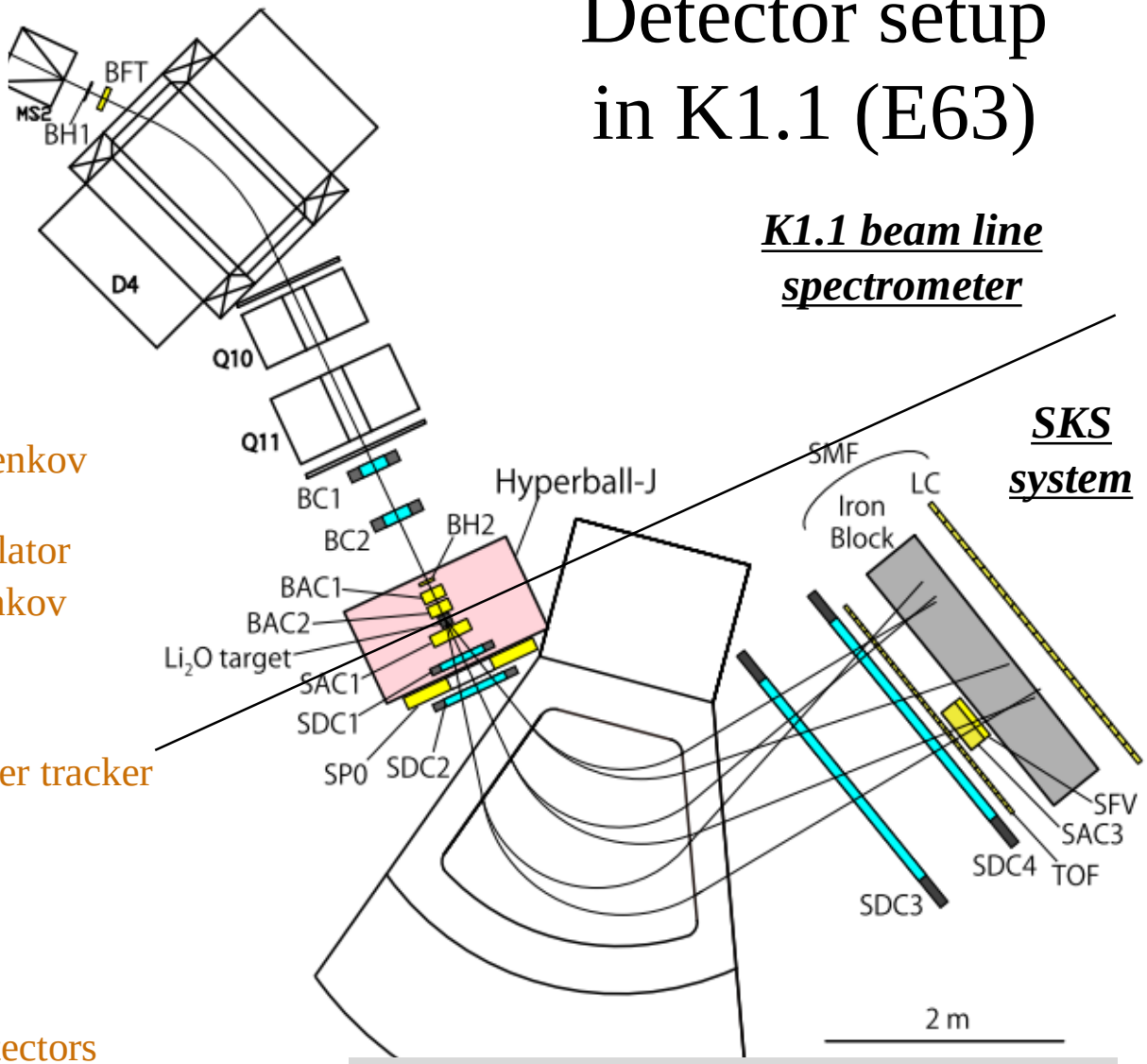
Germanium detectors

+

PWO crystals

K1.1 beam line spectrometer

SKS system



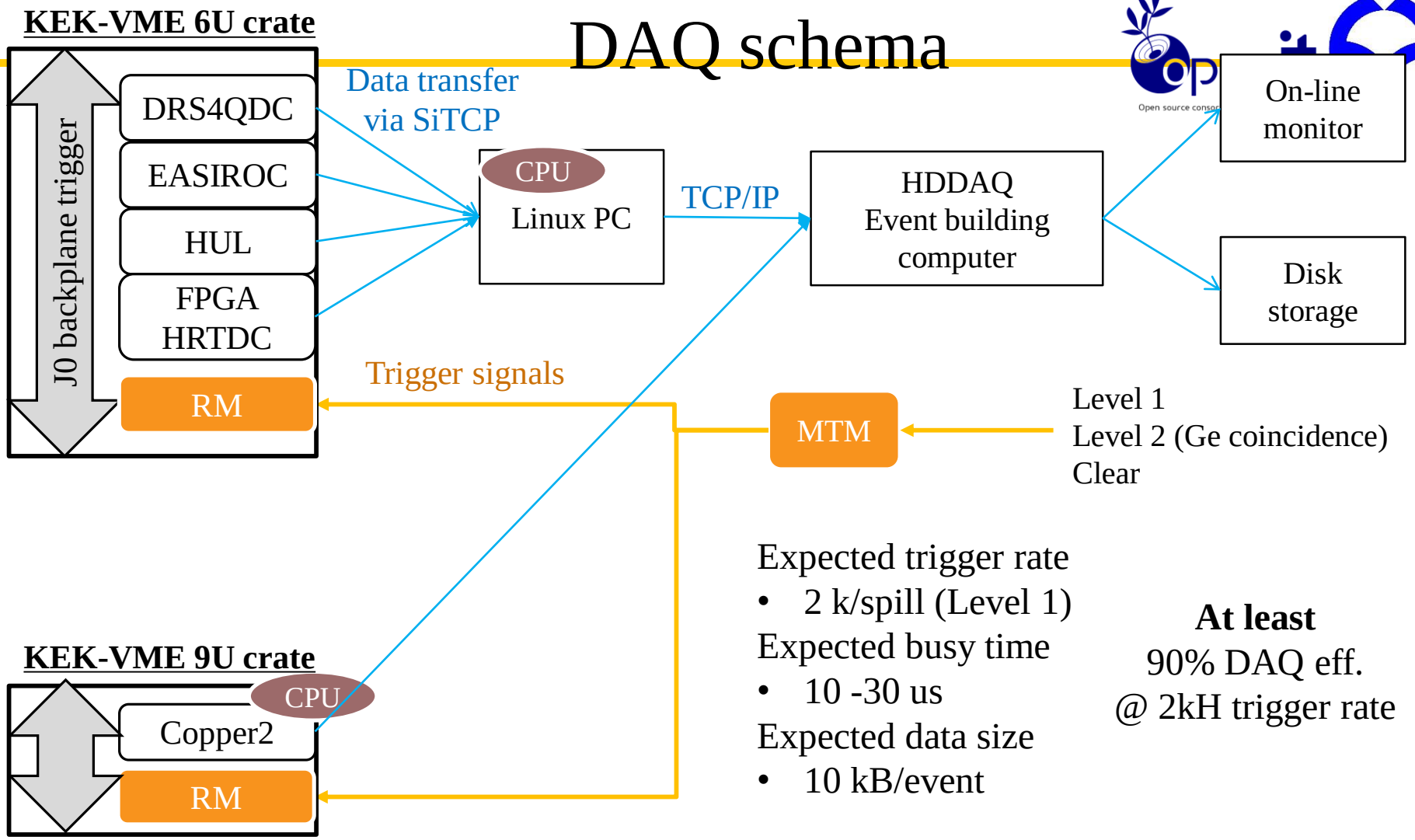
2.5 T (400A) for 1.1 GeV/c beam

List of detector specification and requirements

Detector	Device	# of ch	TDC	ADC	Electronics
Spectrometer systems					
BH1, 2, TOF	PMT	11+5+64	**High Reso.**	**YES**	**DRS4QDC** **FPGA-HRTDC**
ACs	PMT	27	Low Reso.	**YES**	**DRS4QDC**
SP0, SMF, SFV	PMT	80+56+6	Low Reso.	**YES**	**DRS4QDC**
BFT	MPPC	512	Low Reso.	No	**VME-EASIROC**
BC1,2	Wire chamber	3072	Low Reso.	No	Copper2
SDC1, 2	Wire chamber	576+448	Low Reso.	No	**HUL**
SDC3, 4	Wire chamber	1392	Low Reso.	No	**HUL**
Hyperball-J					
Ge	Ge	32	Low Reso.	**YES**	AD413A **HUL**
PWO	PMT	238	Low Reso.	(NO)	**HUL**

Only 80 ch need high-resolution TDC while a lot of low-resolution TDC are necessary.
Cost per channel in LR-TDC is a matter of concern.

DAQ schema



Expected trigger rate
- 2 k/spill (Level 1)

Expected busy time
- 10 -30 us

Expected data size
- 10 kB/event

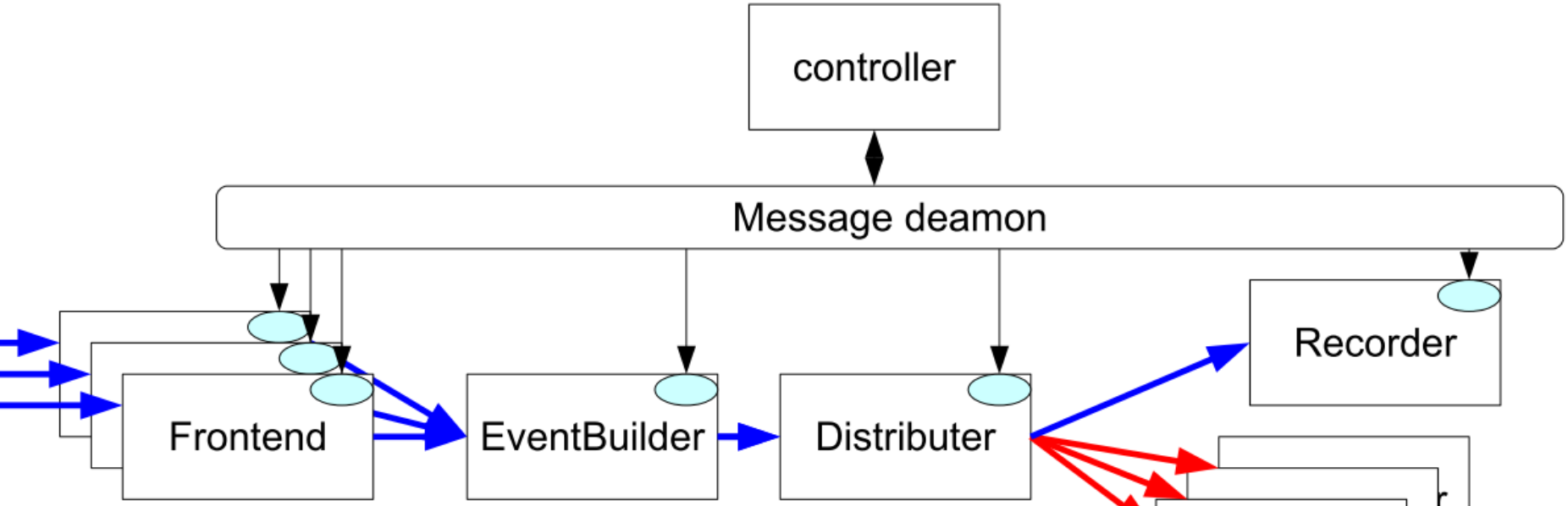
At least
90% DAQ eff.
@ 2kH trigger rate

Front-end process of HDDAQ are running on the machine with CPU mark

Almost the same as the K1.8 system, but all the electronics must be developed except for copper2.

Hadron DAQ (HD-DAQ)

TCP/IP oriented DAQ system



Data node
- Collect data from modules.
- Control modules

Distribute event packet to
- Recorder port (All events)
- Distributer port (best effort)

Collect data from Frontend
Build event packet

Developed electronics

DRS4QDC

Analog

- Number of channel 16
- Input range 2 Vp-p
- Common mode input range ±1 V
- Absolute input range ±2.8 V
- Buffer range 2 μs @ 1 GSPS

Digital I/O

- Discriminator outputs (LVDS), 16 ch parallel
- NIM level I/O (4 inputs, 2 outputs)
- Receive triggers from the KEK-VME J0 bus

Data transfer & control

- TCP & UDP realized by SiTCP (100 Mbps)

PCB standard

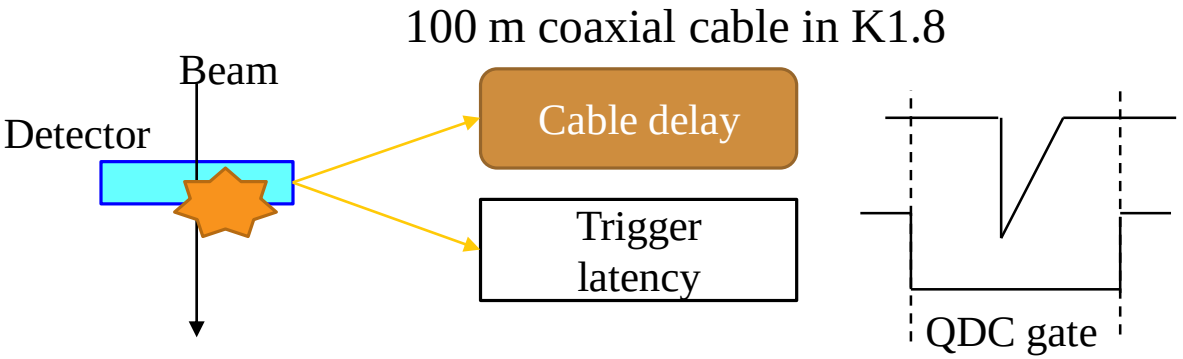
VME 6U KEK VME
Only J0 is mounted

- ±3.3 V from J0
  - +3.3 V ~ 4.2 A
  - -3.3 V ~1.8 A

Open-It project :
ADC HRTDC with DRS4

Open source consortium of Instrumentation

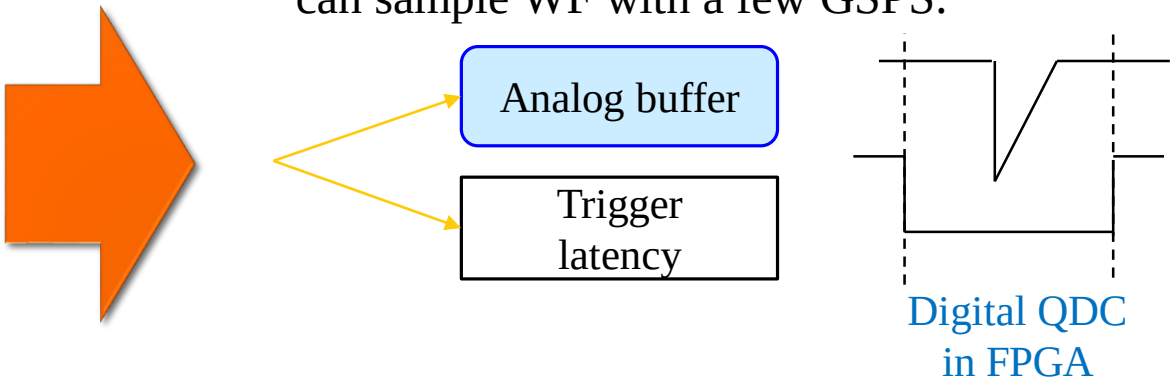
Motivation of DRS4QDC



Cable delay is unrealistic in future experiment.

- Expensive.
- Trigger latency is strongly limited.
- Not suitable for multi-channel.

DRS4 is analog buffer
can sample WF with a few GSPS.

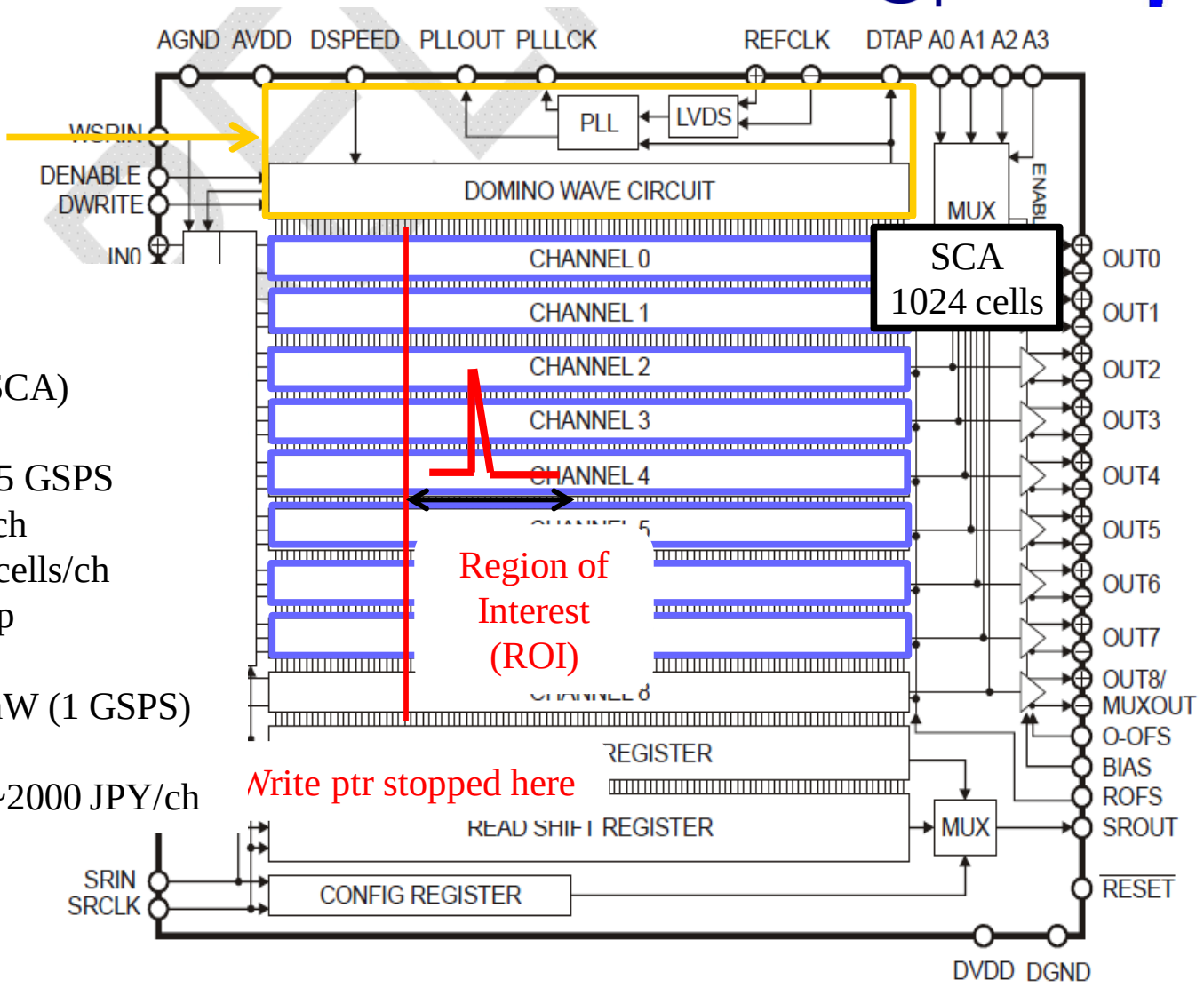


DRS4 – Method of sampling

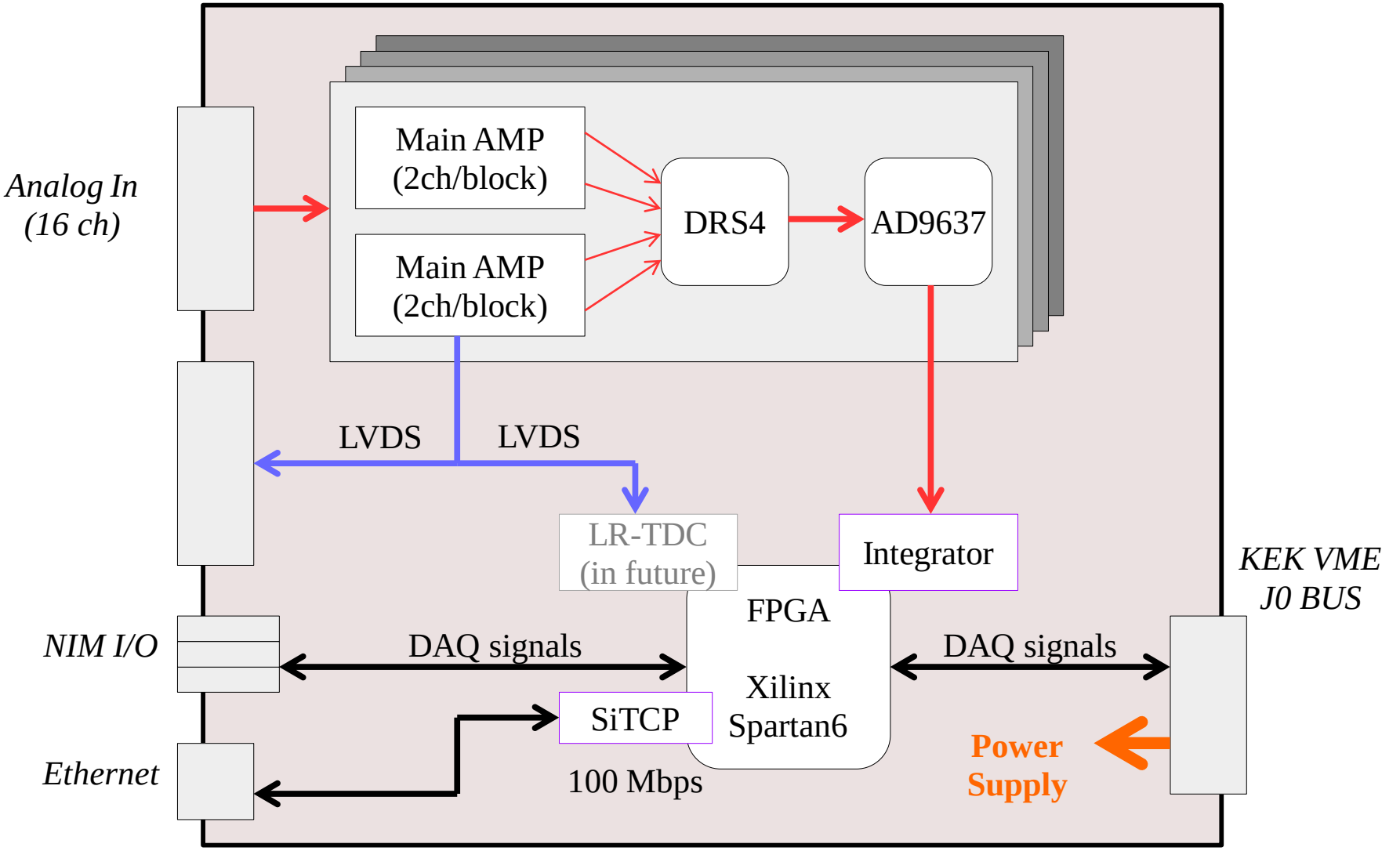
Domino wave
0.7 ~ 5 GSPS

Analog buffer
DRS4 (Developed by PSI)
Switched Capacitor Array (SCA)

Sampling rate	0.7 ~ 5 GSPS
Input ch	8 (9) ch
Number of cells	1024 cells/ch
Input range	1 Vp-p
Power consumption	110 mW (1 GSPS)
Cost	1000~2000 JPY/ch



DRS4QDC block diagram



DRS4QDC DAQ functions

Busy time

- 30 ns × N samples (if the event buffer is not full.)
- e.g. 100 sample : 3 μs + α = 10 μs

Data type

- QDC (integrated wave form)
- Wave form (can be switched off)

Multi-event buffer

- There is 2048 words FIFO in each channel. It play as an event buffer.
- e.g. 100 samples : 2048/100 = 20 events buffer.
- If full QDC mode is selected, it is 2k events buffer.

Zero suppression

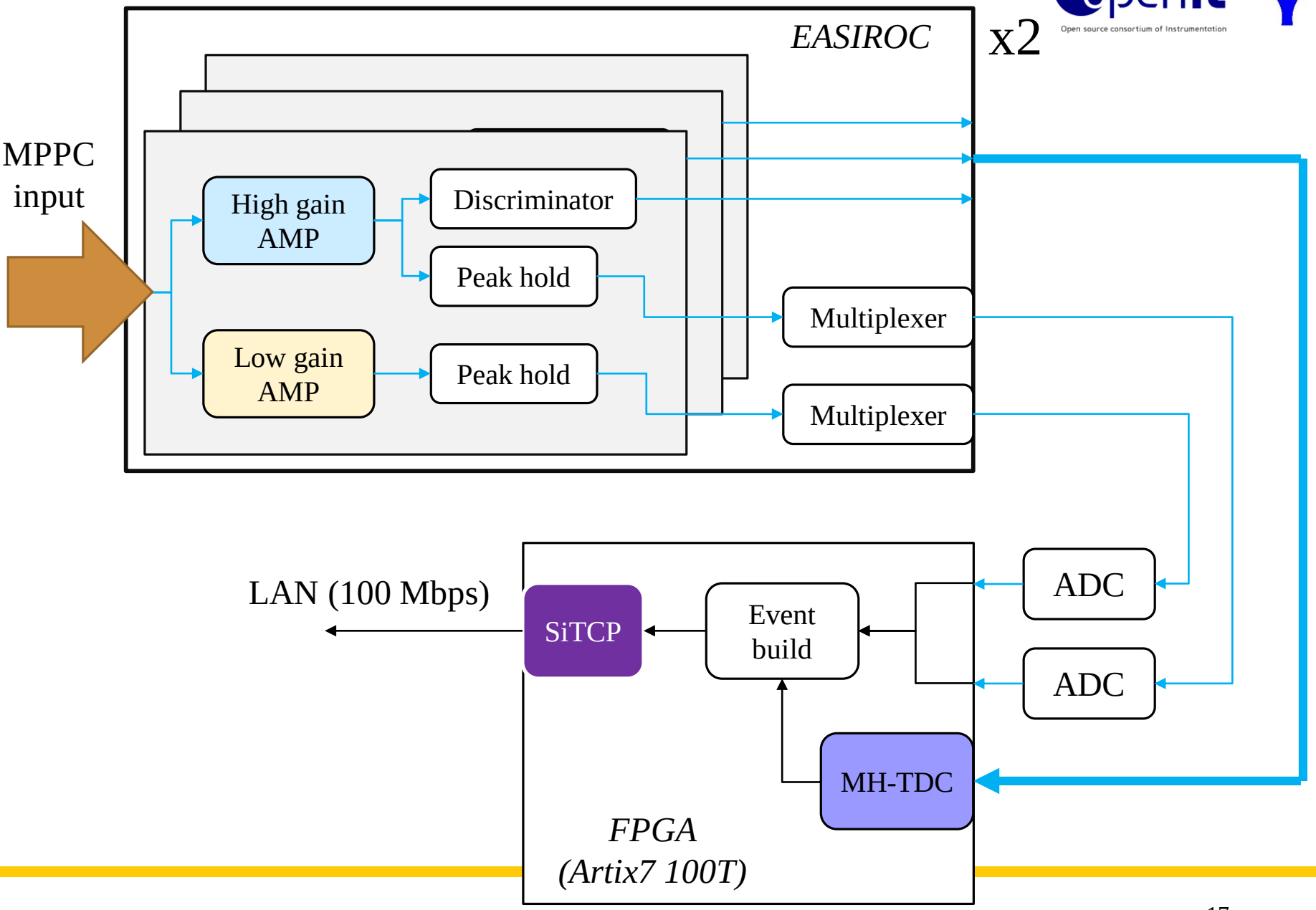
VME-EASIROC

Multi-MPPC readout system
VME-EASIROC

- 64 MPPC input (2 EASIROC)
- ADC + MHTDC in FPGA (1 ns precision)
- Dead time 10 -20 us
- SiTCP (100 Mbps)
- Powered by +5V form J1.
- KEK-VME J0 is supported.

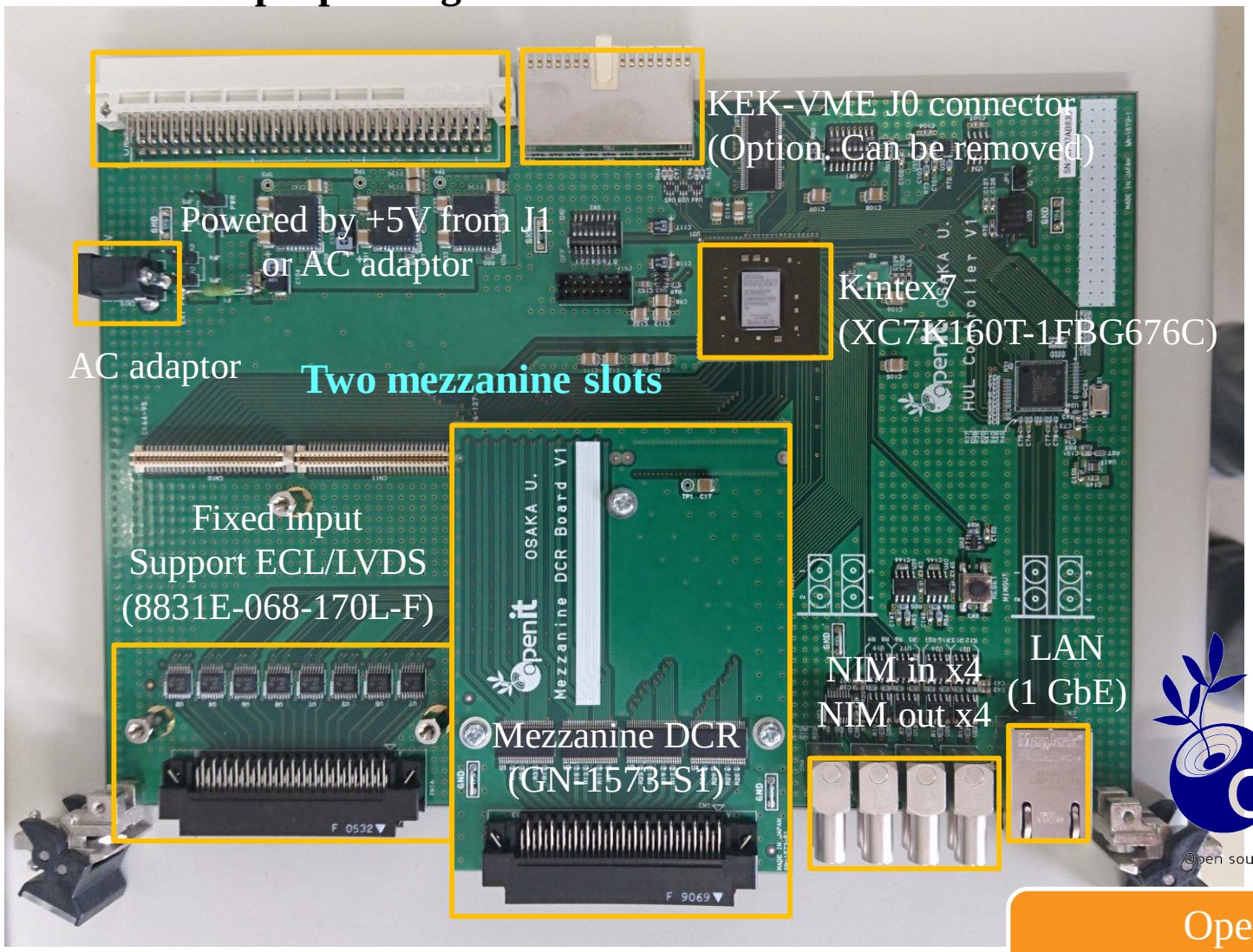
Open-It project :
VME EASIROC module
(Developer 塩崎健弘)

VME-EASIROC block diagram



Hadron Universal Logic (HUL) module specification

General purpose logic board with Kintex7 and SiTCP



Fixed input (64ch) + Mezzanine (64ch in max.)

= 128ch direct connection to FPGA

Open-It project :
Hadron Universal Logic Module

Requirements to new module

As cheep as possible
- Requirement : 1500 JPY/ch

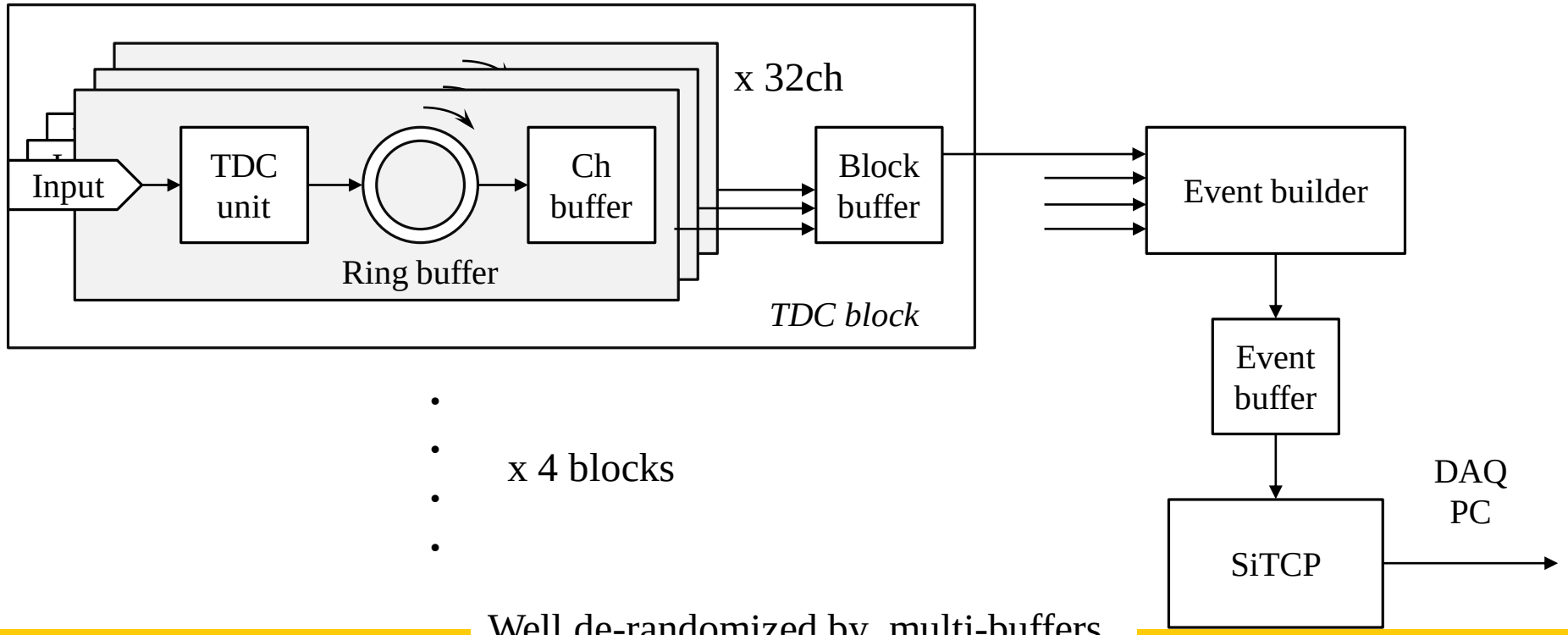
Data communication via TCP/IP
- Register setting
- Usage as DAQ module
- Downloading MCS file via network

Mount the mezzanine card slots
- Capability for various types of the signal standard
- Increase the maximum input channels up to 128 ch
- Extension to various kinds of applications

Example of application (1)

Multi-Hit TDC (Under development, but almost finished)

- Input : 128 ch
- LSB : 0.83 ns
- Resolution : ~ 300 ps (r.m.s)
- Ring buffer length : 13.7 μs
- Almost dead time free.



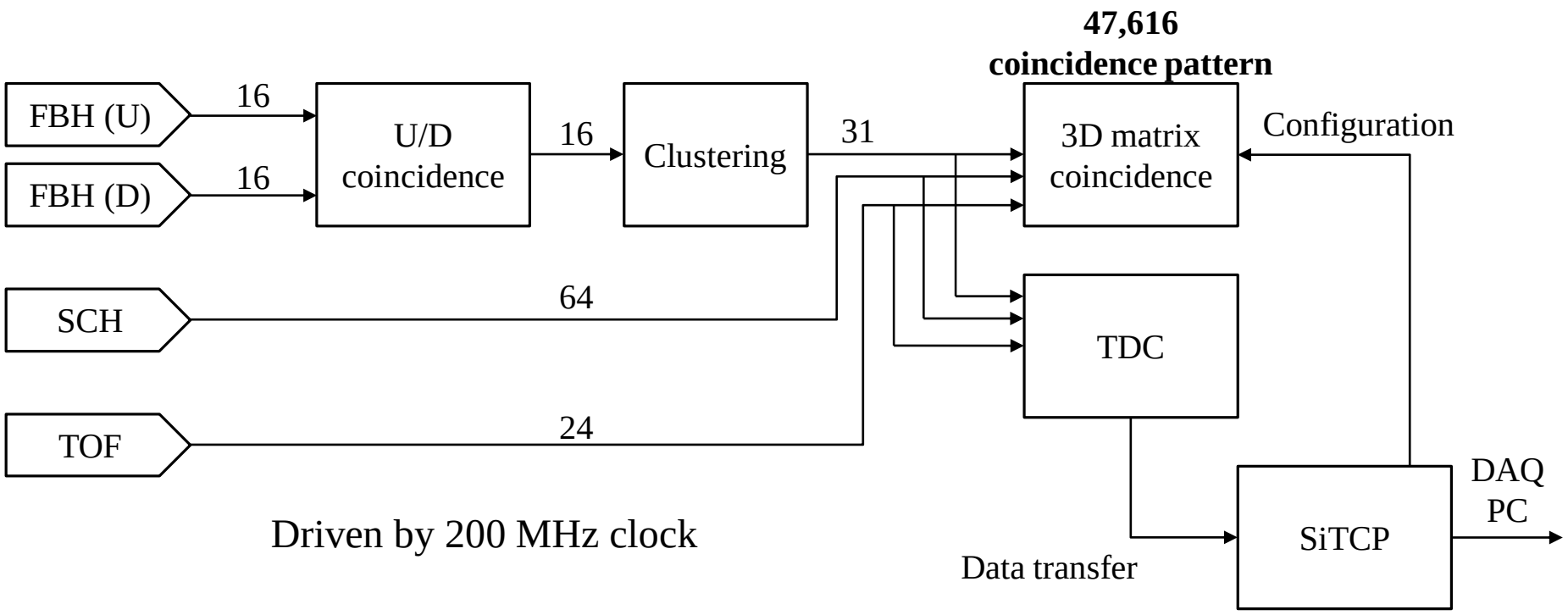
Well de-randomized by multi-buffers

Example of application (2)

Matrix coincidence trigger

3 dimensional matrix trigger for E07 experiment (**Already used in actual beam time**)

- TOF (24 seg) x SCH (64 seg) x FBH (31 seg) = 47,616 pattern.
- Enable/Disable of each matrix element is selectable via SiTCP.
- Driven by 200 MHz clock.
- Single hit TDC with 5 ns precision was implemented. We can see what happened inside FPGA.



Summary

Construct the full network based DAQ system in the K1.1 beam line

Required busy time is less than 30 us.

Development items

- DRS4QDC
- Multi-Hit TDC on HUL
- VME-EASIROC
- FPGA based HR-TDC

Except for HR-TDC, the development were almost finished.