計測システム研究会2016 @ J-PARC
October 13-14, 2016

J-PARC T59 WAGASCI実験の信号読み出しシステムの開発

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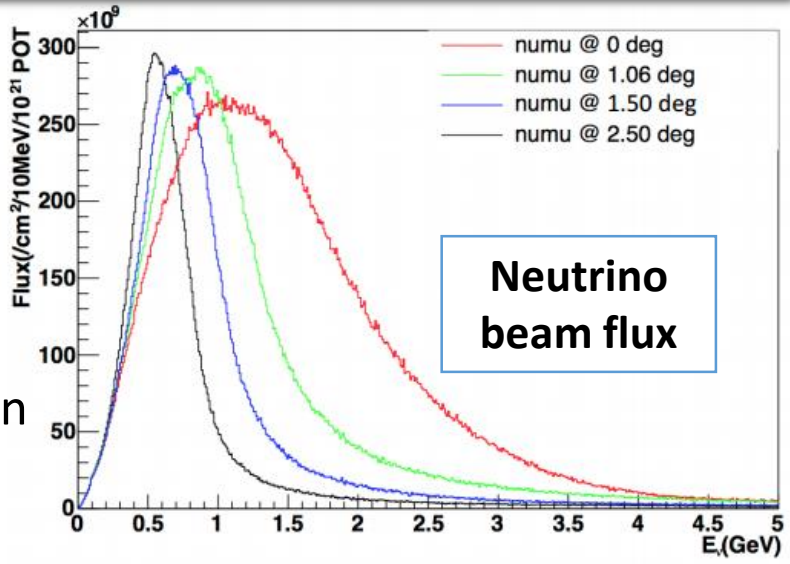
J-PARC T59 experiment: WAGASCI

Experiment

- *J-PARC neutrino beam* at Neutrino Monitor Hall.
- *1 ton* target with half H2O/half CH.



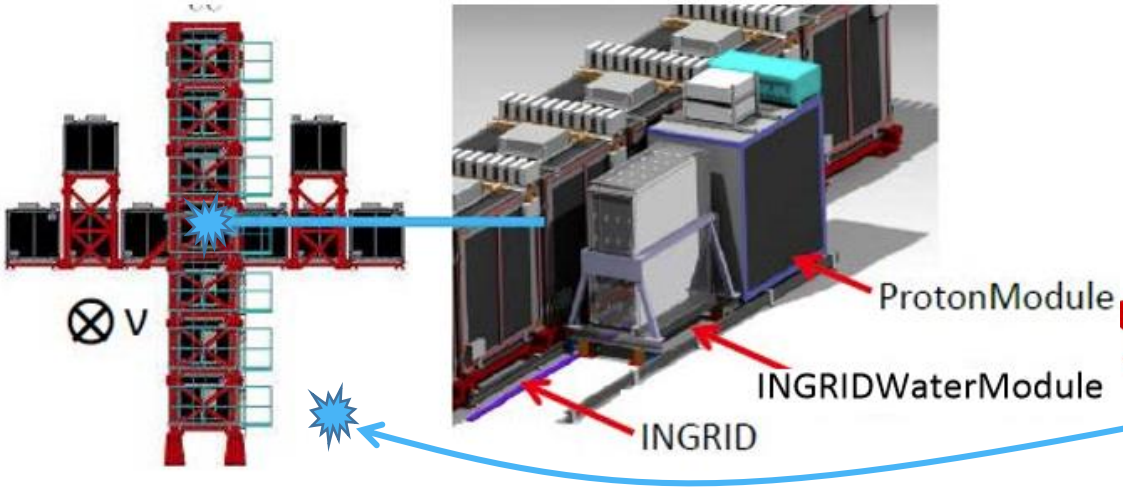
Physics goal

- ***Cross section ratio measurement between H_2O/CH*** for charged-current interaction with different neutrino energy ranges.

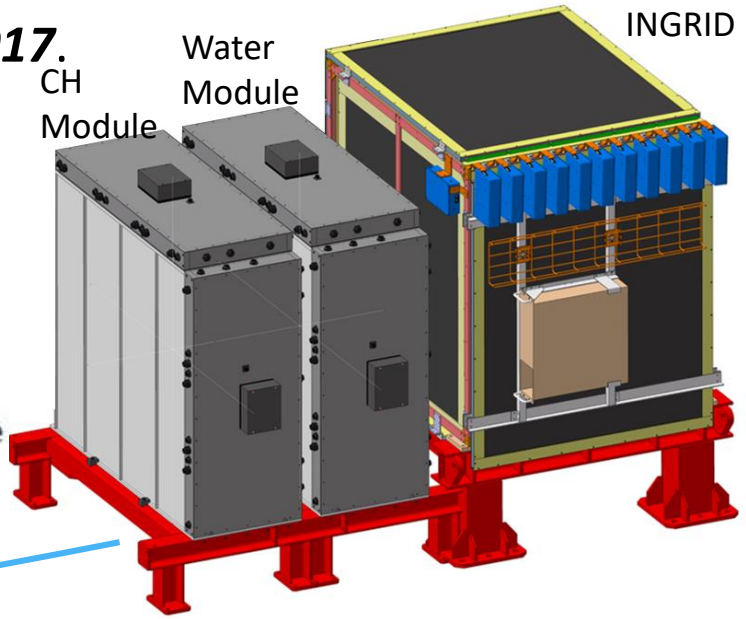
Schedule

- Detector construction: ***Started now!*** Complete H_2O/CH Module ***by Feb/Mar 2017***.
- NU beam data taking: will start ***at the autumn 2017***.

On-Axis (0 deg)

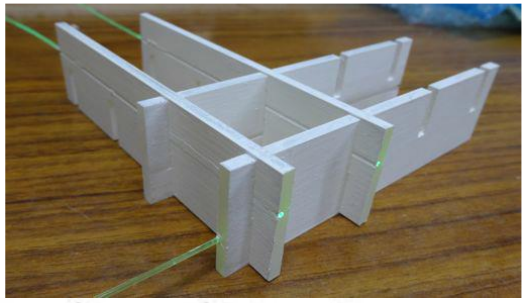


Off-Axis (1.5 deg)

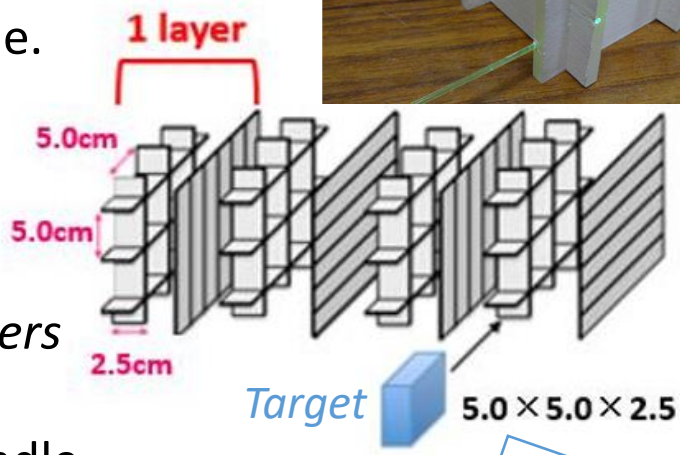


Detector configuration

Three-dimensional grid structure of scintillator bars.

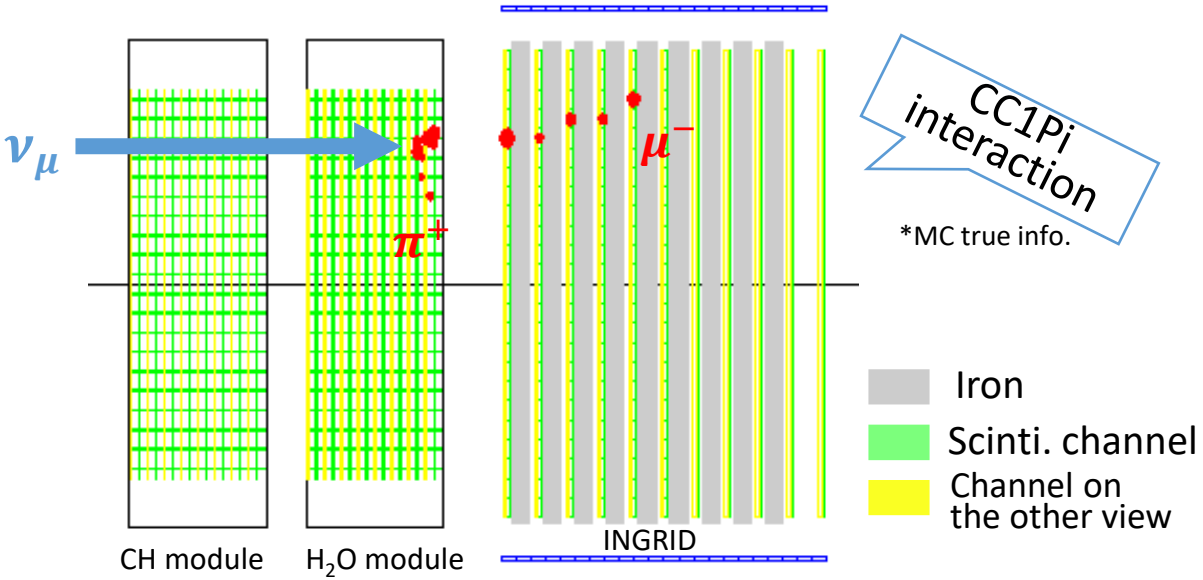


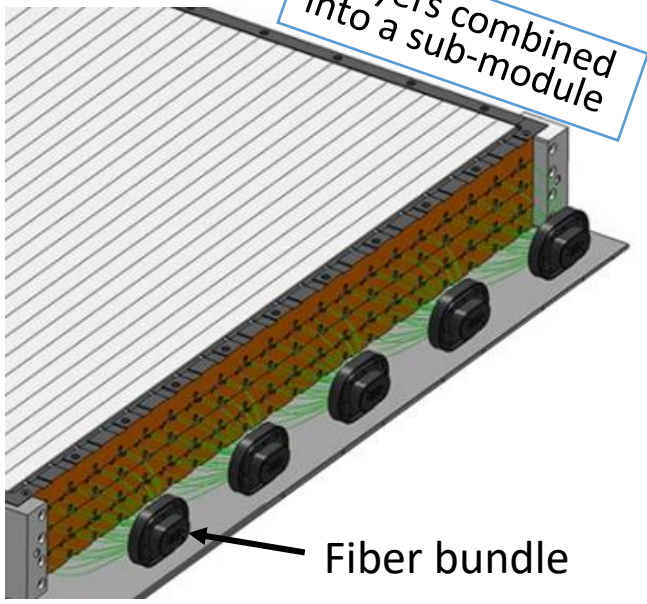
- *4π* solid angle acceptance around target.
- *3-mm*-thick scintillator bars.
  ➔ Large target mass of *80%* in fiducial volume.
- 16 layers compose a H_2O/CH module.
  ➔ *1m x 1m x 0.5m* target region.



Charge measurement

- Scintillation light is collected through *WLS fibers* to 32-channel arrayed MPPCs.
- 32 fibers are gathered together by a fiber bundle.





Neutrino beam measurement

J-PARC Neutrino beam

8-bunch spill structure.

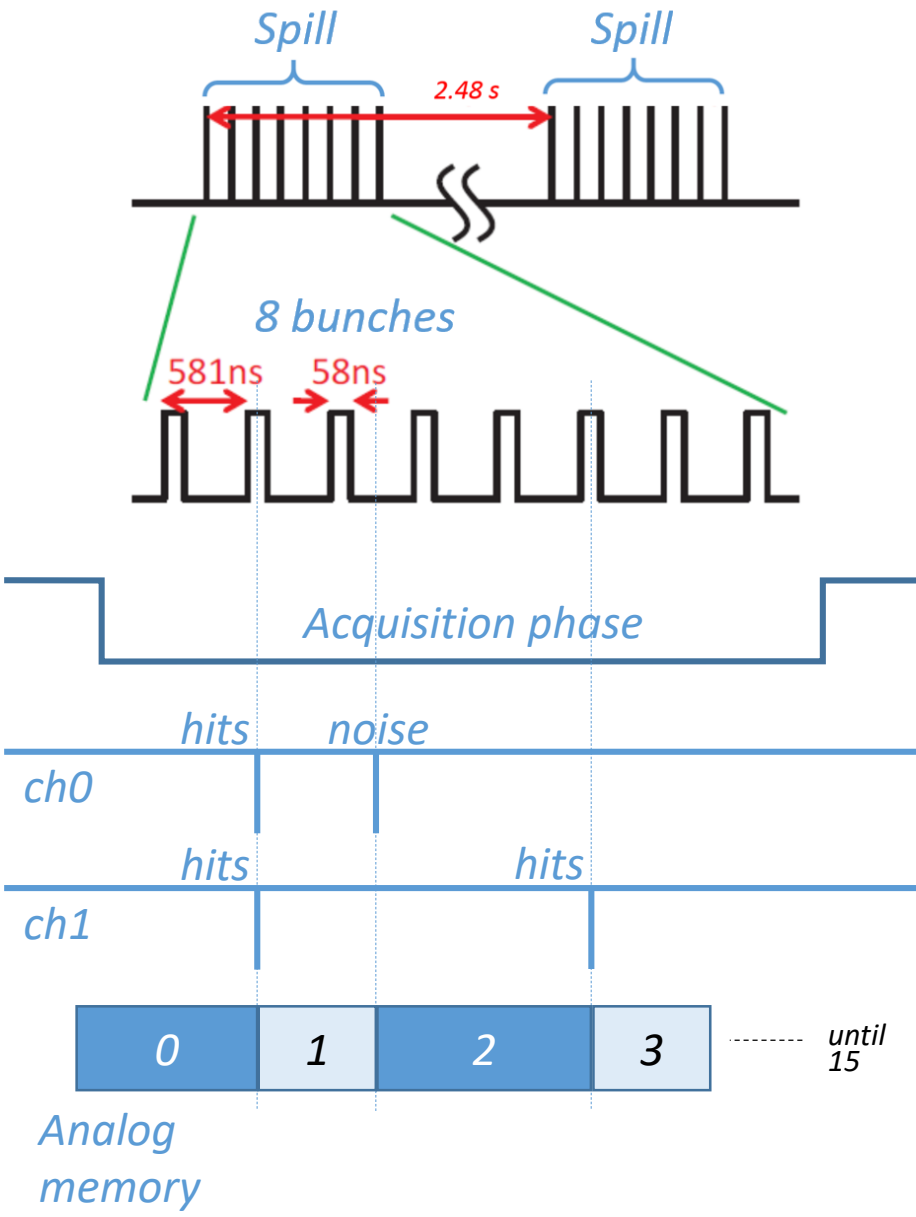
- *2.48sec* cycle.
- 8 bunches w/ *580ns* time gaps.

Requirement

- **Energy deposit** --> Tracking, Particle ID.
  ~10 p.e. in average.
  - Threshold *@1.5 p.e.*
  - High accuracy of *a few %*
- **Hit timing** --> Hit clustering, TOF.
  - *3ns* resolution.

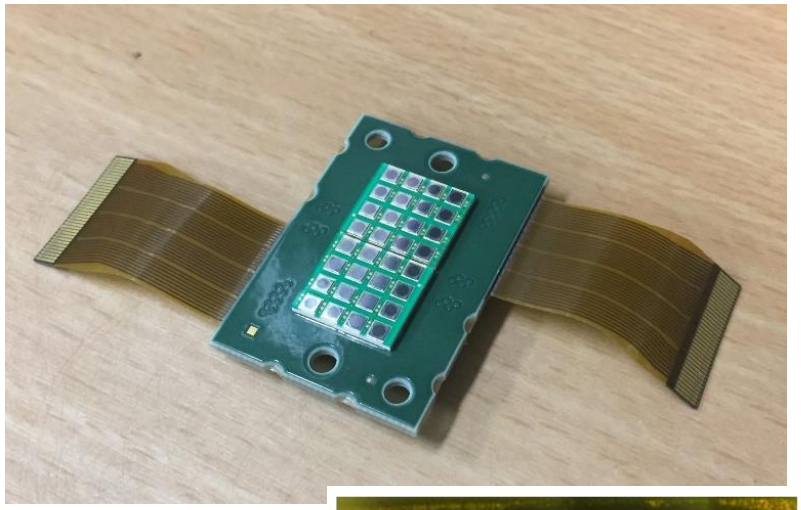
The WAGASCI DAQ

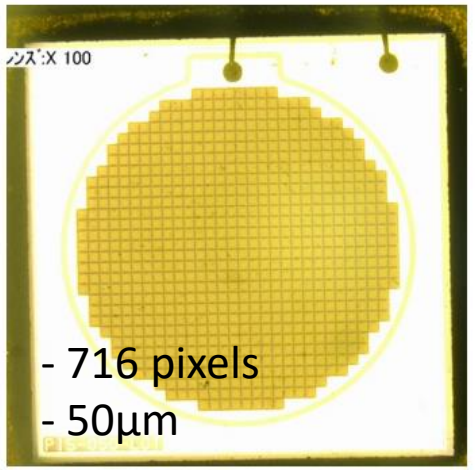
- Open an acquisition gate for the whole period of a spill: *~5 μs*.
- Conversion/readout: *~A few ms*.
- Any hits over a fixed threshold during acquisition period are **automatically triggered chip by chip**.



Photodetector

- 32-channel arrayed MPPC.
  - Type No. S13660(ES1)
  - Dark noise & after pulse suppressed.
  - Noise rate:
    ~6kHz /channel (V_{th}~0.5 p.e.)
    ~100Hz /channel (V_{th}~1.5 p.e.)
    *Over voltage~3.0V
  - Operation voltage: *~56V*
  - Gain: *~10^6*
  - Flexible printed circuit cable.





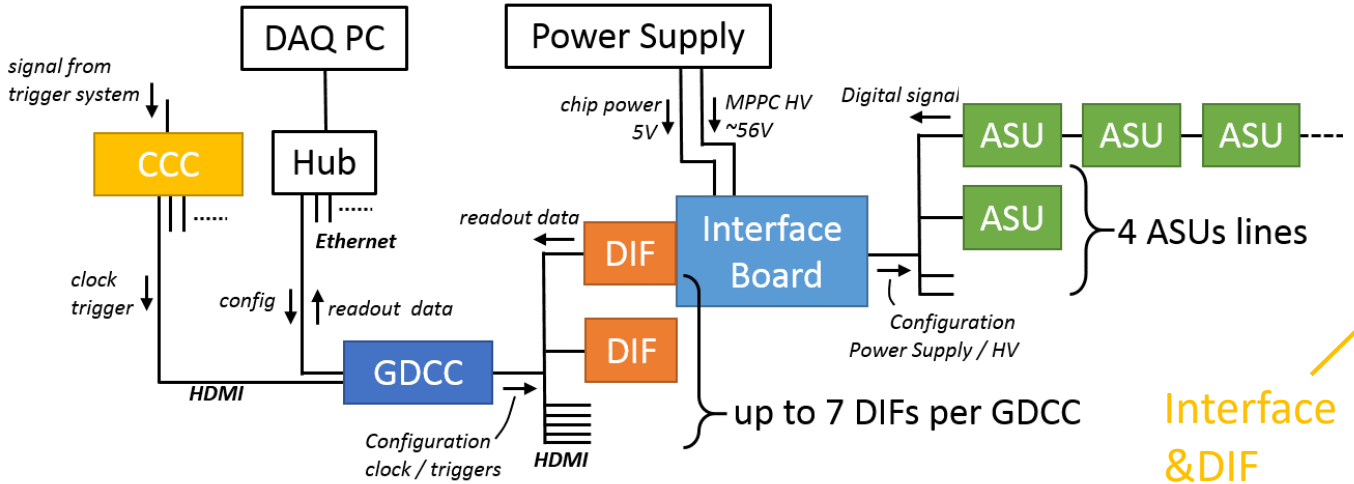
	Number of channel
Water Module	1280
CH Module	1280
INGRID	528

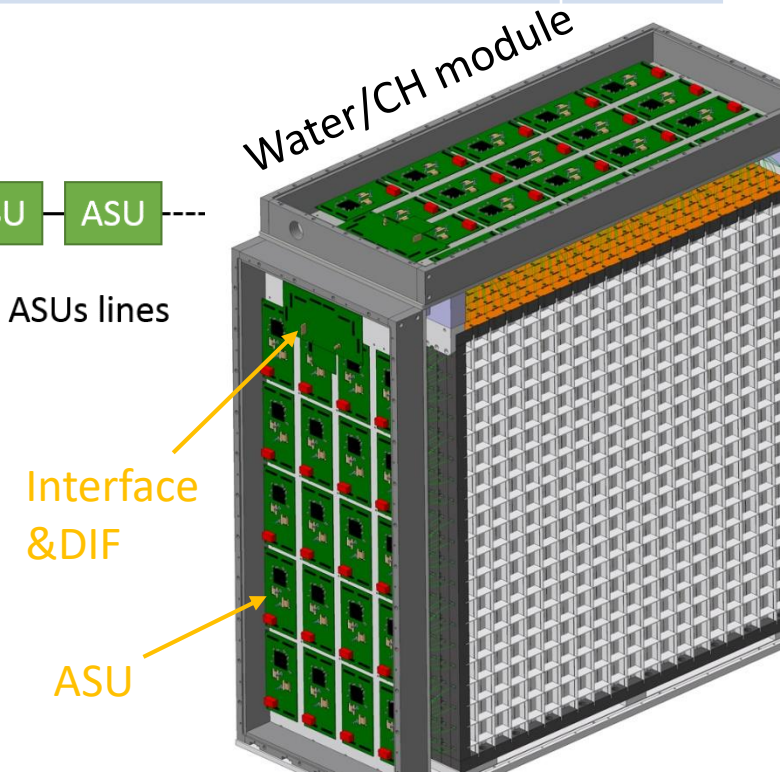
*INGRID modules are not readout by the WAGASCI electronics, but by the T2K electronics with TFBs.

*see supplemental slides.

WAGASCI electronics

Electronics boards		Num /Mod
ASU (Active Sensor Unit)	Readouts a 32ch MPPC array with a SPIROC chip.	40
Interface	Transfers DAQ signals and MPPC bias voltage.	2
DIF (Detector InterFace)	Send DAQ signals and SPIROC configuration.	2
GDCC (Giga Data Concentrator Card)	Transfer signals between DAQ PC and DIFs.	1
CCC (Clock & Control Card)	Provides clock signals and fast control.	1



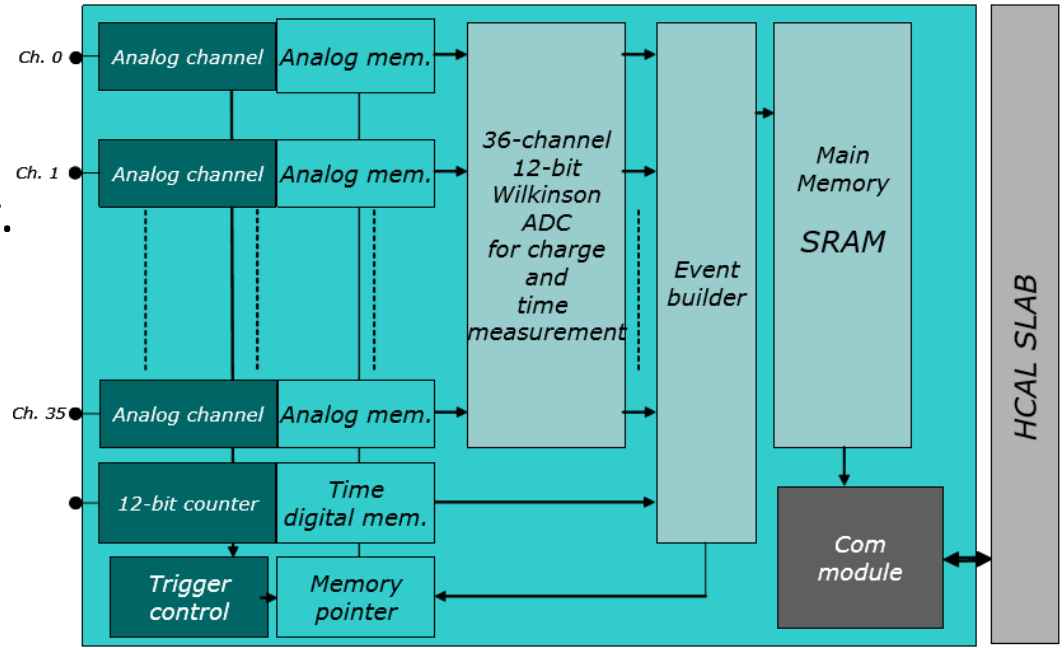


ASIC at front-end readout

SPIROC (Silicon PM Integrated Read Out Chip)

- Product of Omega (France).
- Dedicated very front-end ASIC for an ILC.
- Both analog signal processing and digital are contained in chip.

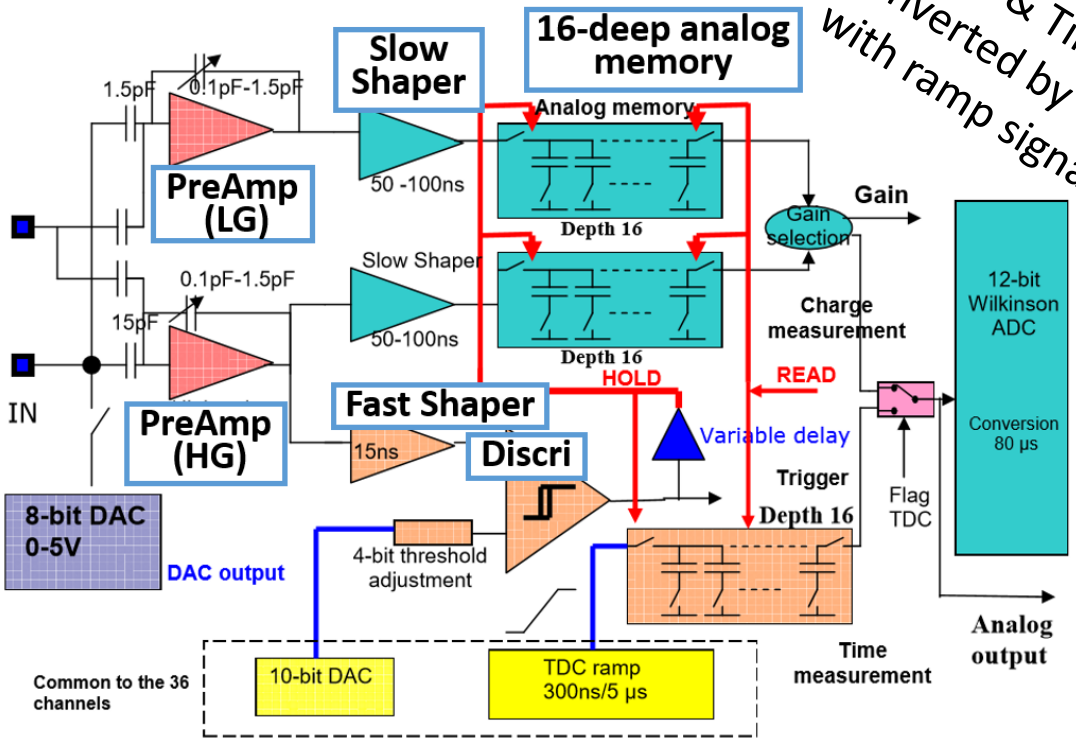
- **Charge measurement.**
  2 gains/ 12-bit ADC → wide dynamic range: *1pe – 2000pe*.
- **Time measurement.**
  12-bit TDC with *~100ps* step.
- **Auto-trigger**.
  Internal discriminated signal is used for *Track-and-Hold circuit*.
- **36-channel** readout.
- **16-deep analog memory.**
- *CQFP240* package.
- *5V/3.5V* operation.
- *25μW* per channel

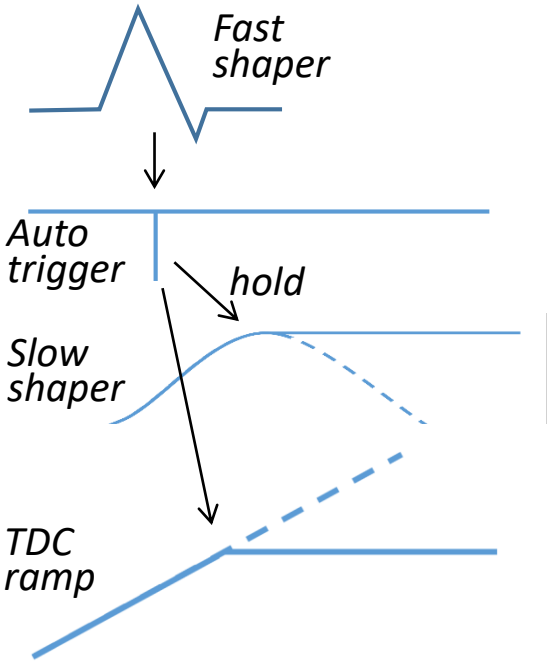


SPIROC2D analog part

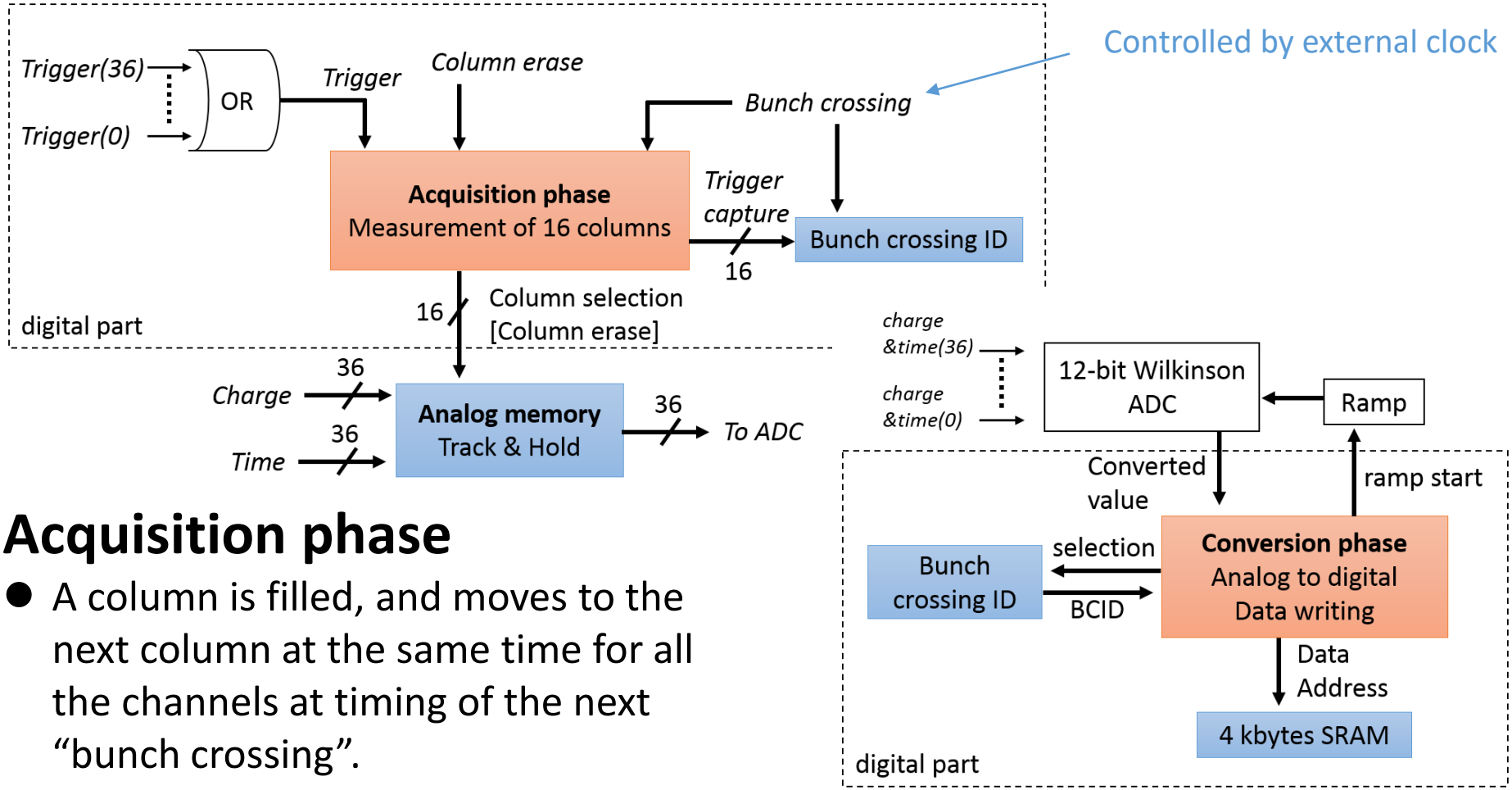
- PreAmp
  - ✓ Low gain: x1 - x15
  - ✓ High gain: x10 - x150
- Slow Shaper
  - ✓ 50 - 100ns shaping time
  - ✓ Charge is stored in analog memories with Track&Hold
- Fast shaper & Discriminator
  - ✓ 15ns shaping time
  - ✓ 10-bit DAC threshold
  - ✓ Auto-triggering with this discriminated signal
  - ✓ Time measurement

Charge & Time is converted by the ADC with ramp signals.





SPIROC2 digital part



Acquisition phase

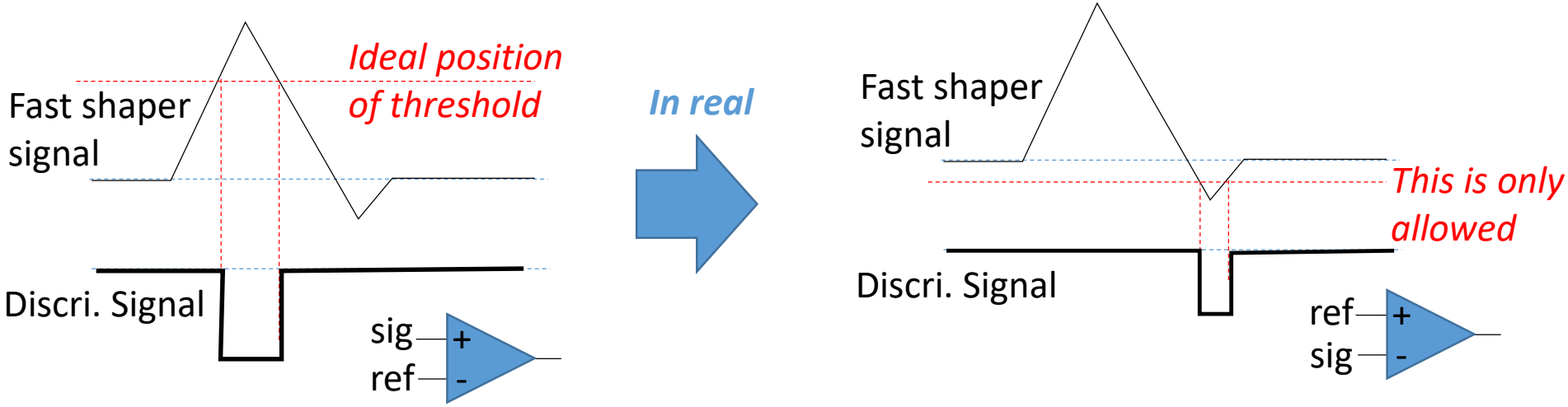
- A column is filled, and moves to the next column at the same time for all the channels at timing of the next "bunch crossing".
- "Bunch crossing" is a coarse time flag for the triggers.
- BCID is controlled by external 2.5MHz clock.

Conversion phase

- 36 charge/36 timing in the analog memory are sequentially converted at an ADC with using ramp signals.
- The digital data are stored in 4kbytes SRAM.

Issues on SPIROC2D

- It is only possible to set the discriminator threshold at its undershoot.
  - Due to wrong position between signal and reference in the comparator.



➔ Much more sensitive to noises on ground.

➔ But still able to trigger on 0.5 p.e. level.

- Column 10&14 do not work.
  - Reset of the column is not properly done.
  - Still able to be used for T2K neutrino beam structure with 8 bunches.

➔ ***Requirement***: Rate of noise and hits from cosmic rays << *2 per spill*

➔ ***OK***

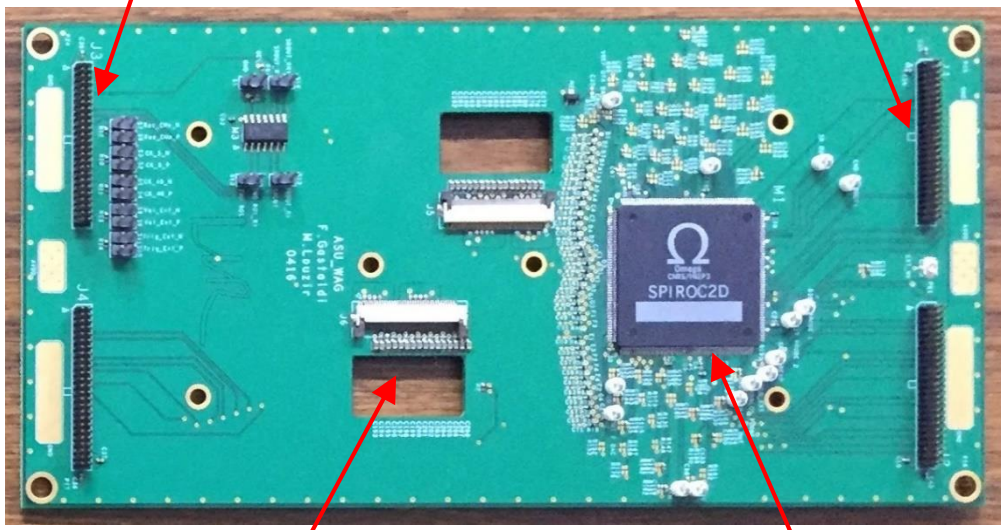
*MPPC noise rate:~10^{-2}/32ch/5μs@1.5PE_{th}, Cosmic ray hits: <4x10^{-3}/32ch/5μs@ground

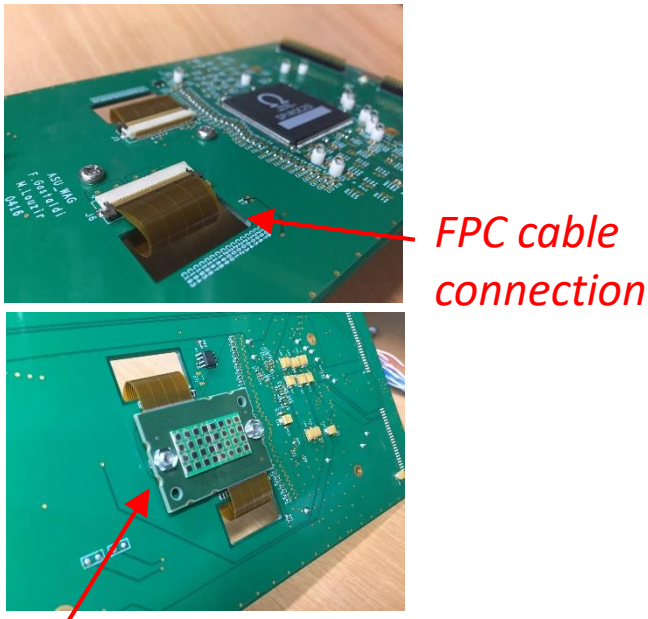
Front-end boards

F. Gastaldi & M. Louzir

ASU (Active Sensor Unit)

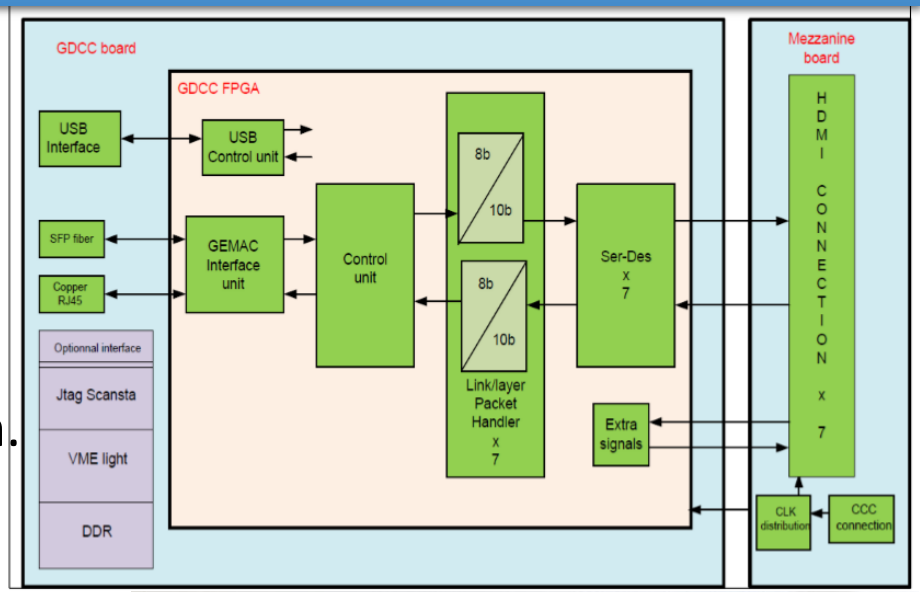
- A SPIROC2D is embedded.
- Direct connection to 32-channel arrayed MPPC.
- 50-pin connection to an Interface board.
- Another ASU board can be put serially via the 50-pin connection.



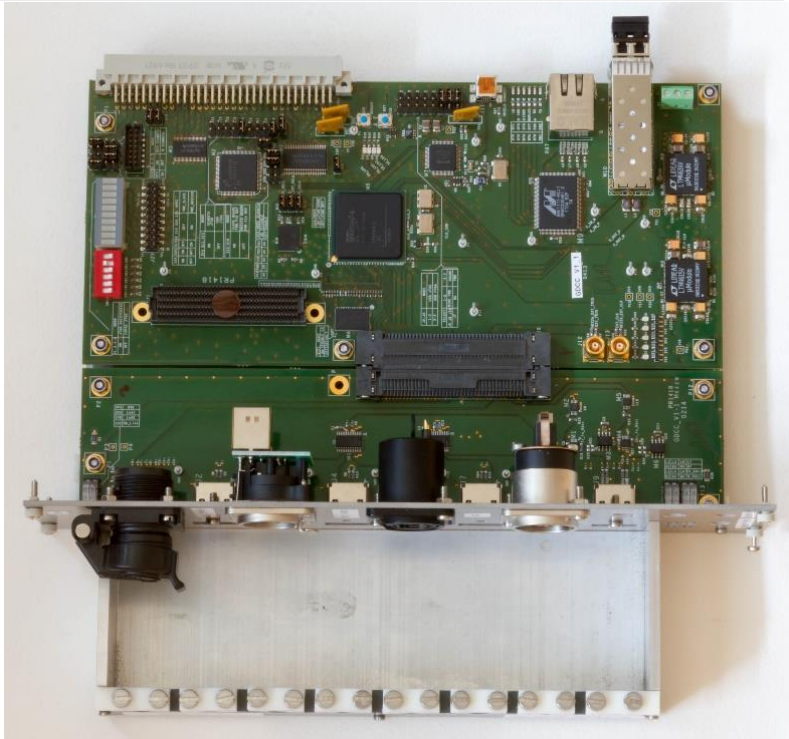


Back-end boards

- **GDCC** (Giga Data Concentrator Card)
  - Designed on 6U VME format.
  - 7 DIFs connections (HDMI). 50Mb/s.
  - 1 CCC connection (HDMI).
  - XILINX FPGA Spartan6.
    - Connection's speed auto-negotiation.
    - Preamble bits.
    - Trailer check-sums.



- **CCC** (Clock & Control Card)
  - The GDCC board can also be operated in CCC mode, just by programming the CCC firmware.
  - Generate/distribute 50MHz clock.
  - Synchronize the whole DAQ system.
  - Receive spill signal from beam trigger.



cnrs dépasser les frontières
IN2P3 Les deux infinis
ÉCOLE POLYTECHNIQUE UNIVERSITÉ PARIS-SACLAY

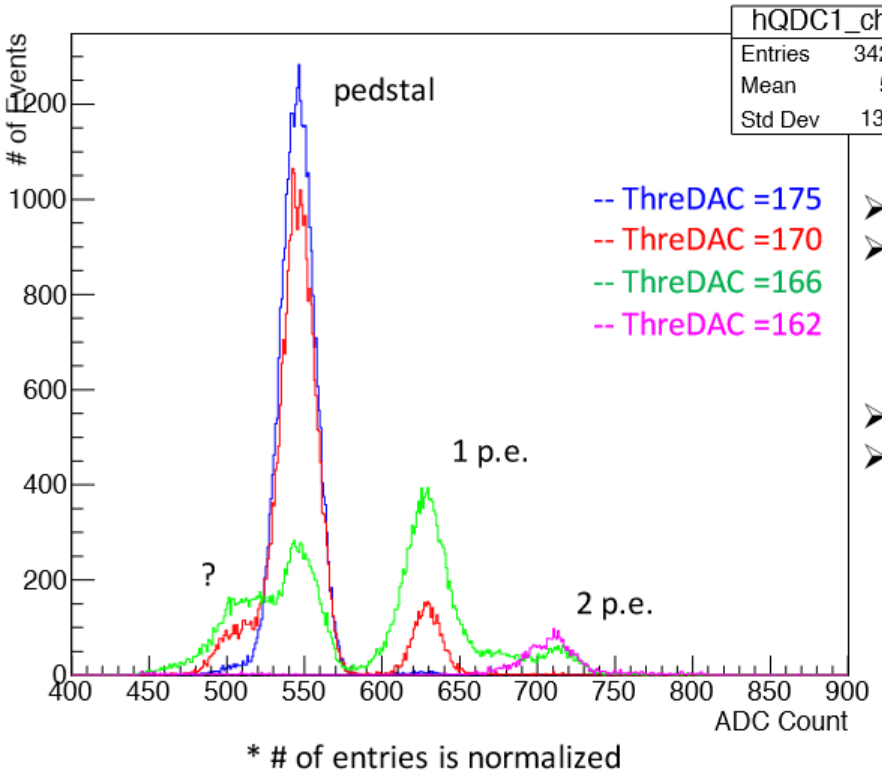
Status of electronics development

Production

- ASU, Interface – Test production is done. Tested at Utokyo & Ecole Polytechnique.
- GDCC, CCC, DIF – Final production is done. Tested at Ecole Polytechnique.

Test operation has been done.

- Periodic data taking only with MPPC dark noise.
- Confirmed it could be operated at threshold of 1.5 p.e.



* # of entries is normalized

Threshold

Good

- trigger channel : single (0ch)
- Overvoltage : ~2.1V
  - ✓ HV :56.0V
  - ✓ breakdown Voltage:51.4V
  - ✓ InputDAC value : 1(2.5V)
- Gain value(capacitance) : 60
- Gain Select : OFF
  - ✓ (this means that the data takes by HighGain)

- Event rate matches darknoise & crosstalk rate !

Bunch crossing

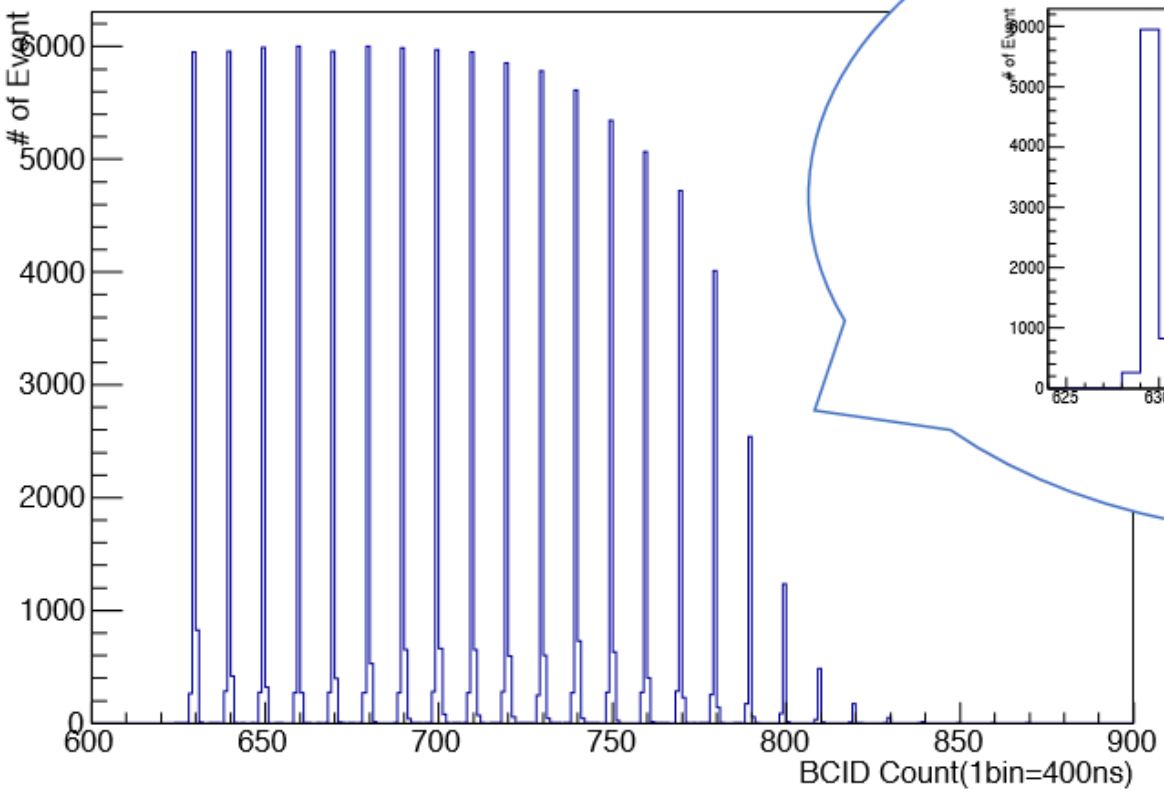
BCID

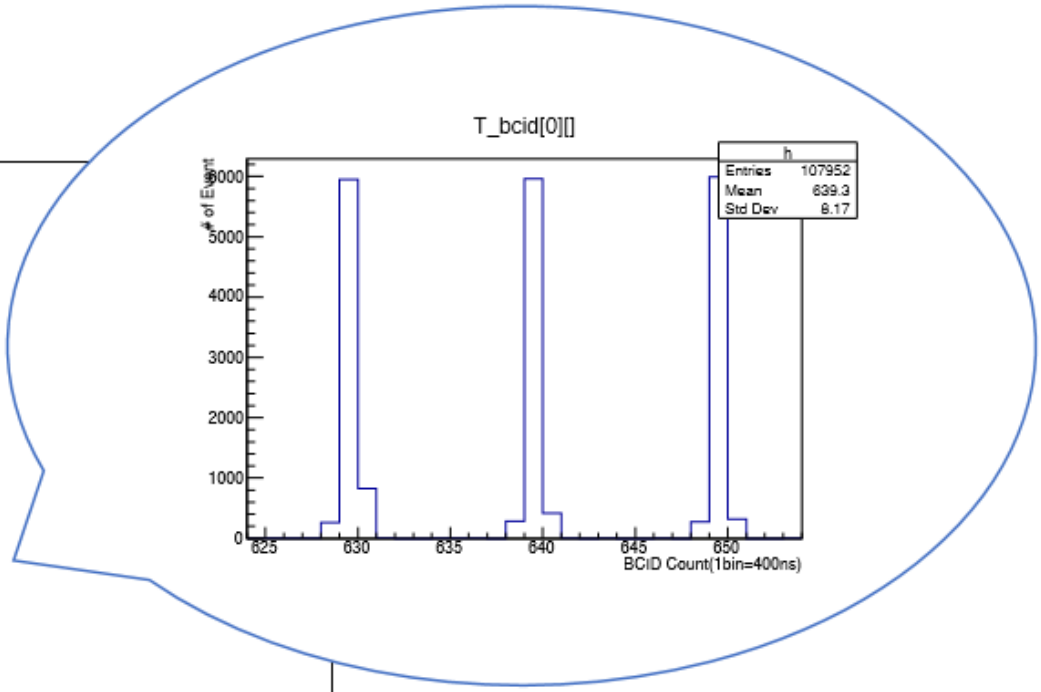
Good

- Bunch crossing ID. coarse timing of triggers.
- Bunch structure is well seen.
  - ✓ Peak width : ~1 bin
  - ✓ but a bit broad…?

- ✓ trigger channel : single (0ch)
- ✓ Bunch: width=50ns, freq:250kHz (10bin)
- ✓ Threshold : 2.5p.e. level (DAC value=160)

T_bcid[0][]

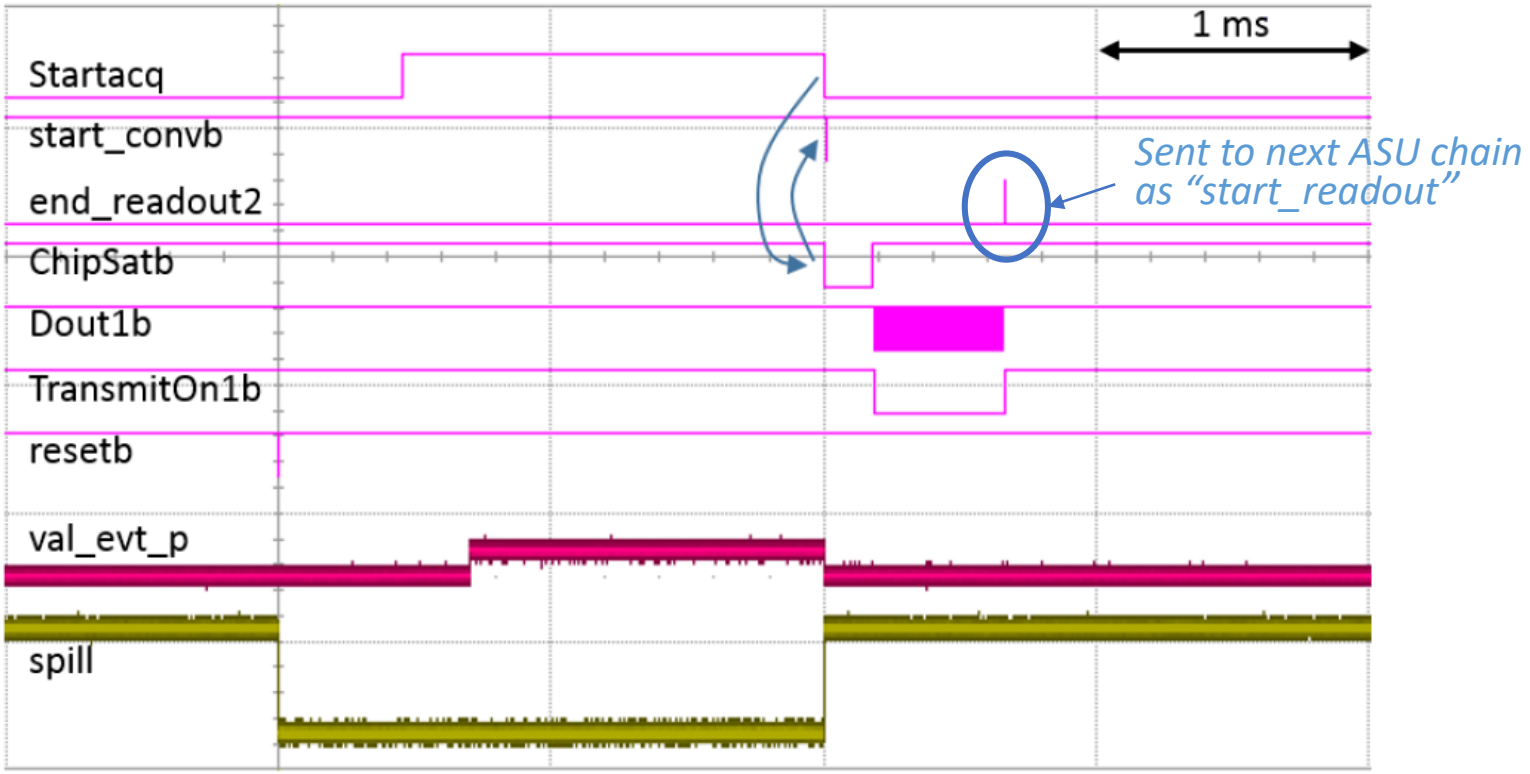




*LED keeps injected during the whole acquisition period.
*Some events filled into two columns, due to reflection or slow recovery.

DAQ signals

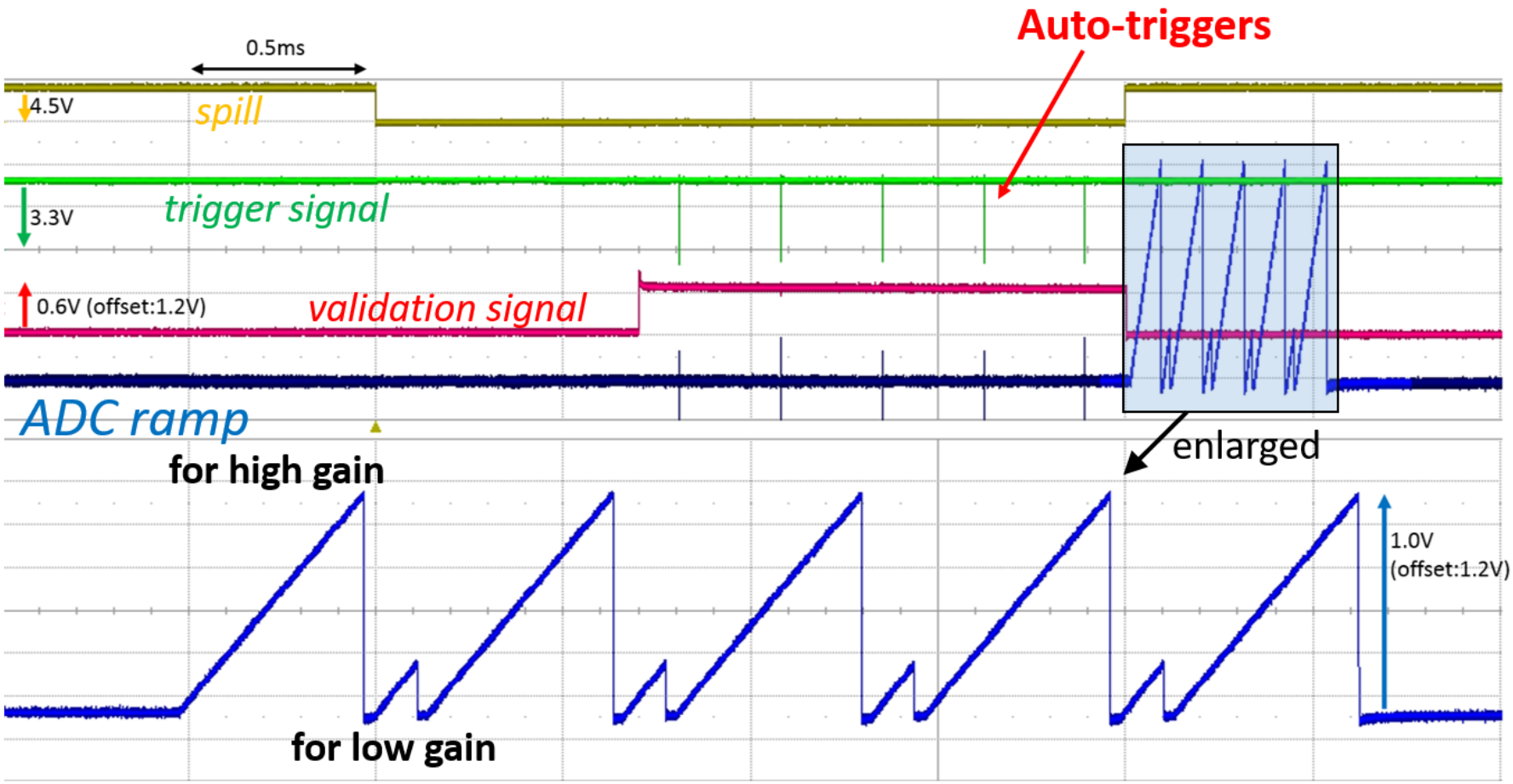
- Reset ⇒ Acquisition ⇒ Conversion ⇒ Readout.
- Output data (Dout1b) are transmitted to back-end boards.
- Conversion starts (start_convb) after all of 16 analog memories are filled (ChipSatb).
- Auto-triggers are only valid during the validation signal (val_evt_p) from DIF.



Ramp signals

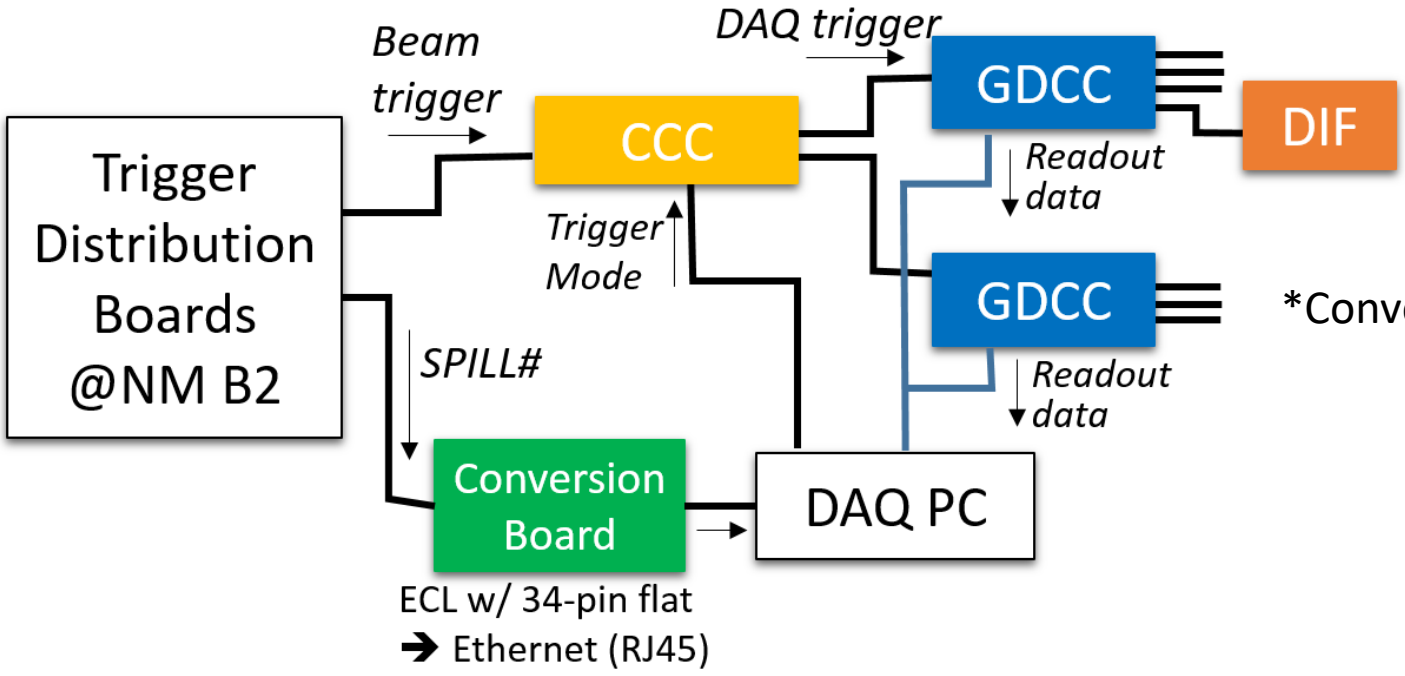
- SPIROC2B/D contains two PreAmps of different gains.
- 12-bit Wilkinson ADCs are embedded for each.
- Correct behavior of ADC ramp signals.
  - $N_{peak\text{-}ADCramp} = 2 \times N_{trigger} - 1$
  - in order of high, low, high, ... , high

*SPIROC2B ignore the first ADC ramp for low gain because of its fluctuation. This is solved in SPIROC2D.



Neutrino beam synchronization

- **Beam trigger** signals are sent to CCC.
  - ✓ Data acquisition is done every spill. → Every 2.48sec.
  - ✓ The whole DAQ system is **synchronized to 50MHz** clock generated on CCC.
- Event tagging system:
  - ✓ ***SPILL# information*** is merged into the readout data at DAQ PC.
  - ✓ Readout data contain ***BCID*** (bunch crossing ID), that gives timing of each auto-trigger as count of 2.5MHz clock signal after acquisition starts.

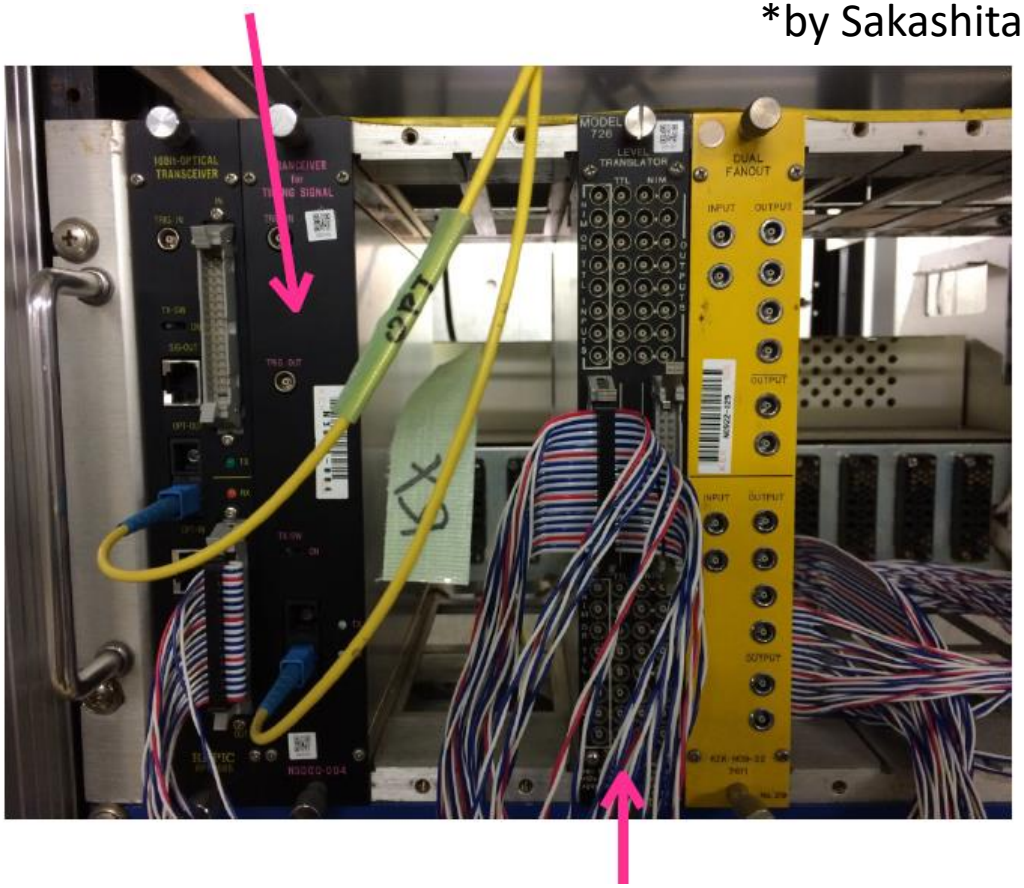


*Conversion board candidate.

Beam trigger & spill# system @NM B2floor

Synchronous beam triggers are distributed out through “TRIG OUT”
*NIM level / LEMO connection

*by Sakashita-san



✓***Pre-beam trigger***
→ *100msec* before beam trigger.
* w/ 16-bit spill number

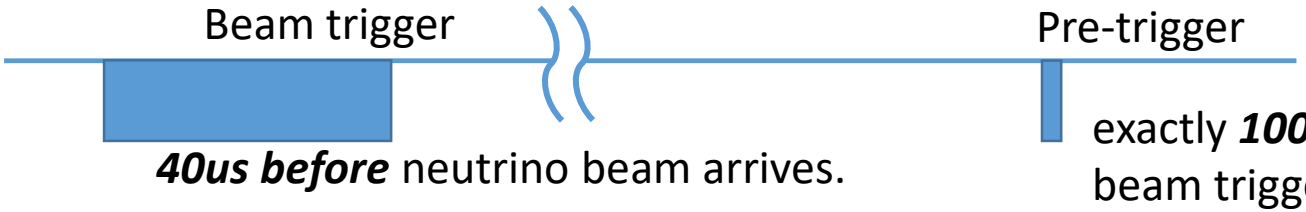
✓***Beam trigger***
→*40usec* before neutrino arrives.

*SPILL# offset should also be taken into account.

SPILL# (lower 16-bit) is distributed out from 16-bit output of ECL/NIM converter module.
*ECL / 2.54-mm-pitch 34-pin flat connection (or 16 NIM out / LEMO)

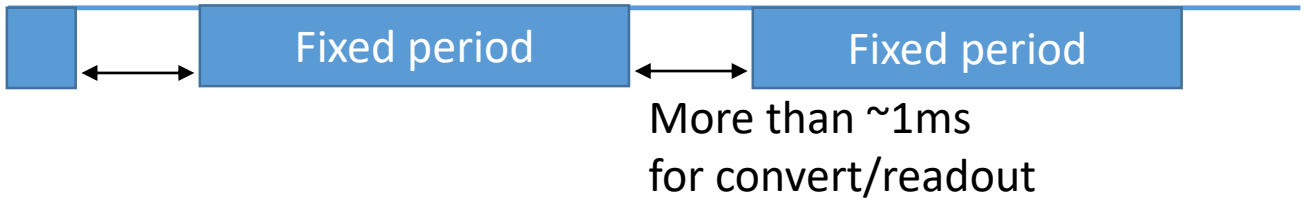
Trigger patterns

① Beam



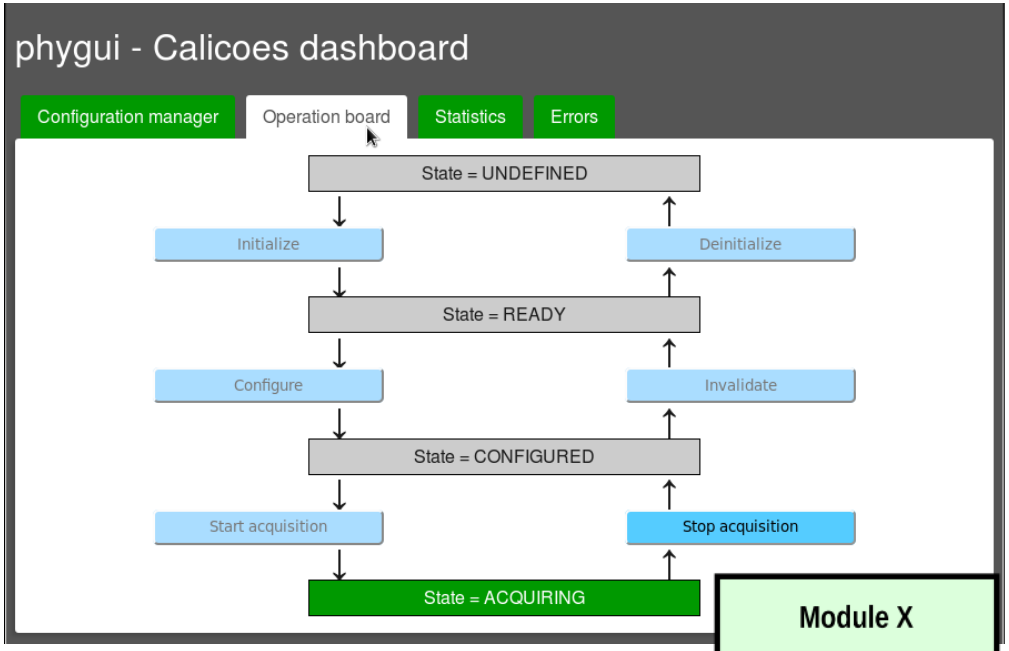
*Pre-trigger stops all the other triggers' activity.
*Beam trigger width/delay must be adjusted on CCC.

② Periodic



*Acquisition width must be calculated and fixed by using noise rate for filling many of 16 deep memories.
*Max of DAQ frequency is 100Hz, due to handshake b/w DIF and GDCC.
*Margin time between beam triggers can also be used for periodic acquisition.

Software



launch_calicoes_gnome.sh
Launch the software

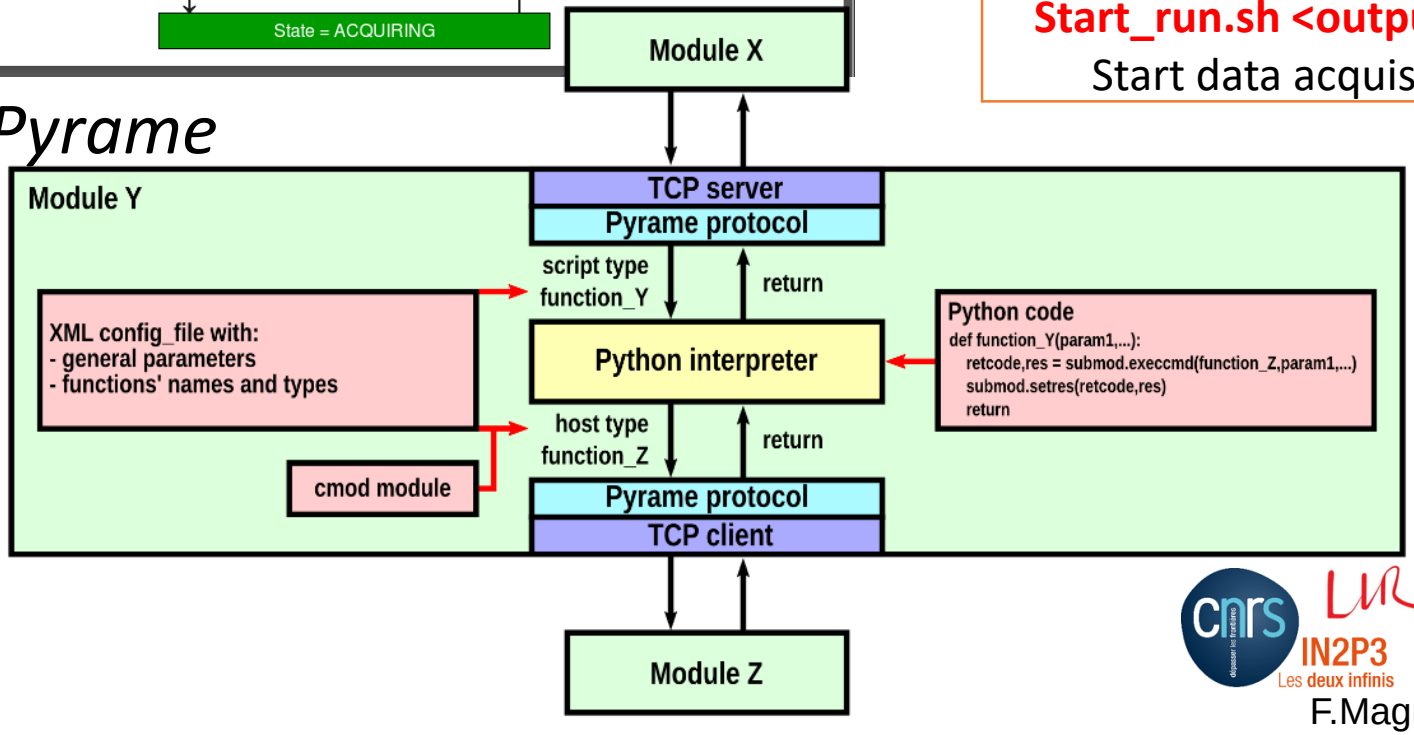
load_config.sh <config_file>
Load configuration file

Initialize.sh
Define commands in software

configure.sh
Send configuration file to chip

Start_run.sh <output_file>
Start data acquisition

Pyrame



F.Magniette, M.Rubio-Roy

Summary & Future

Summary

- The WAGASCI electronics has been designed with SPIROC2D.
- Test operation is being performed at LLR and UTokyo.
- Synchronous readout system for neutrino beam is being designed.

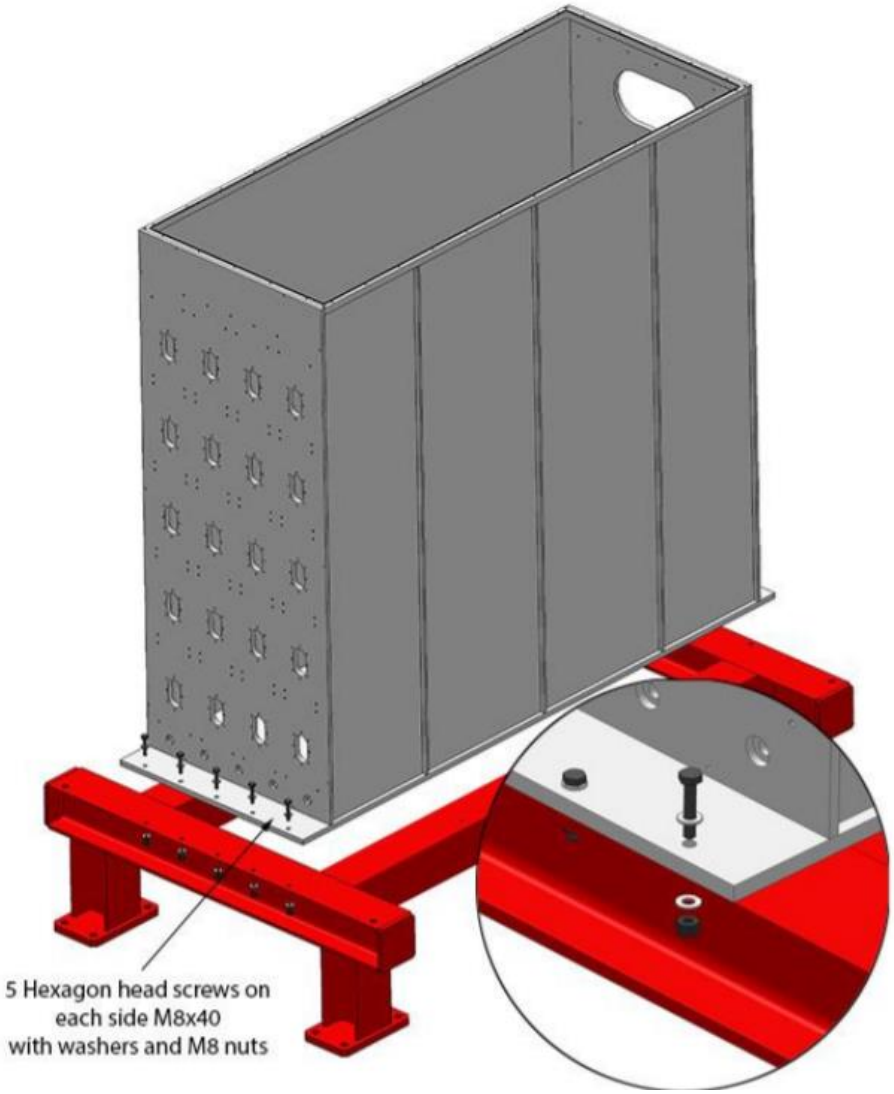
Schedule

- The whole DAQ system construction by beginning of 2017.
- Will be ready at spring 2017, after test operation and modification.

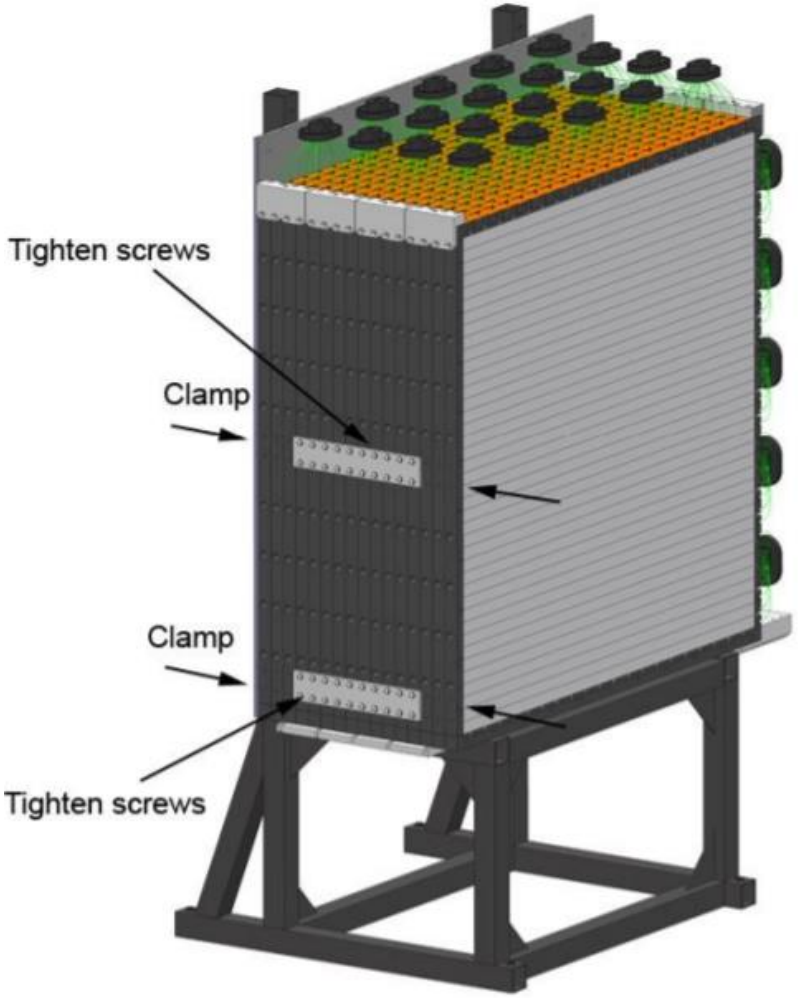
Supplemental slides

The WAGASCI detector

Water tank



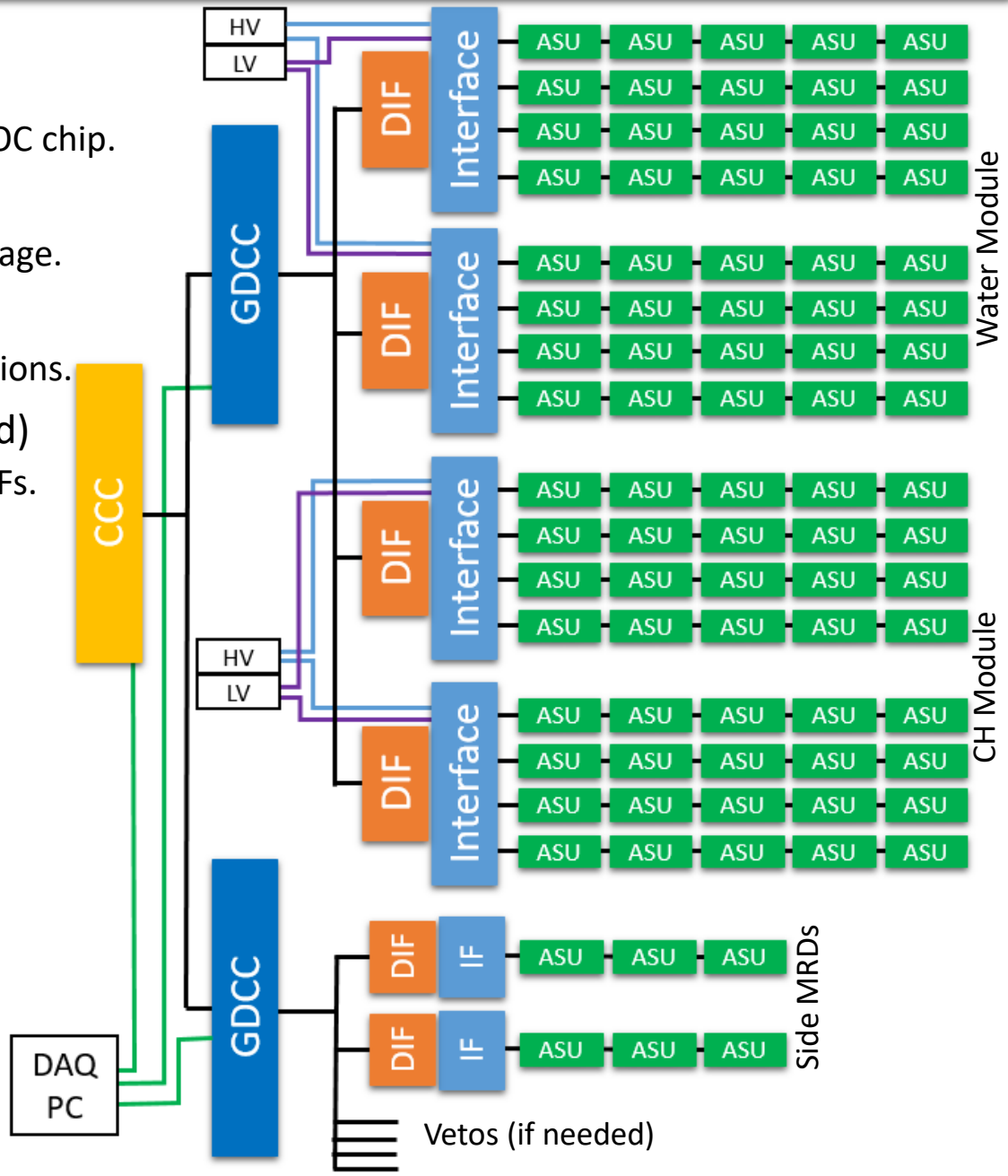
Module



WAGASCI DAQ system

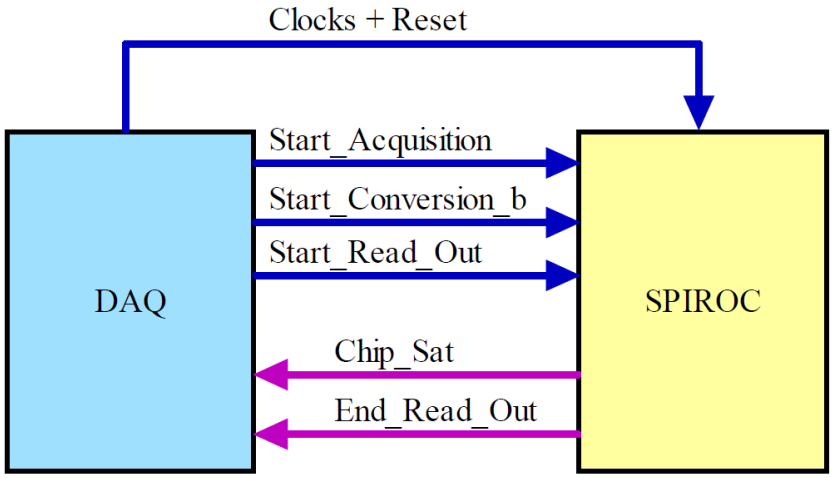
- **ASU** (Active Sensor Unit)
  Readout a 32ch MPPC array with a SPIROC chip.
- **Interface**
  Transfer DAQ signals and MPPC bias voltage.
- **DIF** (Detector InterFace)
  Send DAQ signals and SPIROC configurations.
- **GDCC** (Giga Data Concentrator Card)
  Transfer signals between DAQ PC and DIFs.
- **CCC** (Clock & Control Card)
  Provide clock signals and fast control.

Modules	# of channels
WaterModule	1280
CH Module	1280
SideMRD (right)	88
SideMRD (left)	88
Vetos	?

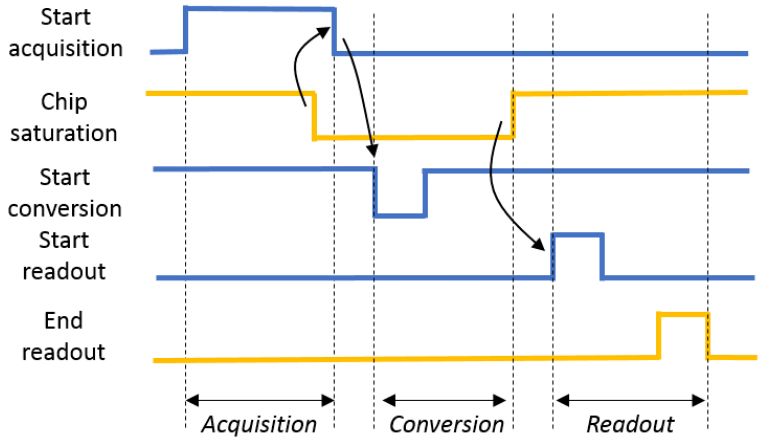


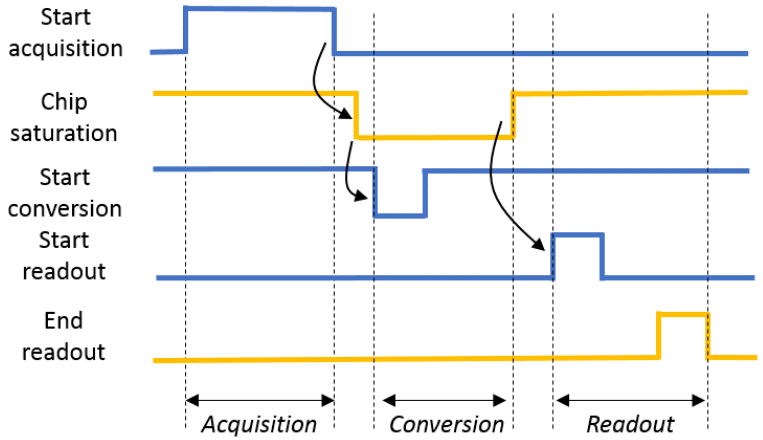
SPIROC DAQ signals

DAQ signals



Main Signals between DAQ and SPIROC

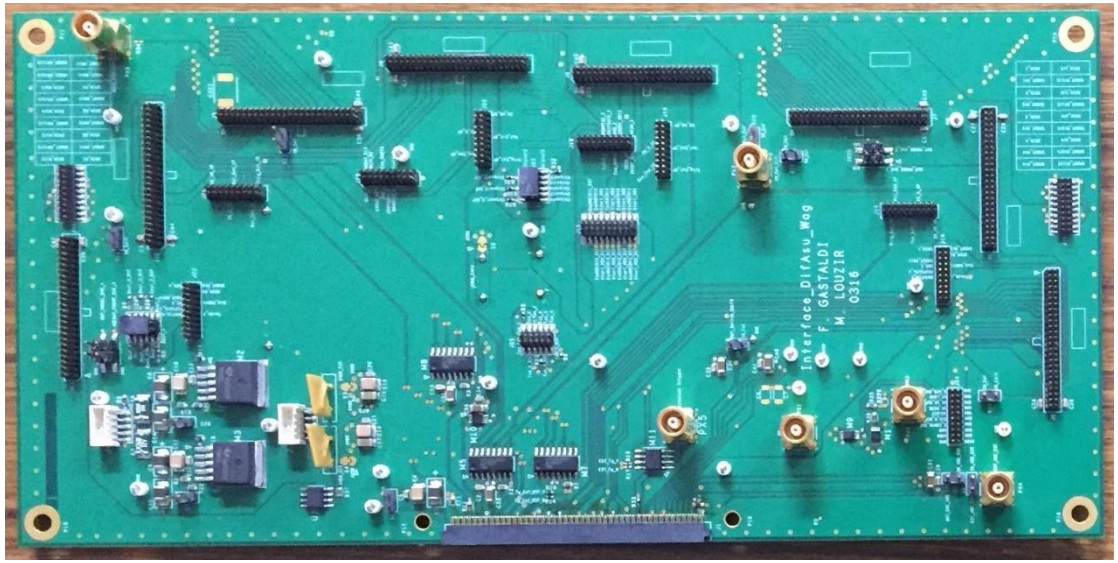




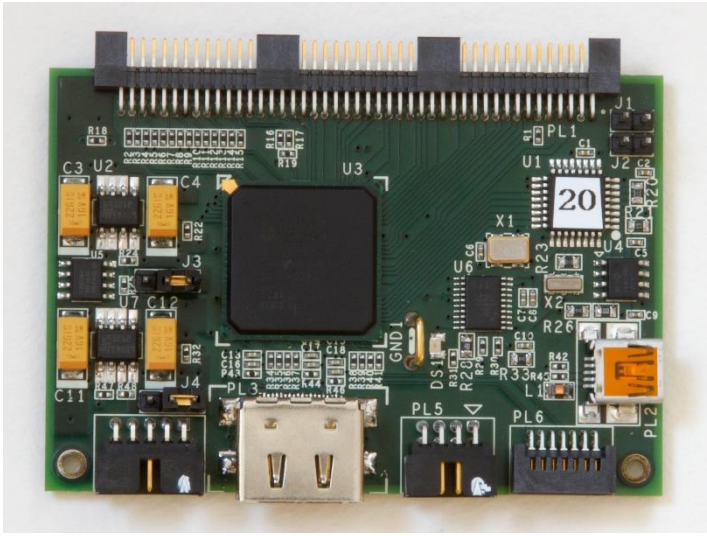
Interface boards

- Interface board
  - 4 ASU chains connection.
  - HV supply connection for all MPPCs via connected ASUs.
  - LV supply connection for DIF and ASUs.
- DIF
  - Send digital signals to all ASUs.
  - Receive raw data from ASUs, and send it to GDCC with header/trailer.

Interface



DIF



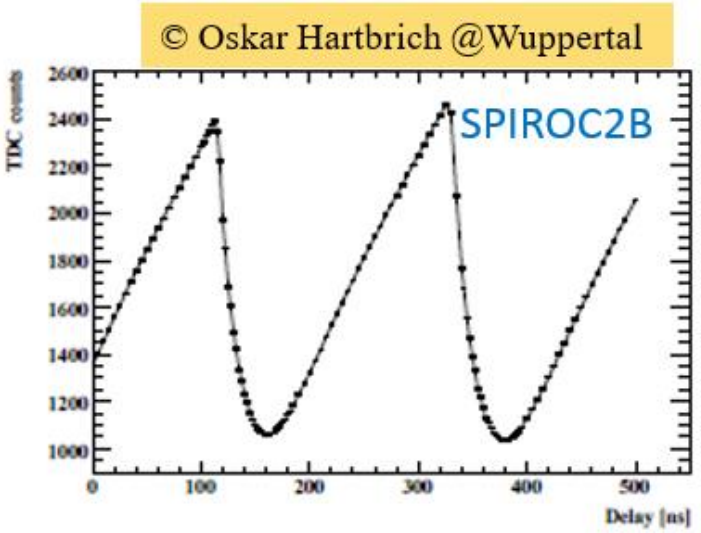
SPIROC2D : Main improvements

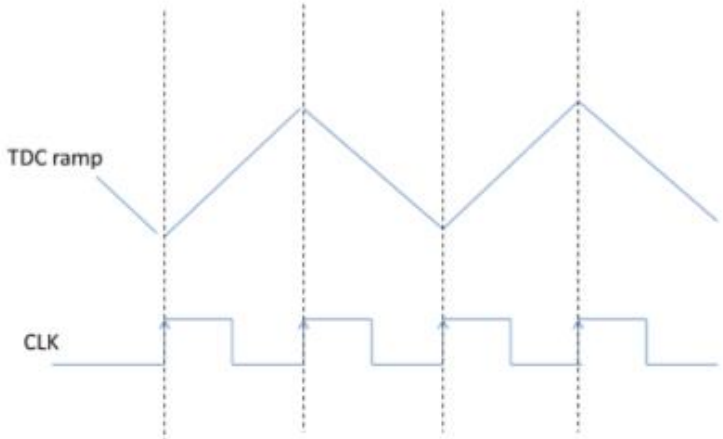
- Many modifications
  - ✓ Most of them tested in Spiroc2c
    - Individual Tunable Gain LG, HG
    - Crosstalk between HG and LG
    - "Zero event" suppression **: CHECKED, OK !**
    - Rate dependency **: CHECKED, OK !**
    - new TDC
    - new Delay cell **: CHECKED, 1 ch fired shows same delay as 36 ch fired**
    - AutoGain fixed **: CHECKED, OK !**
  - ✓ New External Trigger scheme **: CHECKED, OK !**
  - ✓ **Digital part**: Timestamp counter 12 ➔ 16 bits **: CHECKED, OK !**
  - ✓ Improved Input DACs (with probe system)
    - Protection added (PAD Diodes + internal 100ohm)
  - ✓ Channel to channel uniformity **: CHECKED, OK !**
  - ✓ 4-bit DAC adjustment ch. by ch. : no influence on global threshold **: CHECKED, OK**
  - ✓ Temperature sensor added
  - ✓ LVDS receiver boosted for NoTrig/RazChn

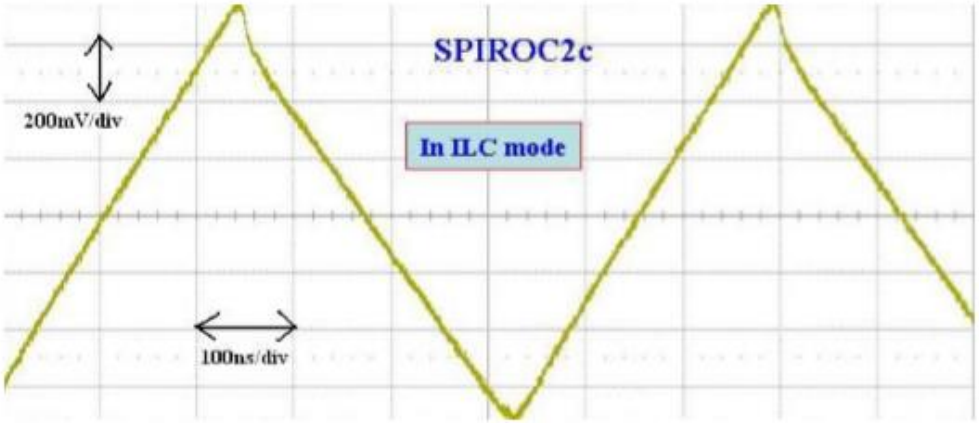
callier@omega.in2p3.fr

SPIROC 2c: TDC improvements

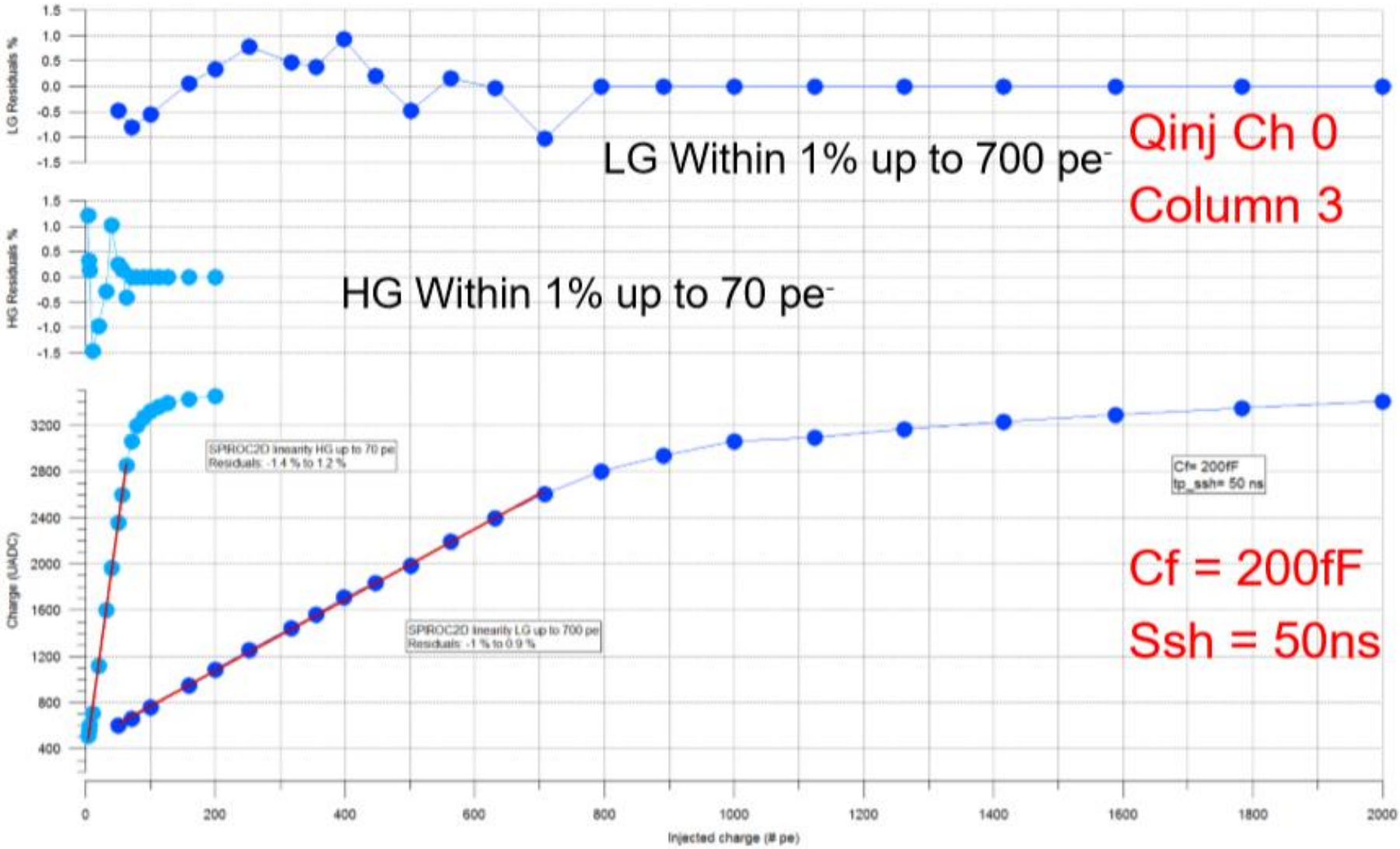
- Modifications on the TDC
  - To decrease dead time during transition => alternation of a rising and a falling ramp implemented
  - Conservative modification but not completely satisfying solution
  - Anyway, a new TDC has to be re-designed in SPIROC 3







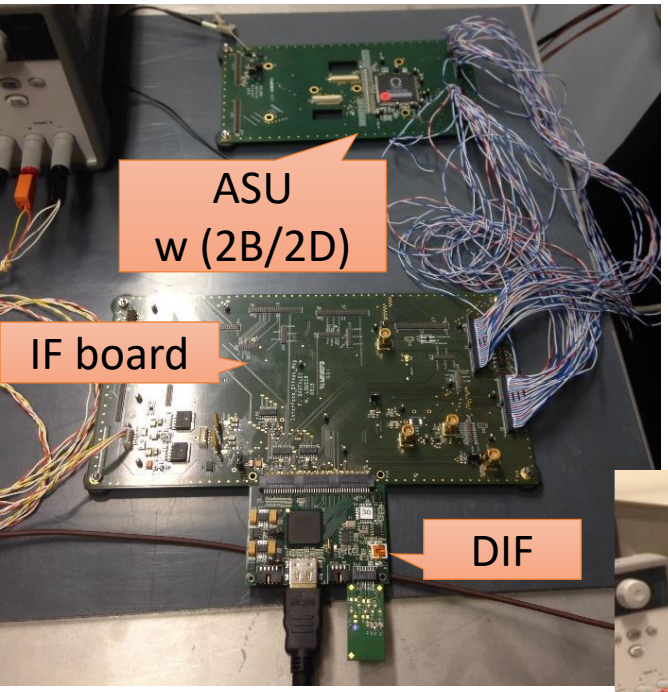
SPIROC2D : Linearity of Charge Measurement

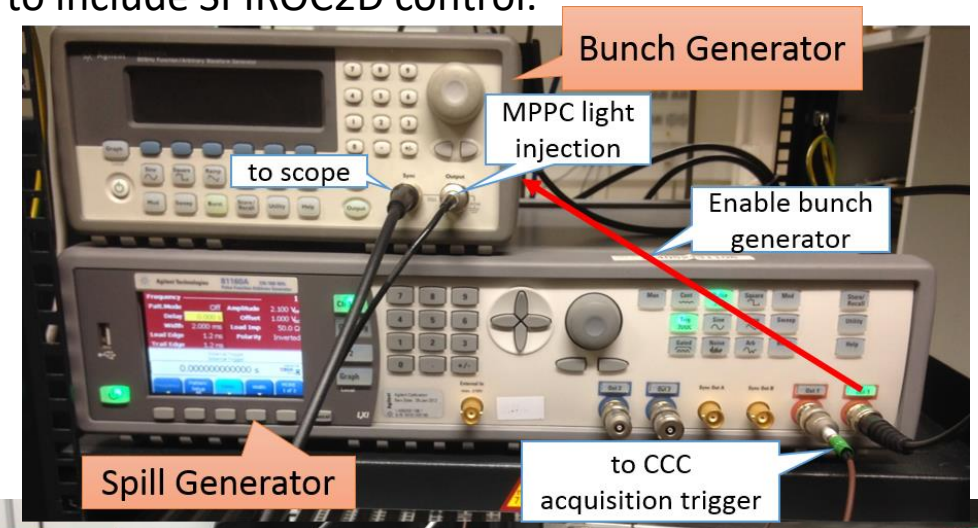


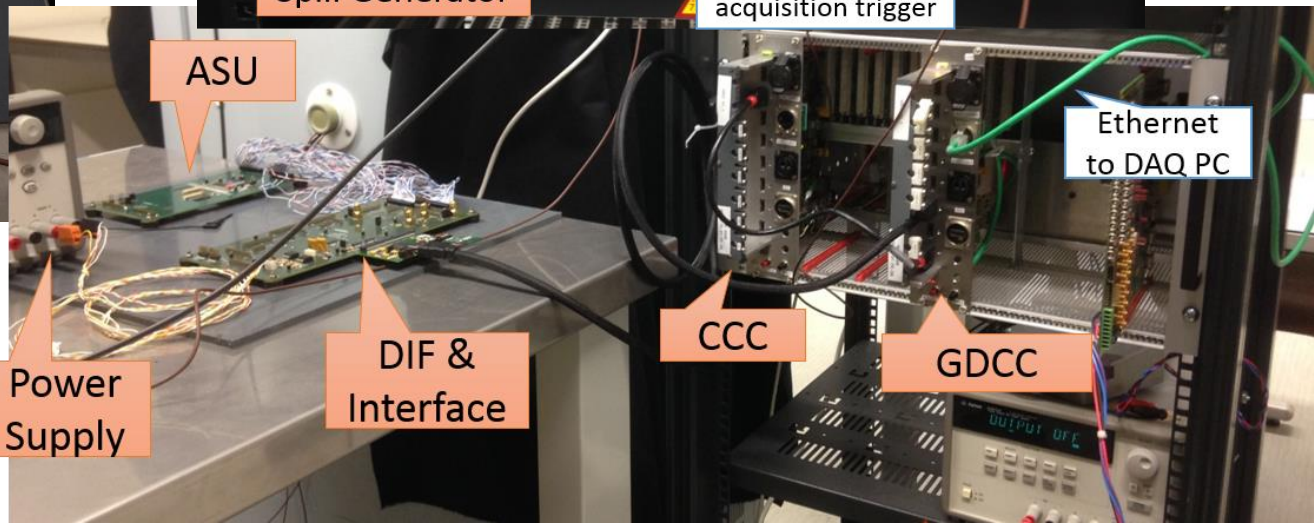
Test operation at LLR

Modules

- New: prototype for the WAGASCI electronics.
  - ✓ new ASU(with SPIROC2B/2D) ... connection with 36-pin FFC.
  - ✓ new Interface board ... transfer of power supply, configuration from DIF, and data from ASU.
  - ✓ new DIF ... the firmware is updated to include SPIROC2D control.



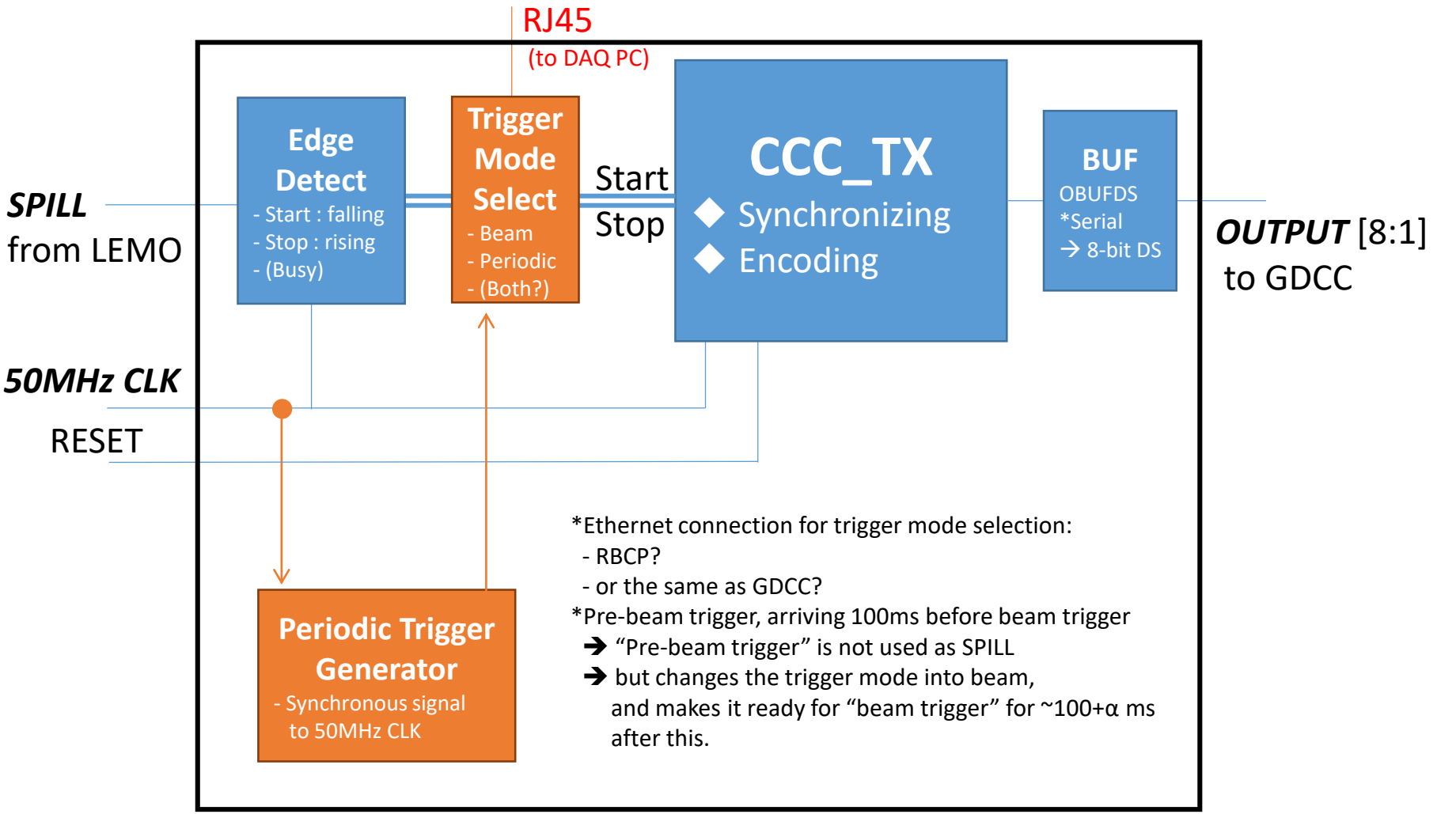




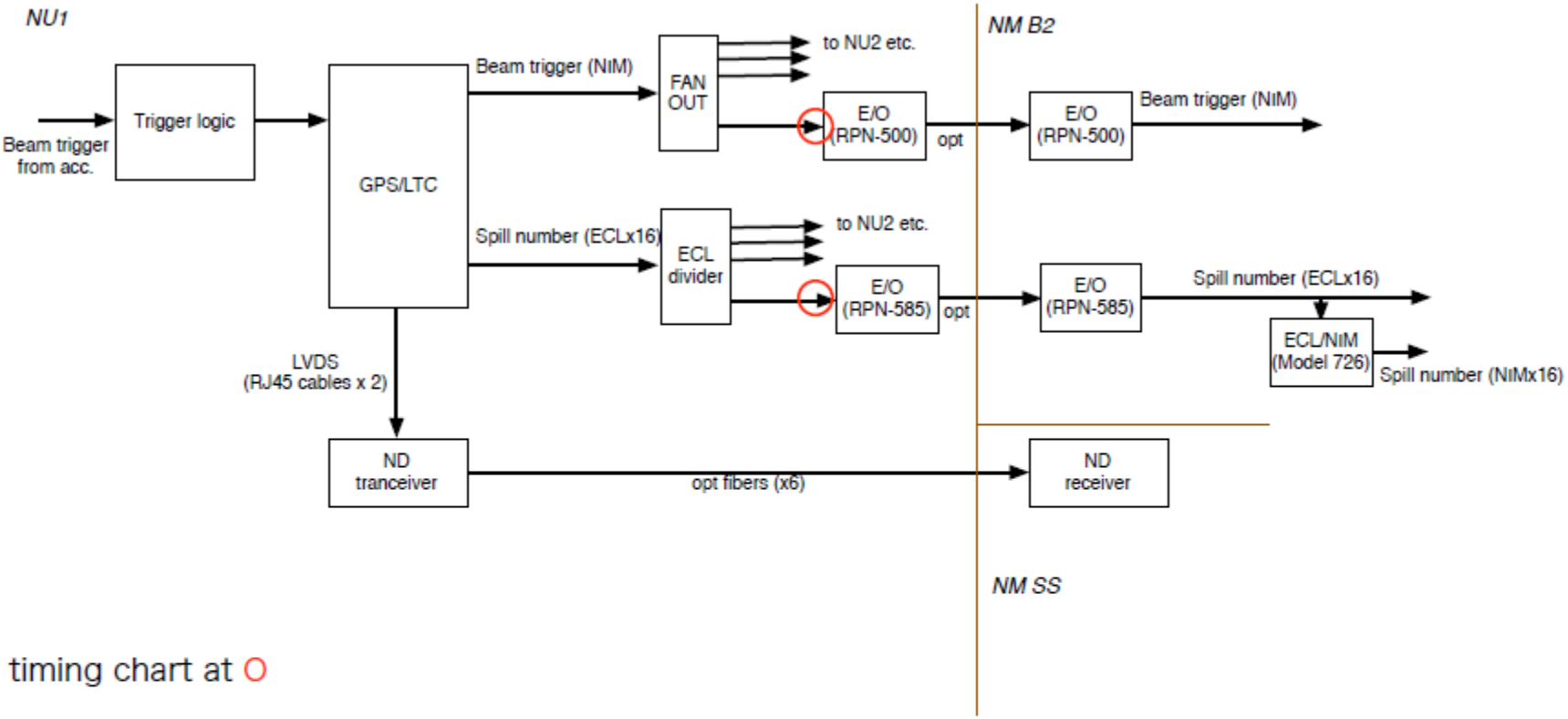
CCC firmware: updated

- Input
  - SPILL_IN
  - RESET_BUTTON
  - LOCAL_CLK_50MHZ
- Output
  - CNTL_BUF_DIF_P[8:1]
  - CNTL_BUF_DIF_N[8:1]

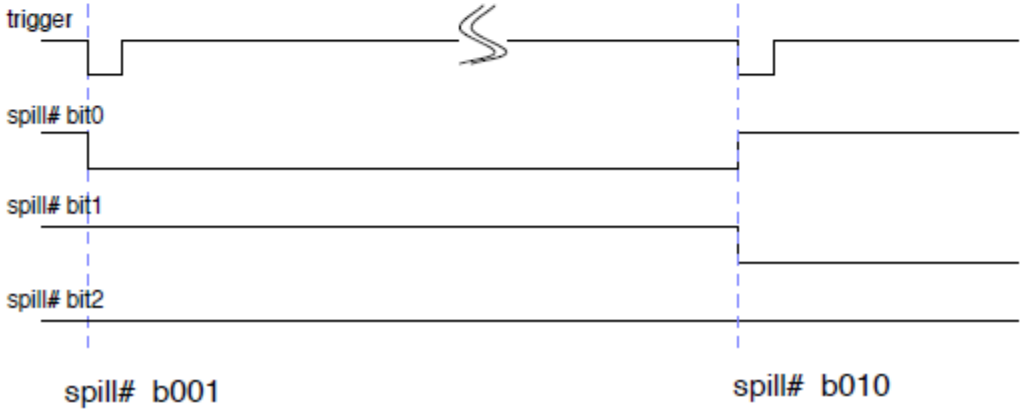
    *Data to GDCC



Beam trigger timing



timing chart at O



Note: there is an offset between spill# in BSD/QSD(beam data) and spill# from LTC

spill#(data) - spill#(LTC output) = 1

Data format

GDCC Packet Format

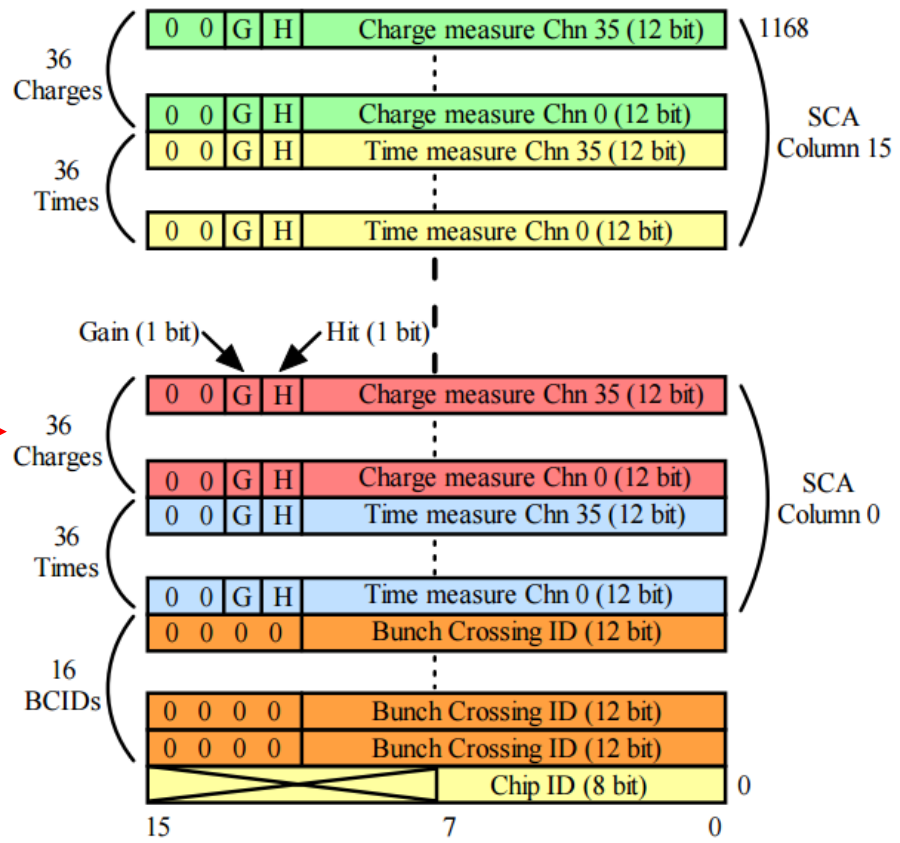
Dst MAC	*Src MAC*	*Ethernet Type*	*GDCC Type*	*GDCC_Modifier*	*GDCC_PktID*	*GDCC_DataLength*	*GDCC_Data*	*PAD*	*CRC32*
6 Bytes	6 Bytes	2 Bytes	2 Bytes	2 Bytes	2 Bytes	2 Bytes	Variable	Pad to Min Ethernet Size	4 Bytes

Used for SPILL#

DIF data format

Section	subsection	field	hex	ascii
SPILL header		Marker	0xFFFC	
		<ACQid> msb	....	
		<ACQid> lsb	....	
		Ascii tag	0x5053	"SP"
		Ascii tag	0x4C49	"IL"
		Blank space	0x2020	" "
	CHIP header	Marker	0xFFFD	
		<ID>	0xFF..	
		Ascii tag	0x4843	"CH"
		Ascii tag	0x5049	"IP"
		Blank space	0x2020	" "
		Raw DATA	binary	
	CHIP trailer	Marker	0xFFFE	
		<ID>	0xFF..	
		Blank space	0x2020	
		Blank space	0x2020	
SPILL trailer		Marker	0xFFFF	
		<ACQid> msb	....	
		<ACQid> lsb	....	
		<nb chip>	0x00 ..	
		<ACQid> msb	....	
		<ACQid> lsb	....	
		Blank space	0x2020	

SPIROC data format

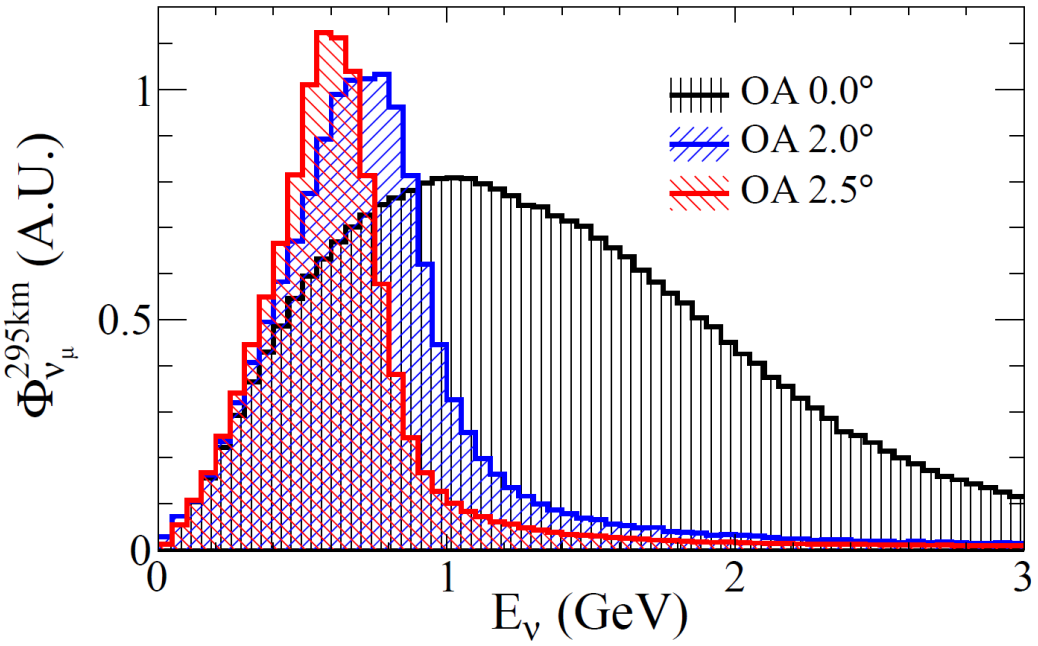


*__Off-axis method__

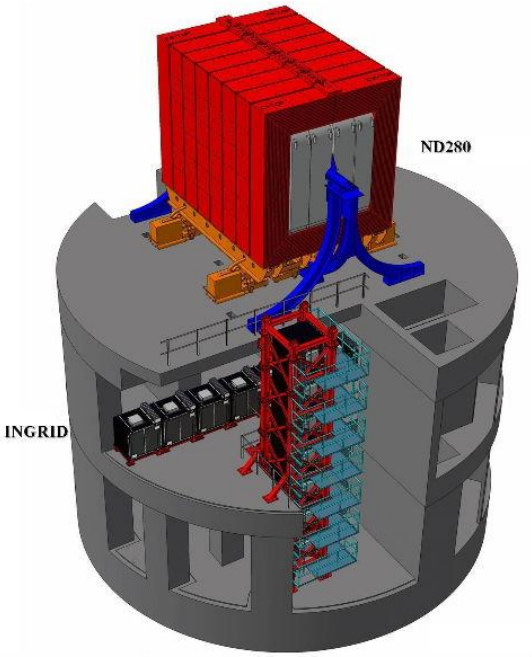
- narrow-band flux
- peak shifted to lower energy

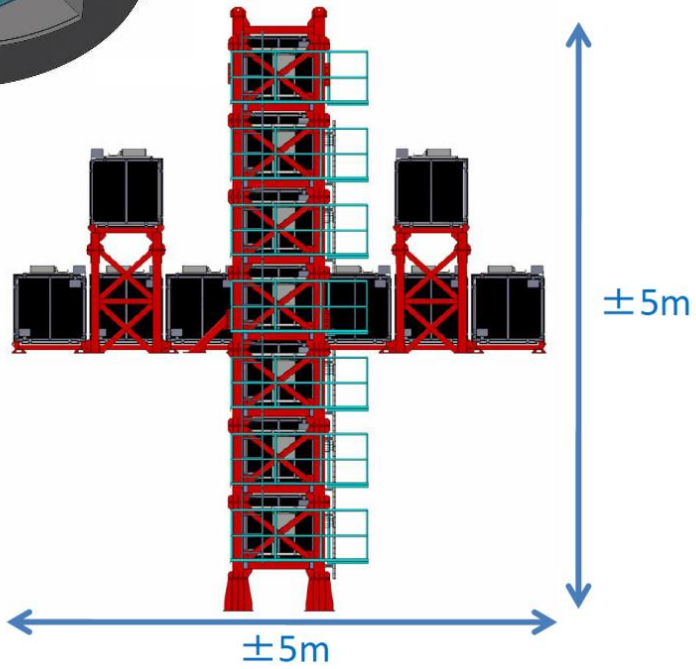
T2K uses 2.5° off-axis ⇒ peak: ~600MeV

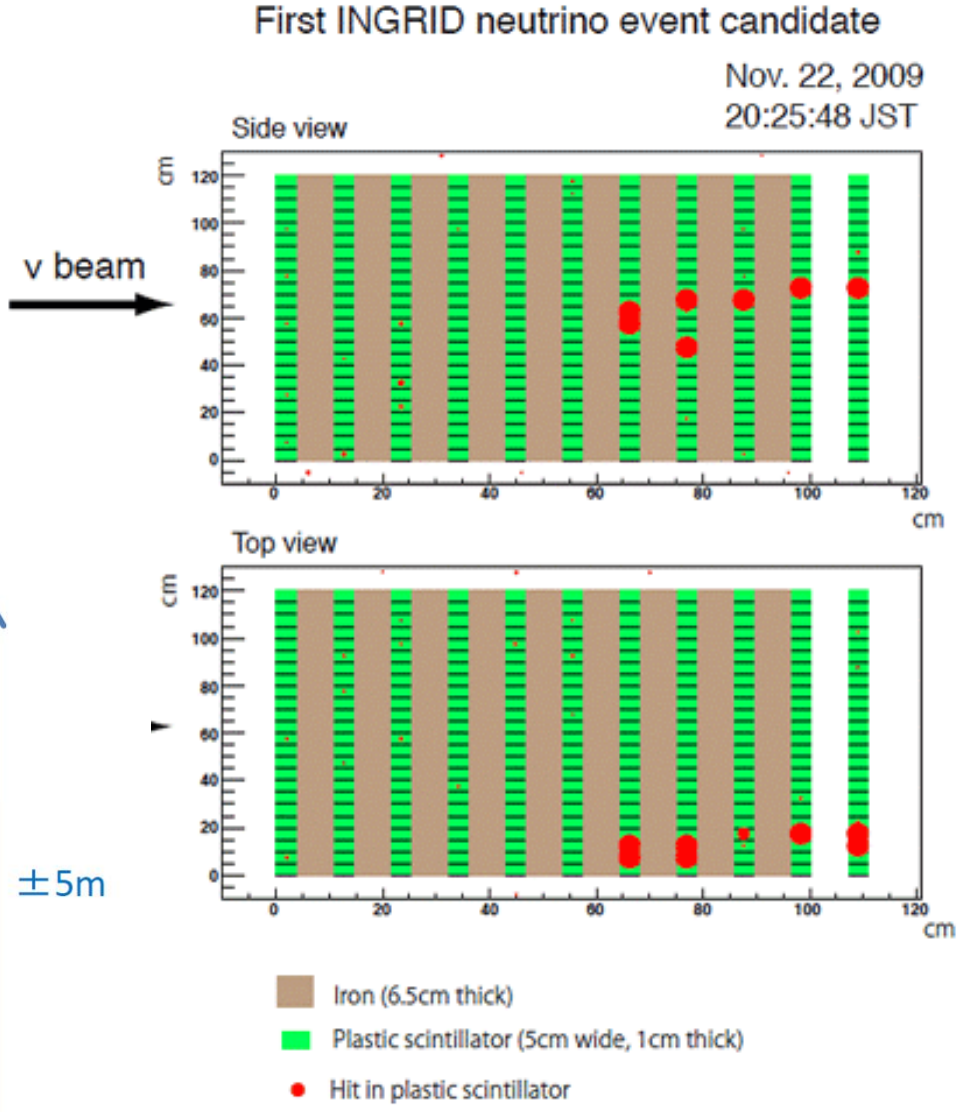
- large ν_e appearance probability
- suppress other interactions than CCQE



INGRID


ND280
INGRID


±5m
±5m


First INGRID neutrino event candidate
Nov. 22, 2009
20:25:48 JST
ν beam
Side view
Top view
cm
Iron (6.5cm thick)
Plastic scintillator (5cm wide, 1cm thick)
Hit in plastic scintillator
MR Run #27, Shot #19655
T2K Spill# 241792

Trip-t Front end Board (TFB)

- 12 layer board (6 signal routing, 6 power/ground)
- 16 cm x 9 cm.
- Each TFB takes 4 Trip-t chips, up to 64 MPPC channels.
- TFB operation is controlled by an FPGA.

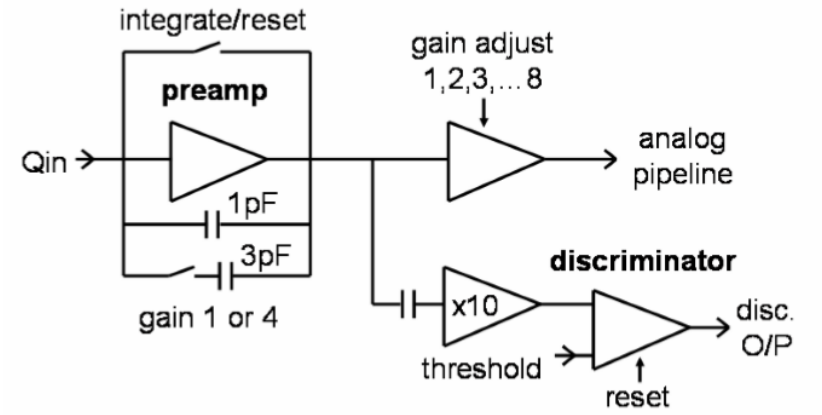


Fig. 4. Schematic of one Trip-t front end channel.