ATLAS実験シリコンピクセル検出器アップグレード用のデータ読出技術

計測システム研究会2020 @ J-PARC

26-27th November, 2020

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On behalf of the ATLAS ITk Pixel group

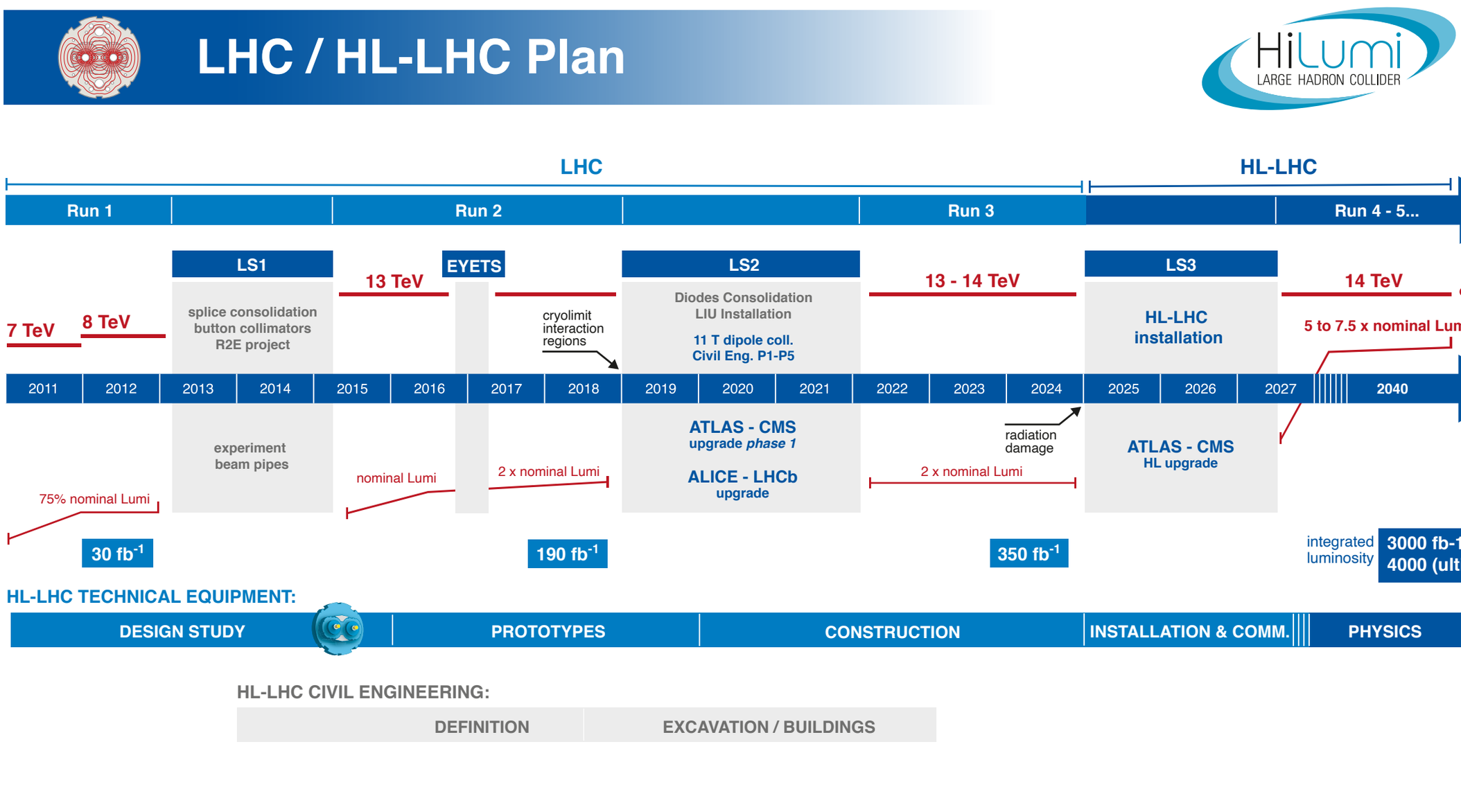
Disclaimer

- Today's talk covers mainly the DAQ system and relating softwares for our Pixel module mass production.

- Planning to talk about three main points.
  - ➡ Database system to track module production history.
  - ➡ DAQ system to perform pixel tests.
  - ➡ Design and performance of a DAQ interface board.

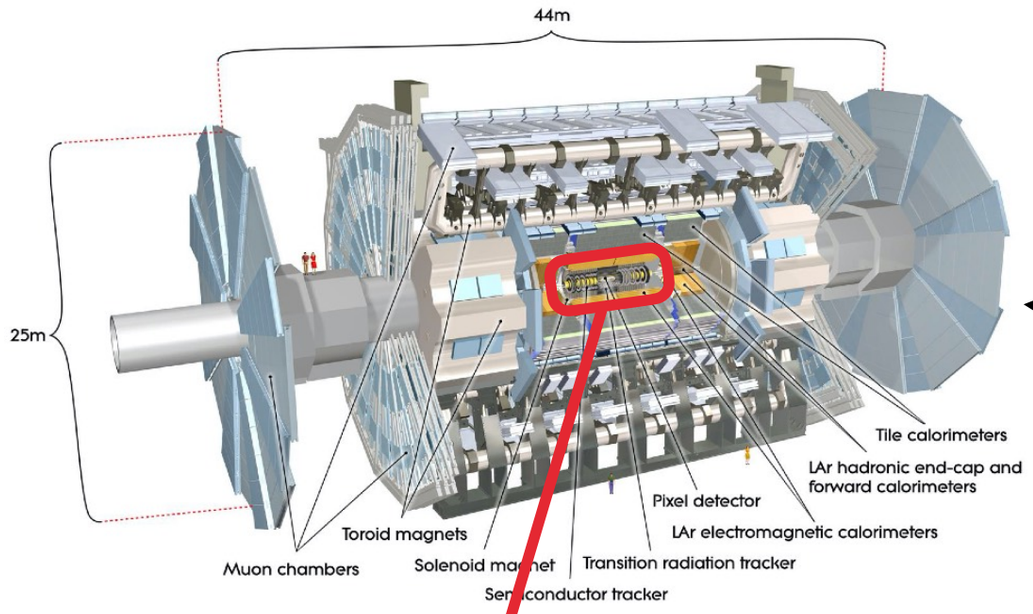
LHC upgrade project

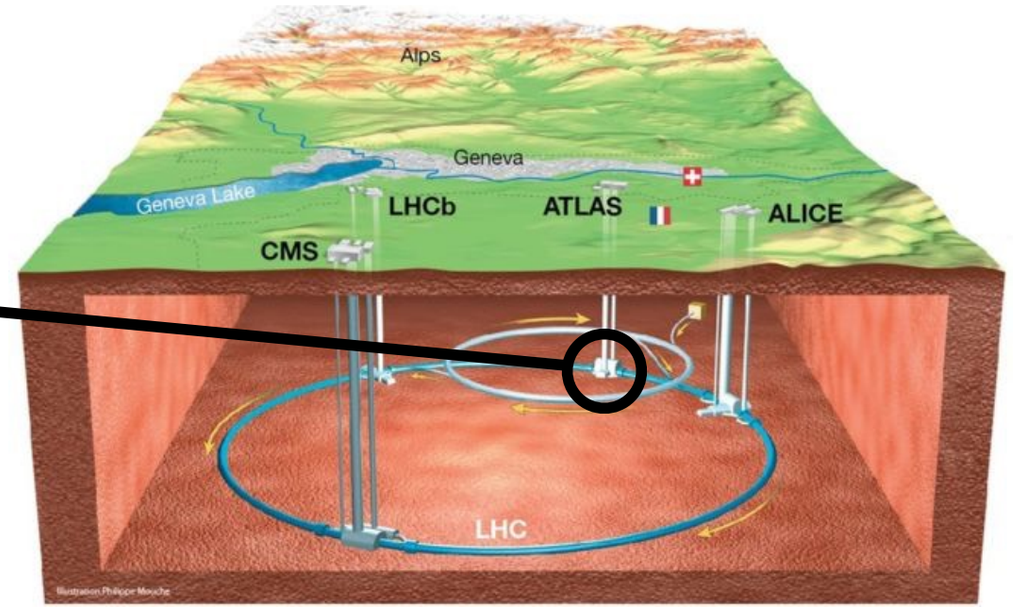
- LHC, world's largest collider, will be upgraded to HL-LHC by 2026.
  - ➡ Aiming to collect ~10 times more statistics.

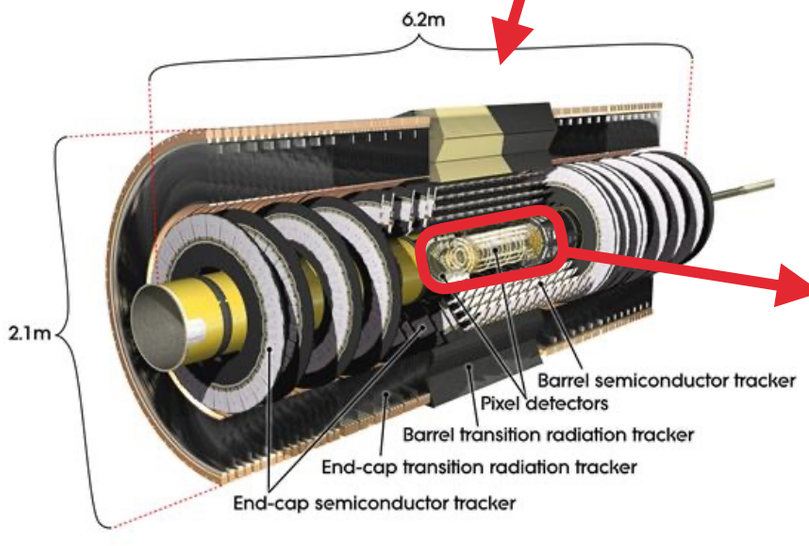


ATLAS detector upgrade

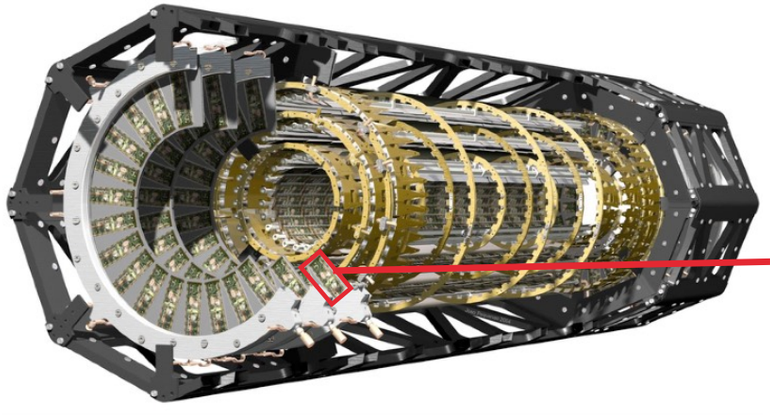
- Silicon Pixel Tracker: Innermost detector of the ATLAS

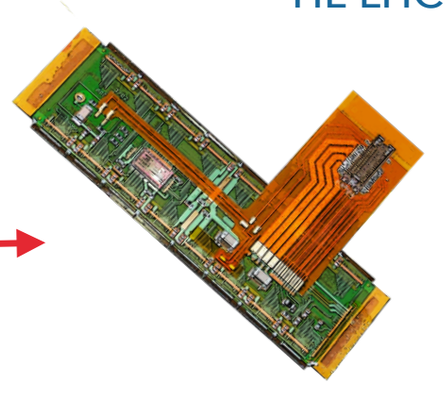






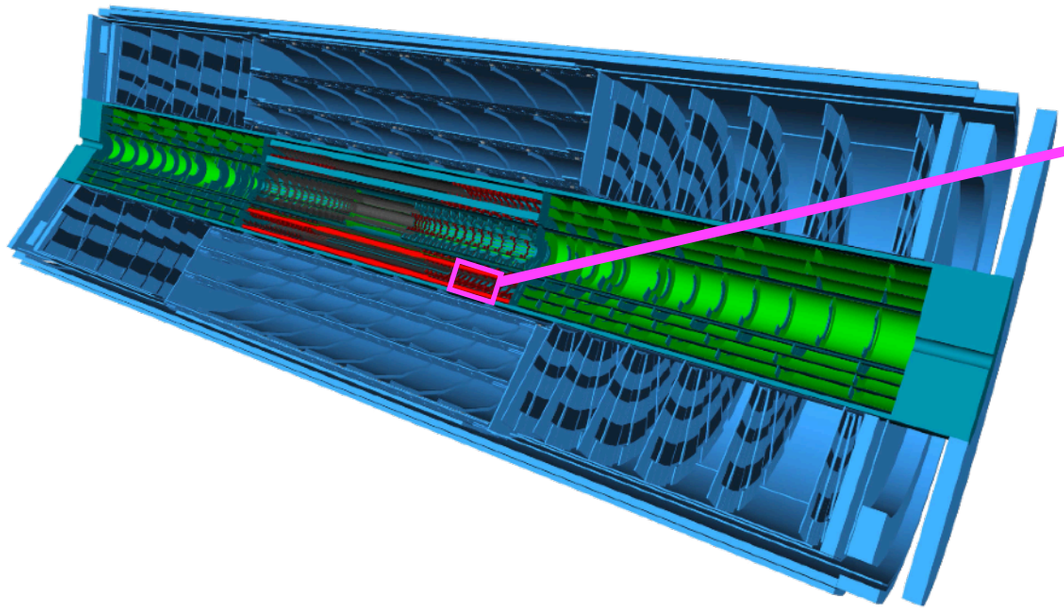
Current pixel modules here have to be replaced for HL-LHC



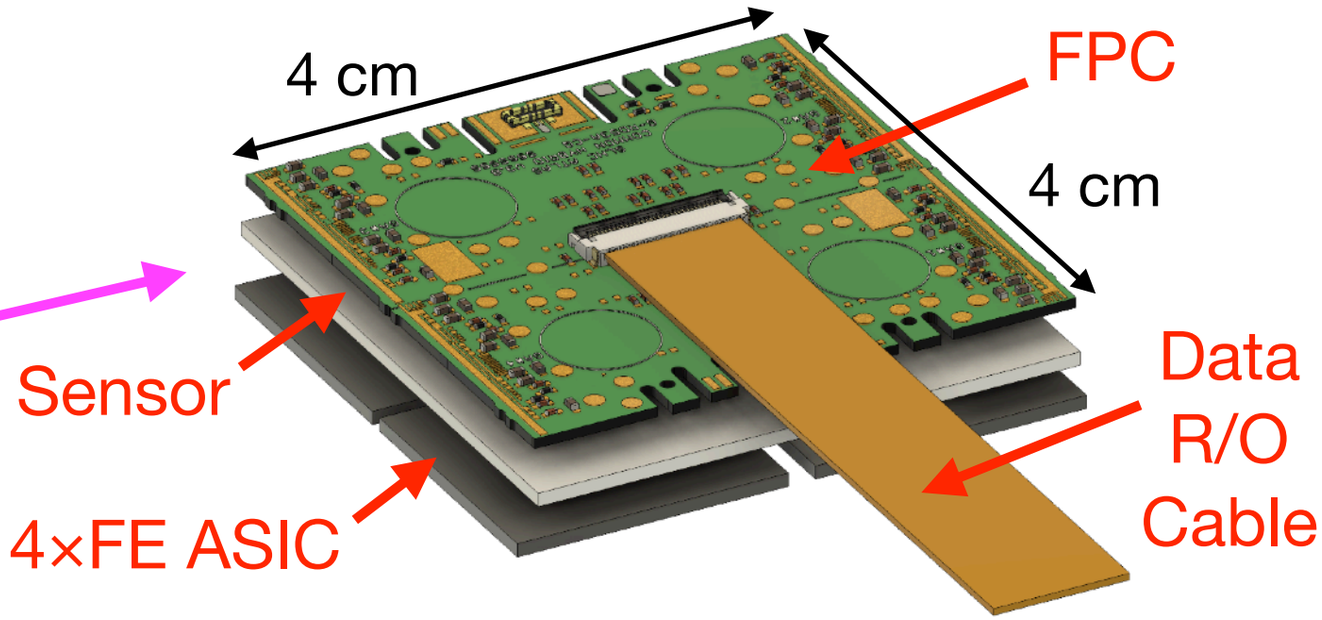


ATLAS Upgraded Pixel detector

- New inner tracker system
  - ➡ Composed of silicon strip and silicon pixel modules.



We need ~10000 pixel modules.
Japan will produce ~2000.

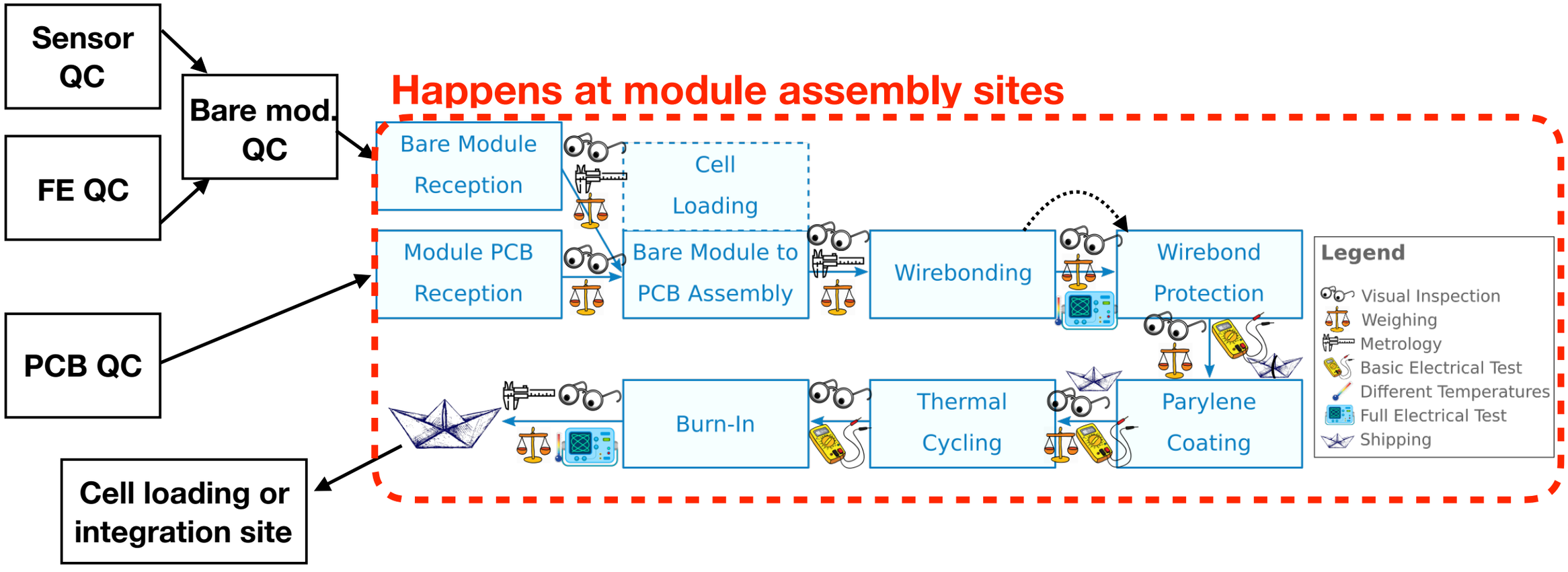


We need to test those modules to control its quality (QC).

2019	2020	2021	2022	2023	2024
Preparations for production	Prototype production	Pre-production	Mass production		

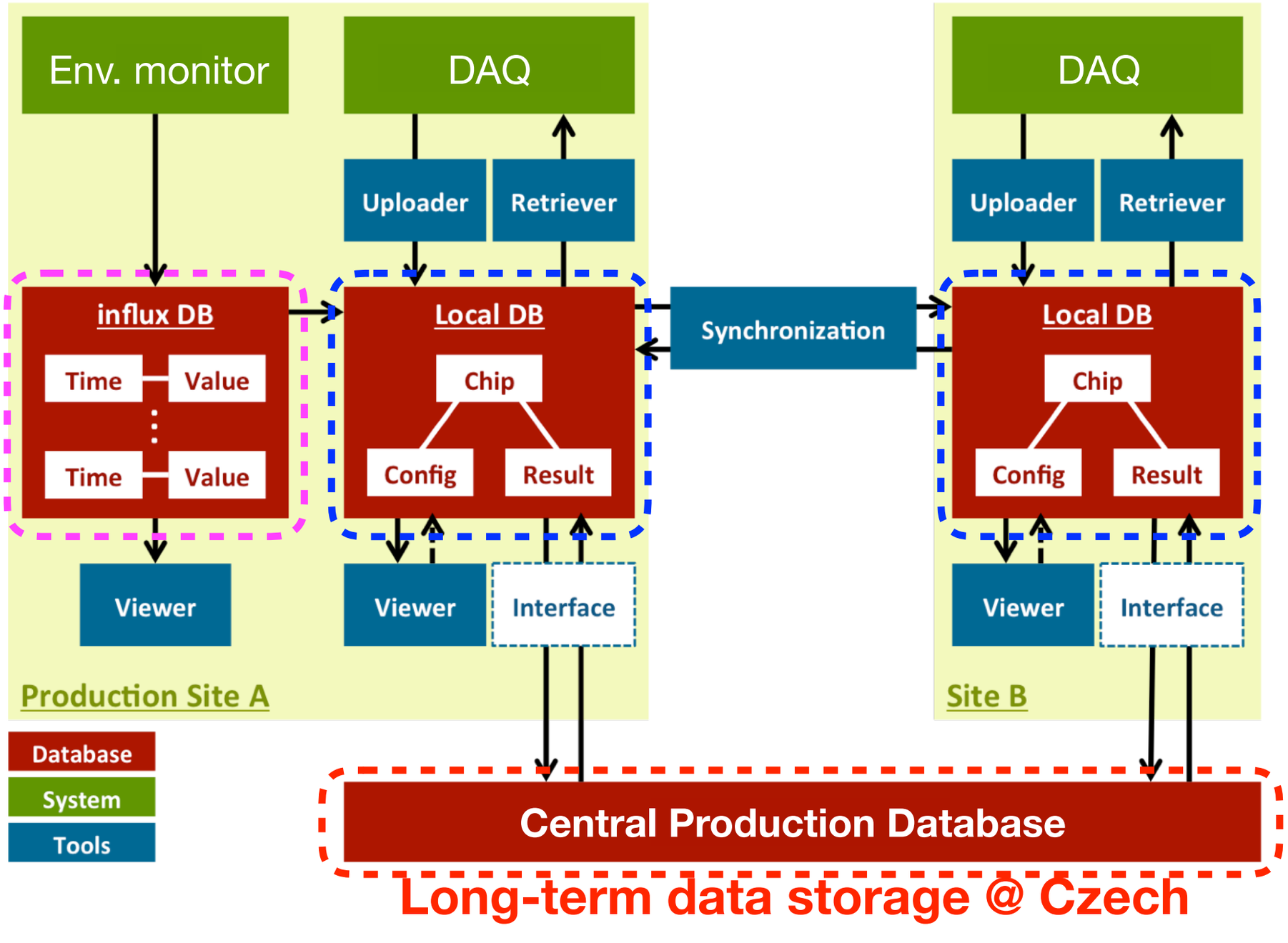
Difficulties for the QC test

- Complicated assembling procedure.
  - ➡ Need to properly handle test results to compare between different stages and/or sites.
- Many institutes (>20) are joining in the production.
  - ➡ Need to perform comparable tests with using variety of setups.



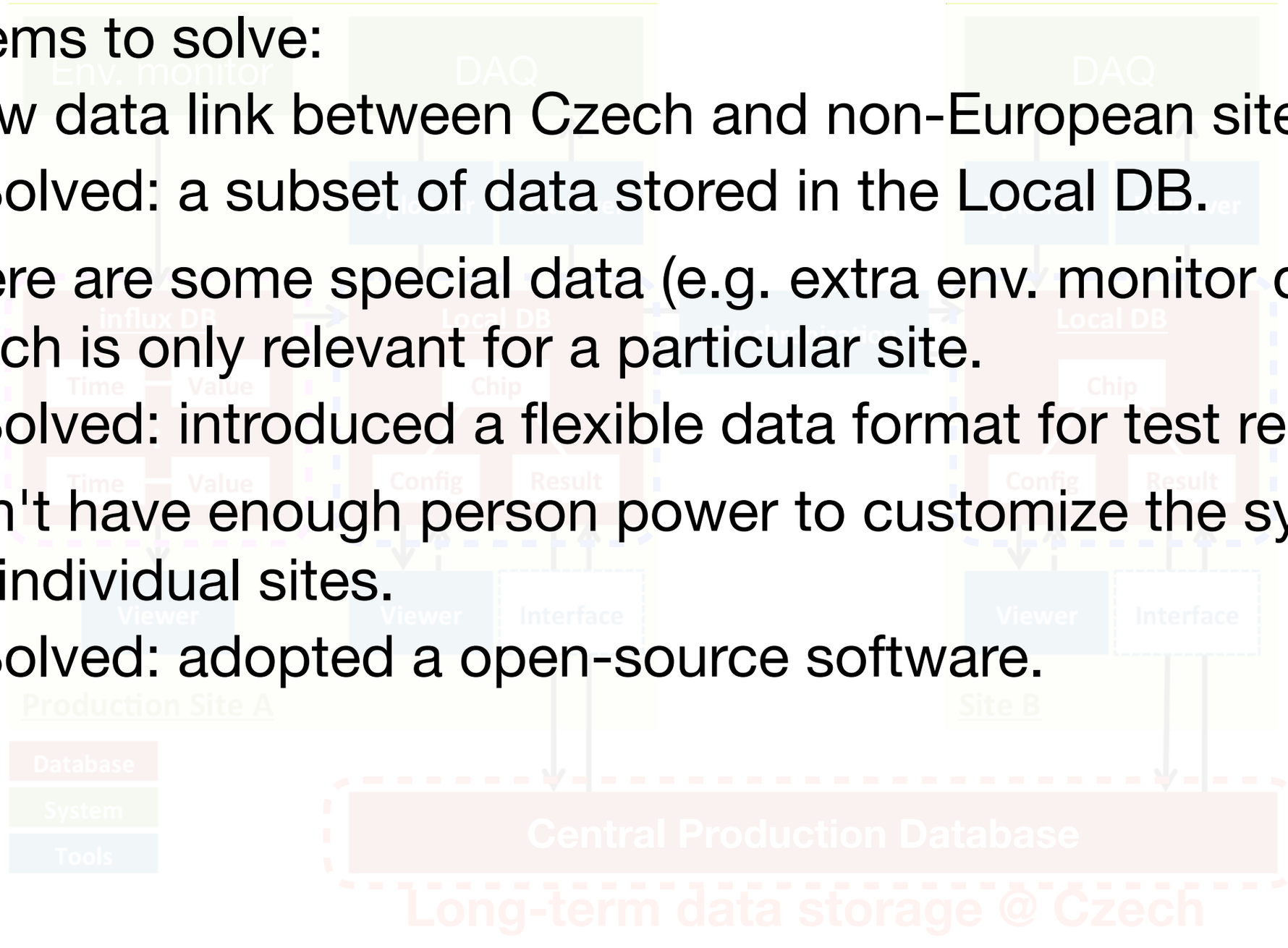
Data handling model for our QC tests

- Three-database system: One central, two local.



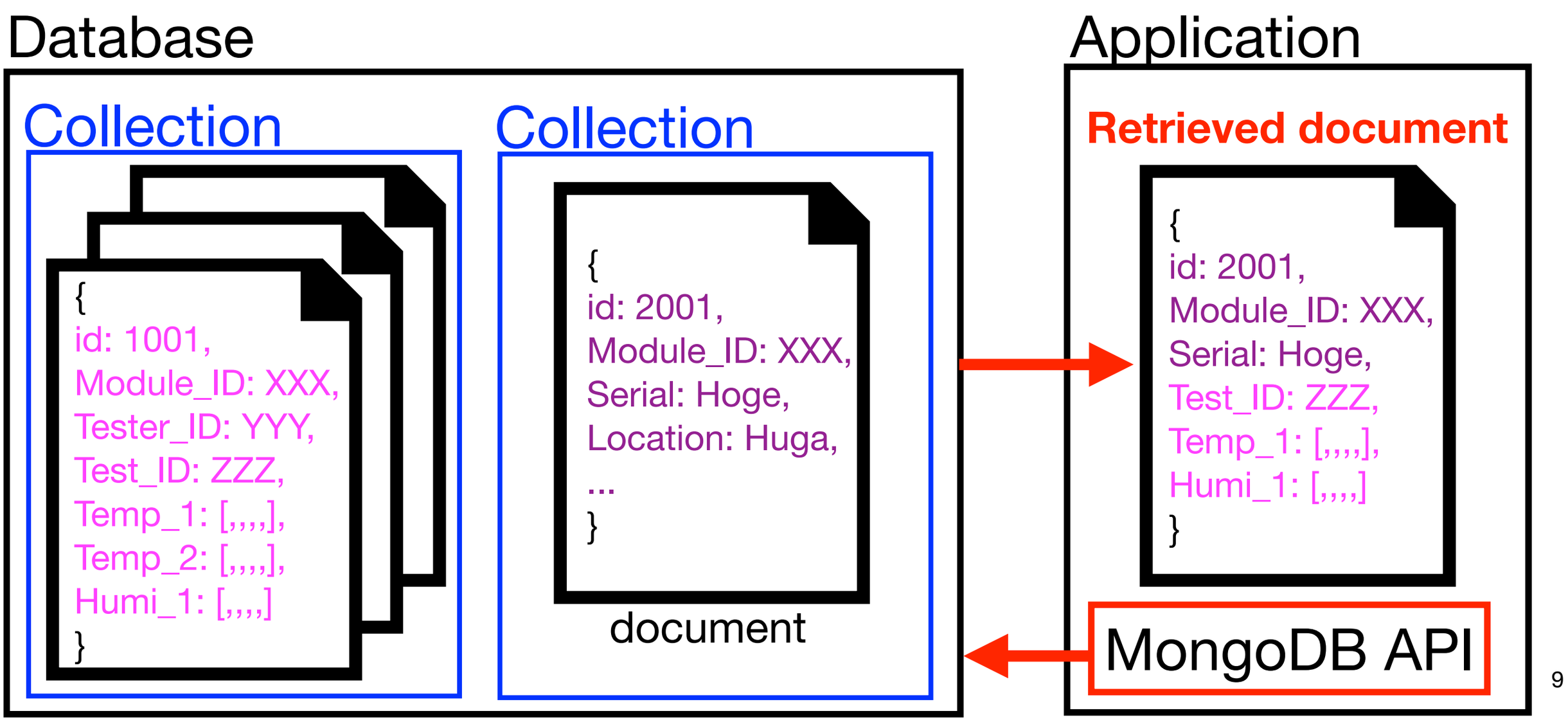
Data handling model for our QC tests

- Three-database system: One central, two local.
- Problems to solve:
  - ➡ Slow data link between Czech and non-European sites.
    - ✓ Solved: a subset of data stored in the Local DB.
  - ➡ There are some special data (e.g. extra env. monitor data) which is only relevant for a particular site.
    - ✓ Solved: introduced a flexible data format for test results.
  - ➡ Don't have enough person power to customize the system for individual sites.
    - ✓ Solved: adopted a open-source software.



Local database system

- mongoDB.: No SQL database
  - ➡ Favored due to flexibility compared to SQL DBs.
  - ➡ Data is stored as a JSON format ("document").



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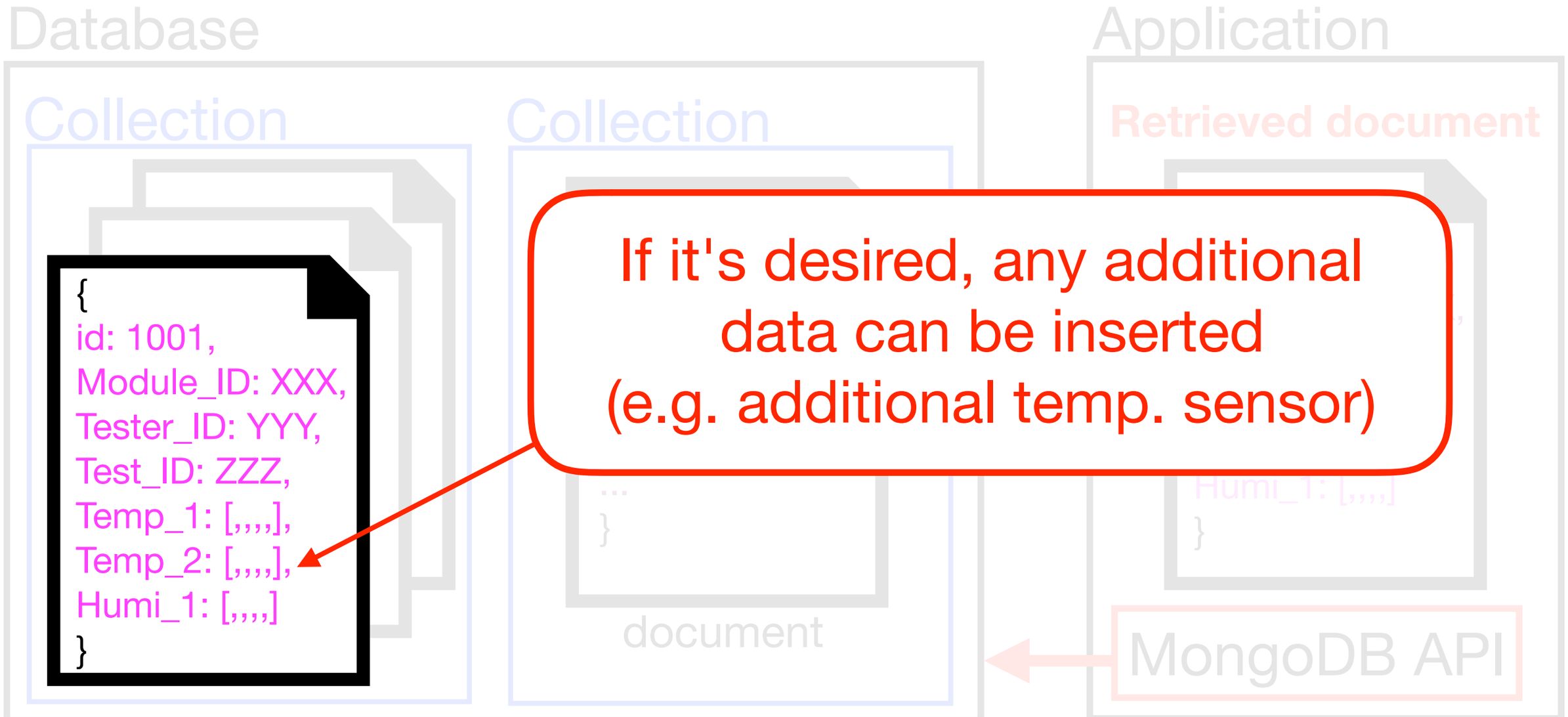
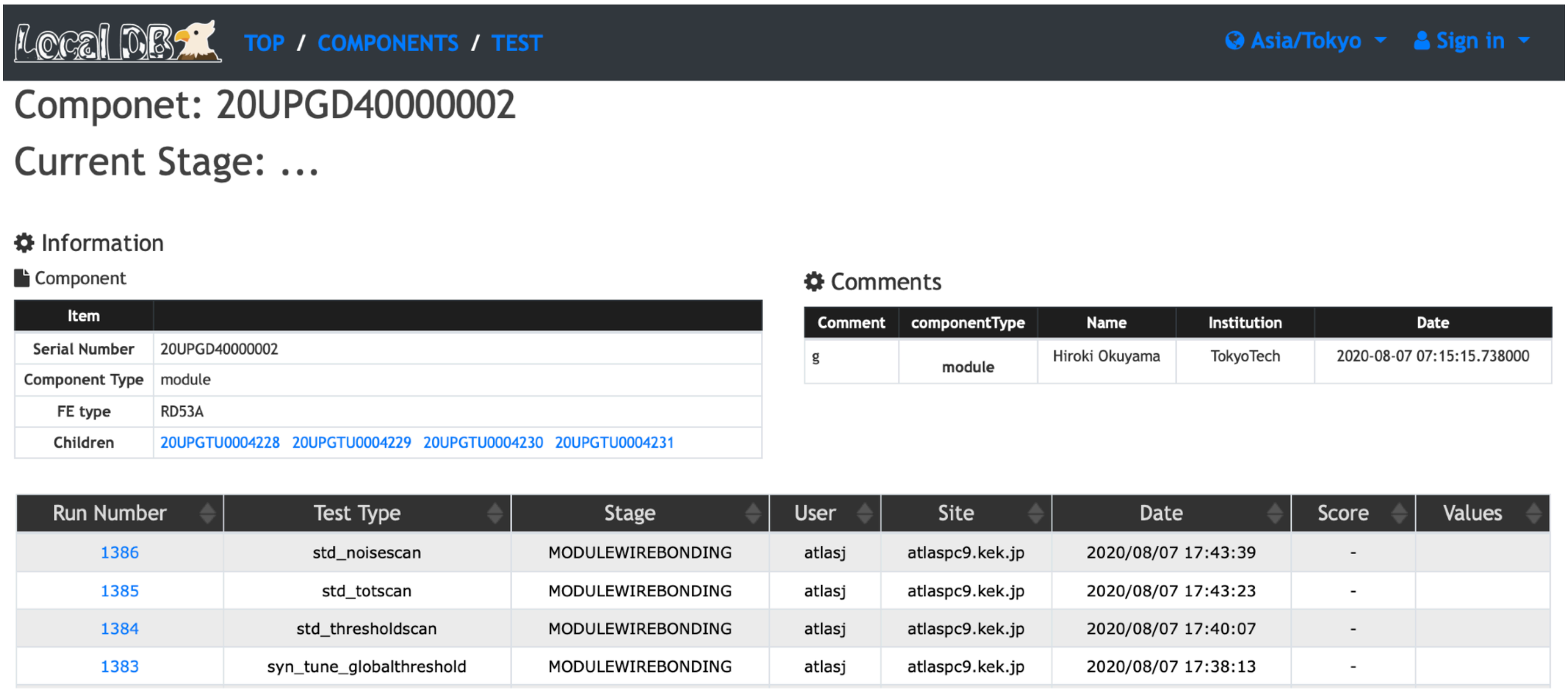


Local DB viewer

- Quick look at each test result as well as associated env. data.
- Custom web application based on Flask (python).
  ➡ Example: http://atlaspc5.kek.jp/localdb/



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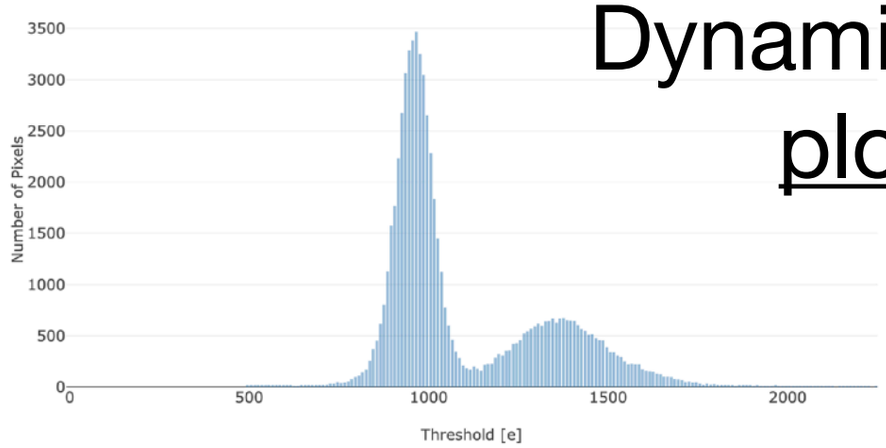
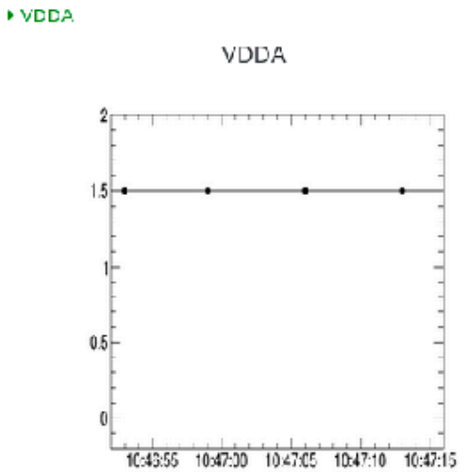


Dynamically generated plot by plotly.



Settings (Start/End : time-axis, Max/Min : y-axis)			
parameter	RunTime	current	modify
Start	2019-05-13 10:17:02	2019-05-13 10:16:52	2019-05-13T10
End	2019-05-13 10:17:06	2019-05-13 10:17:16	2019-05-13T10
Min([V])		-0.2	-0.2
Max([V])		2.0	2
Min([A])		-0.2	0.2
Max([A])		0.7	0.7
		Set Default	Make Histogram

Local DB viewer

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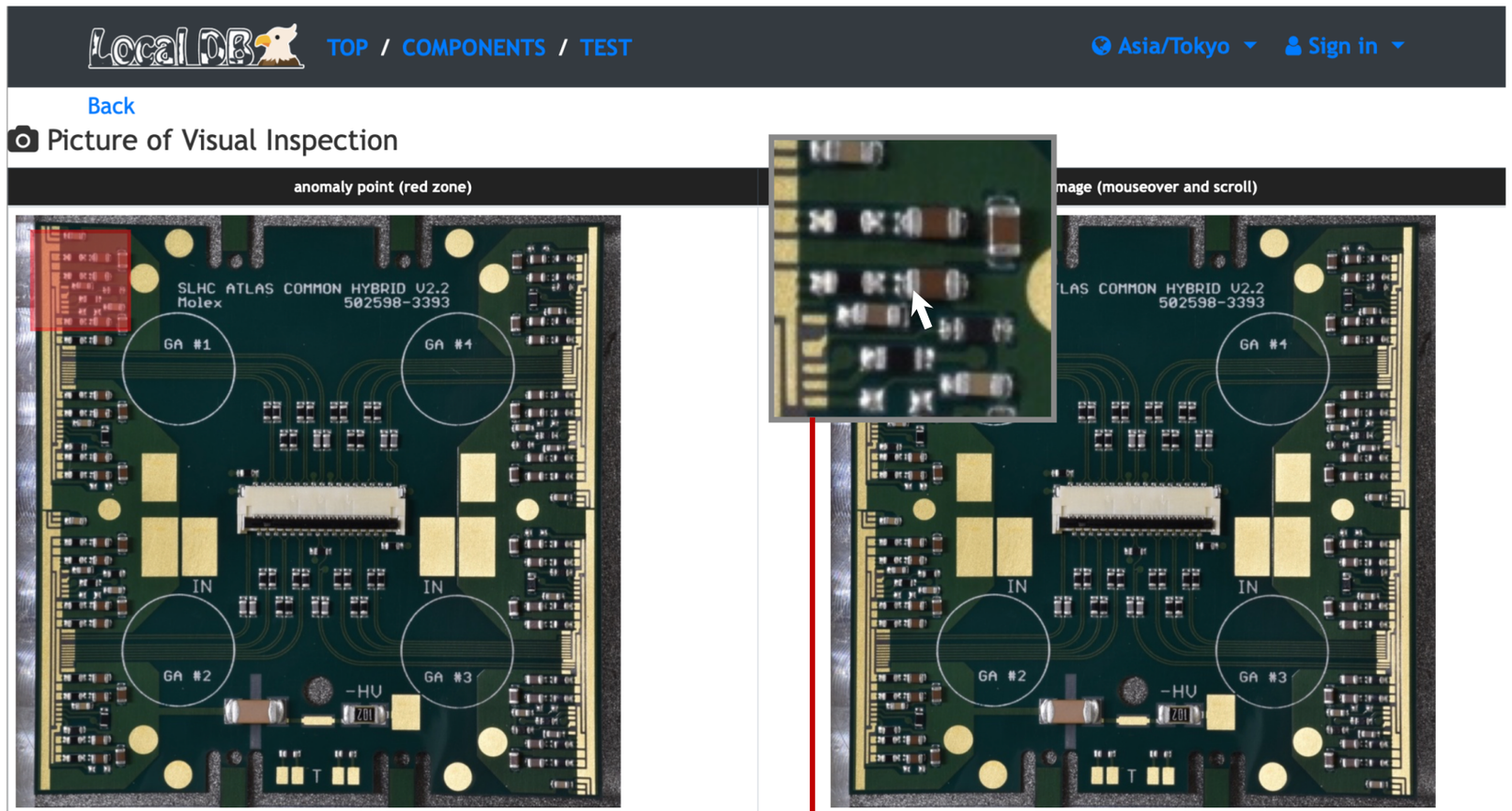


Environmental monitoring system

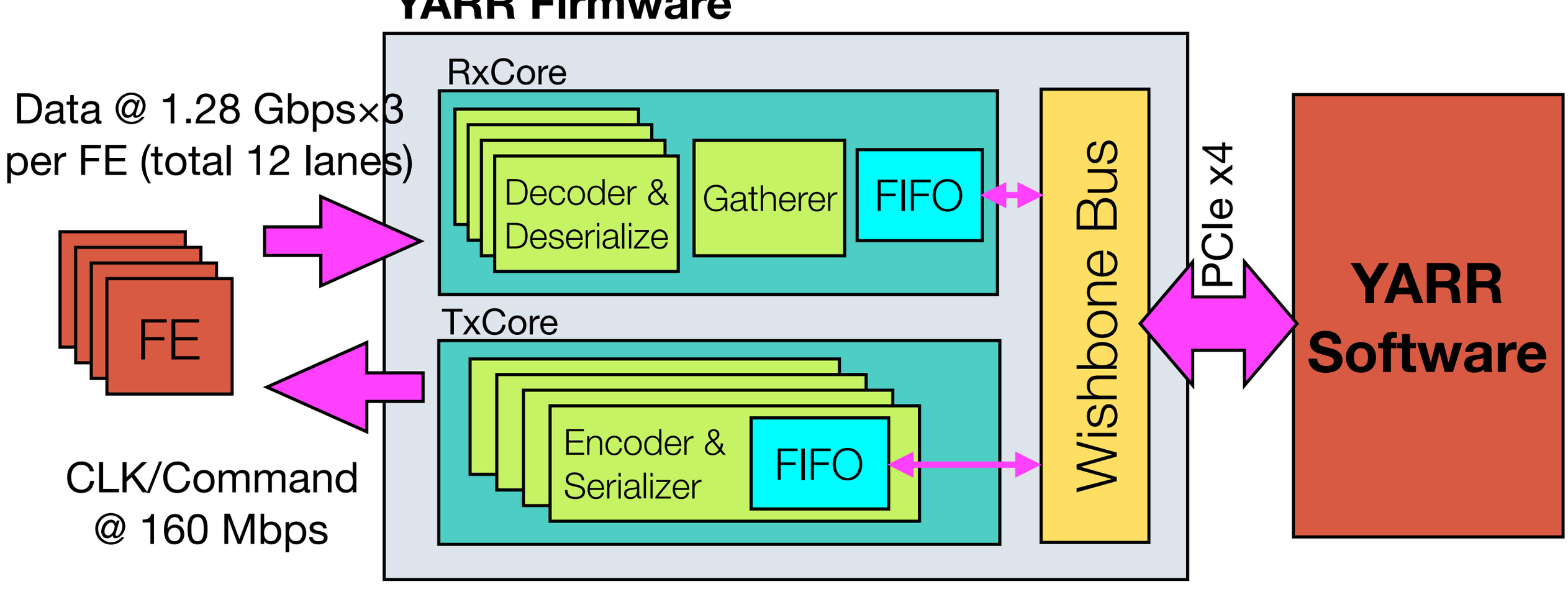
-  : Time series database for env. monitoring.
-  Grafana : Open source analytics and interactive visualization web application.
- Aiming to reduce development and maintenance cost.

➡ One can customize their own monitoring system with well maintained documentation.

DAQ system

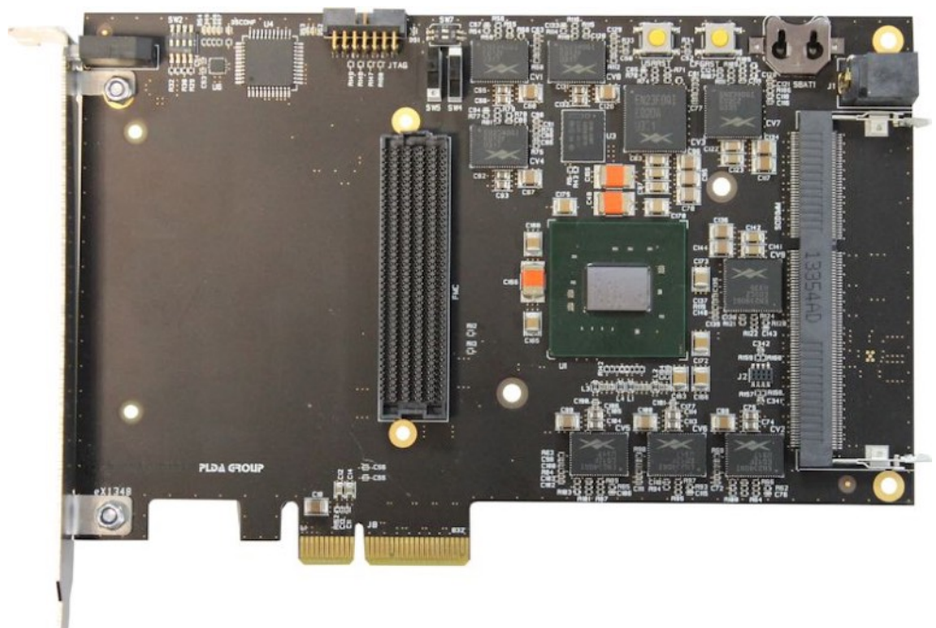
YARR - DAQ system

- PCIe based high-speed DAQ system
  - ➡ FPGA just aggregates data from FE ASICs, everything sophisticated is done by its corresponding software.



YARR - DAQ system

- PCIe based high-speed DAQ system
  - ➡ Supporting commercial PCIe-FPGA boards with FMC.
    - ✓ PLDA XpressK7: ~¥200k
    - ✓ Trenz TEF1001: ~¥100k
    - ✓ Xilinx KC705: ~¥210k
  - ➡ Assuming less expensive Kintex7 (xc7k160t, xc7k325t).



FPGA AC/DC Characteristics

- FPGA on KC705: XC7K325T, speed grade="-2".
  - ➡ 1250 Mbps is the maximum rate.
    (and it's less than the ASIC data output rate...)

Table 17: **Networking Applications Interface Performances**

Description	I/O Bank Type	Speed Grade					Units
		1.0V			0.95V	0.9V	
		-3	-2/-2LE	-1/-1M/-1LM/-1Q	-2LI	-2LE	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	710	625	Mb/s
	HP	710	710	625	710	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	1250	950	Mb/s
	HP	1600	1400	1250	1400	1250	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	HR	710	710	625	710	625	Mb/s
	HP	710	710	625	710	625	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	HR	1250	1250	950	1250	950	Mb/s
	HP	1600	1400	1250	1400	1250	Mb/s

ref. DS182

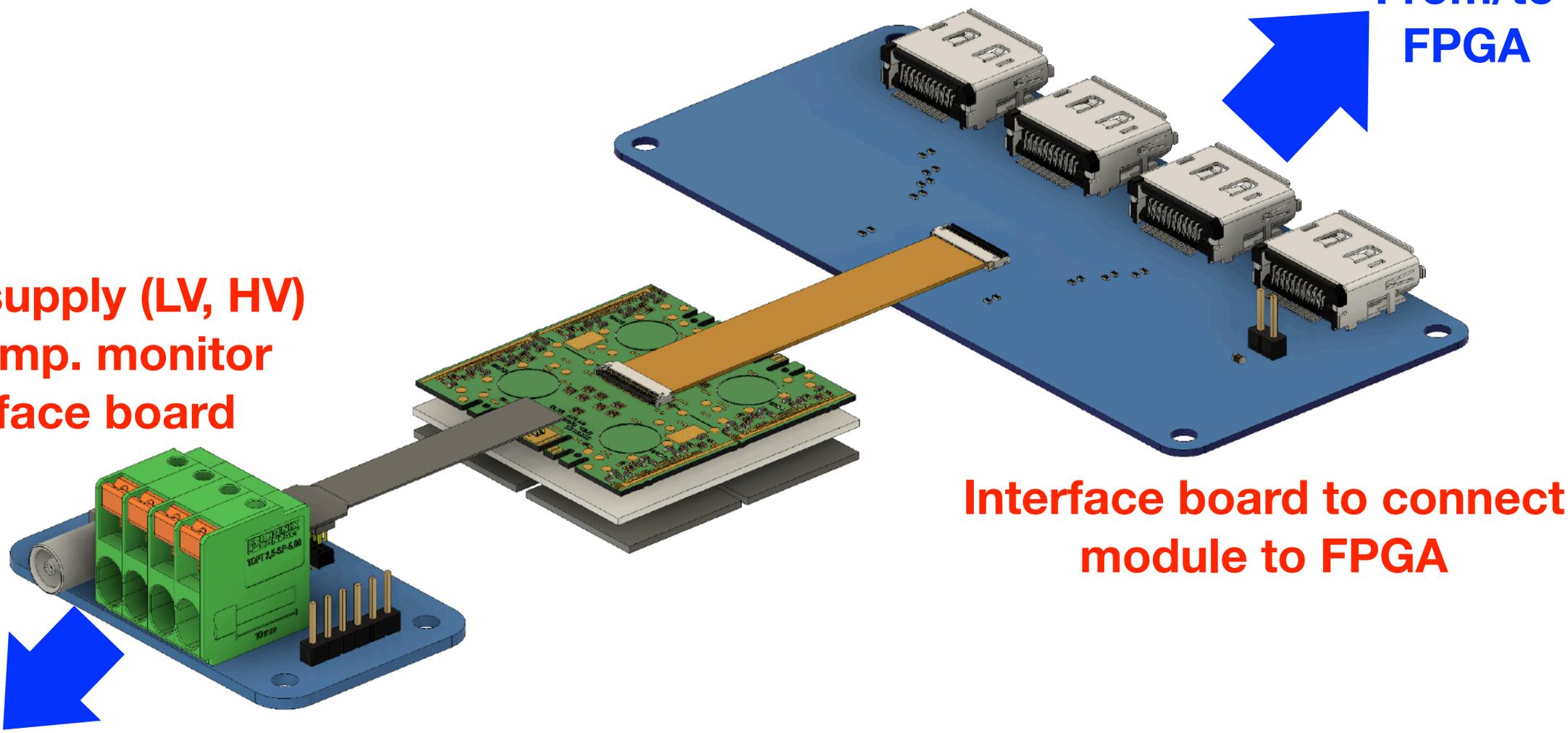
Challenges

- Readout options for 1.28 Gbps data rate
  - ➡ **Option.1**: abuse normal pins beyond FPGA specs.
    ✓ Already gave it a shot, but unsuccessful so far.
  - ➡ **Option.2**: use multi-gigabit transceivers (e.g. GTX).
    ✓ Implemented and worked, but #GTX is not enough for the module testing (12 required, max 8 available).
  - ➡ **Option.3**: buy or design a board with more expensive FPGA.
    ✓ Difficult in terms of budget.
- Currently adopted solution:
  - ➡ Operate ASIC with a test mode with half (640 Mbps) speed.
  - ➡ Unknown how this affects to the production yield:(
- Any good idea...?

Interface board

Interface board for module testing

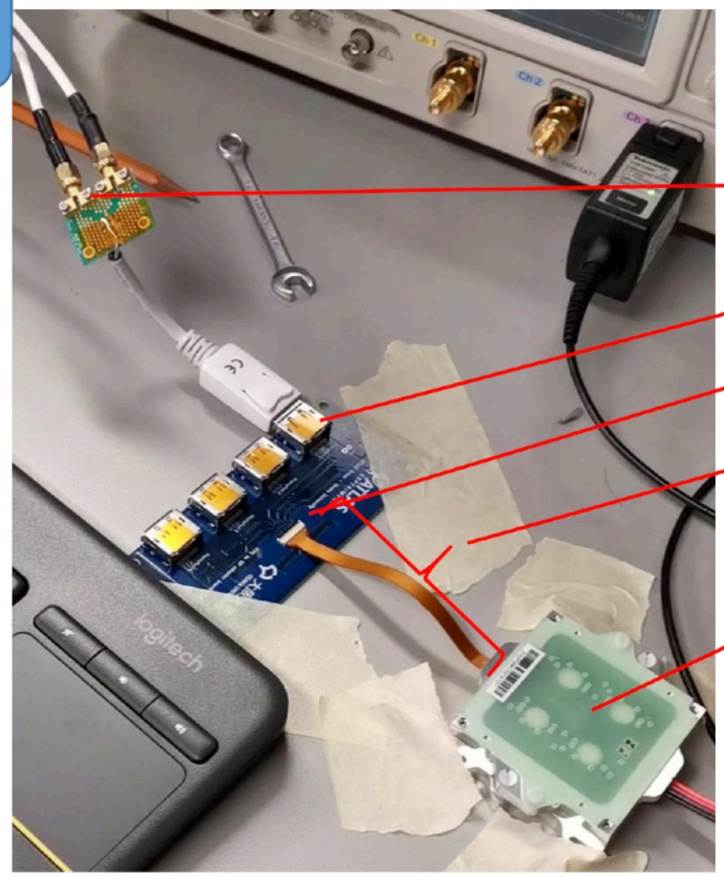
- Custom PCB for testing modules.
  - ➡ Submitted to a cheap Chinese company (e.g. PCBway, JLCPCB) which may sound a bad choice...

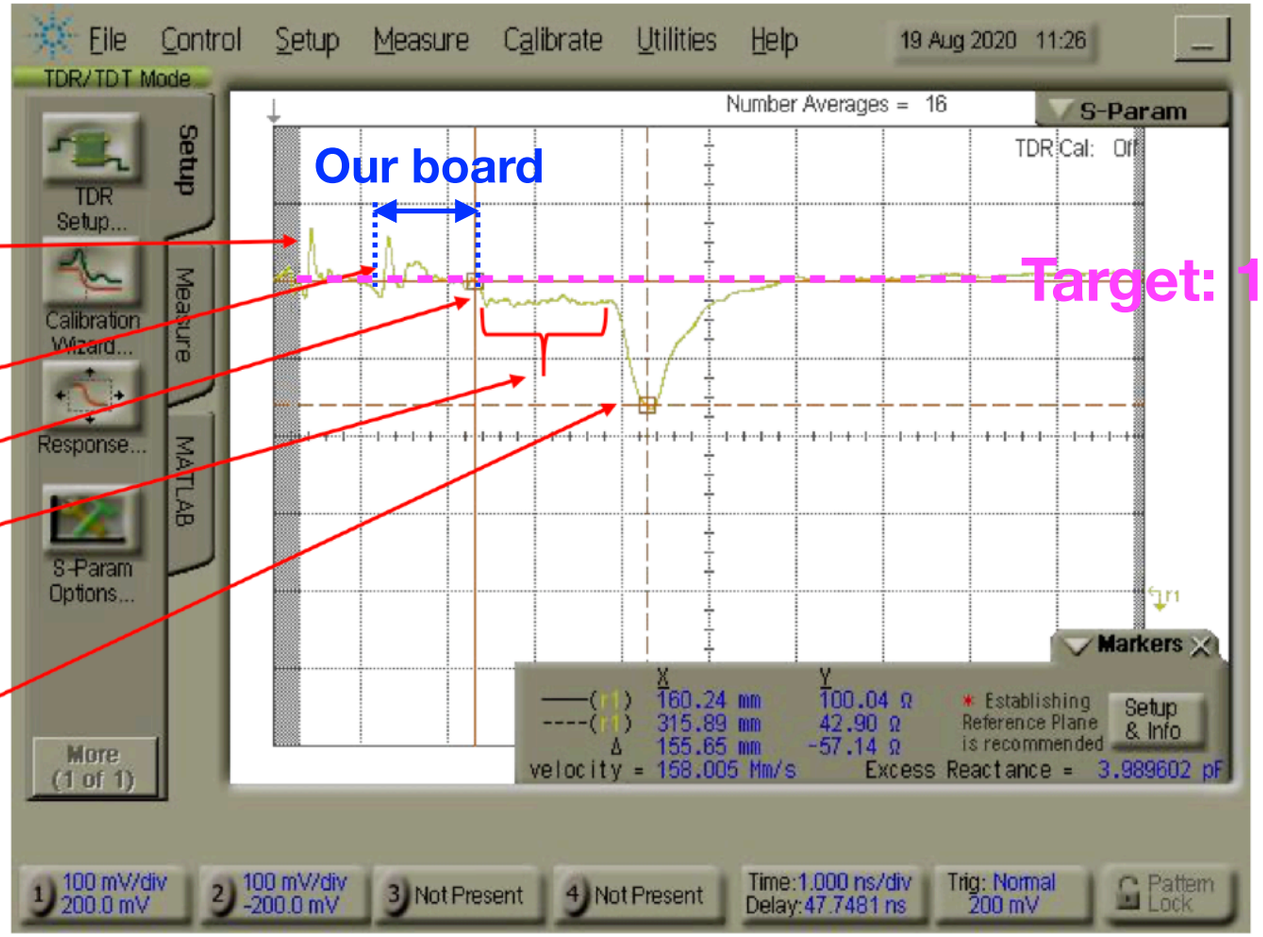


Interface board for the module testing

- Quality and their skill are actually good:)
  - ➡ FMC HPC, 0.5 mm pitch pads successfully assembled.
  - ➡ Impedance could be controlled very well.
- Low cost by a factor of ~10 compared to P-ban.

TDR machine





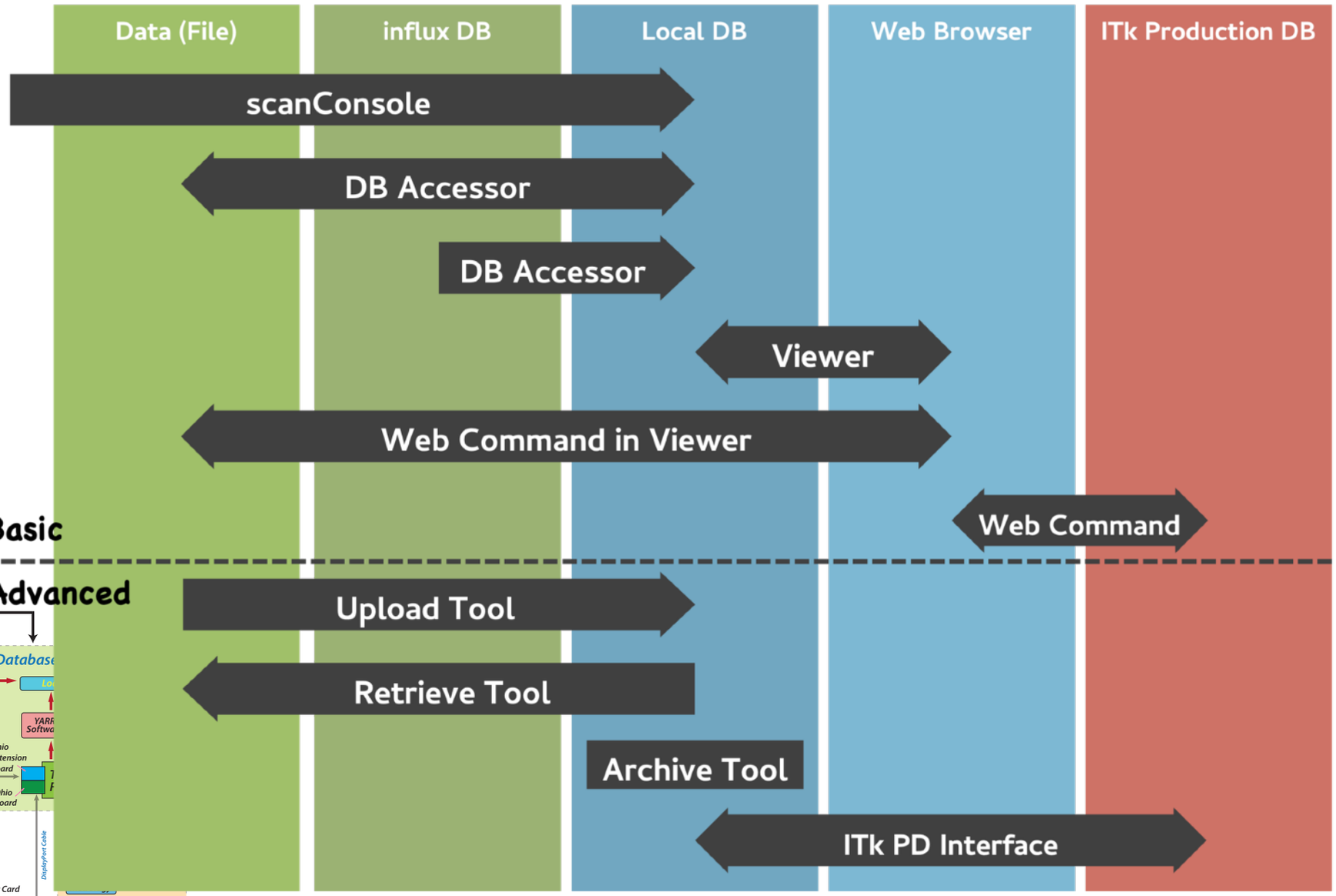
Summary

- ATLAS pixel detector will be upgraded for HL-LHC..
  - ➡ Preparing for the mass production of Pixel detector.
    - ✓ In terms of not only hardware itself, but also a software infrastructure to test detectors.
- To share the tasks among the international collaboration, data handling tend to become complicated.
- Real production phase is approaching, need to wrap up soon!!

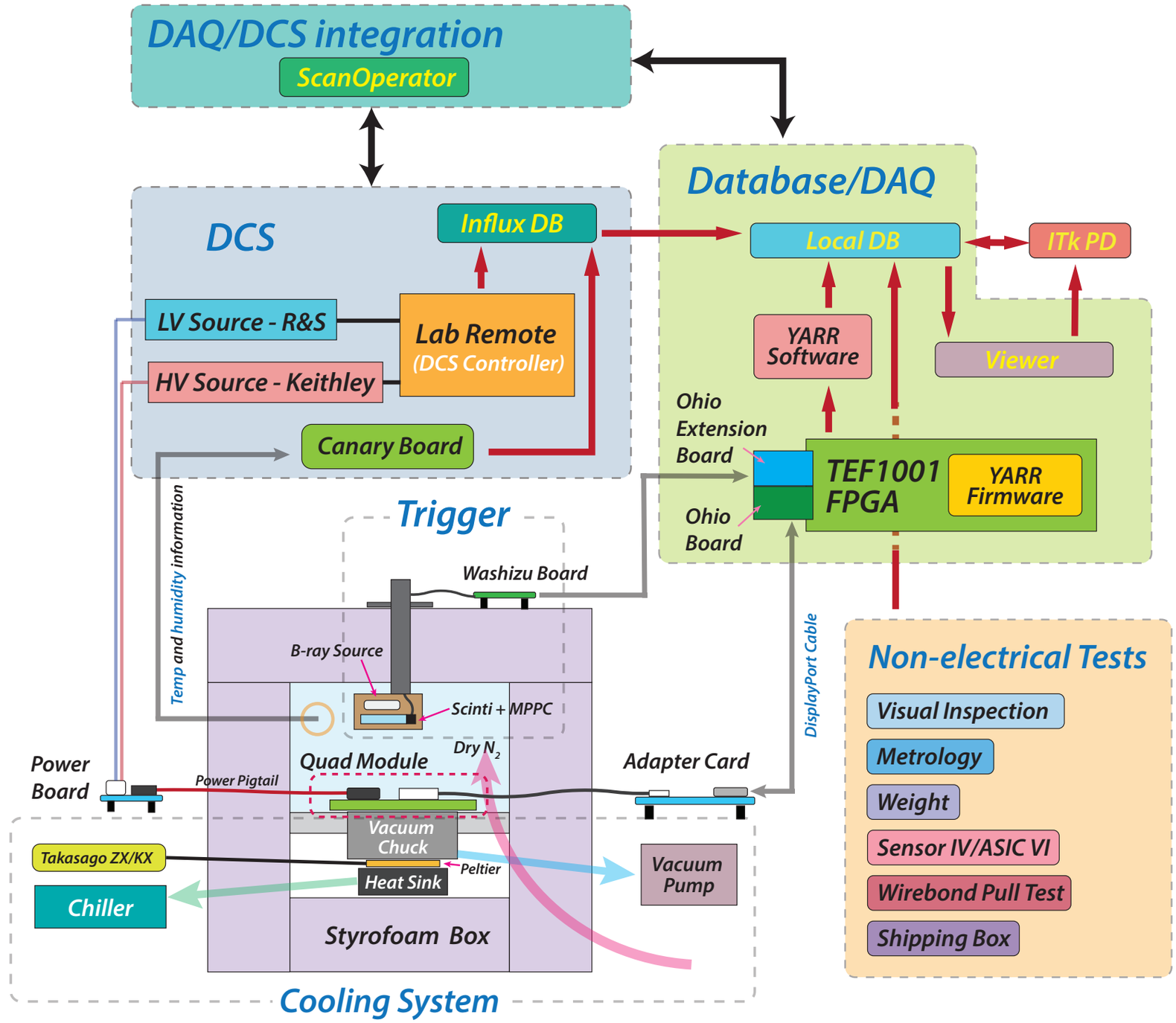
Backup

Overview of our QC test system

- Complicated software infrastructure



QA/QC system


DAQ/DCS integration
ScanOperator
DCS
Influx DB
LV Source - R&S
Lab Remote
(DCS Controller)
HV Source - Keithley
Canary Board
Database/DAQ
Local DB
ITk PD
YARR
Software
Viewer
Ohio
Extension
Board
TEF1001
FPGA
YARR
Firmware
Ohio
Board
Trigger
Washizu Board
Temp and humidity information
B-ray Source
Scinti + MPPC
Dry N2
Power
Board
Power Pigtail
Quad Module
Adapter Card
DisplayPort Cable
Vacuum
Chuck
Takasago ZX/KX
Peltier
Heat Sink
Chiller
Vacuum
Pump
Styrofoam Box
Cooling System
Non-electrical Tests
Visual Inspection
Metrology
Weight
Sensor IV/ASIC VI
Wirebond Pull Test
Shipping Box

Sampling point tuning algorithm

- Based on Xilinx XAPP1017.

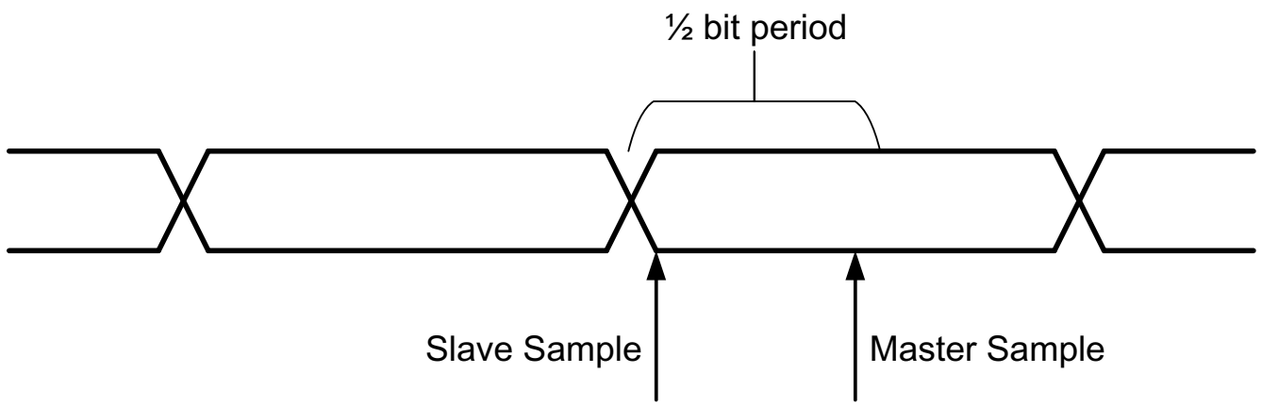


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Figure 6: **Data Sampling Delay Too Long**