

J-PARCハドロン実験用の 連続読み出しDAQ開発の現状

Outline

- Introduction
- Front-end electronics
- Clock/command/timing distribution
 - CDCM transceiver
 - SPDT protocol
 - Test results
- Summary

KEK素核研

本多良太郎

for the J-PARC E50 experiment

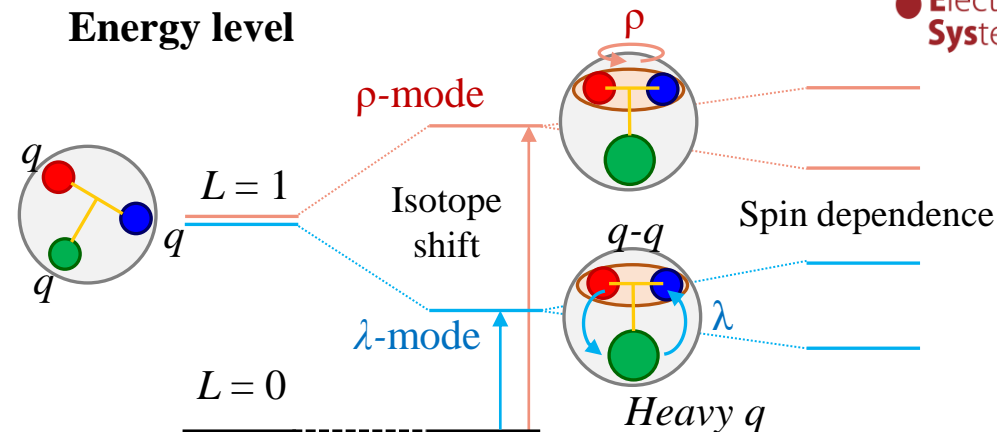
Introduction

Motivation

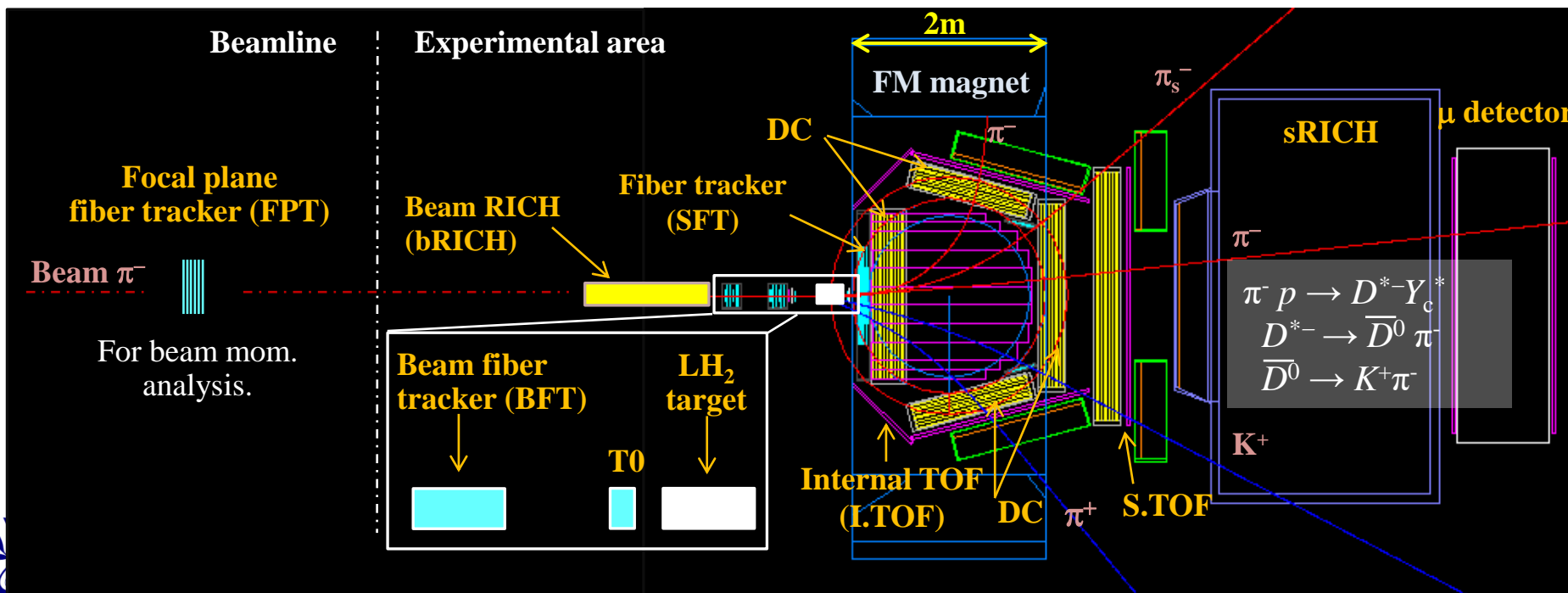
- Reveal the effective degree of freedom of the baryon internal structure, the di-quark correlation, by introducing heavy (c) quark.

Strategy

- Missing spectroscopy via the $\pi^- p \rightarrow D^{*-} Y_c^*$ reaction.
- Measure production cross and decay branching ratio simultaneously.



The experimental setup at J-PARC E50 experiment



Secondary π^- beam

- 20 GeV/c
- 30 MHz (60 M/spill)
 - (2s duration for slow extraction)

Target

- Liquid H₂, 4-g/cm²

Reaction

Charmed-baryon production

- ~1 nb/sr

Background reaction

- 2.4 mb/sr

Total reaction rate

- 1.5 MHz

Charged-particle multiplicity

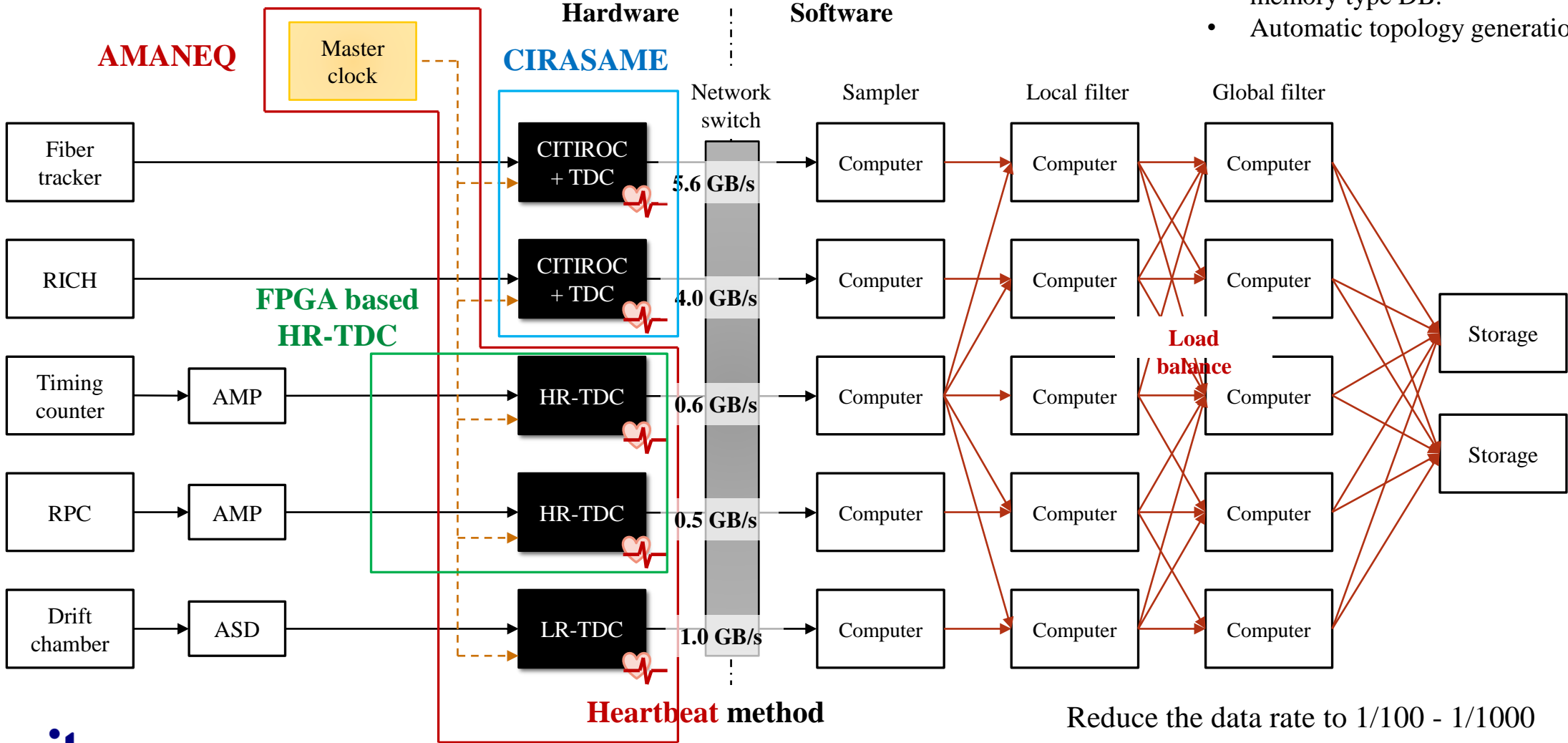
- 4

Trigger-less data-streaming-type DAQ system



Clock/command/timing distribution
(MIKUMARI)

Schema of the DAQ system



FairMQ +

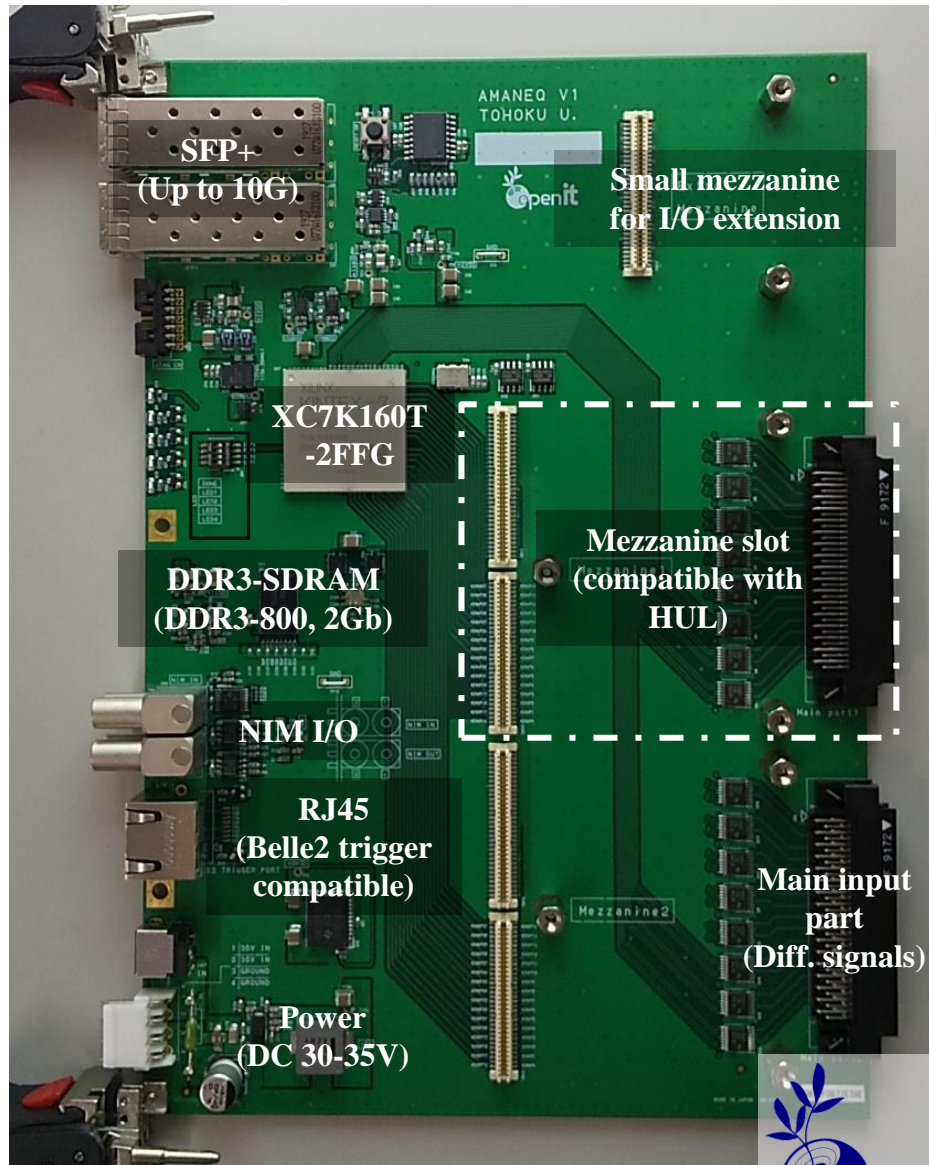
- Process monitor and control via in-memory type DB.
- Automatic topology generation

Reduce the data rate to 1/100 - 1/1000



Total data rate: ~12 GB/s (25 GB/spill) (E50 case)

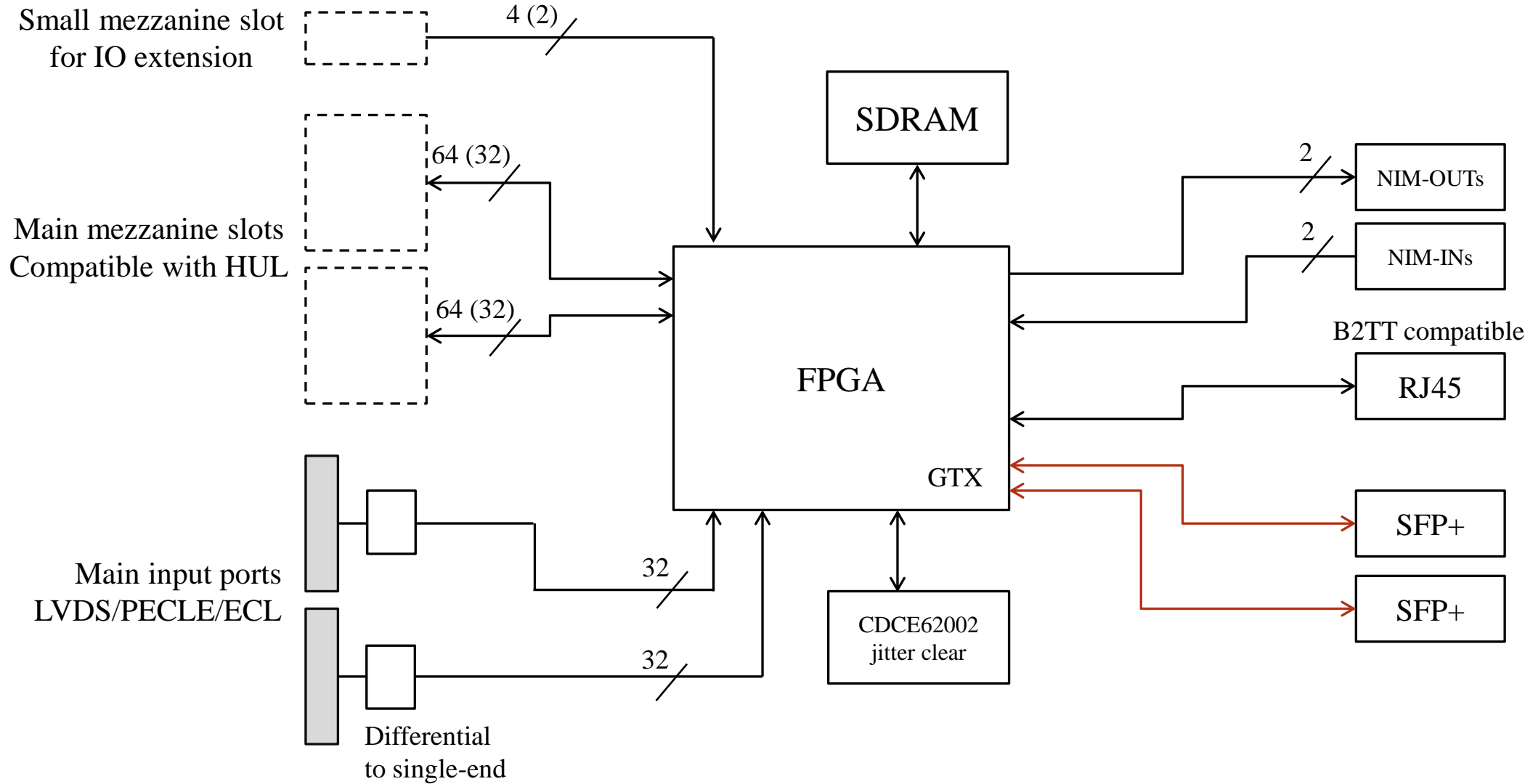
Front-end electronics



A main electronics for network oriented trigger-less data acquisition system (AMANEQ)

- VME 6U size but it doesn't have VME bus
 - VME crate without the power is used as a housing box
- Kintex7 with speed grade -2
 - Transceiver bandwidth up to 10Gbps
 - Can implement **SiTCP-XG**
 - **Throughput: 9.12 Gbps (96% of payload limit)**
- Main input ports compatible with HUL
- Has two mezzanine slot
 - **Compatible with HUL**
 - Hadron Universal Logic module (J-PARC hadron)
 - Mount HUL mezzanine HR-TDC
 - Mount DCR mezzanine for DC readout
- Belle2 trigger port (master clock)
- **Has a jitter cleaner (CDCE62002)**
- **DDR3-SDRAM** as a de-randomizer
 - DDR3-1333 with 16-bit bus width.
 - 2 Gb
- Powered by the external power supply with DC **30-35V**

AMANEQ

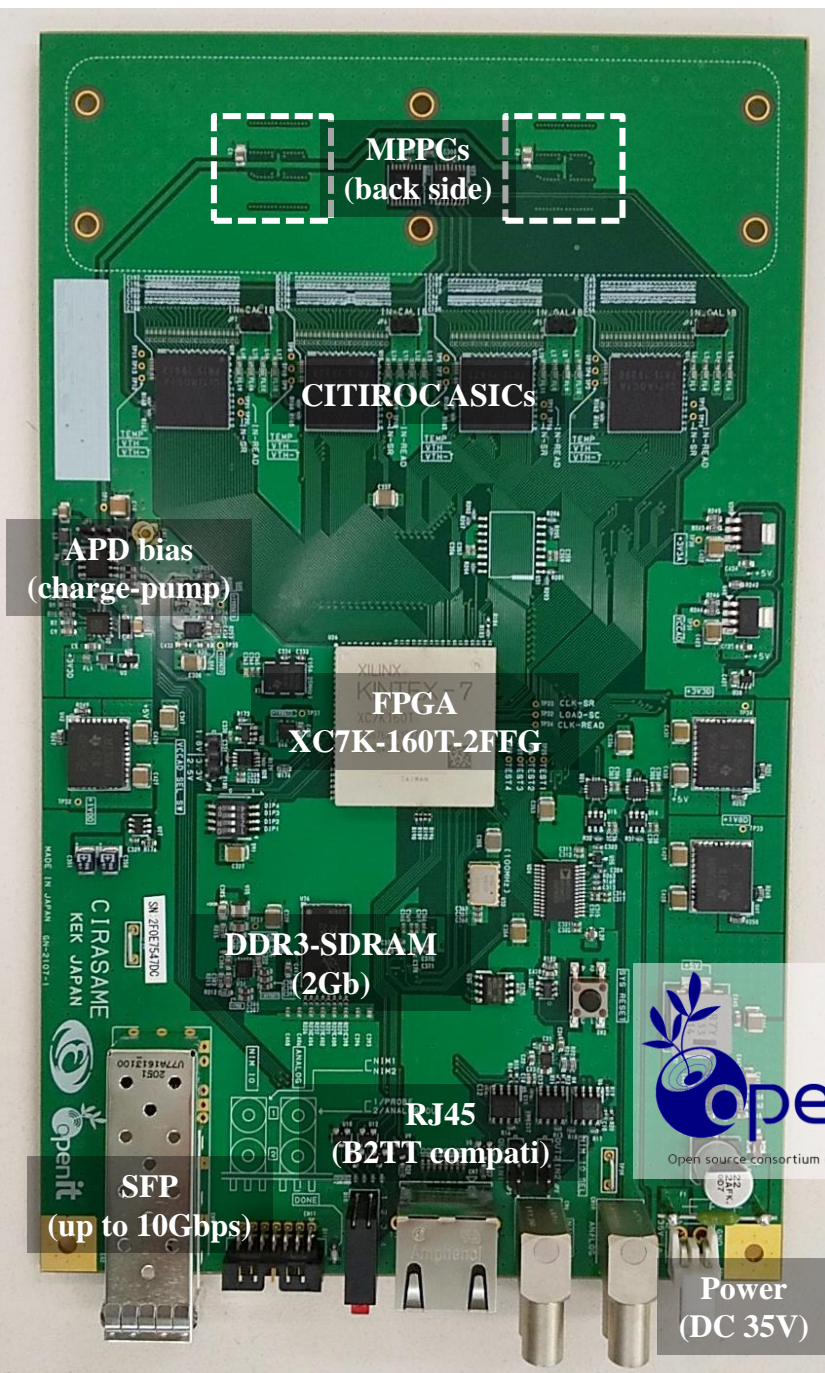


CIRASAME

CITIROC based multi-MPPC readout electronics for continuous timing measurement (CIRASAME)

- On detector FEE for scintillating fiber trackers and RICH.
- **Two 8x8 MPPC** arrays are directly attached. (128 ch)
- **Four CITIROC** chips read them.
- Kintex7 with speed grade -2
 - Can implement **10G SiTCP (SiTCP-XG)**
- Belle II link port (master clock)
 - Has a **jitter cleaner** to clean up the master clock
- **DDR3-SDRAM** as a de-randomizer
 - **DDR3-1333** with 16-bit bus width.
- Powered by the external power supply with **DC 35V**

Digital part is the same as that of AMANEQ.



MIKUMARI

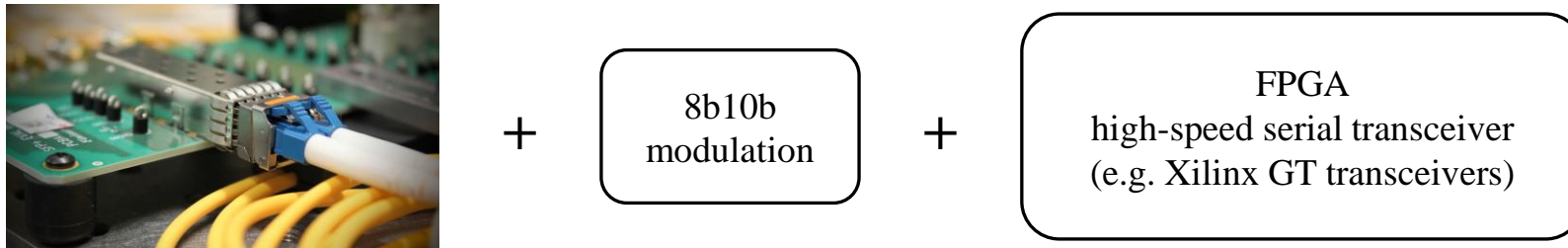
(Clock/command/timing distribution)

Clock-duty-cycle-modulation (CMCM) based transceiver

Requirements

- Low jitter (better than 20 ps)
- Synchronous timing/command/tag distribution
- Controllable phase of the recovered clock
- Distribute a clock over 100 m
- As few transmission lines as possible

Usual solution



It actually works well, but

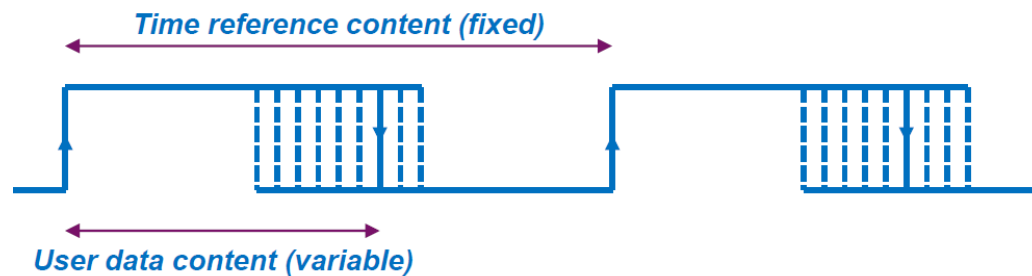
- Strongly depends on FPGA built-in blocks.
- **Need a special electronics** dedicated for distributing clock/data via serial transceivers.

Develop a serial transceiver independent clock/timing distribution system.

Develop a protocol to send a data and synchronous pulse over.

Adopting clock-duty-cycle-modulation (CDCM) as a core technology

- CDCM is a **data-on-clock** type modulation. (8b10b is a clock-on-data type)
- Data bits are embedded to the trailing edges of the clock signal.

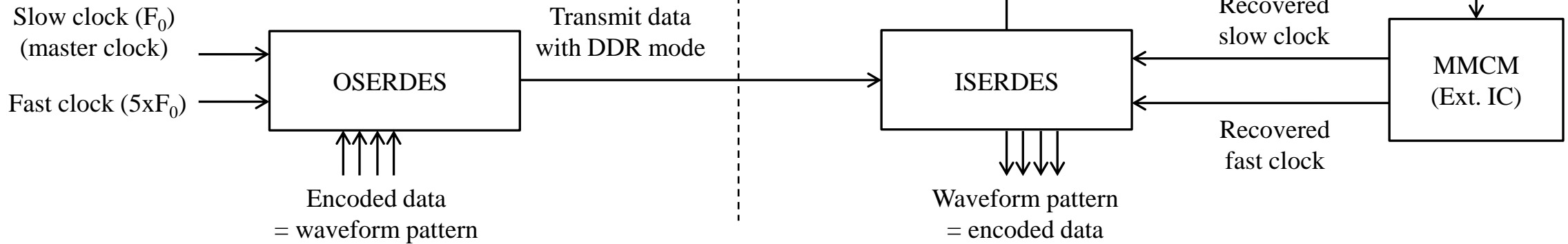


Denis Calvet,
IEEE TNS (Volume: 67, Issue: 8, Aug. 2020)

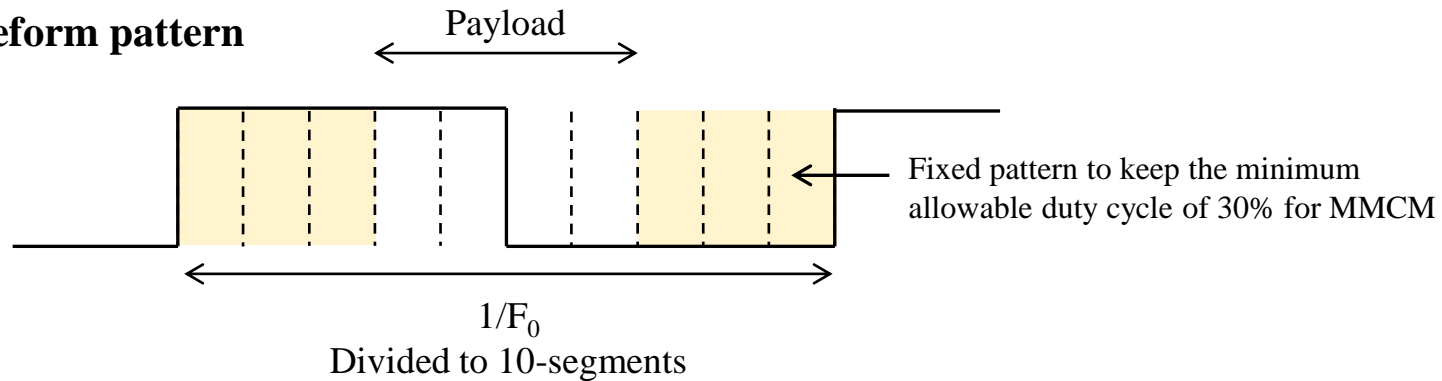
Advantages

- **This modulated clock can be directly input to PLLs and MMCMs in FPGA and external jitter cleaner ICs.**
 - Because the leading edge is used by the phase detector to control VCO, but the trailing edge is not.
- Output clock skews from MMCMs respect to the input modulated clock are automatically adjusted by using the global clock network in FPGA.
 - Automatic phase alignment among front-end electronics.
 - Recovered clock by MMCM can give a phase reference for a clock from the external PLL, which does not have a zero-delay mode.

Modulation and demodulation by IOSERDES



Waveform pattern

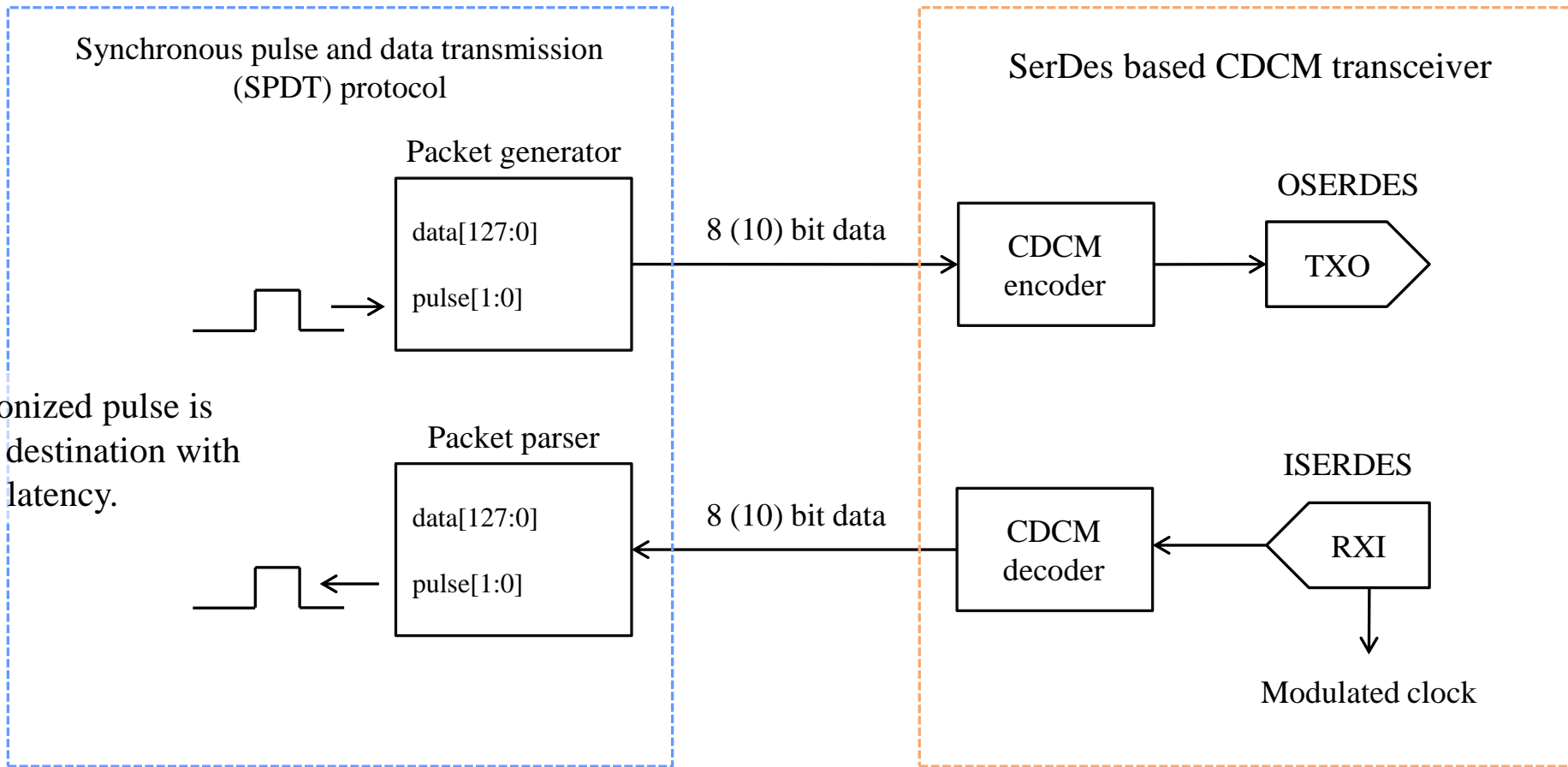


*0.5 means idle pattern
 Naming rule is defined in Ref. [1]
 CDCM-10-2.5
 CDCM-10-1.5
 are realized by IOSERDES

For skew adjustment between slow and fast clocks, the global clock buffer is necessary.

- Maximum transferrable frequency: 125 (142) MHz due to the limitation of the BUFG performance.

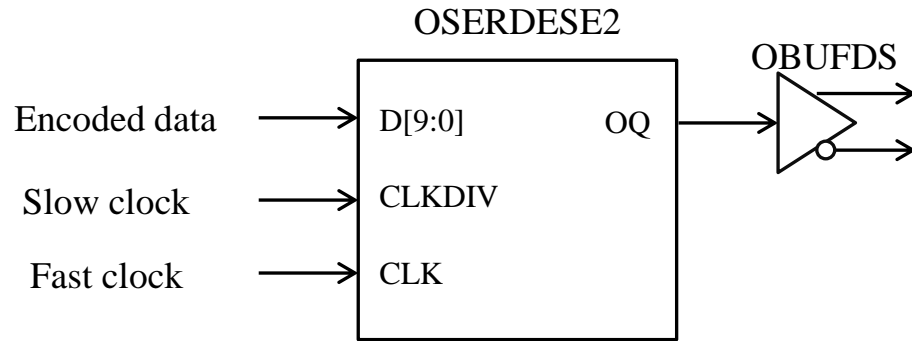
[1]. D. Calvet, IEEE TNS (Vol67, Issue8, Aug. 2020)



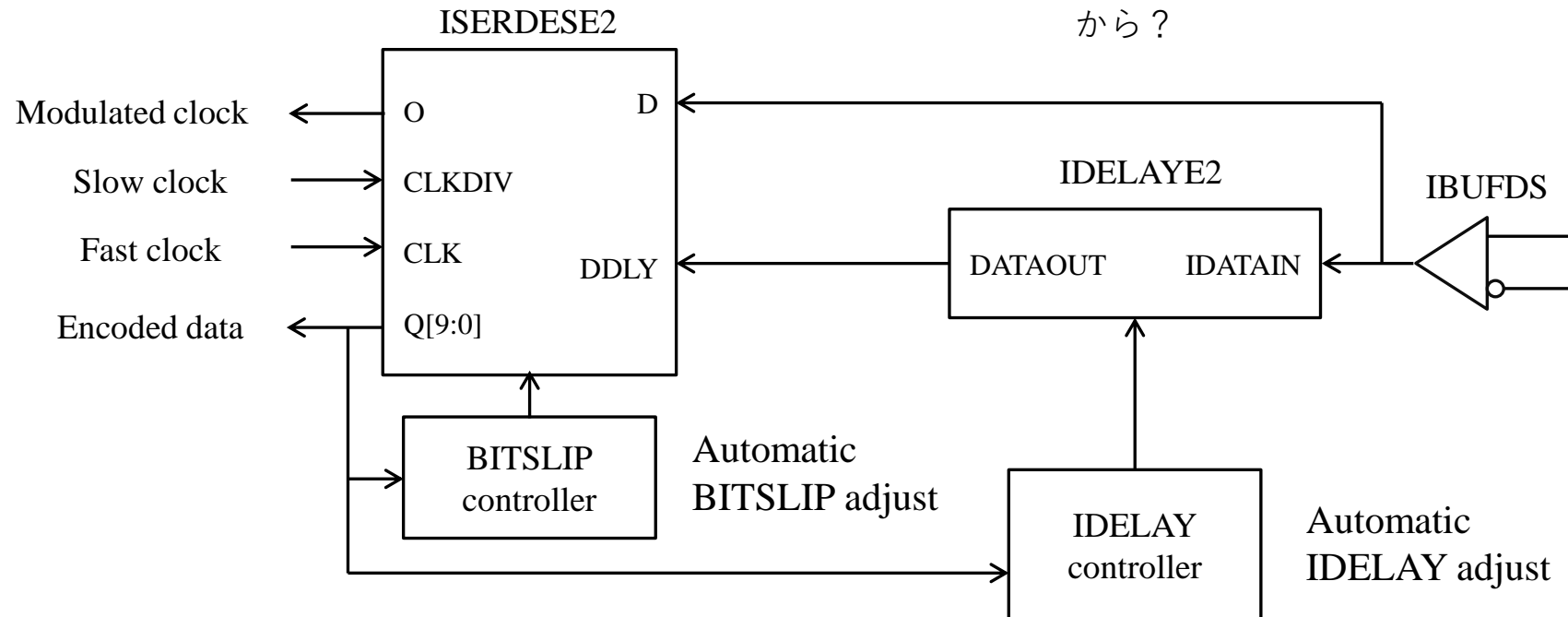
MIKUMARI

水分神 (みくまりのかみ): 水の分配をつかさどる神

TXO



RXI

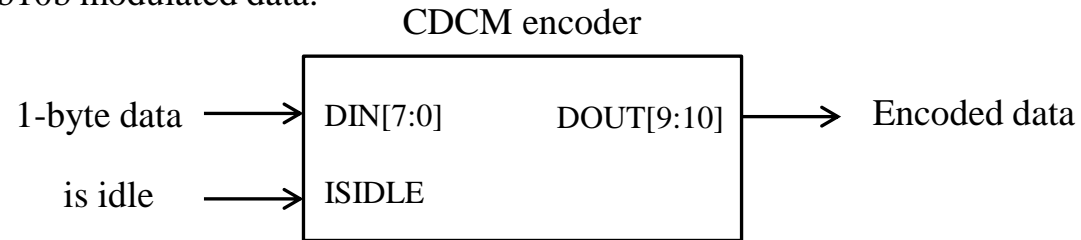


余談

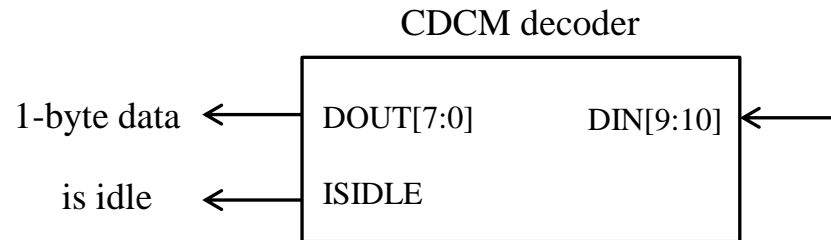
- IDELAYE2を実装するとmodulated clockを直接取り出せなくなる。専用配線が割り当てられるから？

Encoder

*10-bit length data input
is also supported for
8b10b modulated data.



Decoder



CDCM-10-2.5 encode table

Binary	Encoded
00	0000
01	0001
IDLE	0011
10	0111
11	1111

Synchronous pulse and data transmission (SPDT) protocol

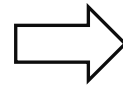
SPDTP packet structure

Magic (0xFD)	Data length + Instruction	Pulse timing	Reserve	User data	Check sum	IDLE
1 byte	1 byte	2 byte	1 byte	0-16 byte	2 byte	1 byte

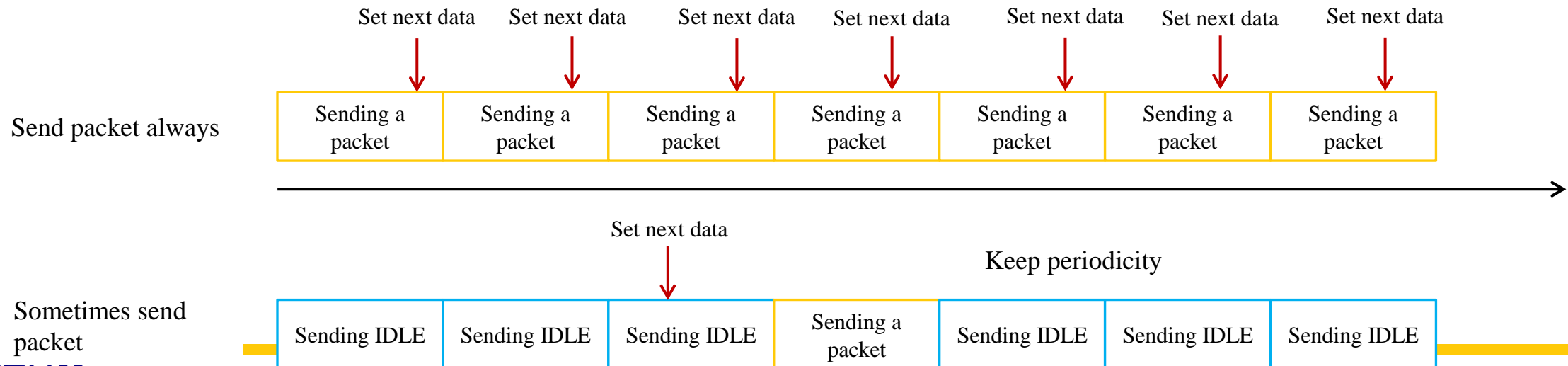
- CDCM data rate: **2-bit per clock-cycle** (CDCM-10-2.5)
- Encoder/decoder need **4 clock-cycles** to encode/decode 1-byte data.
- SPDTP packet size: 8-bytes + user data (0-16 bytes)
 - **32-96 clock-cycles** are necessary to send/receive a packet.

***IDLE: duty 50% pattern.

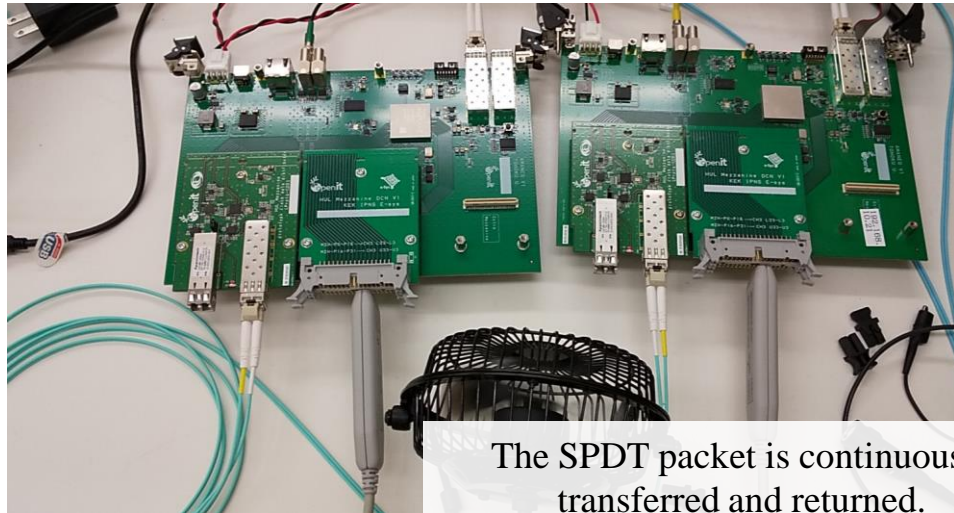
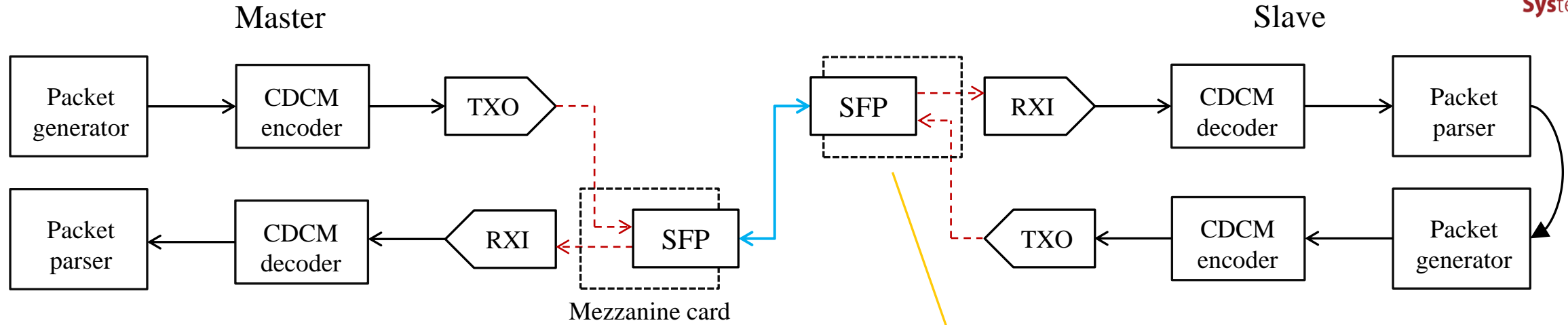
Expect to periodically transfer a fixed size packet.
Currently, interrupt at any timing is not considered.



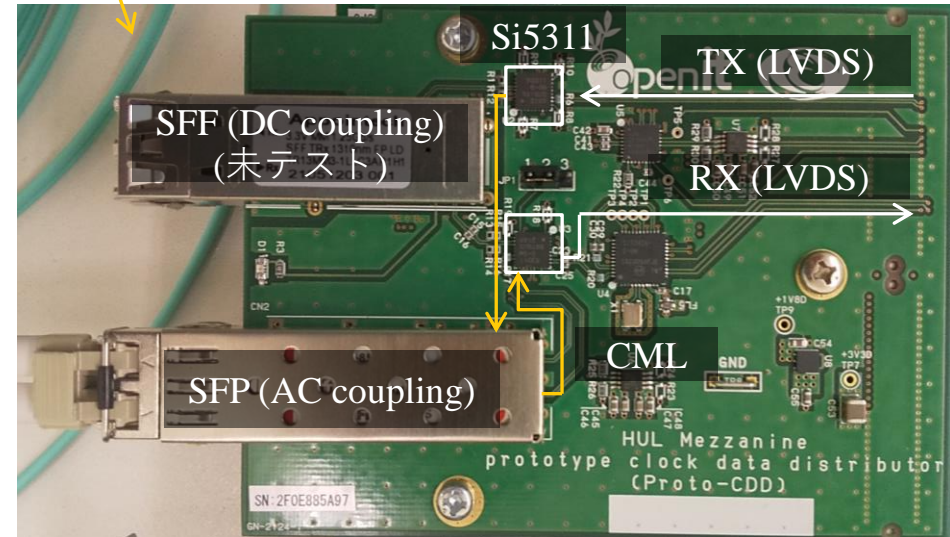
Pulse timing is included in a packet.

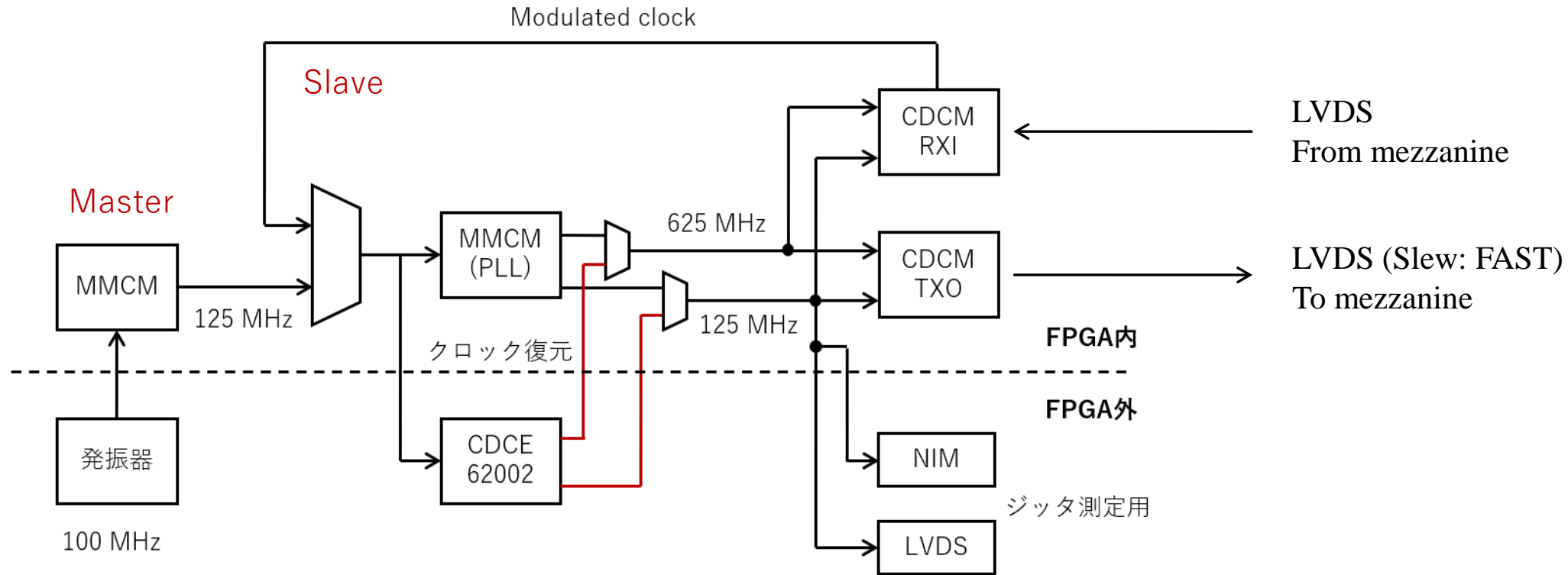


Test results



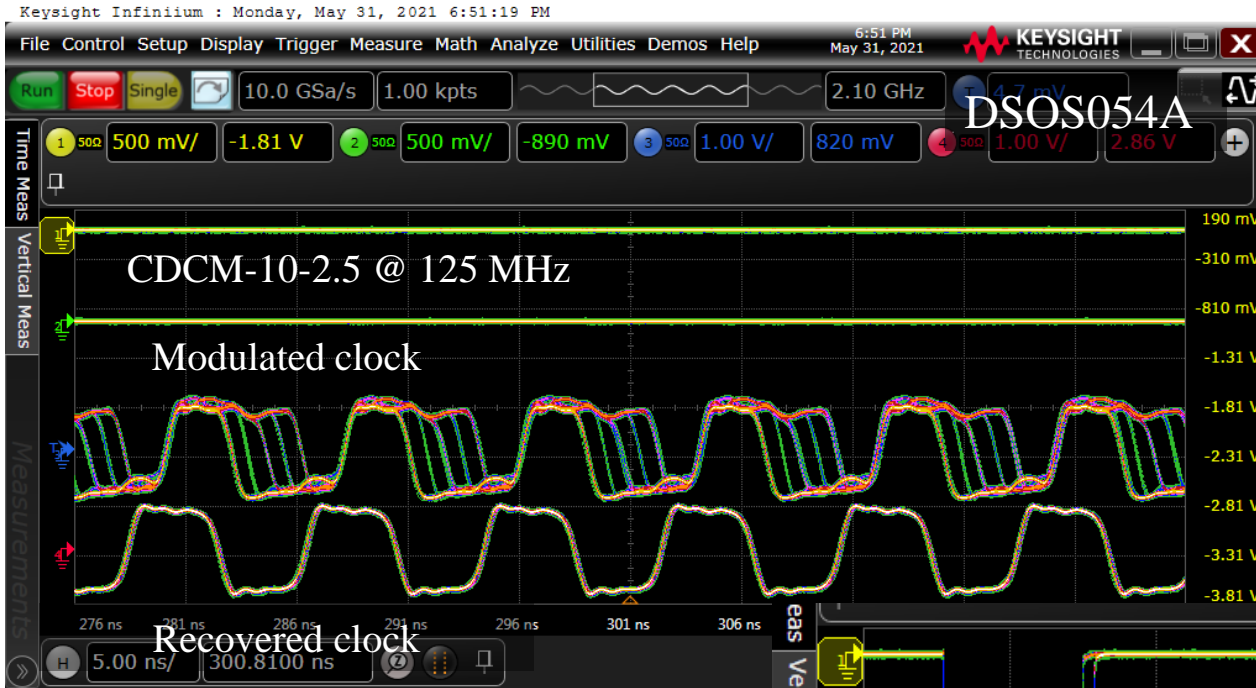
The SPDT packet is continuously transferred and returned.
User data: incremental data.





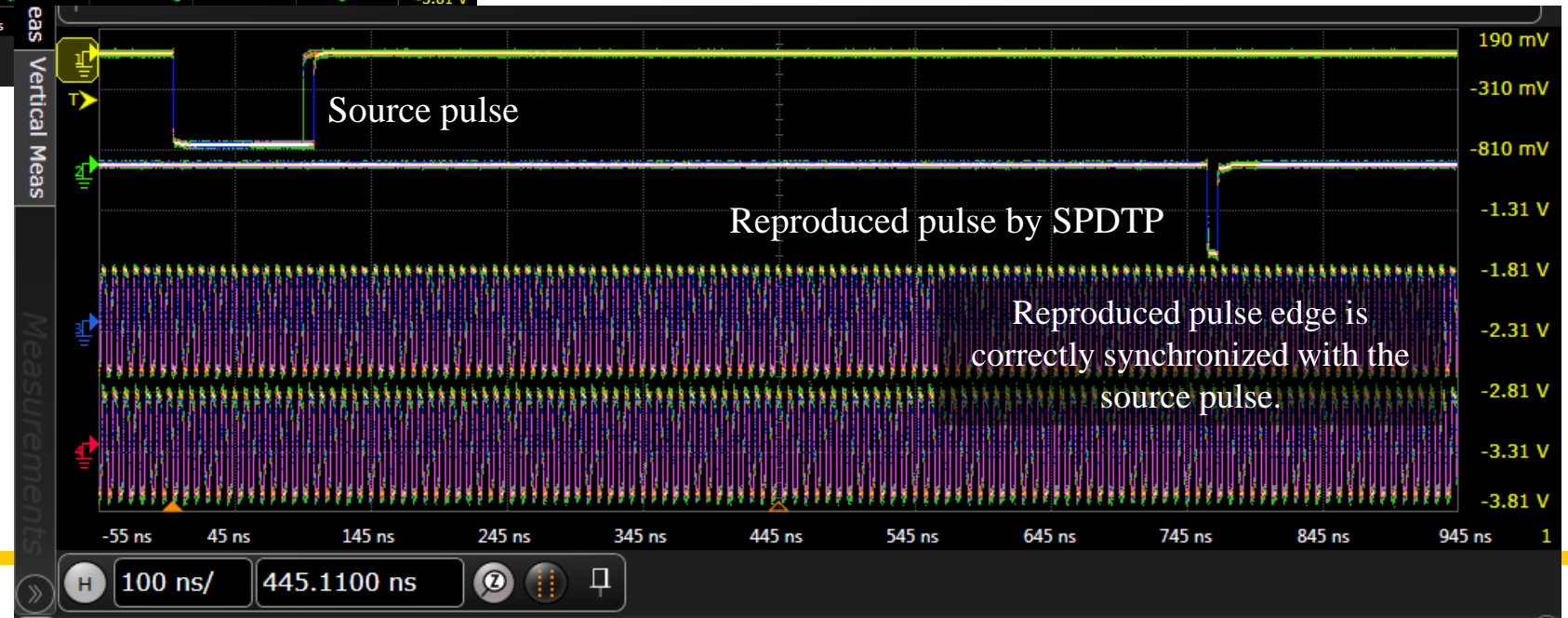
Used oscilloscope

- Keysight DSOS054A (Analog BW: 2.1 GHz, 20 GS/ps)
 - For NIM signal measurement
- Tektronix DPO 7254 (Analog BW: 2.5 GHz, 40 GS/ps)
 - For LVDS measurement



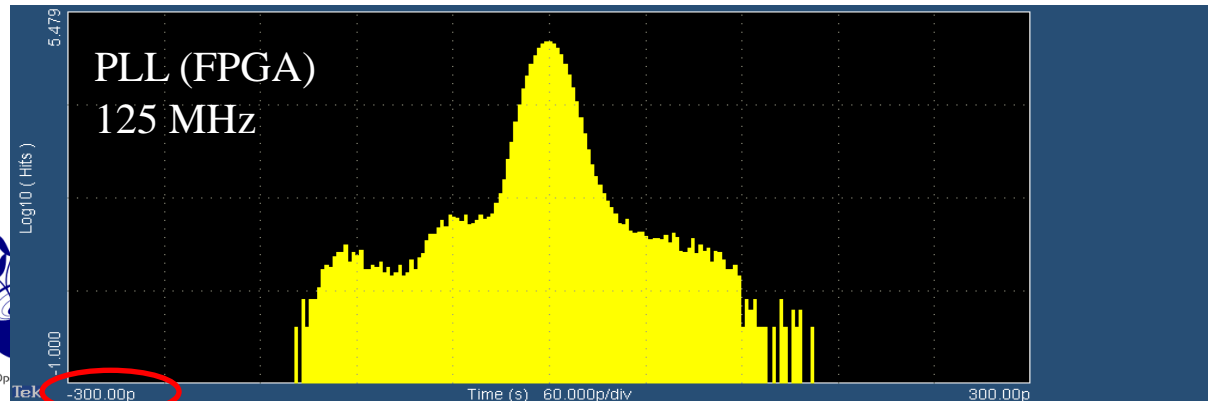
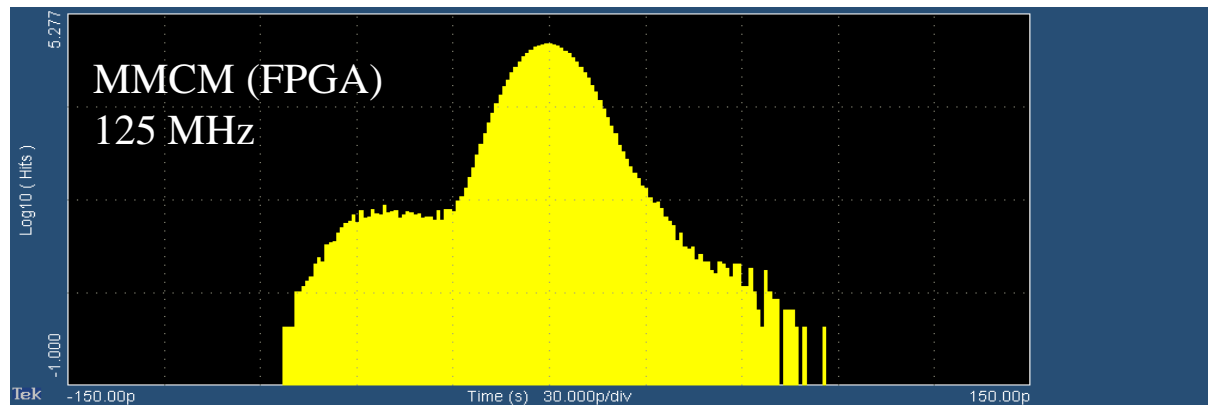
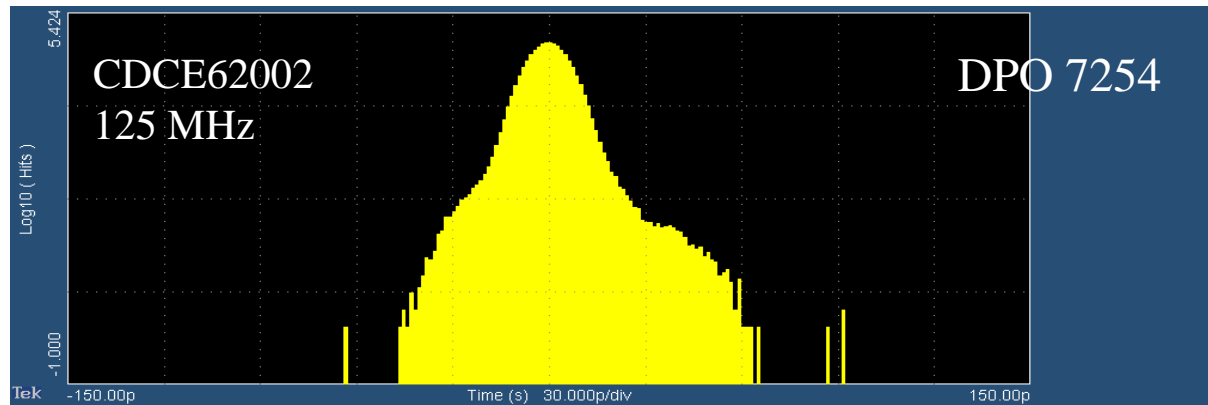
40T packets were transferred in this demo.
No packet drop and checksum mismatch were happened.

Pulse transfer by SPDT protocol



Jitter performance of master clock

Jitter distribution of master clock



	Std. div.	Total jitter (Tj) @ BER 1e-12
CDCE62002	5.0	110 77
MMCM	7.9	190 106
PLL	8.8	297 114

DPO7254
DSOS054A

Unit: ps

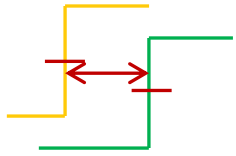
	CDCM linkup	SPDT data transmission
CDCE62002	Succeed	Succeed
MMCM (FPGA)	Succeed	Succeed
PLL (FPGA)	Succeed	Fail

Linkup: Completing IDELAY adjust and bit slip for SERDES and encoder/decoder.

FW with PLL detects the broken modulated pattern soon after the communication start.

Modulated pattern transfer and/or receive don't work well due to the large clock jitter.

Jitter performance of recovered clock

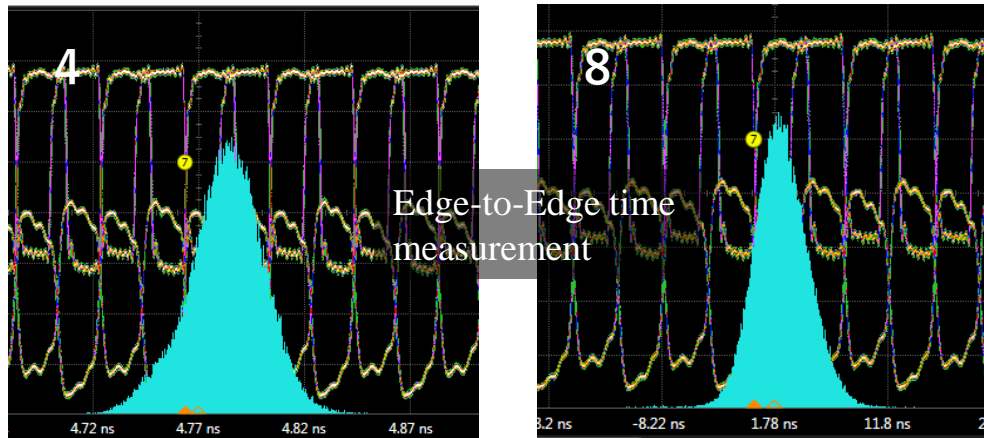


Edge-to-Edge time measurement
between master and recovered clock

Recovered clock jitter

Condition	Master	Slave	データ送信	Edge-Edge Std. div.	Std. div.	Tj @ BER 1E-12
1	CDCE	CDCE	SPDTP	12.5	8.9	158 70
4	MMCM	MMCM	SPDTP	17.7	15.5	240 168
5	CDCE	CDCE	アイドル	11.4	8.8	162 71
8	MMCM	MMCM	アイドル	11.9	7.6	213 121

Unit: ps

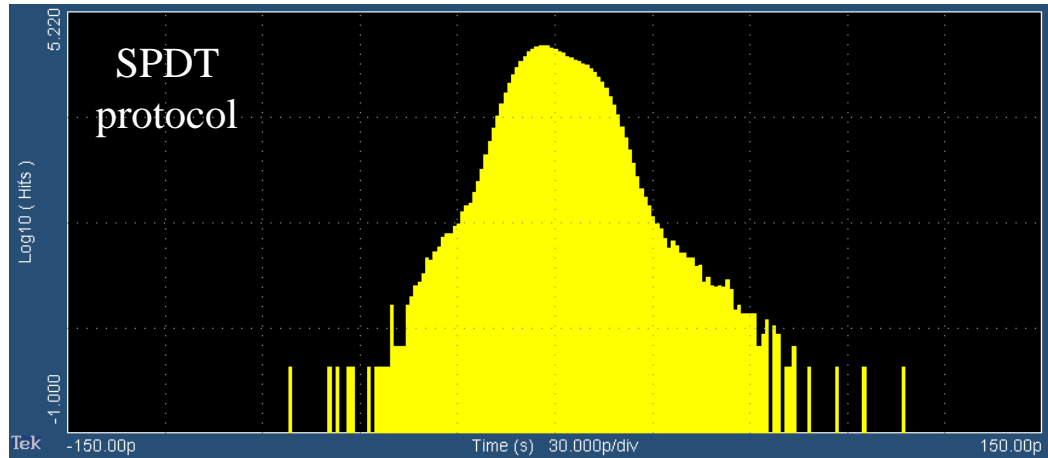


Edge-to-Edge measurement reflects the structure of the main peak of the jitter distribution.

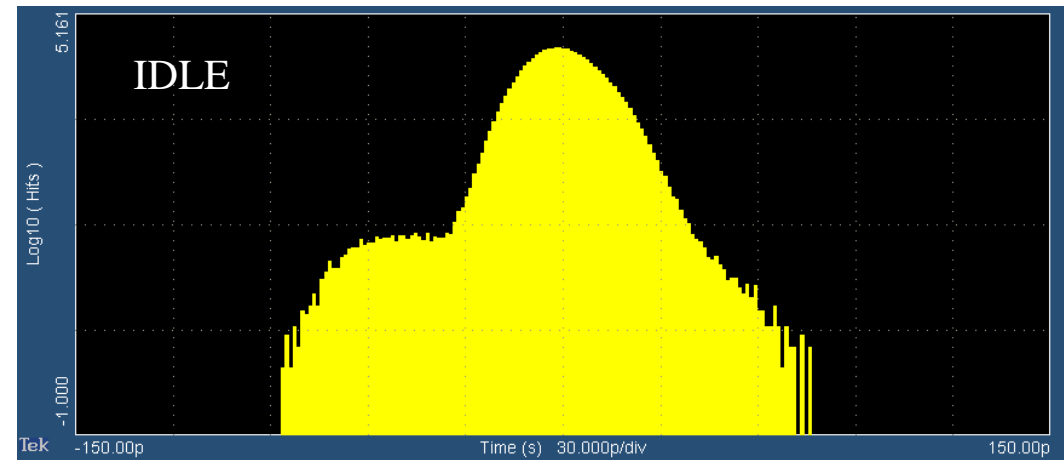
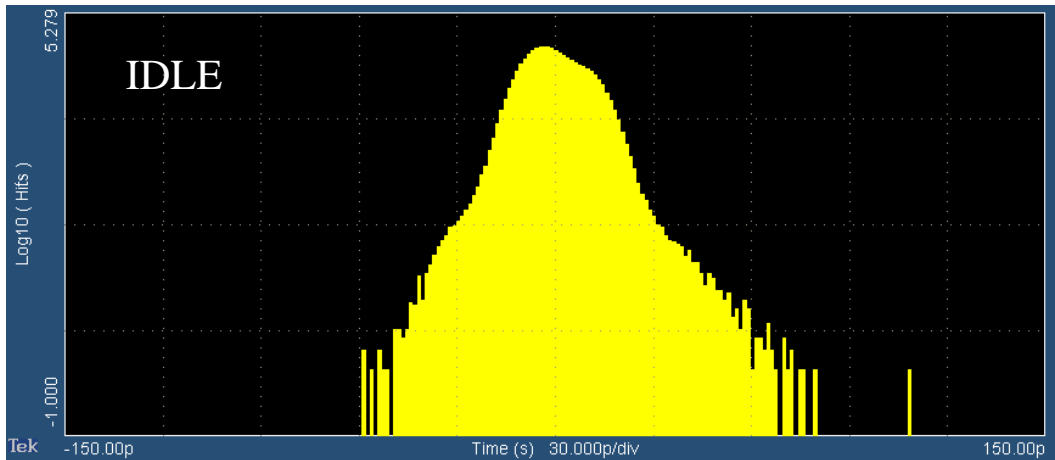
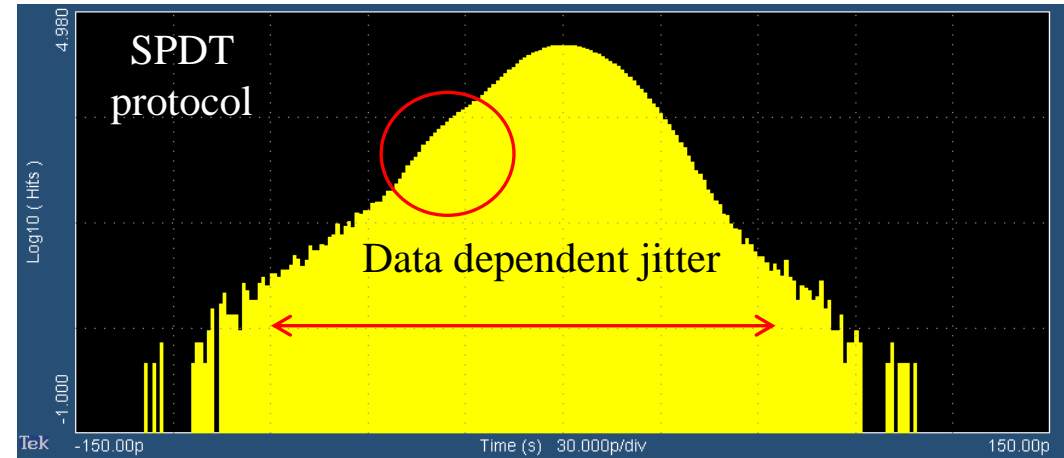
In order to take into account the long tail structure, additional jitter measurement using the spectrum fitting is necessary.

Jitter performance of recovered clock

Jitter distribution of recovered clock
(CDCE62002 - CDCE62002)



Jitter distribution of recovered clock
(MMCM - MMCM)

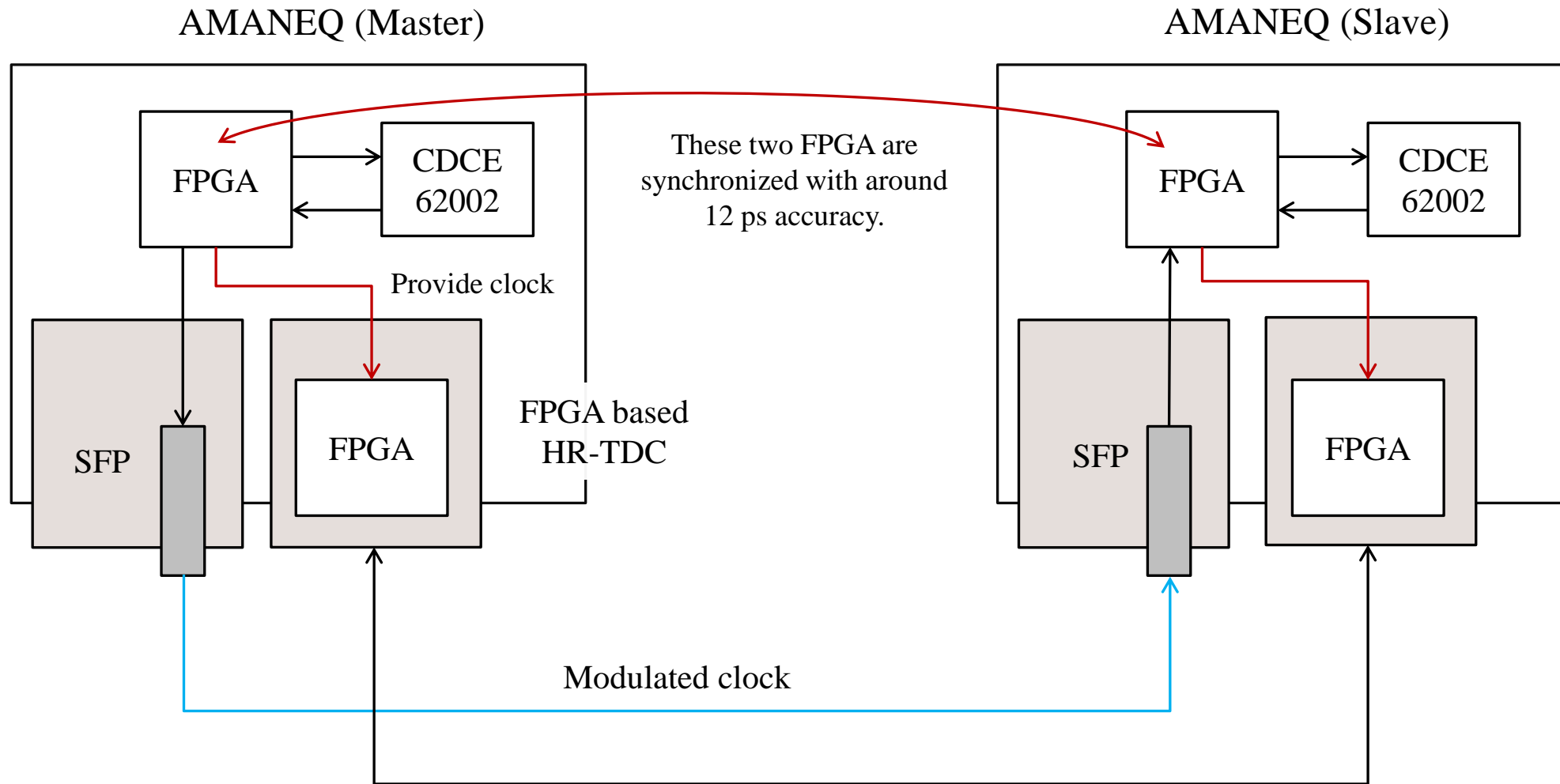


Data dependent jitter is suppressed in the case of CDCE62002.

If you use MMCM, sending IDLE pattern provides a better jitter performance.

Synchronize FPGA HR-TDC

Test setup (HR-TDC)



What we really want to know:
Timing resolution of synchronized HR-TDC

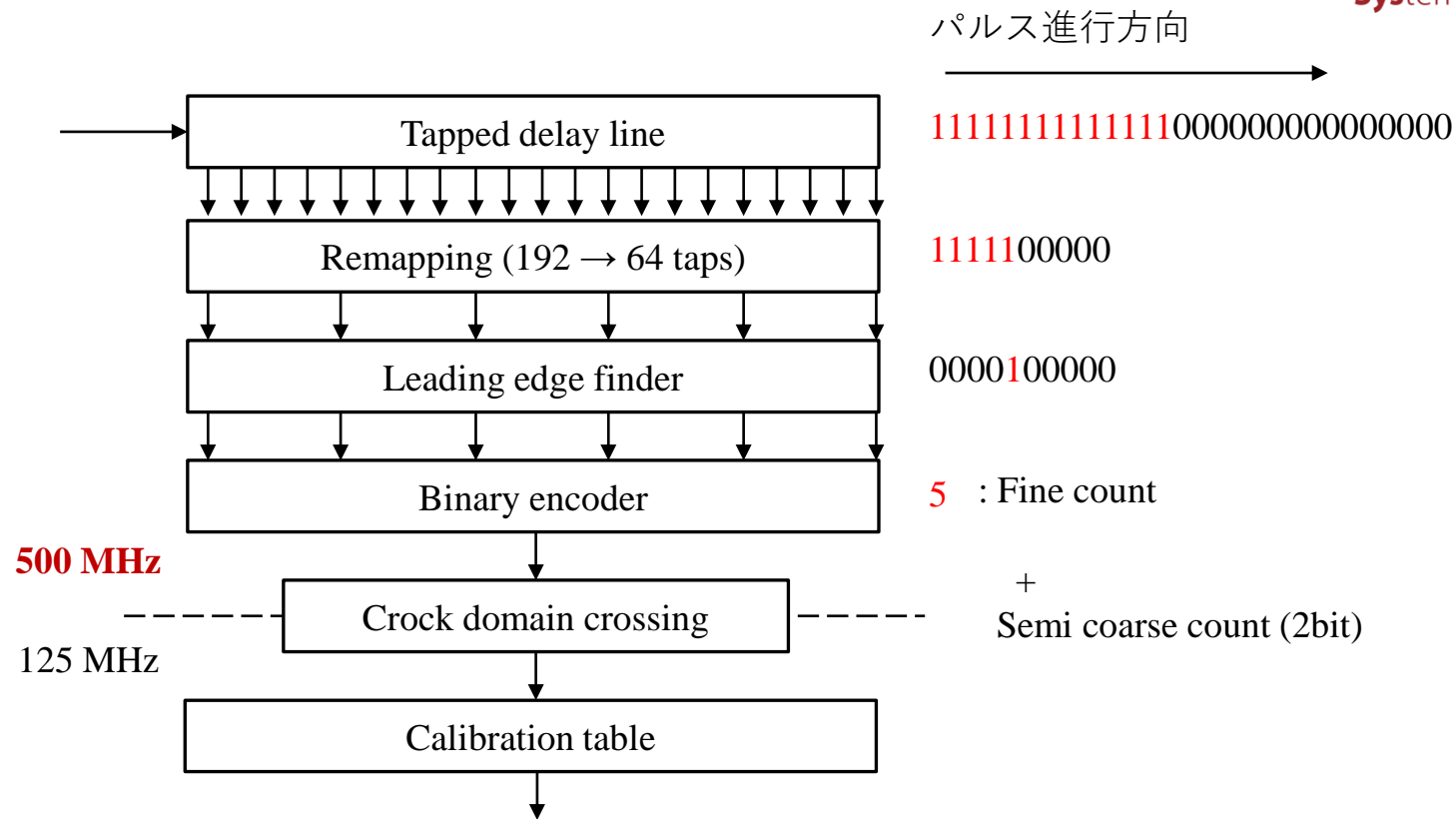
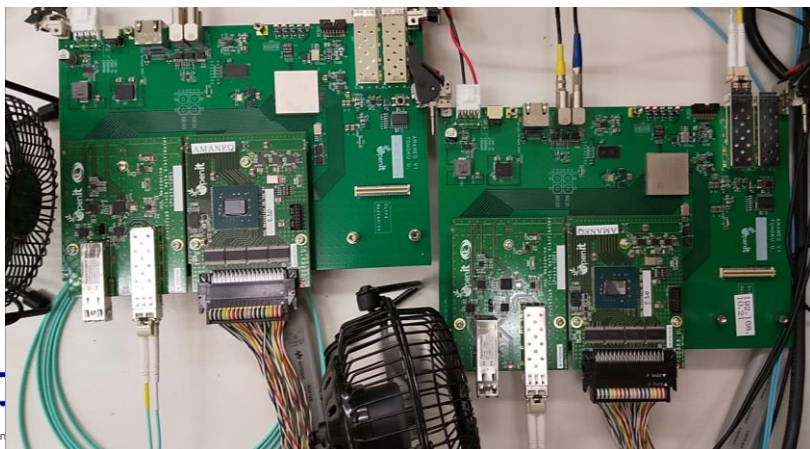
FPGA based HR-TDC

HUL/AMANEQ mezzanine HR-TDC



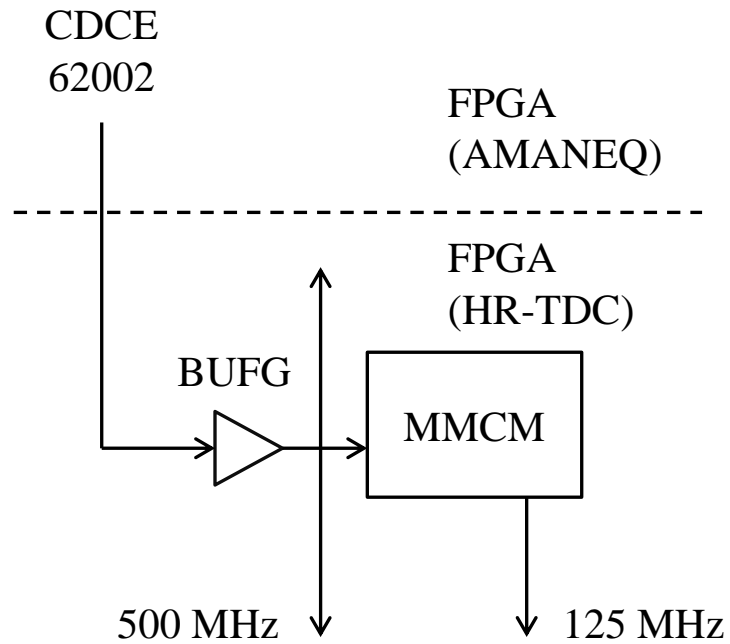
32 ch FPGA based HR-TDC

- Both leading/trailing edges
- Intrinsic resolution: 15 ps (σ)

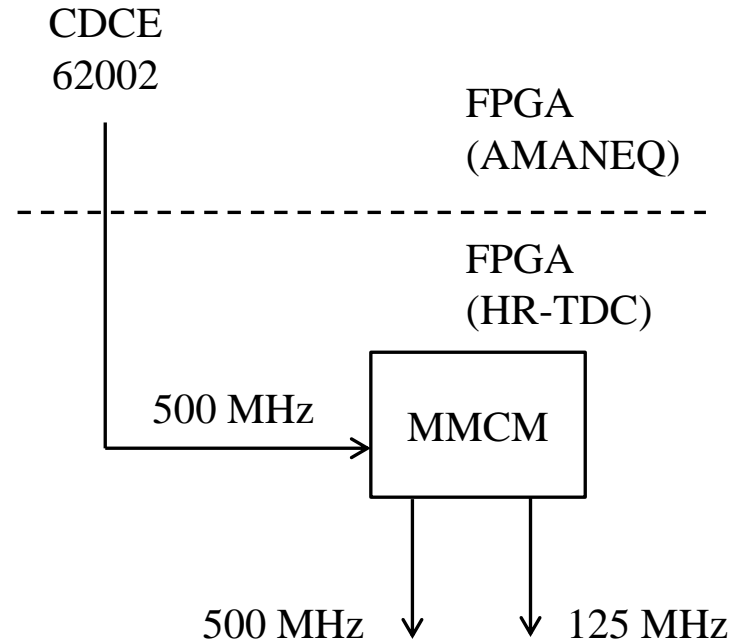


Precise synchronization of the sampling clock (500 MHz) is the key.

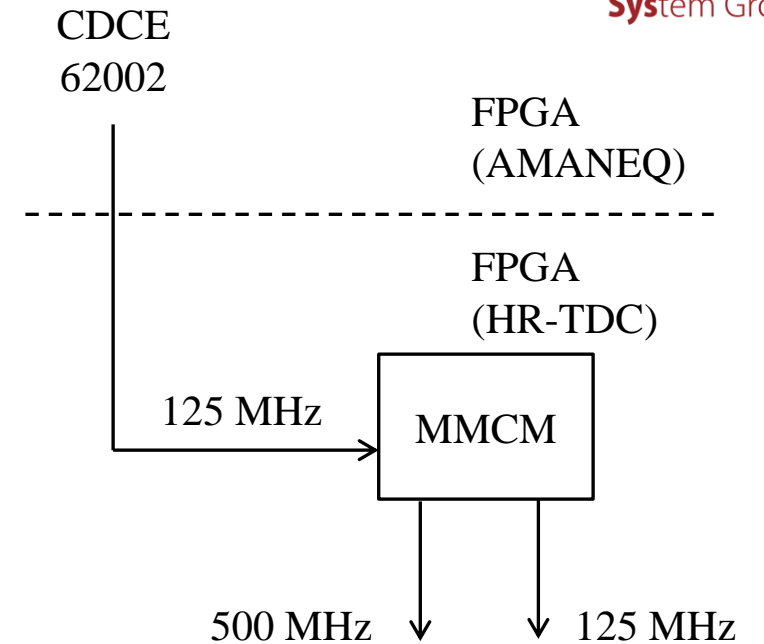
Possible clock path



Pattern 1



Pattern 2



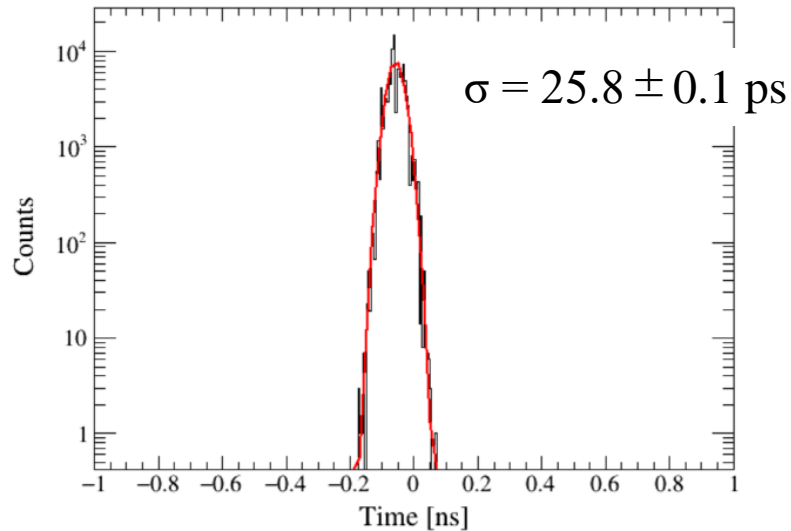
Pattern 3

Test results

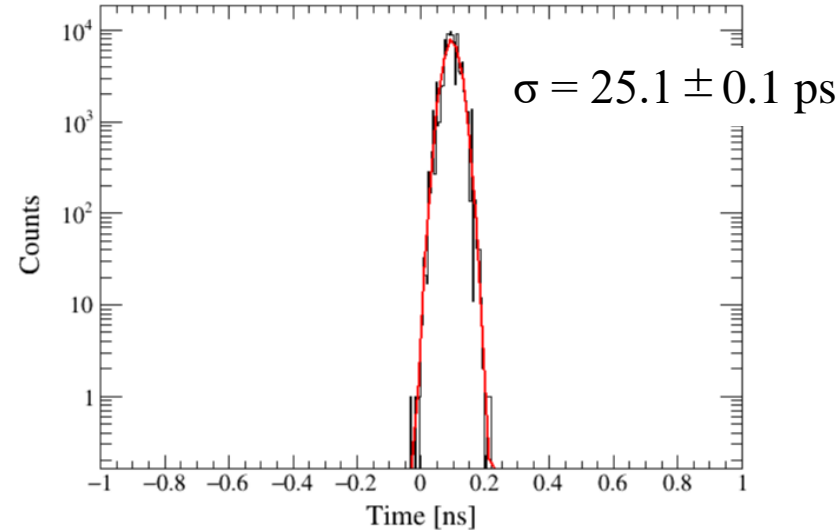
The resolution when two signals were input to the same HR-TDC.

- 20.6 ± 0.1 ps (σ), $\Rightarrow \sqrt{2} * (\sigma_{\text{intrinsic}})$

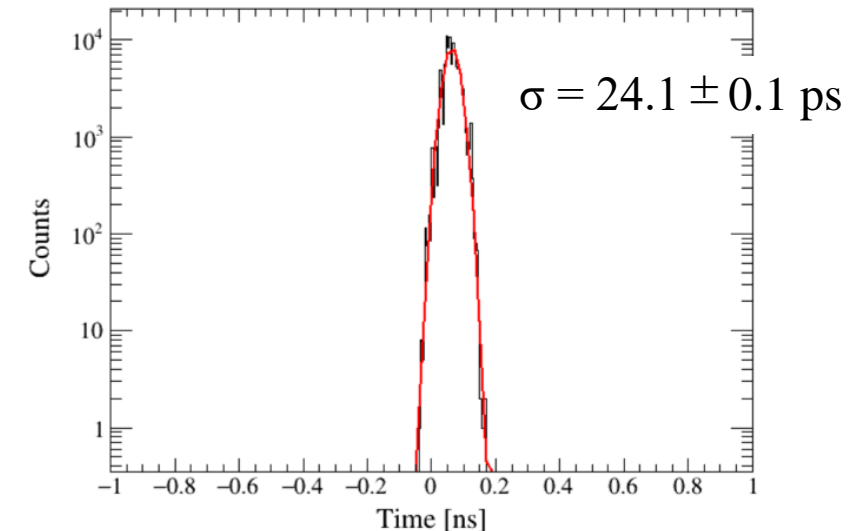
Time difference (pattern 1)



Time difference (pattern 2)



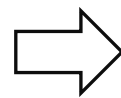
Time difference (pattern 3)



The sufficient performance for the J-PARC E50 experiment.

Pattern 3 is preferred because the 125 MHz clock phase is aligned to that of input clock (recovered clock from CDCM).

$$\sigma = \sqrt{2\sigma_{\text{intrinsic}}^2 + 2\sigma_{\text{random}}^2}$$



$\sigma_{\text{random}} \sim 8-10$ ps

Consistent with the result so far.

- CDCMを利用したクロック・タイミング伝送は、SiTCPを使っている実験では、良いツールになると思われる。
- GTトランシーバを使ってデータ読み出しと同期を行っているシステムでは恩恵がない。
- FPGAの一般IOを使ってIOSERDESで変調クロックのやり取りを行う事がキモであるため、信号規格は問わない。短距離であればメタルケーブルでつないでもよいと思う。
- 伝送可能なクロックスピードは下がるだろうが、単一端信号でも同様の事が可能である。
- AMANEQのメザニンのような拡張基板を用意すれば、MIKUMARIは簡単に実装できる。
- 7シリーズのファミリ、HP・HRバンクの別でIOスピードが異なるのでその点だけ注意。
- 今回使ったSFPモジュールはFS.comの1000BASE-SR用の光モジュール。
- SFP+のTXとRXの信号線はSFF-8431の規格でCMLを使う事が決められているが、差動振幅(V_{OD})は400-2000 mVと幅がある。実際に測ってみるとFS.comのモジュールは $V_{OD}=800$ mV程度。普通のCML信号だと思われる。
- 今回はまじめにCML-LVDS変換を行っているがRXは直接FPGAへつないでも大丈夫 (V_{OD} だけ要確認)。通常SFPモジュールはAC結合なので、FPGA側はre-biasするかDCIを使って入力同相電位を決める必要がある。
- TX側はLVDSのスイングが小さいので、ICでCMLへ変換した方が無難だと思われる。

- The trigger-less data-streaming-type DAQ system is introduced in the J-PARC E50 experiment and is shared among the other experiments in the high-p beam line.
 - The total expected data is 12 GB/s for the E50 case.
- A main electronics for network oriented trigger-less data acquisition system (AMANEQ) was developed.
 - Two mezzanine slots, which is compatible with HUL, for the function extension.
 - Two data link with the speed up to 10 Gbps. Realized 10 Gbps TCP communication by SiTCP-XG.
 - 2 Gb DDR3-SDRAM.
- The obtained throughput of **SiTCP-XG was 9.12 Gbps. 96% of the TCP payload limit.**
- CIRASAME was developed for readout for the scintillating fiber trackers and RICH detectors.
 - It has four CITIROC1A ASICs.
 - Digital part is the same as that of AMANEQ.
- Heartbeat method was developed for the continuous timing measurement without any external timing reference signal.

- AMANEQ will be used for the clock/timing distribution in the J-PARC experiments.
- In order to transmit the clock and data using a full-duplex optical transceiver, **clock-duty-cycle-modulation** was adopted.
 - **The modulated clock can be directly fed into PLL.**
- SerDes based CDCM transceiver and the synchronous pulse and data transmission (SPDT) protocol were developed and implemented in FPGA on AMANEQ.
 - The maximum clock frequency can be transferred by this transceiver is **125 and 142 MHz for the speed grade -1 and -2 FPGA**, respectively.
- The jitter performance of CDCE62002 is better than that of MMCM in FPGA.
 - 5.0 ps in std. div., ~110 ps peak-to-peak (eye measurement.)
- PLL in FPGA accompanies a long tail in the jitter distribution. And the clock from PLL can not drive the CDCM transceiver correctly.
- The two AMANEQs are synchronized within **12-13 ps in std. div..**
- Basically, **sending IDLE patten except when the trigger is transmitted provides the better jitter permeance.**
- **Timing resolution between two FPGA based HR-TDCs synchronized by MIKUMARI is 24-26 ps (σ).**

Requirement from E50

Momentum analysis is essential to reduce the trigger rate to the acceptable ($\sim 10\text{kHz}$) rate.

+

Other physics program at this beam line

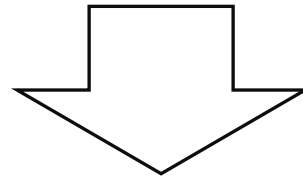
Λp scattering

Ξ^* spectroscopy

Pion-induced Drell-Yan

I=3 dibaryon search

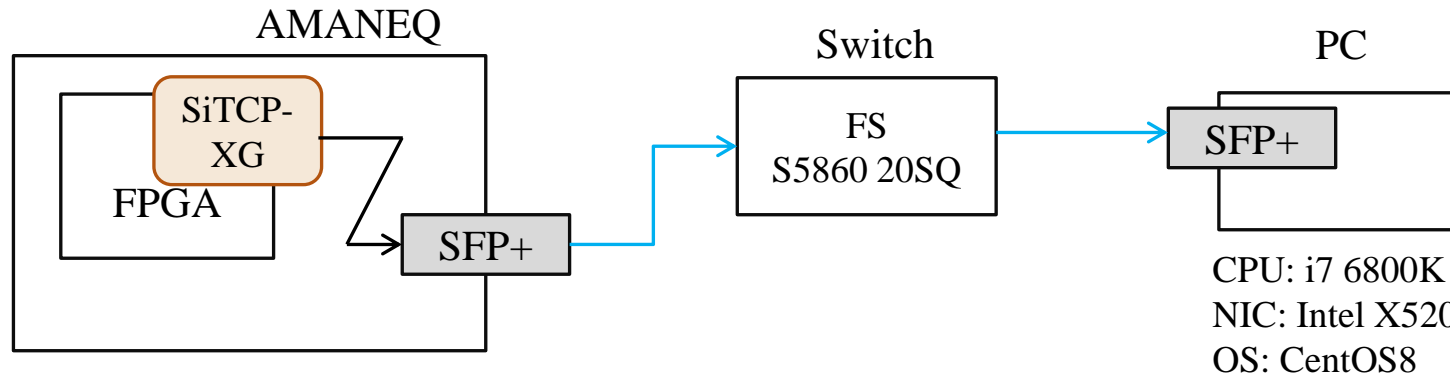
The required trigger condition are different.



The DAQ system must be flexible and scalable.

Omit the hardware (FPGA) based trigger,
and introduce the trigger-less data-streaming-type DAQ system.

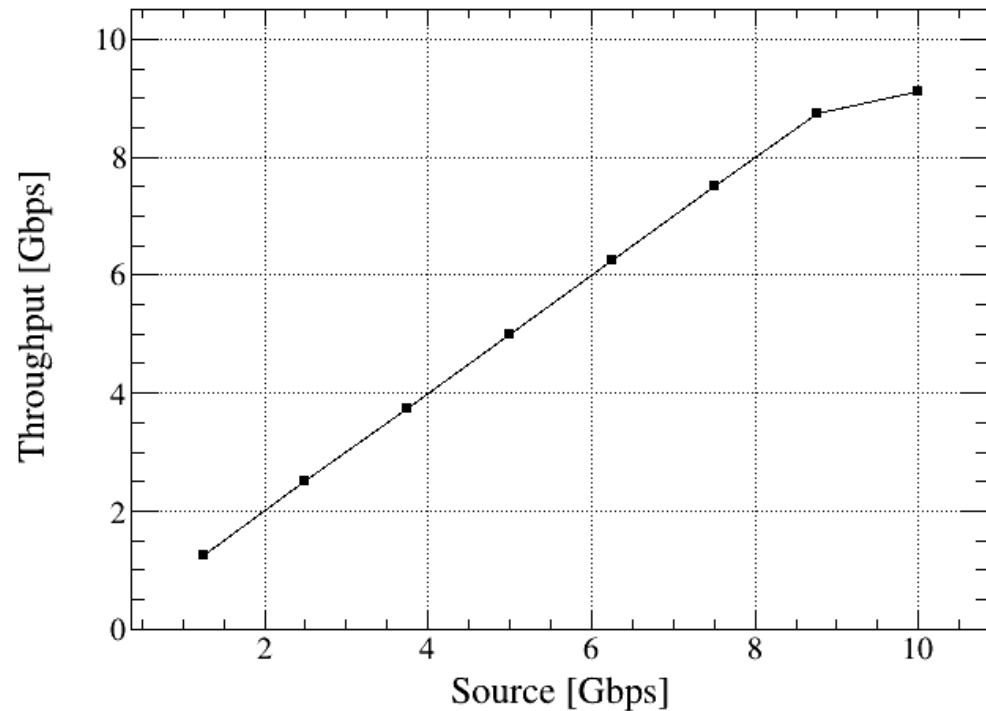
Test setup



Read data using
C++ software.

Tested by H. Sendai (KEK E-sys)

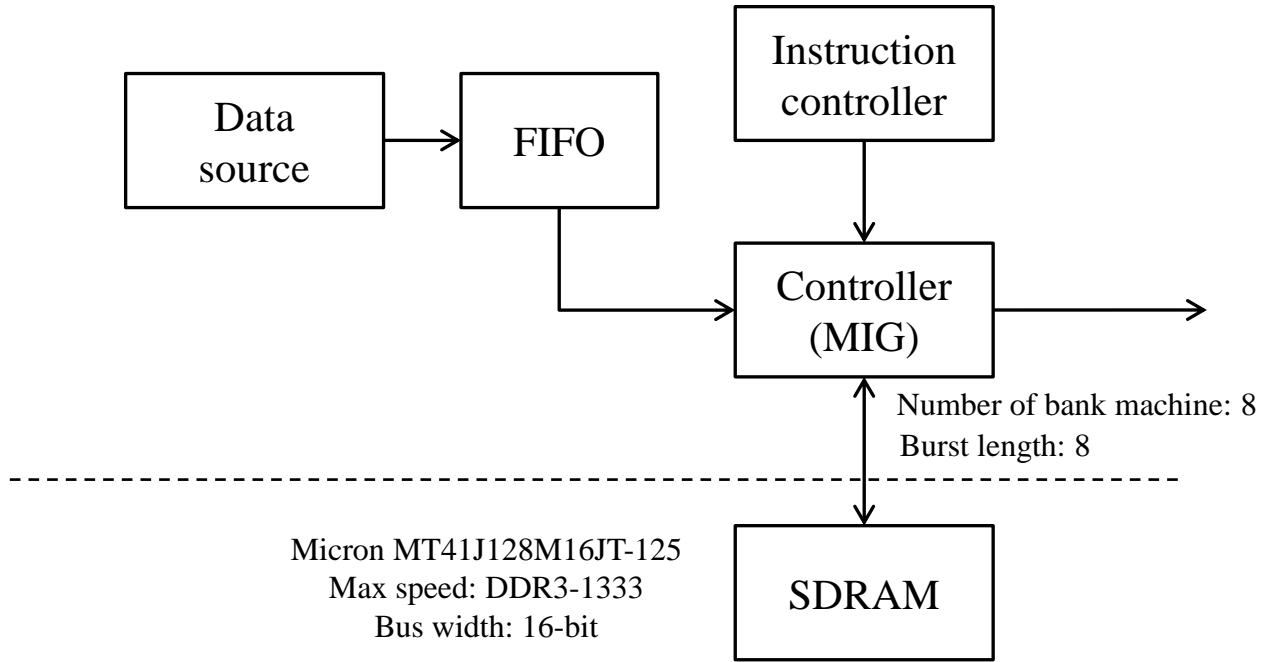
Measured throughput



Obtained throughput: **9.12 Gbps**
~96% of TCP payload limit (MTU 1500)

Throughput of DDR3-SDRAM

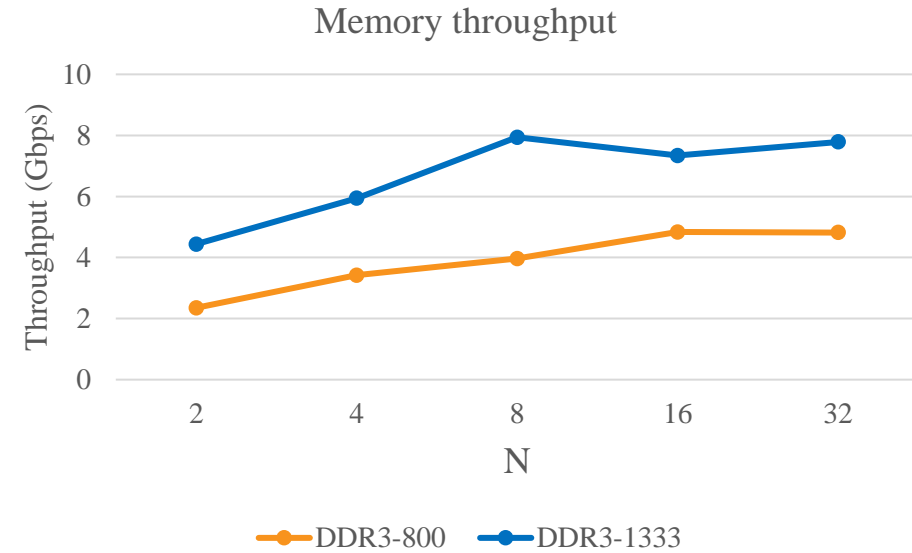
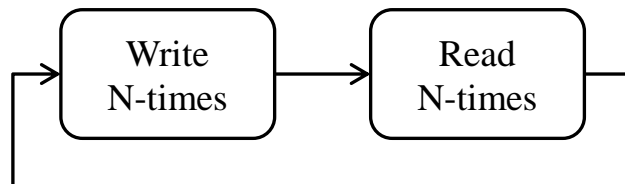
Firmware configuration



Data bus of SDRAM is bi-directional.

Memory operation is determined by command.

Tested write/read pattern.



Obtained throughput (reference value)

DDR3-800

- ~4.8 Gbps (6.4 Gbps)

DDR3-1333

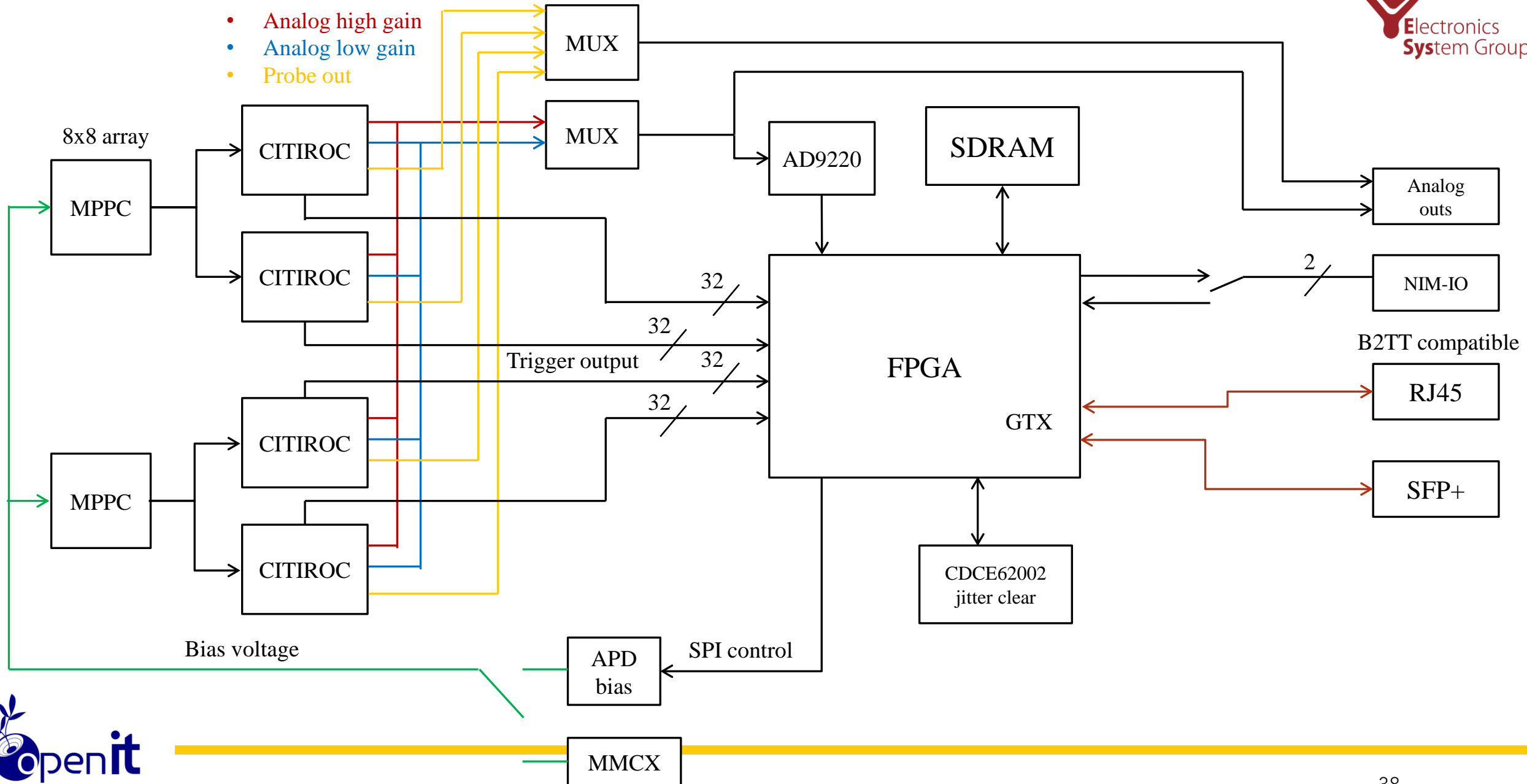
- ~7.9 Gbps (10.66 Gbps)

***Access to the same memory bank.

Larger over head when changing the bank address.

CIRASAME

- Analog high gain
- Analog low gain
- Probe out



CIRASAME arrived

装着OK

ソケットへもピッタリ

BFTの方も一番近いX面のクリアランスOK
段差のクリアランスもOK



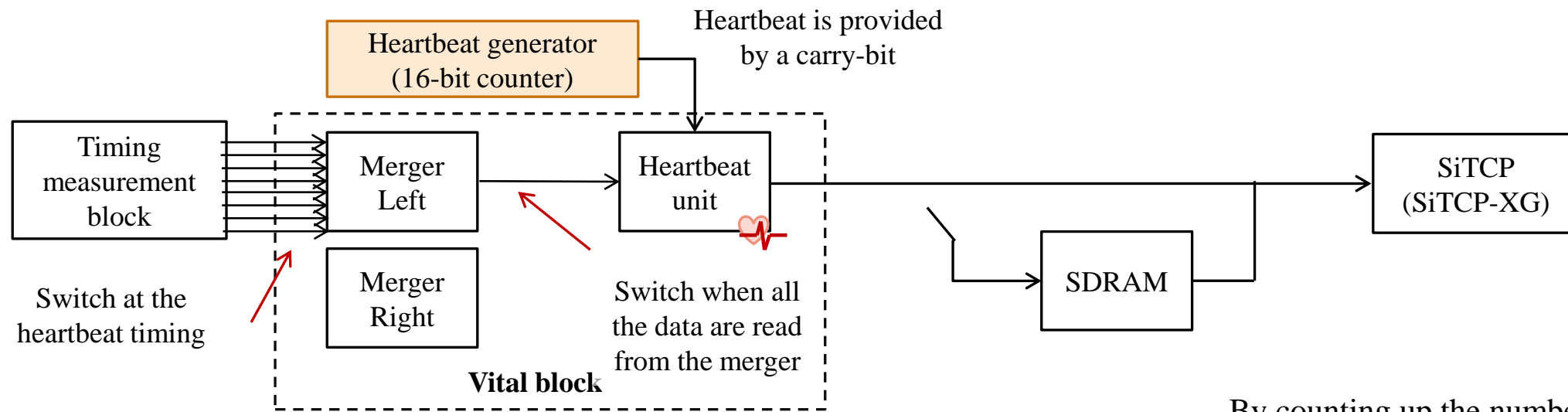
Heartbeat method

Heartbeat method for the continuous timing measurement

We need the continuous timing measurement over 2 s (spill duration of J-PARC slow extraction)

- Required dynamic range: $\sim 10^{10}$ (1 ns TDC case)

Introduce **heartbeat method**: a technique to reconstruct the time without a long-length time stamp.

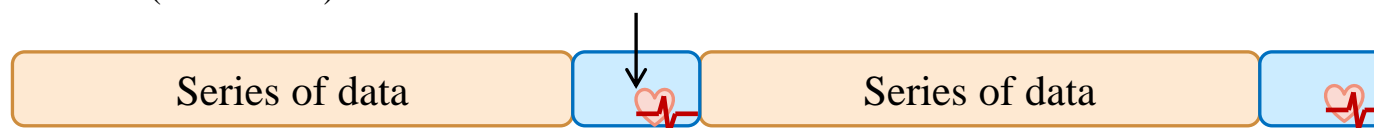


By counting up the number of heartbeat data, the time from the spill start is reconstructed.

Belong to **N-th** heartbeat frame (time frame)

Insert a delimiter data fragment called heartbeat data

Belong to **N+1-th** heartbeat frame



This techniques was tested and used in the J-PARC experiment. (E.g., beam structure measurement)