DAQ System for LEPS2 Solenoid Experiment

2021年10月29日

計測システム研究会＠九州大学
大阪大学核物理研究センター
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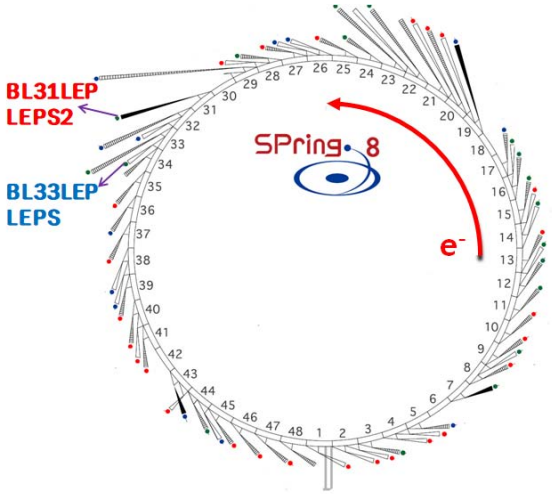
LEPS2 Beamline at SPring-8

Compton backscattered photons from head-on collisions between UV(DUV) laser light and 8 GeV electrons are produced in the energy region 1.3 – 2.4 (2.9) GeV at LEPS2/SPring-8.

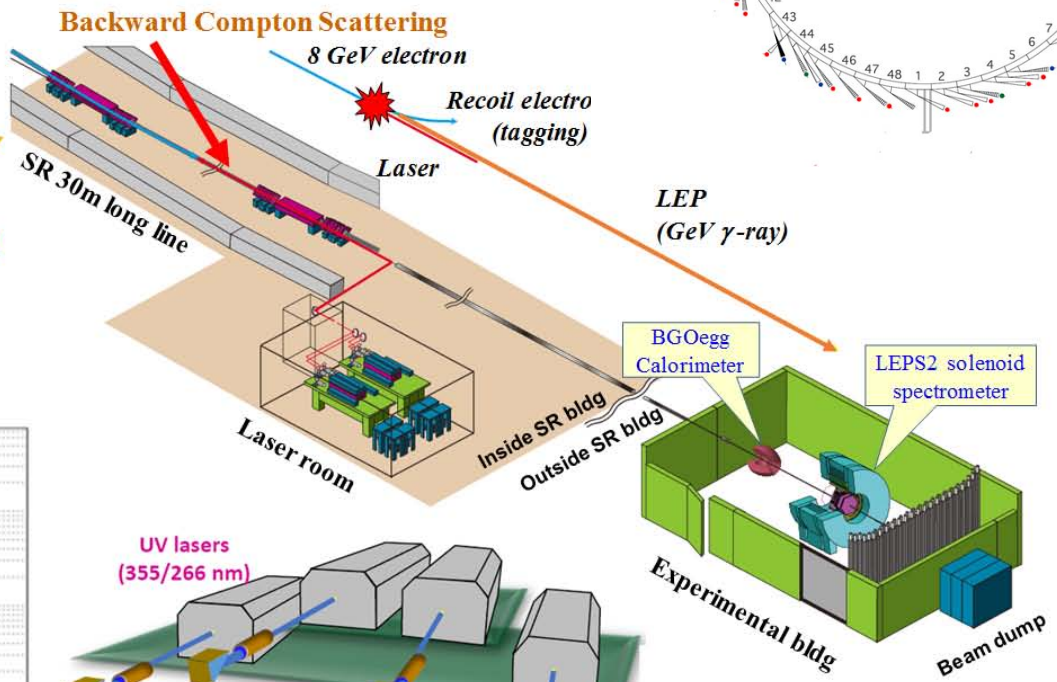


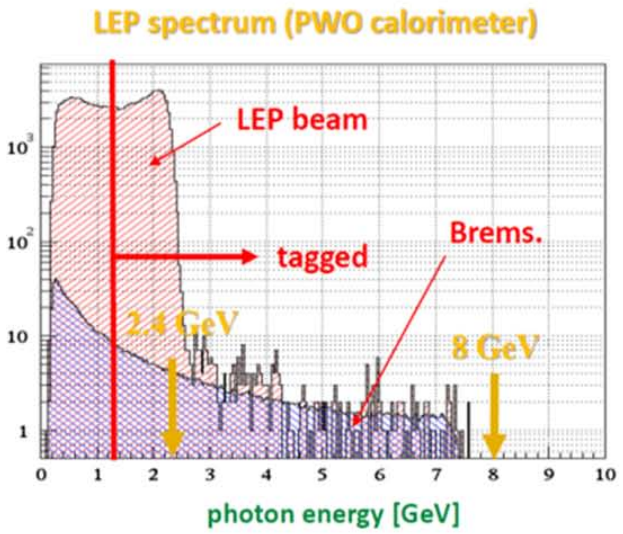
e⁻ Beam Divergence

$<\sigma_{x'}>=12\ \mu rad$

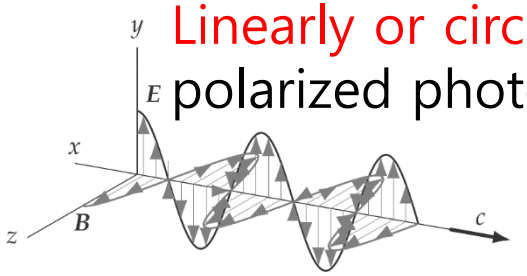
@LEPS2 30m straight section

Only 4 of 62 beamlines

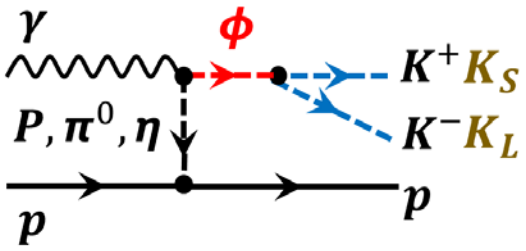


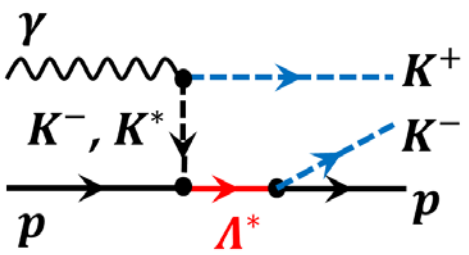


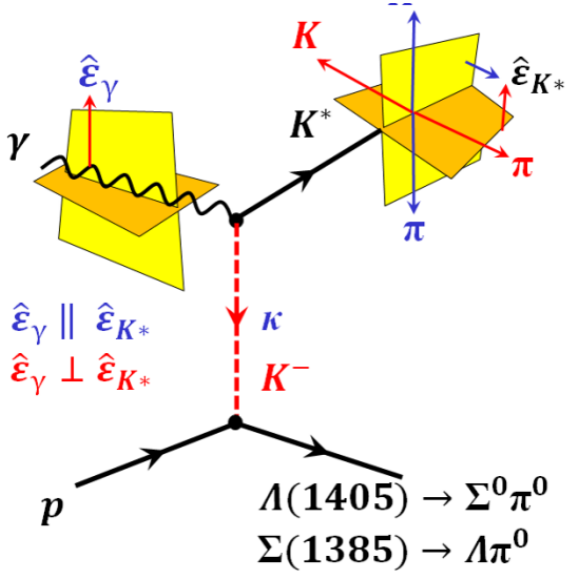
LEPS2 Physics

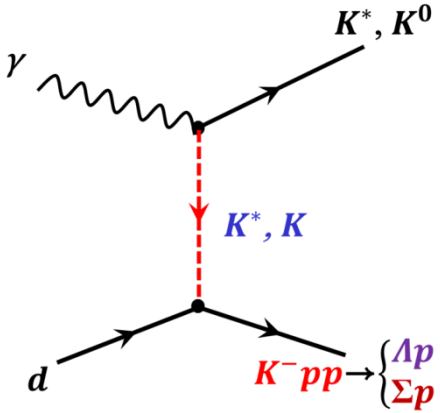


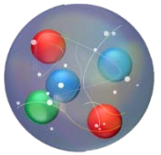
Linearly or circularly polarized photon beam

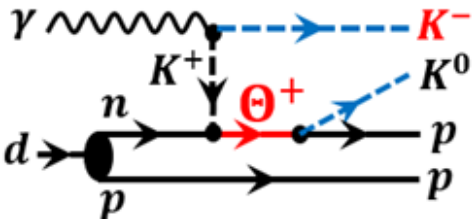






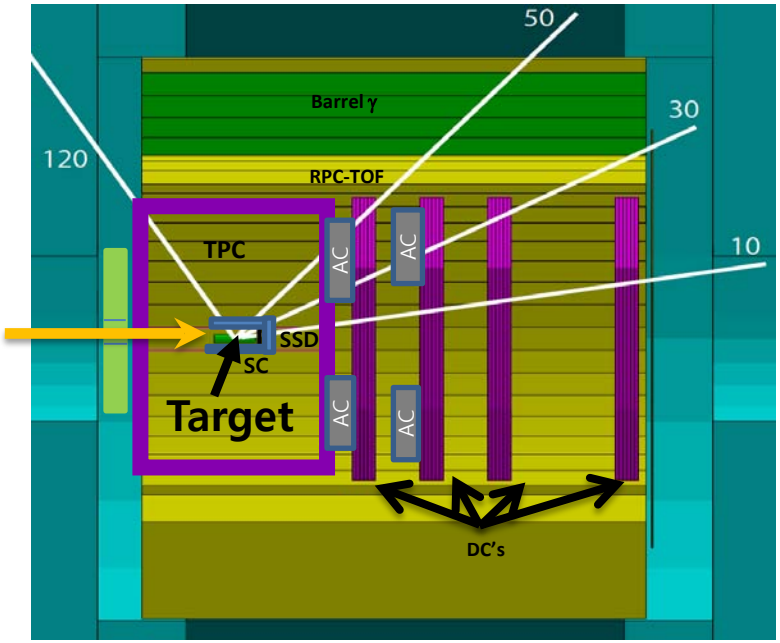




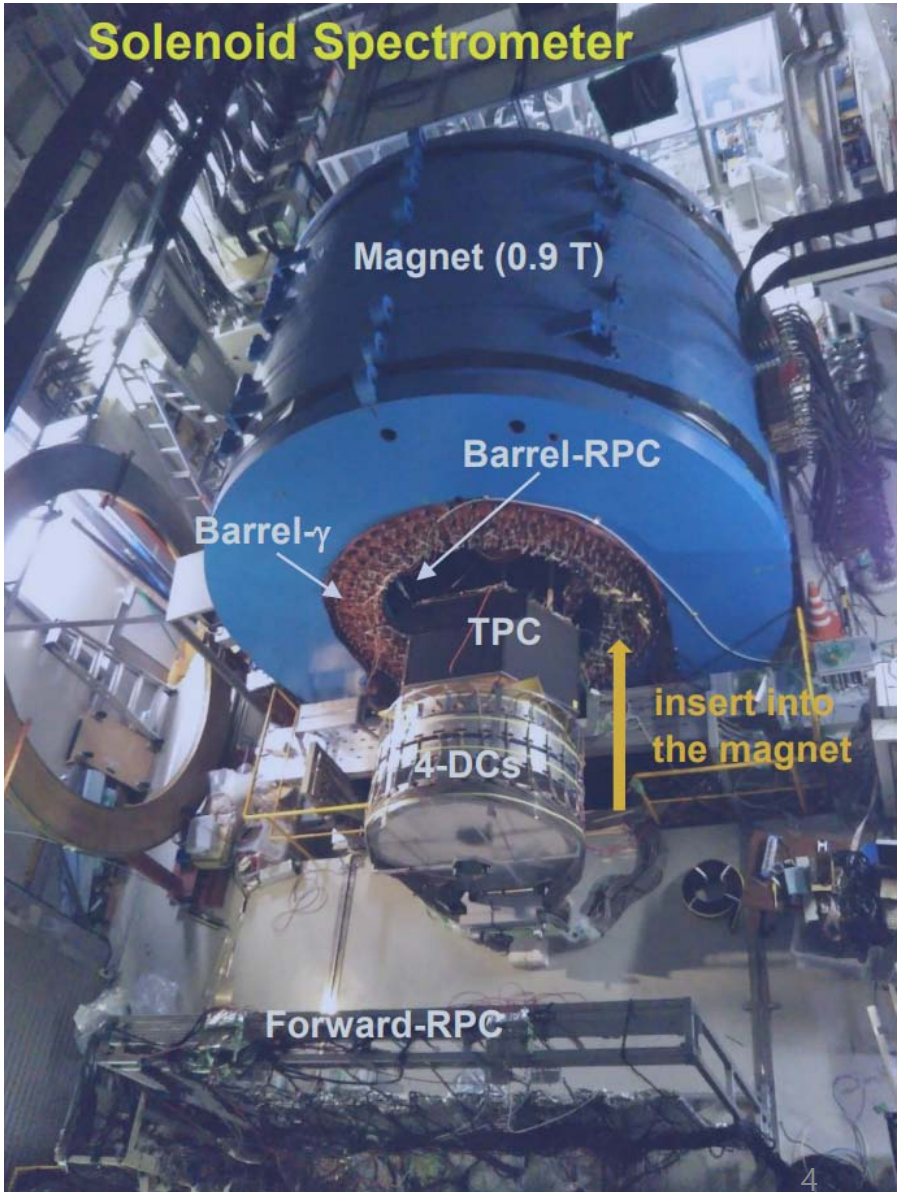


- Experimental program with the LEPS2 detector covers a wide range of hadronic physics topics. Studying the spectrum of the hyperon resonances and the hadron production mechanism are one of the main issues. A large effort is devoted to search for the exotic hadronic systems such as pentaquark states (Θ^+ and P_s) and kaonic nucleus (K^-pp).

LEPS2 Solenoid Detector

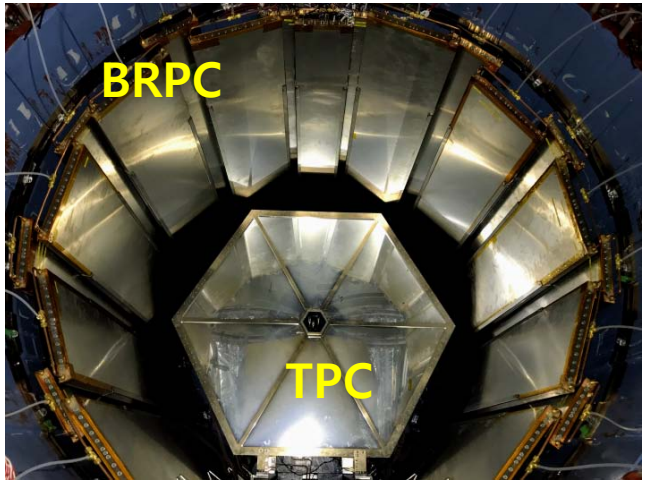


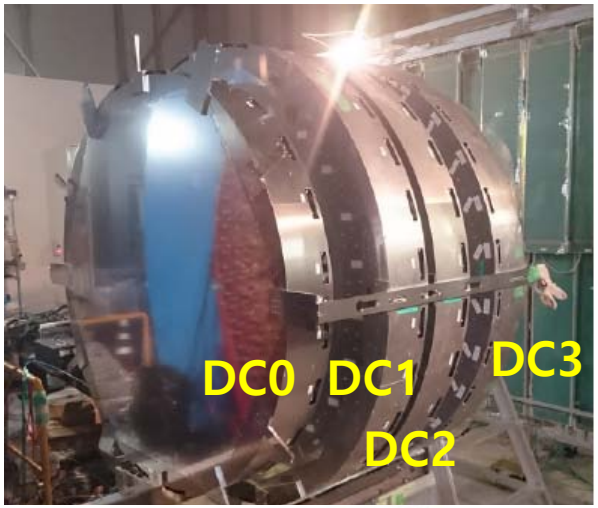
FRPC

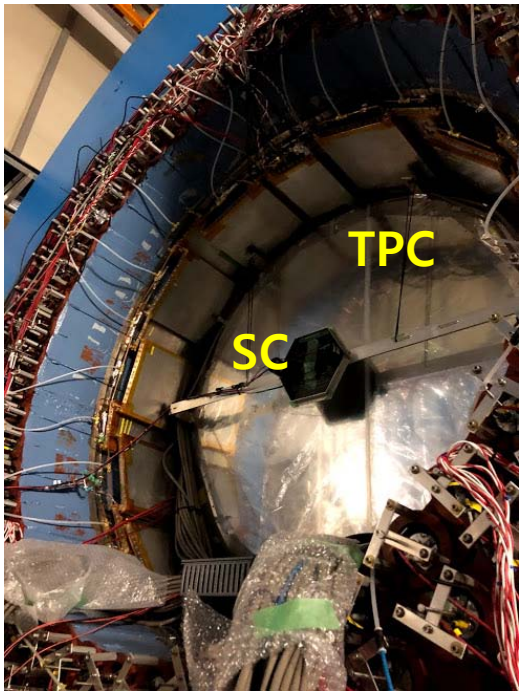


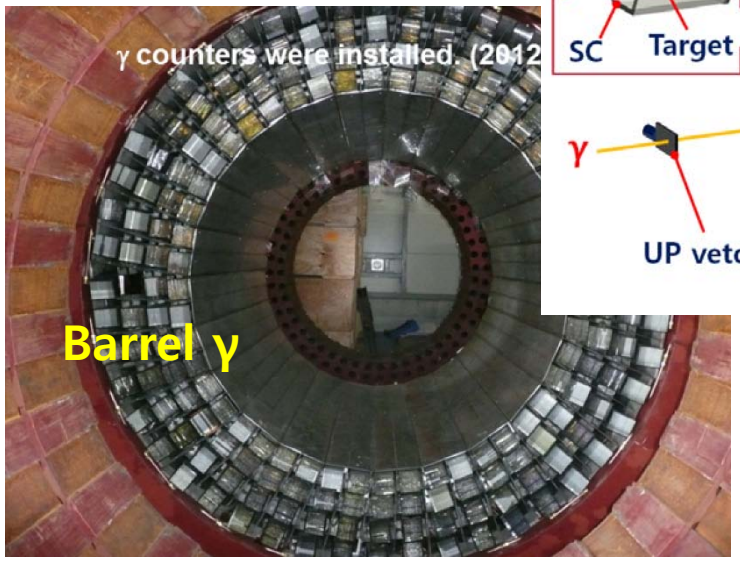
The LEPS2 solenoid detector consists of TPC, SC, DCs, ACs, forward and barrel RPCs, and barrel Pb/Scint calorimeter (14.3 X_0) as well as a photon tagger placed approximately 150 m away.

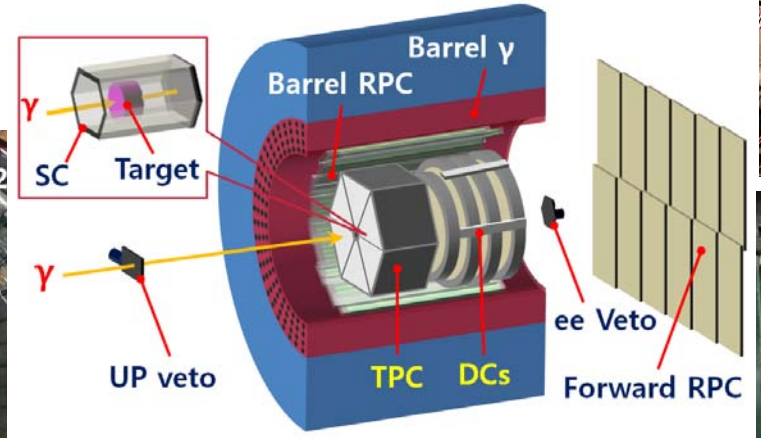
LEPS2 Detector

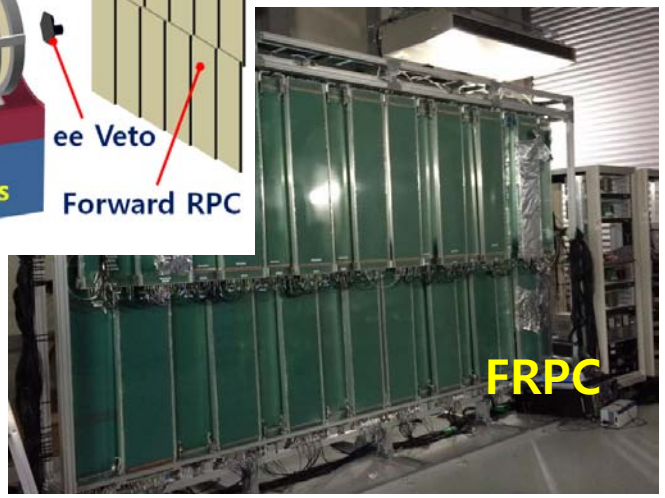




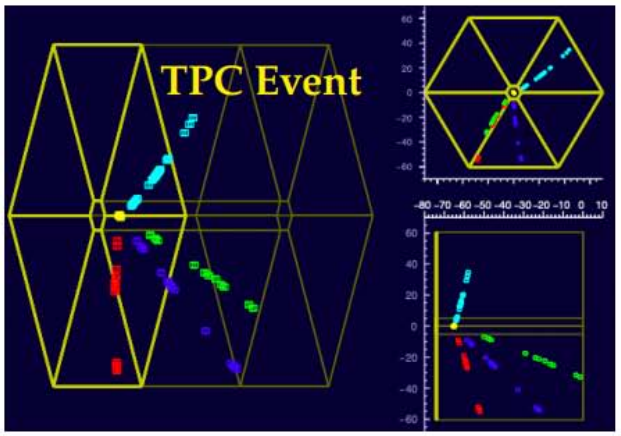


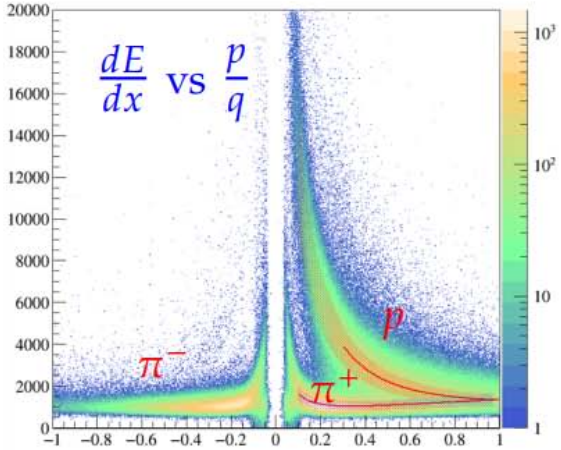


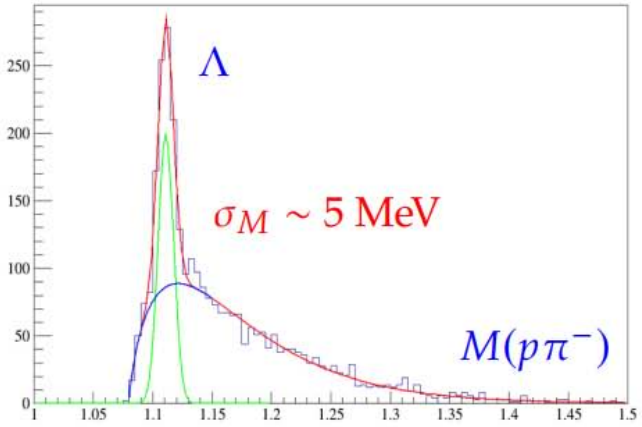


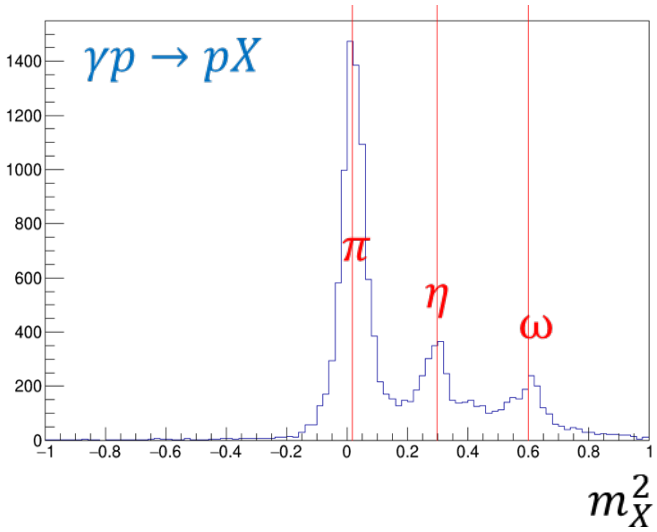


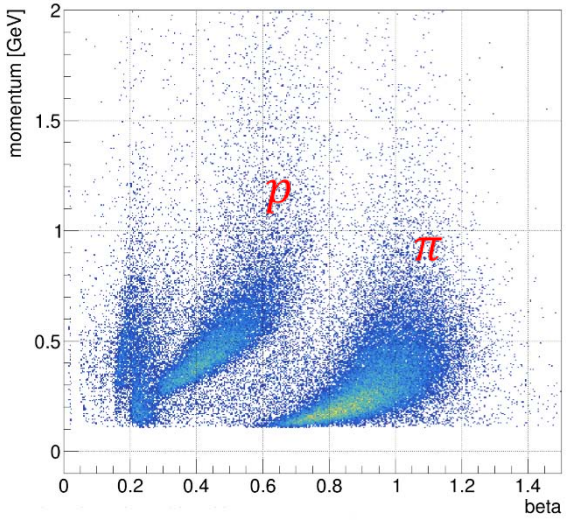
First phase of LEPS2 Physics Runs

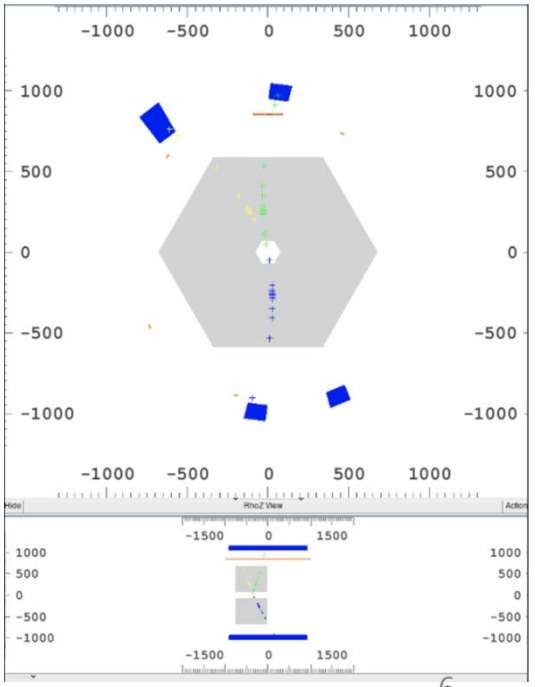








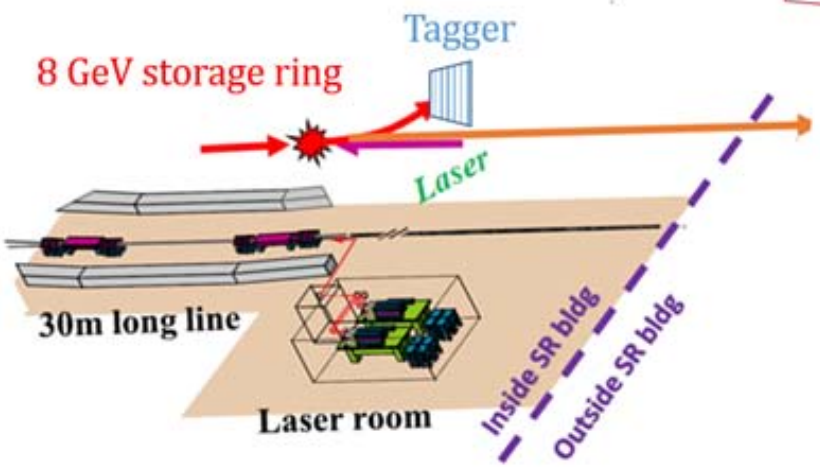


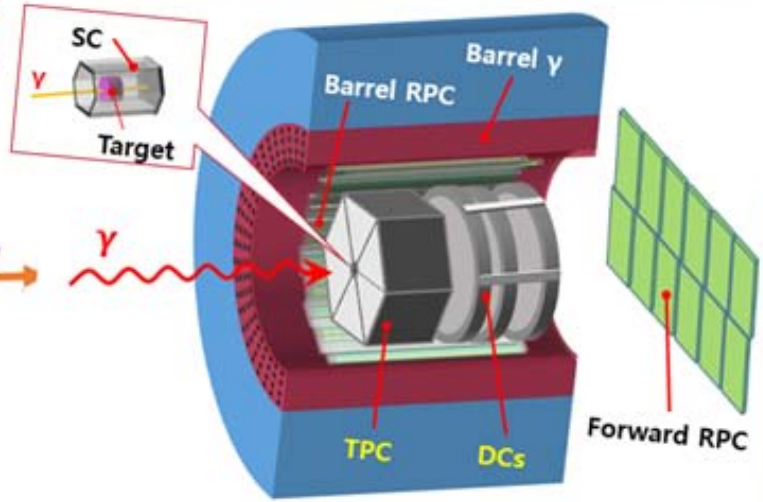


- Λ decays are successfully reconstructed with p and π^- tracks in the first beam commissioning dataset.

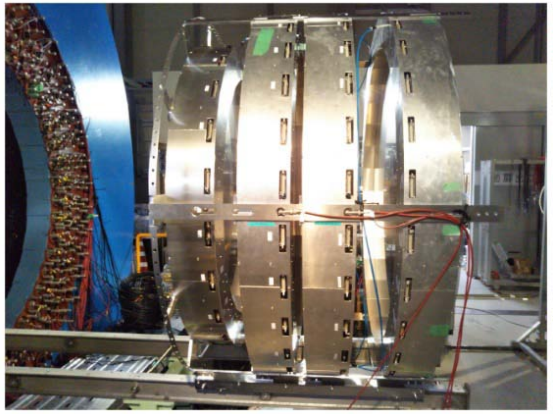
LEPS2 Front-End Electronics

Detector	Tagger, SC, DCs, FRPC, BRPC, BGamma
TDC	V1190A, V1290A, RPV-260(DC), MTDC32(BRPC)
ADC	V792, V965, FERA(FRPC), DRS4(BRPC)





VME SBC and FPGA Modules



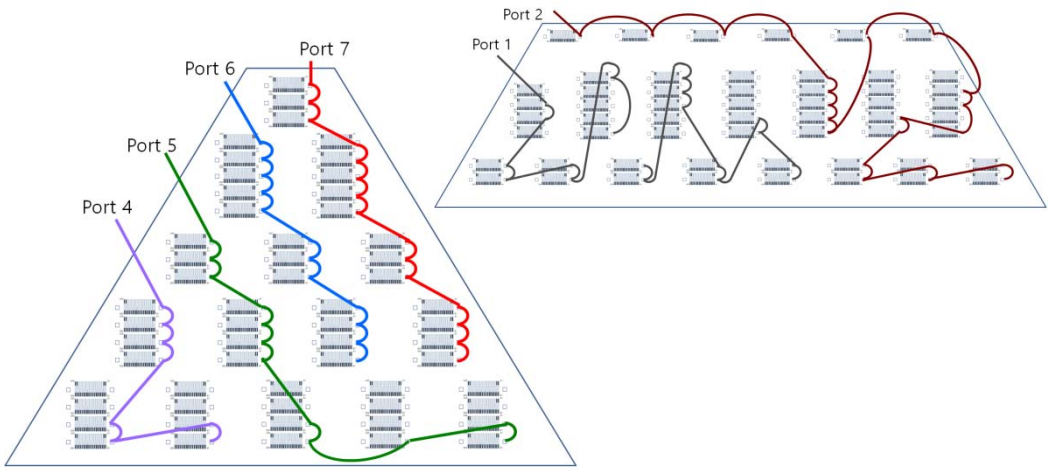
- DRS4 Digitizer FPGA board
- SiTCP protocol via Ethernet
- Direct readout with DAQ middleware
- ADC for Barrel RPC

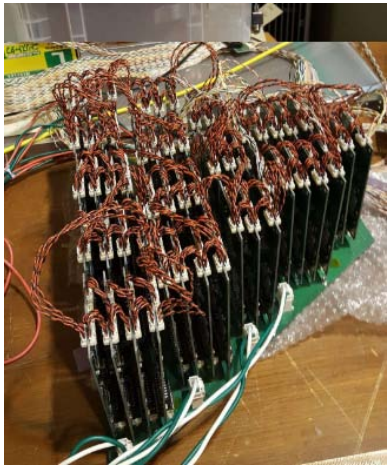
- Four DCs with 1920 channels
- 64ch RPV-260 FPGA board
- SiTCP protocol via Ethernet
- Direct readout with DAQ middleware
- 64ch 1-ns TDC firmware

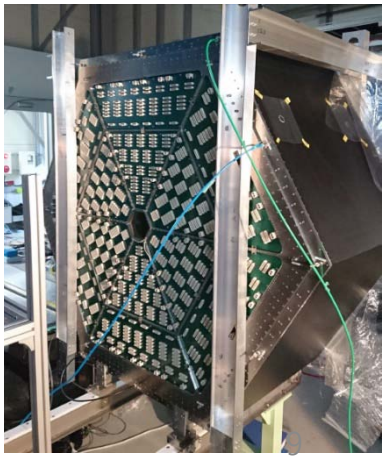
VME SBC	SVA041	SVA051	SVA061
CPU	Pentium M/ 1.1GHz	Core i7 / 1.06GHz	Atom x7-E3050 / 1.6GHz
RAM	512M	8G	8G
Network	1000Base-T	1000Base-T	1000Base-T
Storage	CFast Type-II	CFast Type-II Flash	On Board CFast

TPC Readout

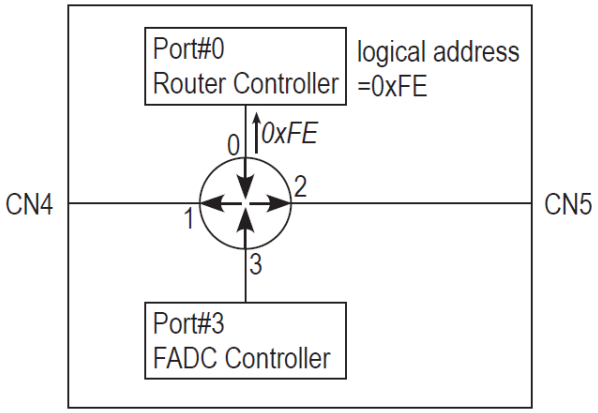
- ASIC: shaping amplifier(8 ch/chip), Gain: 1 V/pC , signal width: 200~400 ns
- FADC: AD9257(8 ch/chip), Accuracy: 14 bit, Input voltage range: 2 V
  sampling frequency: 40 MSPS
- Power consumption: ~230 mW/ch
- Developed by S. Ajimura,





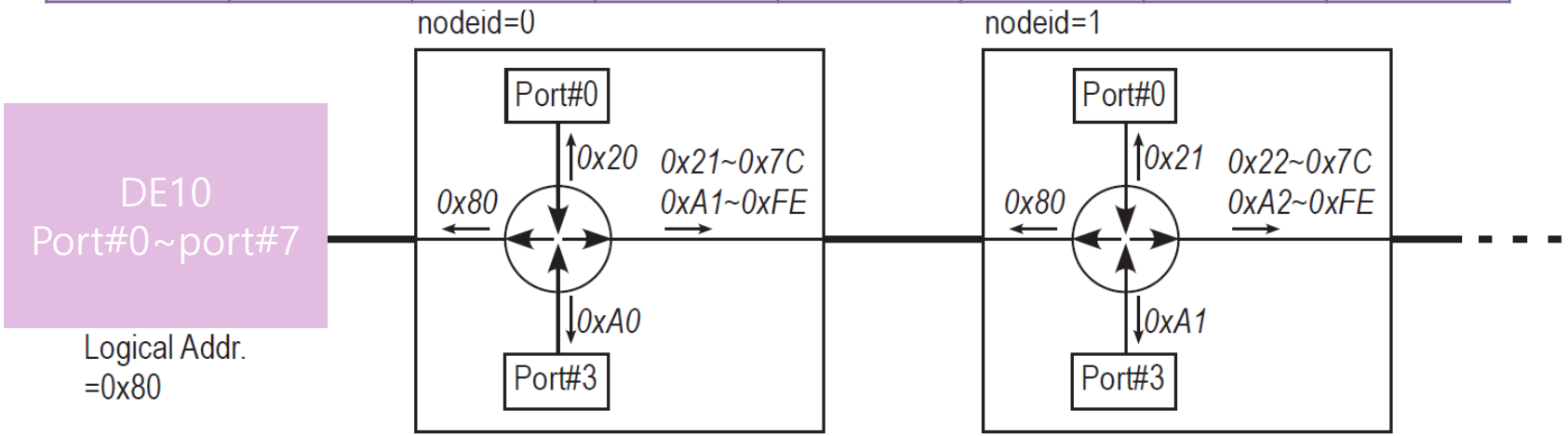


TPC Readout

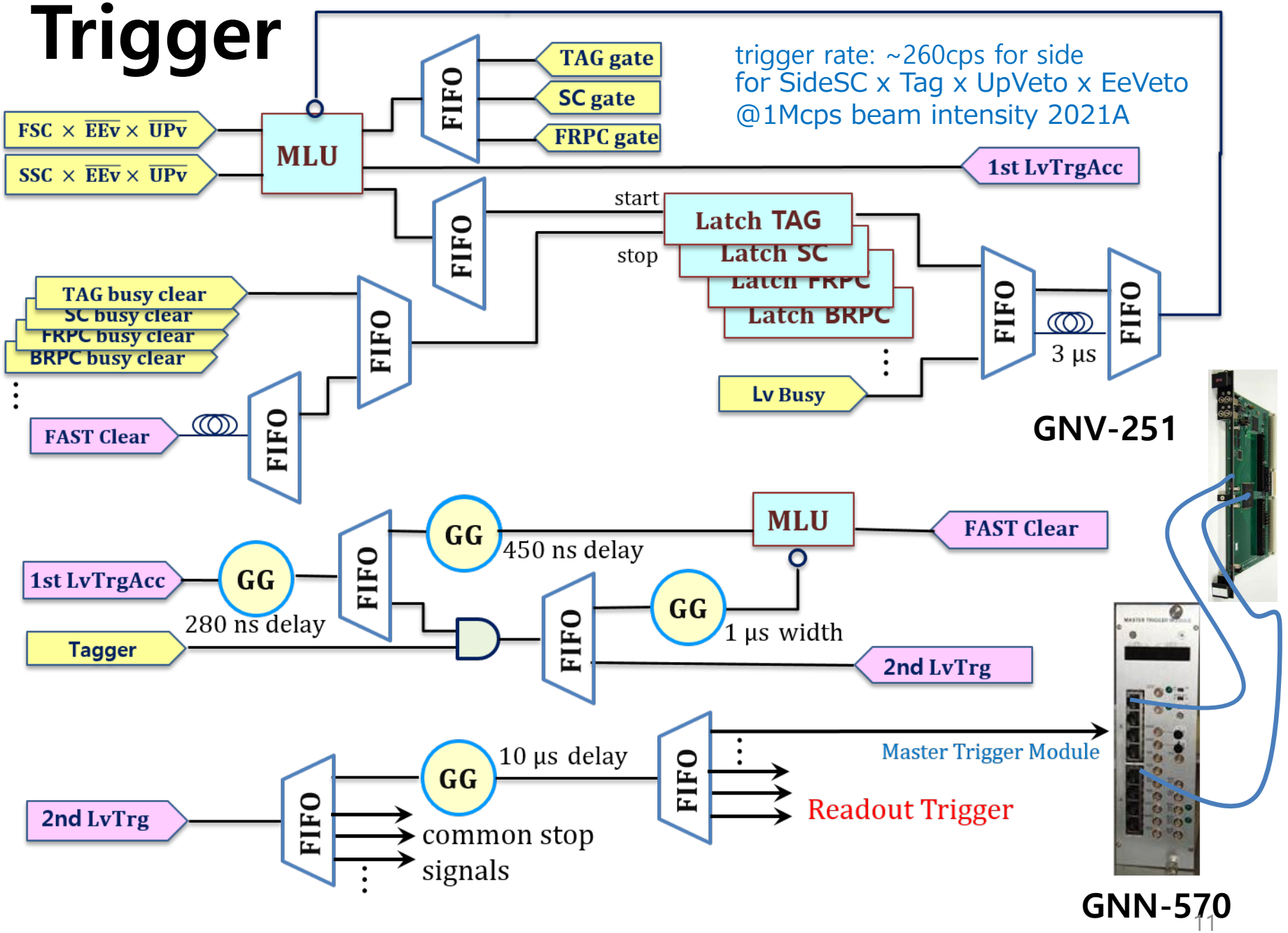


- DE10 board port# and cascade connection node# identify individual FADC boards connected in series.
- RMAP access is available via DE10 board port# and logical address. The maximum number for cascade connection is 93.
- We readout the 88 FADC boards per DE10.

port#0	port#1	port#2	port#3	port#4	port#5	port#6	port#7
0	19	22	0	8	12	12	15



Trigger


trigger rate: ~260cps for side
for SideSC x Tag x UpVeto x EeVeto
@1Mcps beam intensity 2021A
FSC × EEv × UPv
SSC × EEv × UPv
MLU
FIFO
TAG gate
SC gate
FRPC gate
1st LvTrgAcc
start
stop
Latch TAG
Latch SC
Latch FRPC
Latch BRPC
TAG busy clear
SC busy clear
FRPC busy clear
BRPC busy clear
FAST Clear
Lv Busy
3 μs
GNV-251
GG
450 ns delay
280 ns delay
1 μs width
1st LvTrgAcc
Tagger
2nd LvTrg
10 μs delay
common stop
signals
Readout Trigger
Master Trigger Module
GNN-570

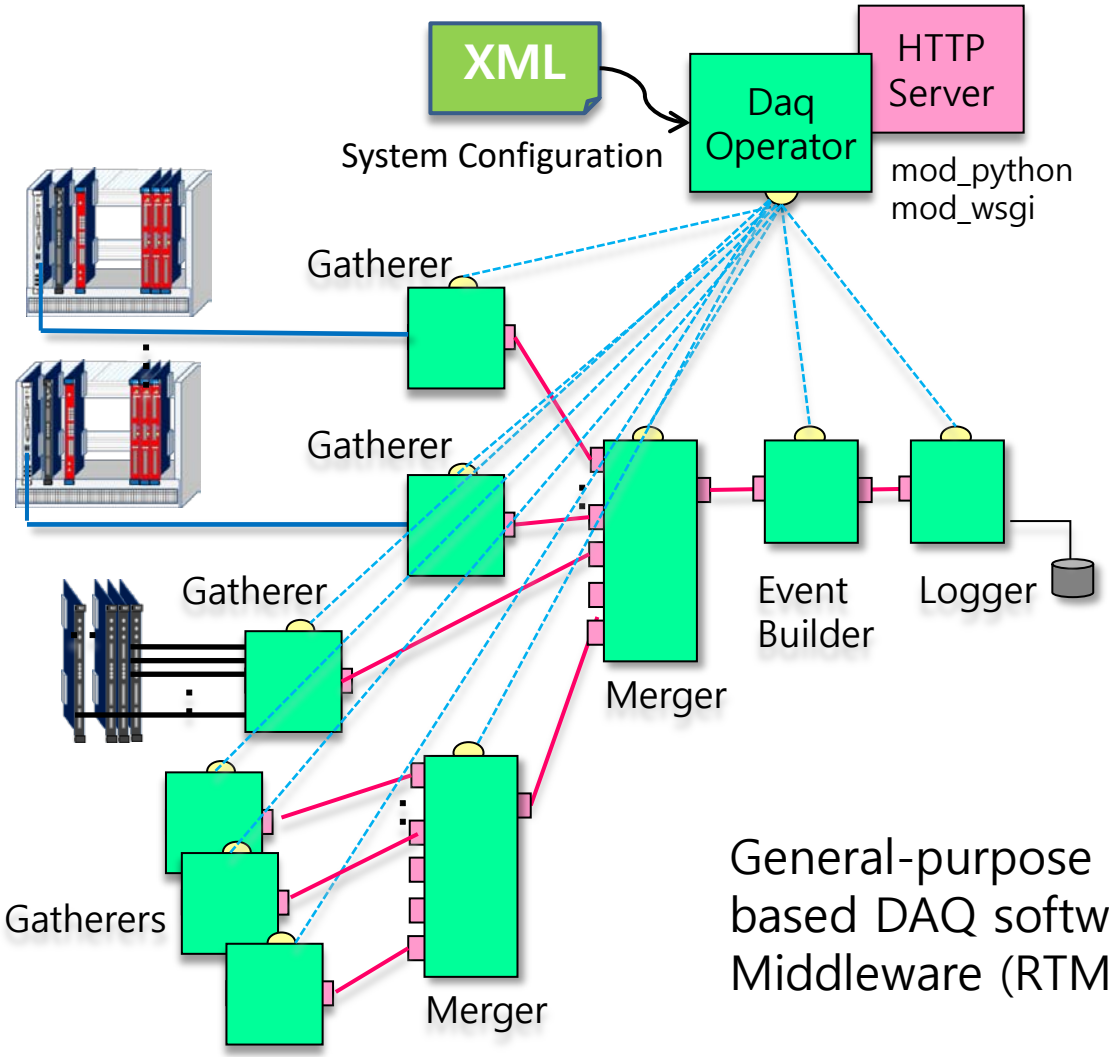
Current Status of LEPS2 DAQ

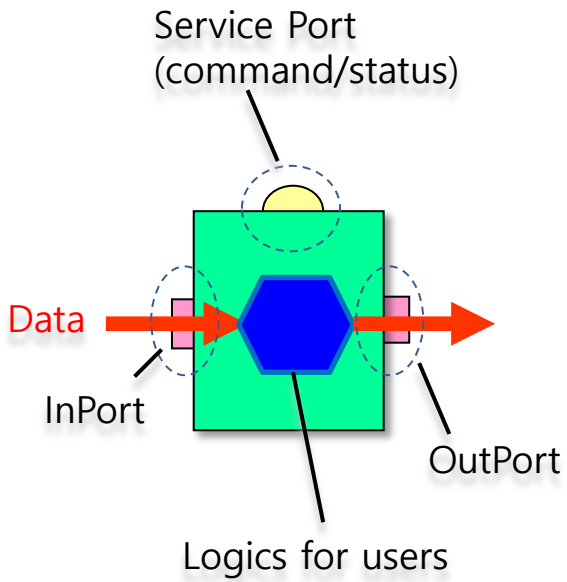
Detector	# of channels* (secured/required)	TDC module	ADC module	VME Controller
Tagger	184 / 184	V1190A x 2	V792 x 2	SVA041 x 2
Start Counter	25 / 25	V1290A x 1	V965 x 2	SVA041 x 1
DC	1824 / 1824	RPV260 x 29		
Forward RPC	288 / 288	V1290A x 9	FERA System	SVA051 x 2
Barrel Gamma	192 / 288	V1190A x 2	V792 x 6	SVA051 x 2
Barrel RPC	480 / 480(TDC) 240 / 240(ADC)	MTDC32 x 15	DRS4 QDC x 16	SVA051 x 2
TPC	8352 / 8352	16ch-FADC x 522		
AC1 and AC2	0+36 / 30+36	V1190A for BG	V792 x 2	
Neutron Counter	0 / 96+2			

*) # of channels for each of ADC and TDC.

- We will prepare the DAQ system for 3rd layer of Barrel Gamma and Neutron Counter this winter.

DAQ middleware

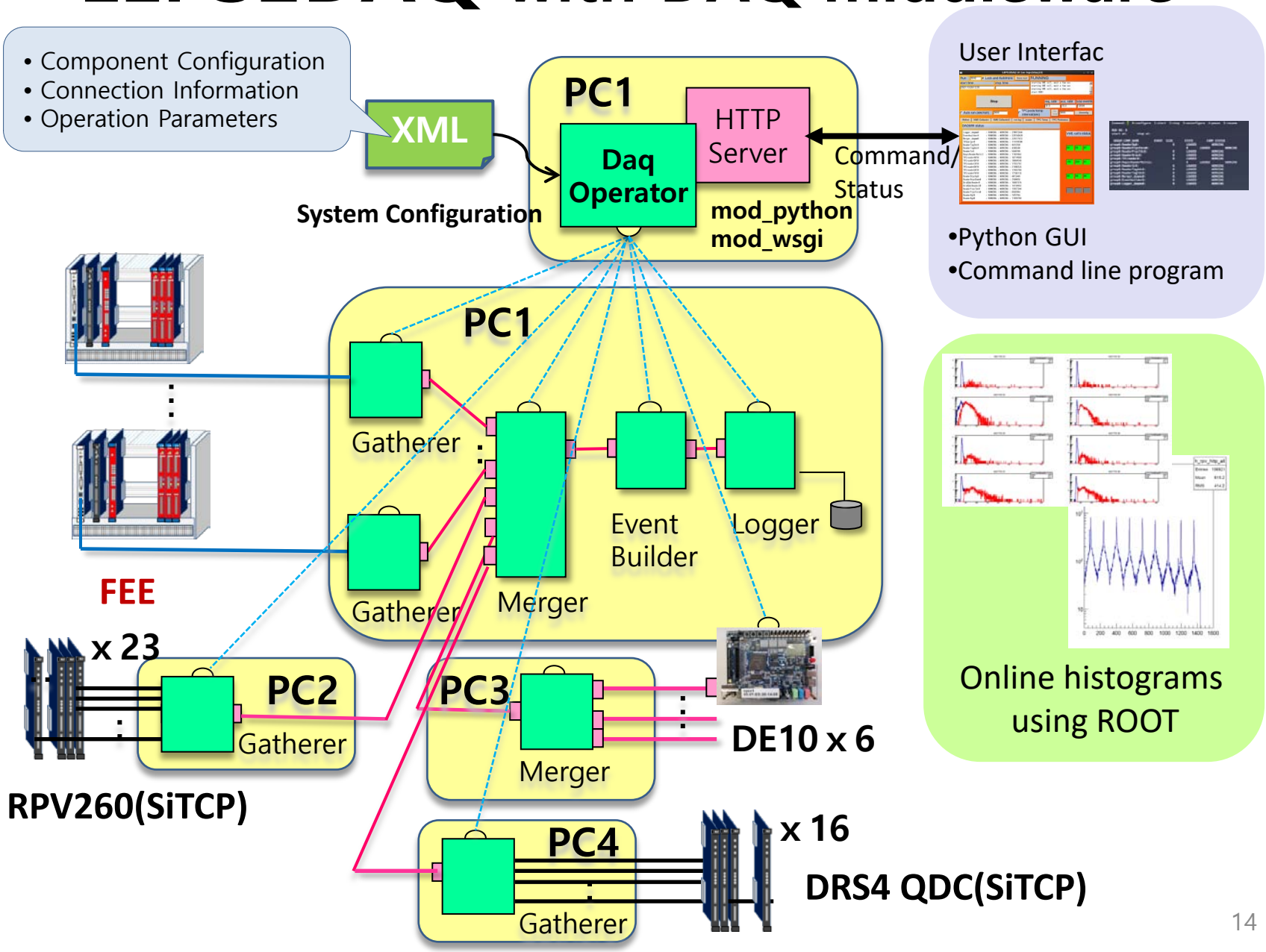




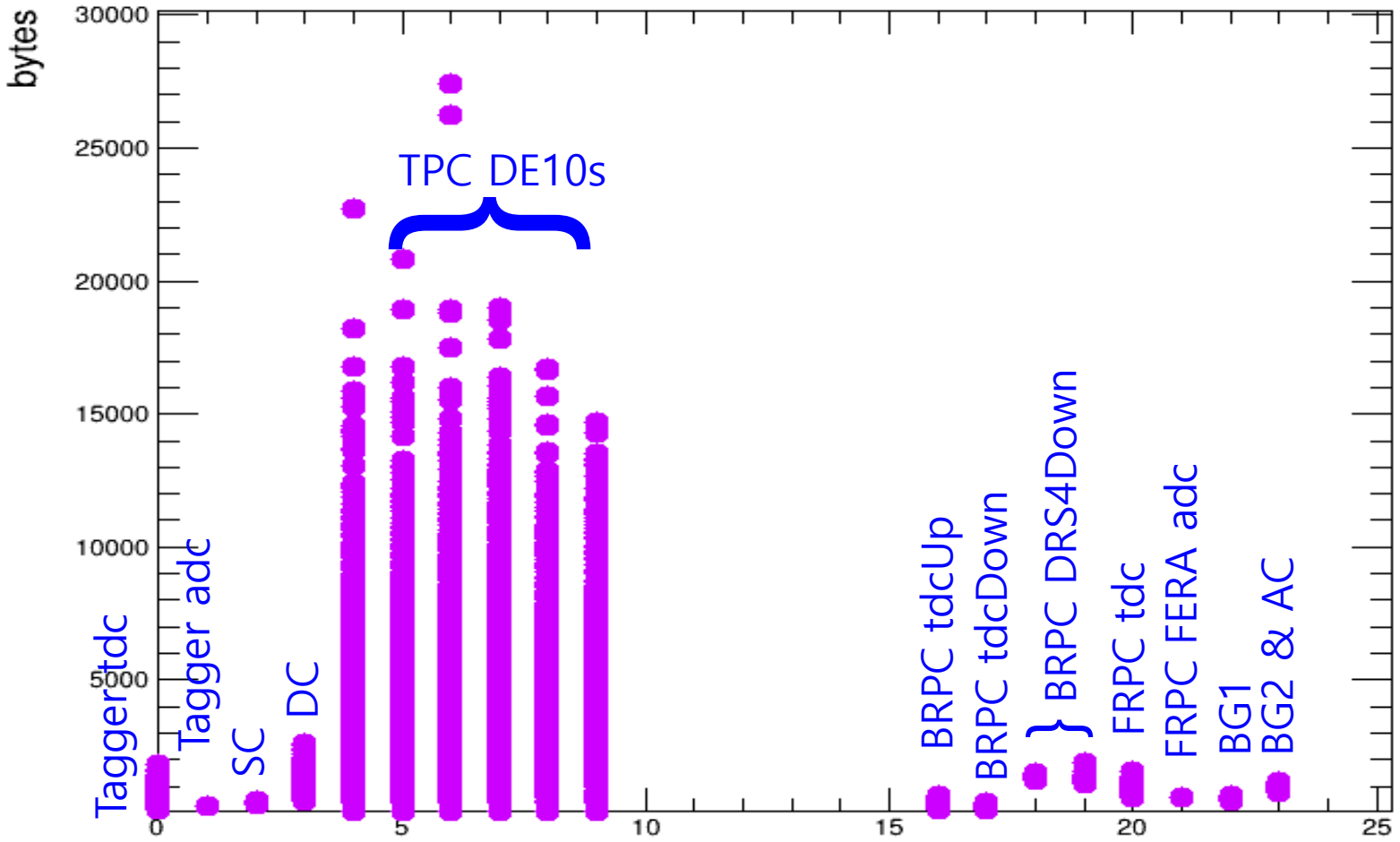
General-purpose framework for network-based DAQ software based on RT-Middleware (RTM)

Developed by KEK and 産業技術総合研究所

LEPS2DAQ with DAQ middleware

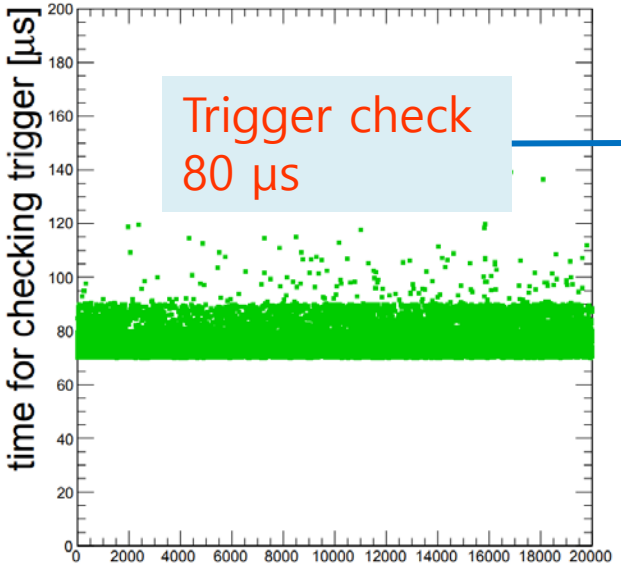


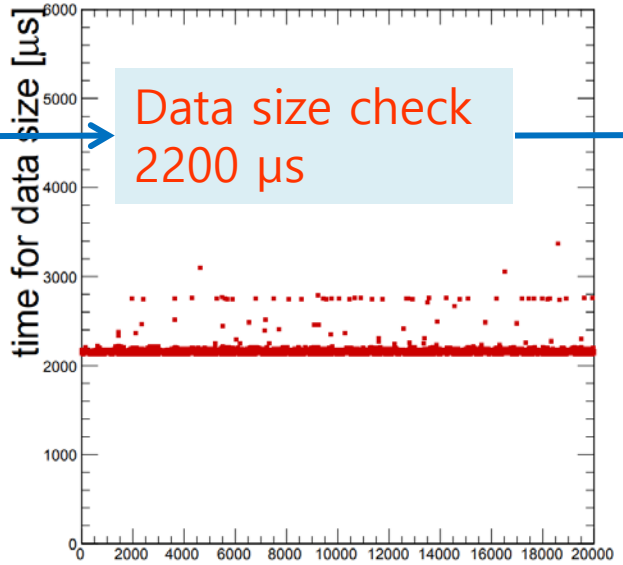
LEPS2 Data Size

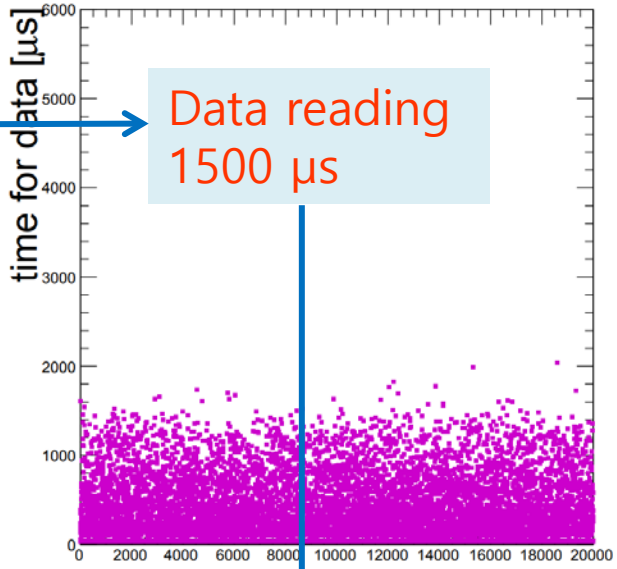


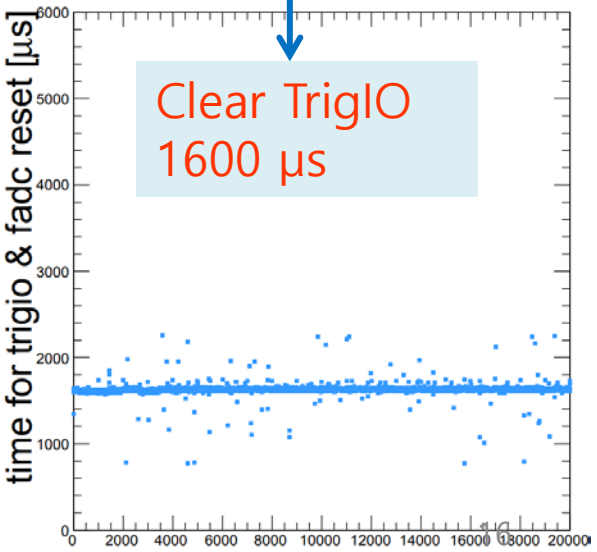
- Data size is dominated by TPC data transferred through GbE from DE10 boards: 90-120kB/event from TPC and 10kB/event from others.
- A few tens MB/s at 100-200 Hz data acquisition rates.

DAQ performance



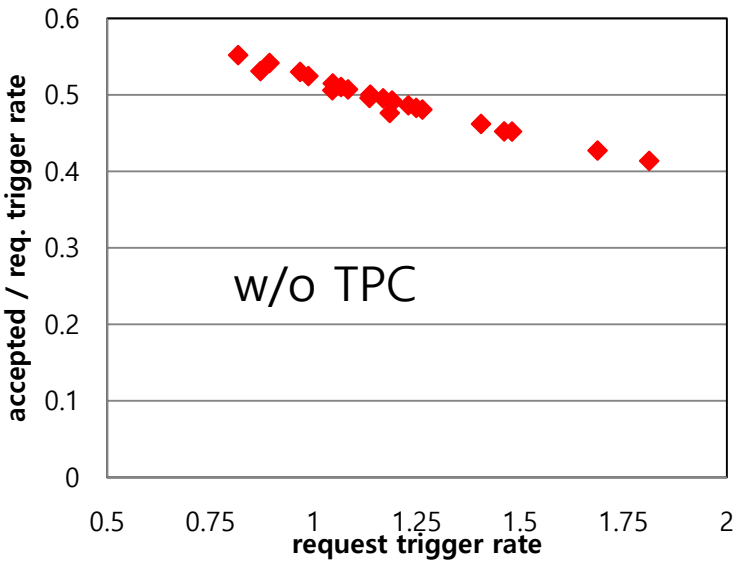


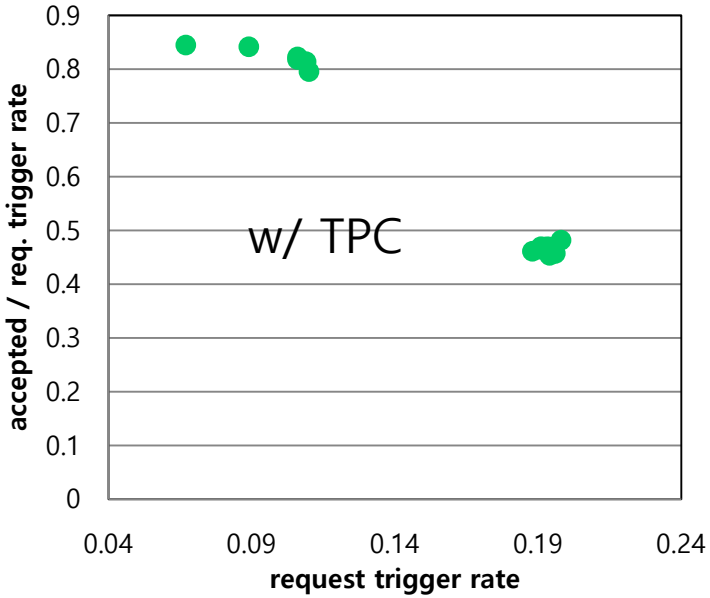




- DAQ quickly checks if FADC begins reading TPC signals from 6 boards (80 μs).
- DAQ reads the data size for each FADC board (2200 μs).
- DAQ starts reading pedestal-suppressed TPC data (1500 μs).
- DAQ clear buffers in TrigIO (RPV260 with TPC firmware) and reset FADC boards (1600 μs).
- A single sequence takes approximately 5.4 ms

DAQ performance





$$\varepsilon = \frac{1}{1 + f\tau}$$

- DAQ efficiency ε (=trigger accept/request) is compared with the curve for τ = 5.4 ms; 65% at 100 Hz, 48% at 200 Hz.
- Without TPC the efficiency ε=0.5 at 1 kHz, which gives τ = 1.0 ms.

まとめ

- レーザコンプトン偏光ビームとLEPS2ソレノイド検出器を用いたハドロン共鳴状態の構造やエキゾチックハドロンの探索実験でクォークからハドロンになるクォーク閉じ込めの謎に迫る。
- DAQ middlewareを用いたDAQを開発し、始めて本実験を走らせている。
- DAQ性能効率はTPCなしの時、1kHzトリガーレートで50%なので改善策として　一つのコレクターに一つのgathererを使うのを代りに一つのgathererに複数のコレクターからデータを取集することでDAQMWのoperatorにかかる負担を軽くする方法を試す。Mergerの分散
- TPCDAQシステムは主にFADCボードのデータサイズの確認、FADCボードリセットとTrigIOのバッファークリアーで時間がかかり、イベント当り約5．4msかかる。この問題を開発者に相談しながらの改善策を探る。
- LEPS2のソレノイド中のFADCボードの温度が夏に78℃以上上がり、DAQエラーの原因になっている。安定的なデータ収集のための温度管理環境を整う。