J-PARCにおけるチャームバリオン分光実験に用いるドリフトチェンバー読み出し回路の性能評価: ASAGI ASDカード

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他 J-PARC E50 コラボレーション

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- Introduction
- Test experiment & analyses
- ASAGI card update
- Summary

Introduction

J-PARC E50 experiment

ASAGI-card

J-PARC E50 experiment

- Charmed baryon spectroscopy experiment（J-PARC E50）

⇒ Investigation of diquark correlation by measuring

charmed baryon (Y_C^{*+}) production and decay

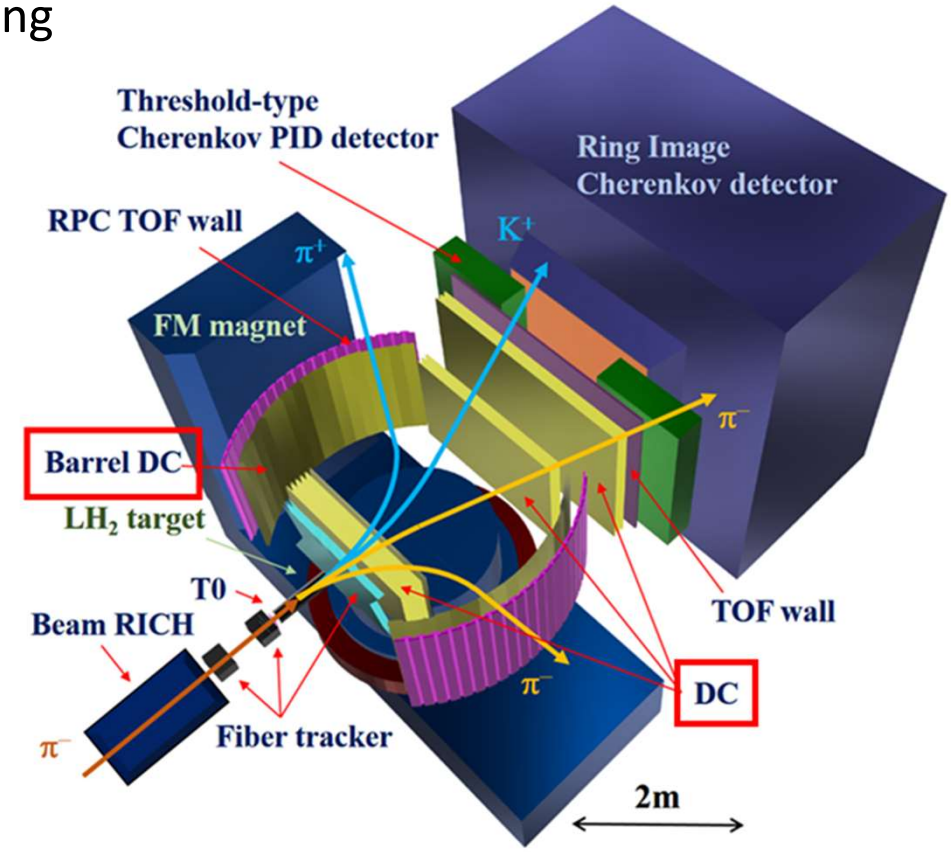
$\pi^- + p \rightarrow Y_C^{*+} + D^{*-}$

$D^{*-} \rightarrow \bar{D}^0\ \pi^- \rightarrow K^+\ \pi^-\ \pi^-$

- **Drift chambers:**

Tracking and analyzing K^+ and π^- momenta

⇒ **New signal readout ASD card**



ASAGI card development

- Development of **an ASD card with a new ASIC chip** for the E50 experiment **: ASAGI card**

⇒ **AGASA ASIC** is a candidate (**AGASA**: **A**sic for **G**as detector **A**mp **Sha**per discriminator)

  - Originally developed for Belle II CDC
  - **Charge amplification factor, pole-zero cancellation effect, shaping time** and **the threshold of the discriminator can be adjusted.**

- **ASAGI cards** can be used for **common readout ADC card** for various gas detectors
  - **SPADI Alliance Task force for developing commonly-used ASD card**
  - **Task force group: RCNP*, KEK E-sys, CNS, RIKEN**

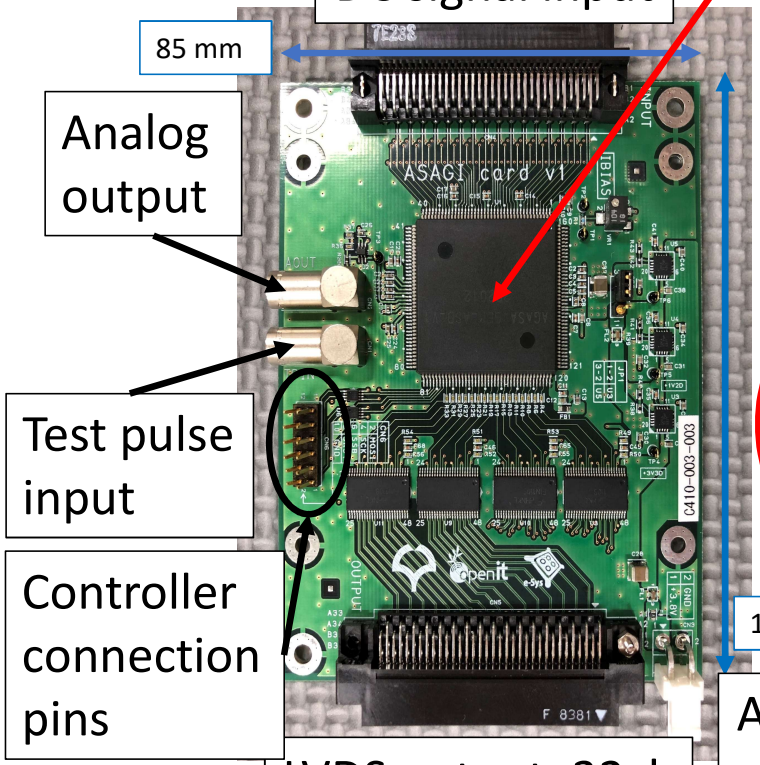
SPADI Alliance

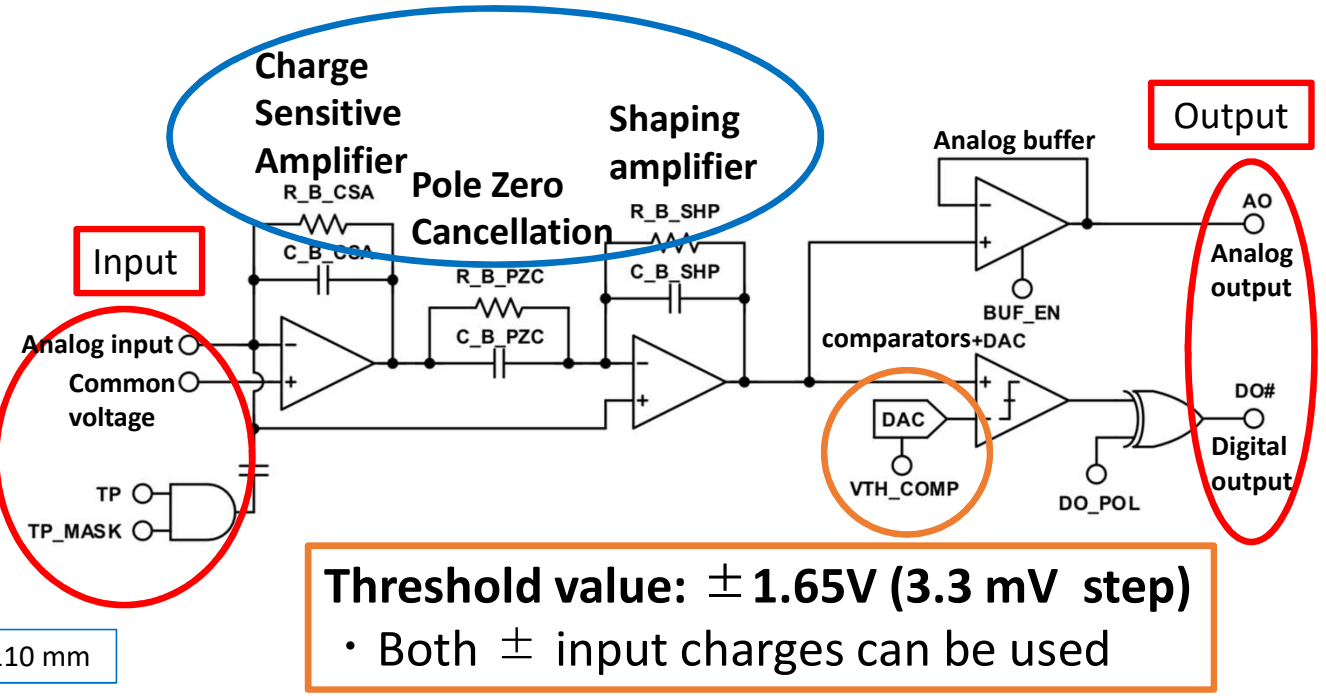
ASAGI card: AGASA based General Interface for write chambers

Prototype card (Version 1.0)

AGASA ASIC

Change number of resistor(1-4) and **capacitance**(1-8)
For adjusting gain and signal width





Threshold value: ±1.65V (3.3 mV step)
・Both ± input charges can be used

ASAGI card param sets

- Param change rules

⇒ PZC: R × C = CSA: R × C

e.g.） PZC: **R=4,C=2 → 4*2 = 8**

CSA: **R=1,C=8 → 1*8 = 8**

↑

Gain: 0.24 times of PZC: **R,C=1**,CSA:**R,C=1**

Total of param sets is **320 ways**!

時定数の積	PZC（R*C）	CSA（R*C）	
2	1*2	2*1	
	2*1	1*2	
3	1*3	3*1	
	3*1	1*3	
4	1*4	4*1	2*2
	2*2	1*4	4*1
	4*1	1*4	2*2
6	1*6	2*3	3*2
	2*3	3*2	1*6
	3*2	2*3	1*6
8	1*8	2*4	4*2
	2*4	4*2	1*8
	4*2	2*4	1*8
12	2*6	3*4	4*3
	3*4	4*3	2*6
	4*3	3*4	2*6
16	2*8	4*4	
	4*4	2*8	
24	3*8	4*6	
	4*6	3*8	

Purpose of test experiment

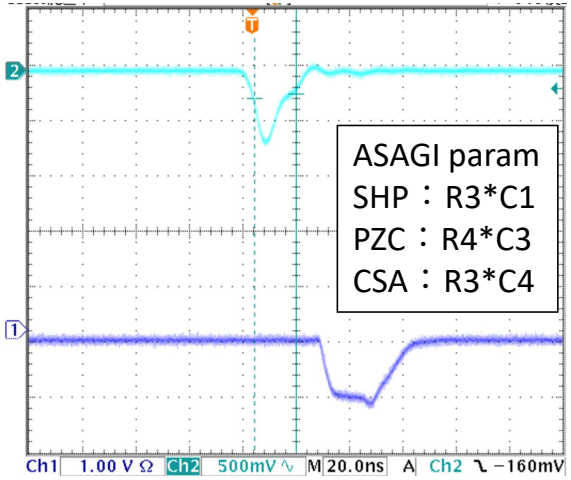
E50: High-counting rate environment to operate drift chambers

a narrow width signal and appropriate gain

Adjust!

CSA (Charge amplification)	PZC (Pole-zero cancellation)	SHP (Shaping time)

ASAGI response to test pulses



- **Search for candidate parameters by test pulse**
  - Conversion gain: 5.8 V/pC (oscilloscope image in right figure)

- **Performance evaluation of ASAGI with a drift chamber at SPring-8 LEPS2**

⇒ Waveform, Signal gain, Noise level, Efficiency (HV dependence), Signal width

Test experiment & analyses

Setup

DRS4 Baseline, Pulse height & Charge

Efficiency, TDC width

Setup

@SPring-8 LEPS2

ASAGI card (attached at bottom side)

Beam direction

Horizontal position can be measured.

900 mm

140 mm

Wire direction

300 mm

cross-section view

Anode wires : 3 layers

Beam direction

Potential wires
Honeycomb cells
Approx. 9 mm per side

Shield wires

Lead plate
Thickness 1 mm

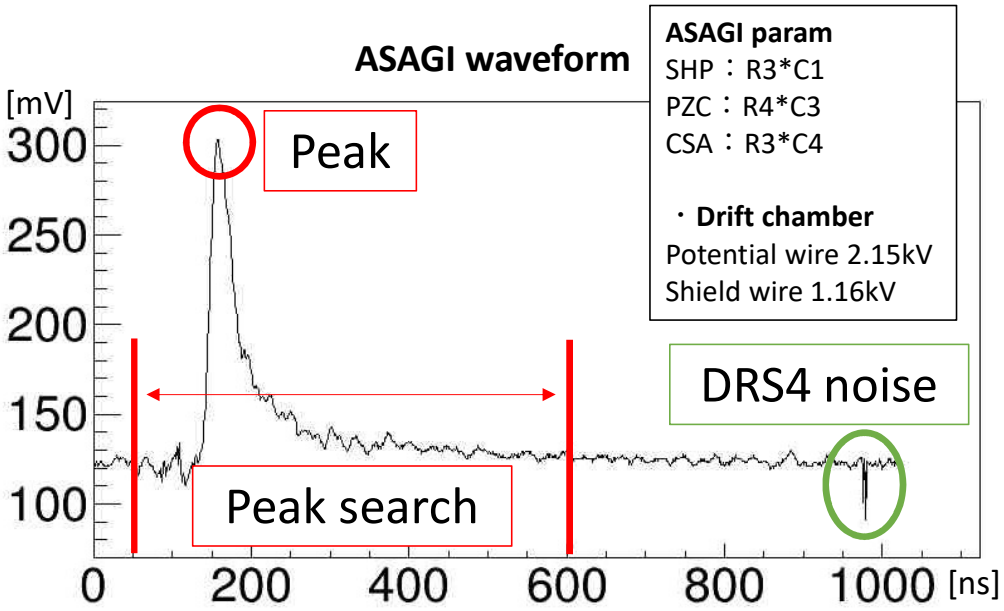
e- beam

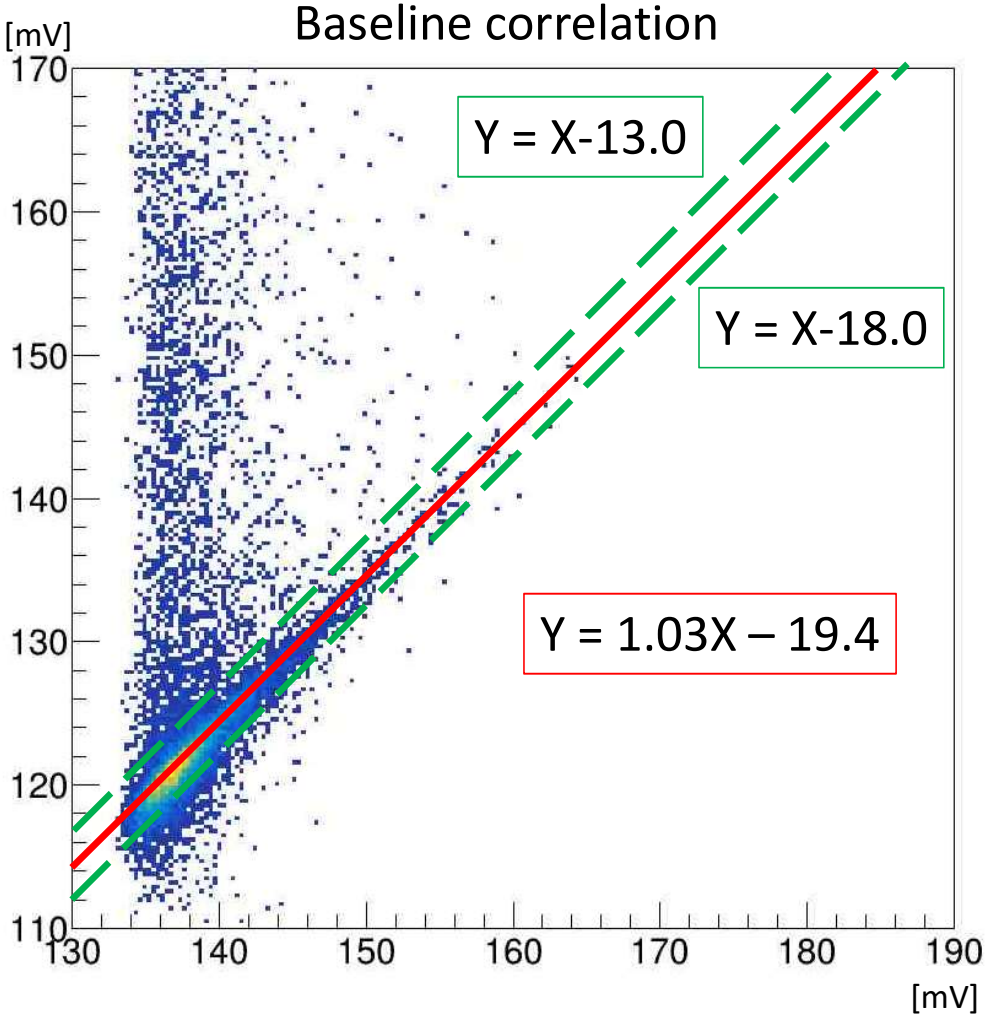
γ beam

Permanent magnet

Digital output : MH-TDC (HUL module)
Analog output : Measure Waveforms(DRS4 module)

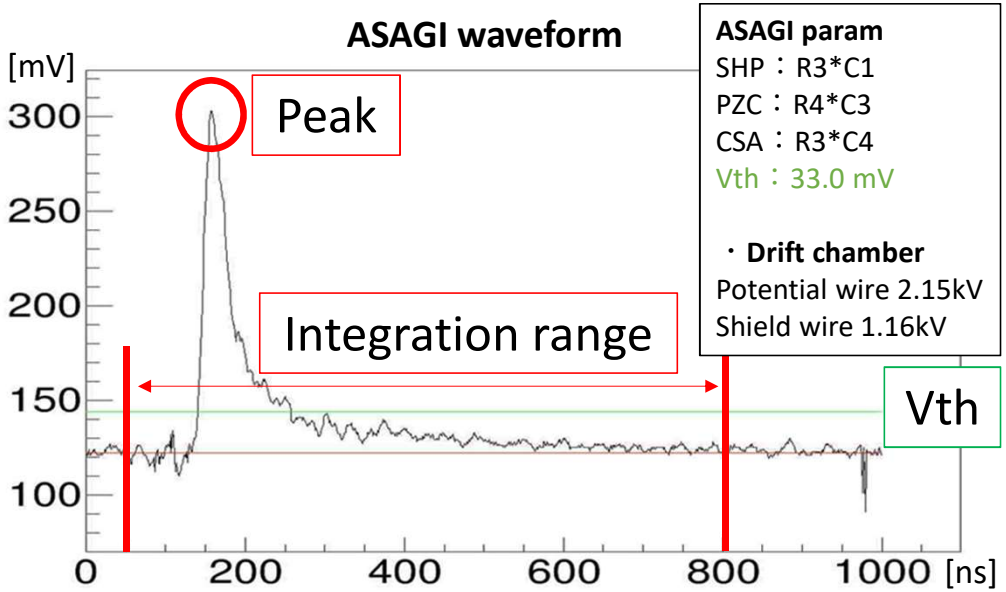
Waveform analyses

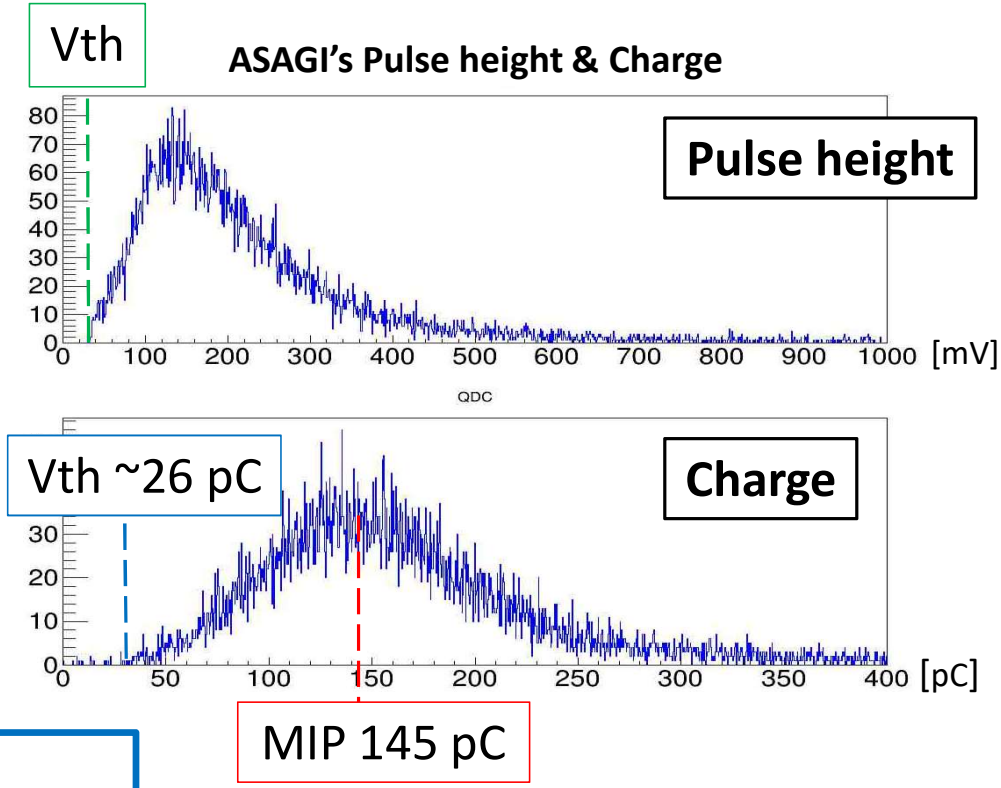




- Peak search
- Calculate baseline voltage
  - Baseline correction by using correlation with a certain channel of DRS4

Waveform analyses





Pulse Height and Charge Calculation Methods

1. Find peak
2. Subtract baseline voltage
3. Integration of peak region

⇒ **Charge**

Charge Vth /MIP ~ 1 / 5.6

Efficiency

$$\textbf{Efficiency} = 1 - \frac{\text{Number of no wire hit events}}{\text{Total number of events}}$$

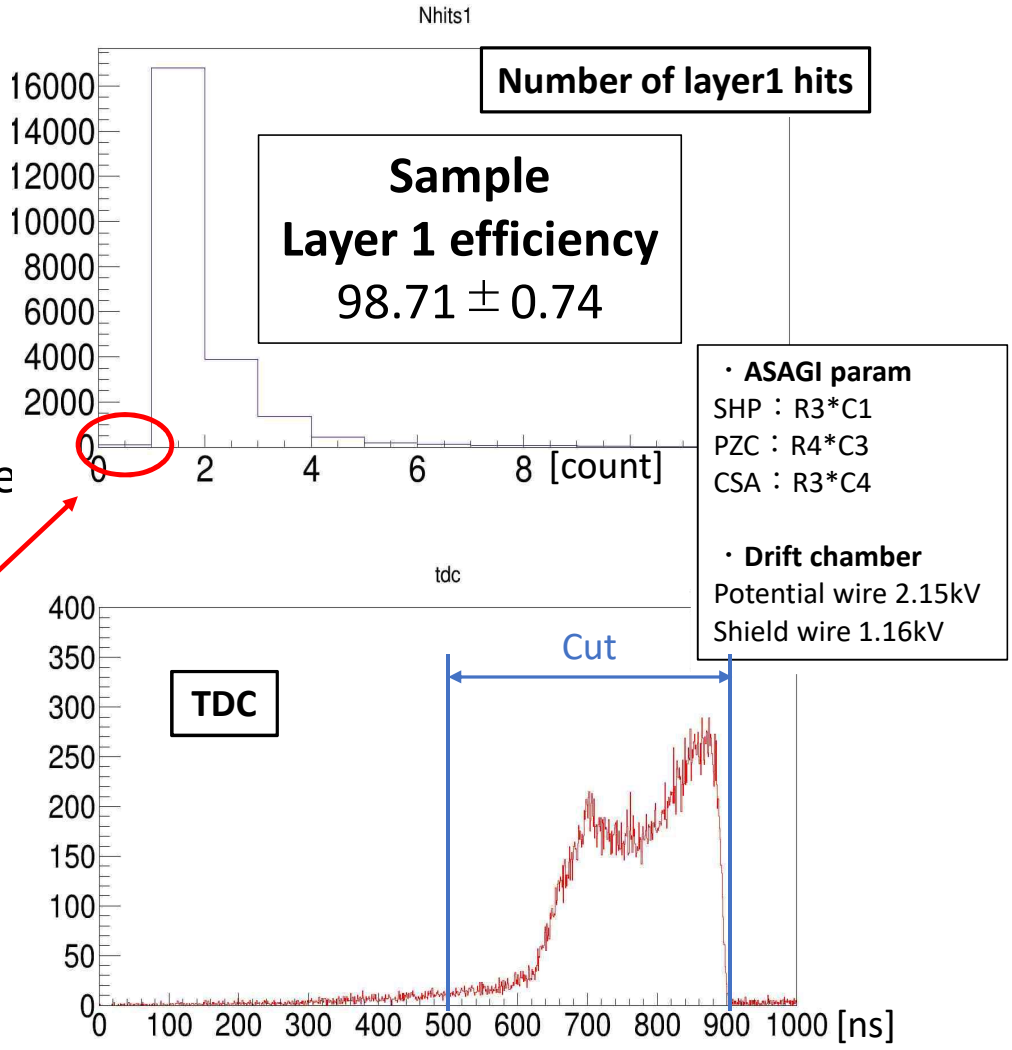
・Charged particle measured by trigger counte

⇒ **Total number of events**

・Layer multiplicity

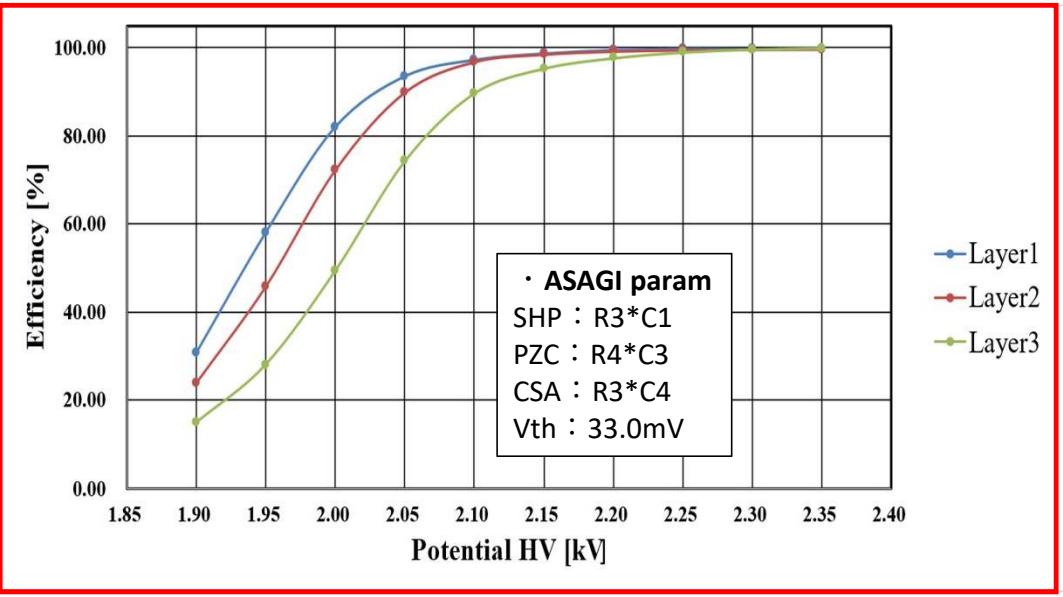
⇒ TDC hit in 400 ns region (500-900 ns)

⇒ Number of no wire hit events

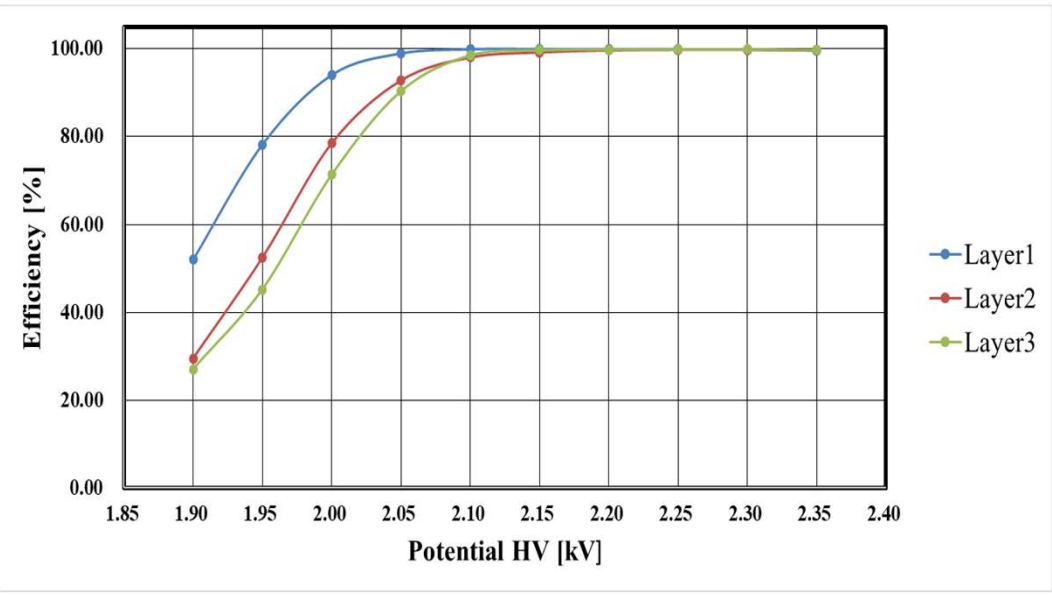


Efficiency

ASAGI-card



SONY ASD-card

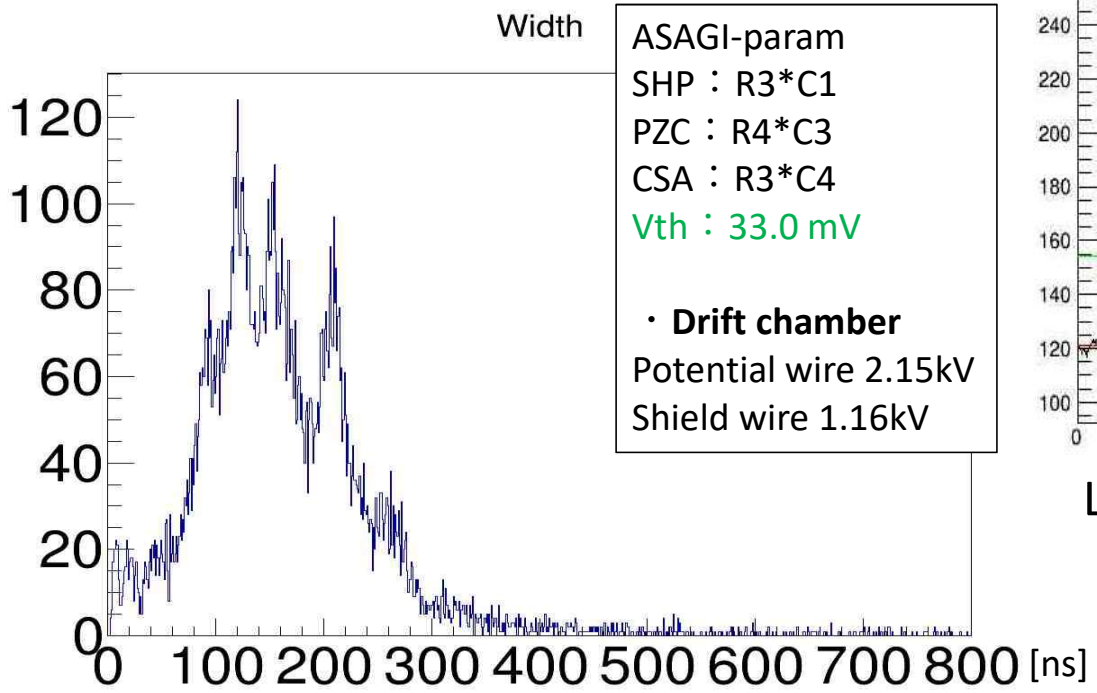


・Plateau curve is similar the old ASD card (TDC cut width is the same at 400 ns)

⇒ **Optimize analysis conditions to evaluate detection efficiency**

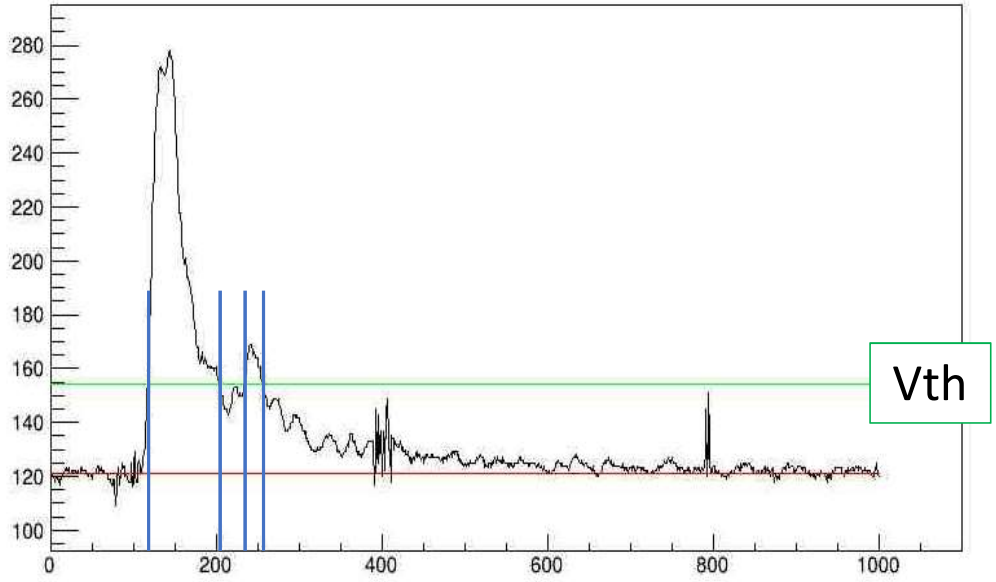
- e.g. **^{90}Sr source test for checking efficiency of layer No.3**

TDC Width



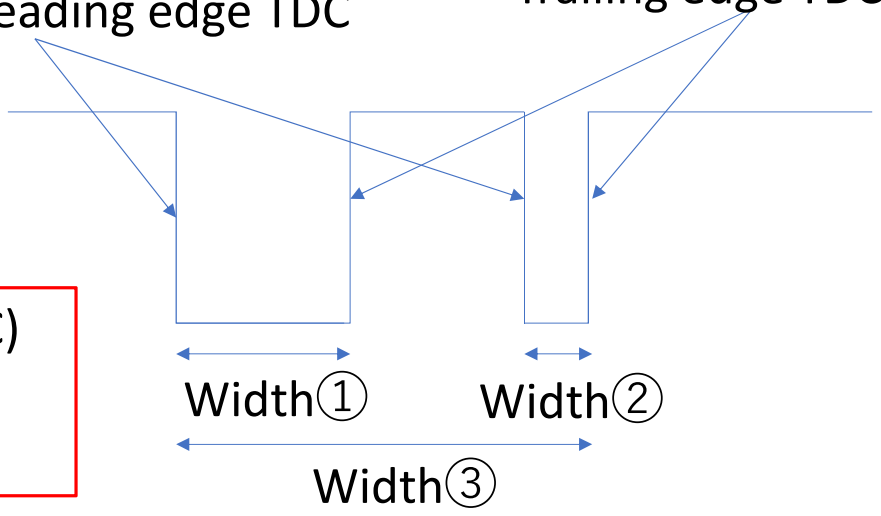
ASAGI-param
SHP：R3*C1
PZC：R4*C3
CSA：R3*C4
Vth：33.0 mV

・**Drift chamber**
Potential wire 2.15kV
Shield wire 1.16kV



Leading edge TDC

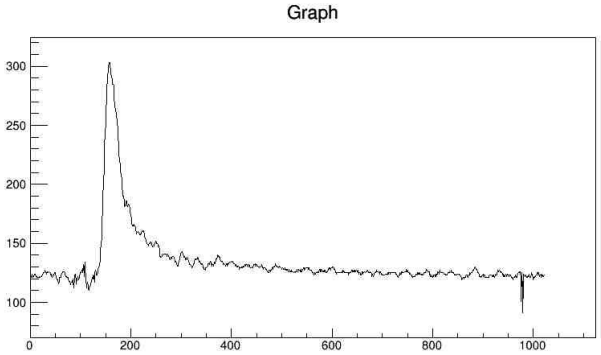
Trailing edge TDC



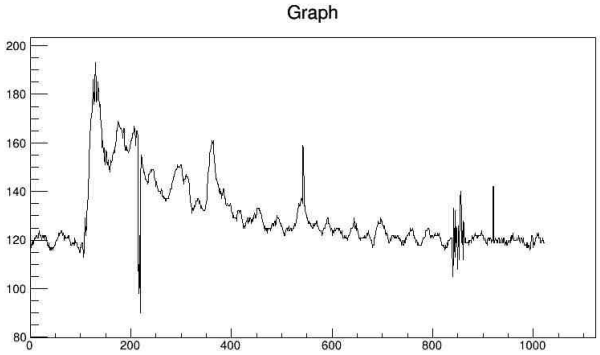
- **Width** = (Leading edge TDC) – (Trailing edge TDC)
  - First hit of both edge selected

⇒ 100–300 ns

Strange waveforms



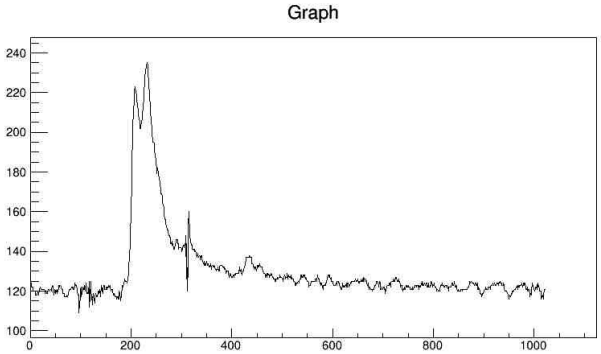
Sample 1



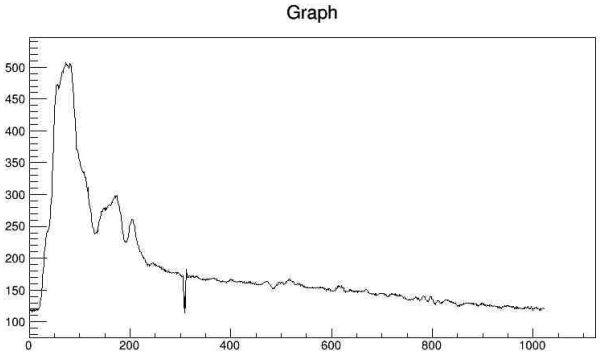
Sample 2

・**ASAGI param**
SHP：R3*C1
PZC：R4*C3
CSA：R3*C4

・**Drift chamber**
Potential wire 2.15kV
Shield wire 1.16kV



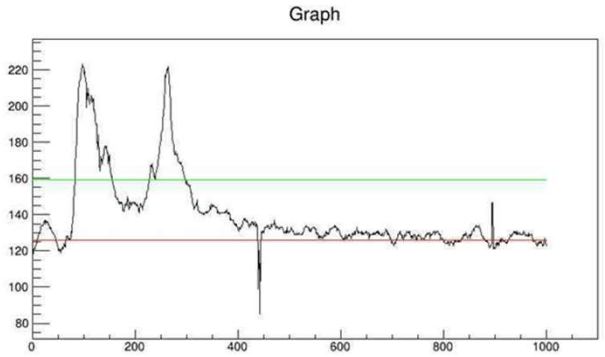
Sample 3



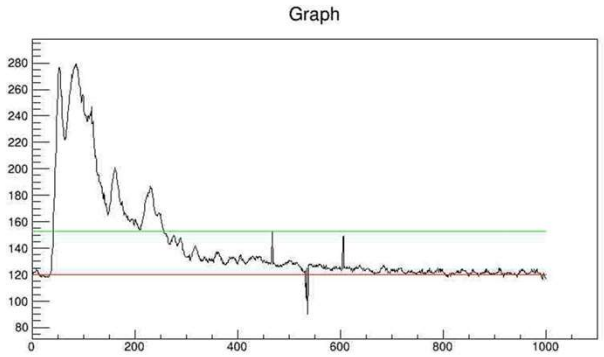
Sample 4

Sample 1 : 28 %
Sample 2 : 57 %
Sample 3 : 13 %
Sample 4 : 2 %

Strange waveforms



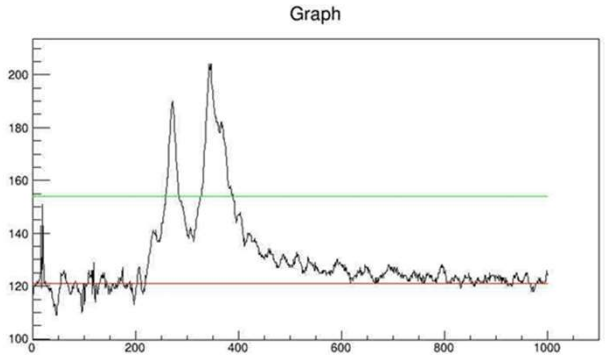
Sample 1 ?



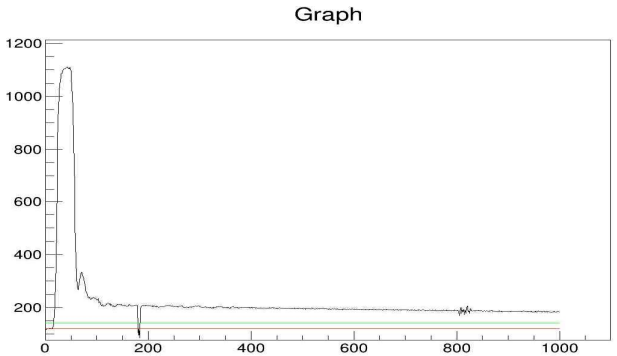
Sample 2 ?

・**ASAGI param**
SHP：R3*C1
PZC：R4*C3
CSA：R3*C4

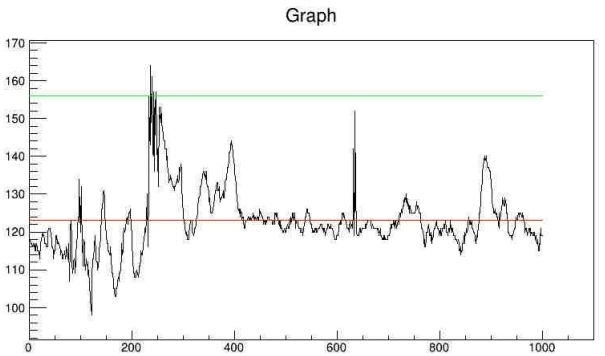
・**Drift chamber**
Potential wire 2.15kV
Shield wire 1.16kV



Sample 3 ?



Sample 4 ?



? ? ?

Homework

- **Efficiency**
  - Evaluation from tracking analysis
    - Calculate **drift velocity** and find tracks
    - Discard wrong hit events by using track information
  - Investigate **low efficiency** of layer No.3
    - ^{90}Sr source test for checking relative efficiency
      - Both ASAGI and GNA-200 used
- **TDC width check by using ^{90}Sr source**
  - Investigate **spik structure**
  - Measurement with **narrower width parameters**

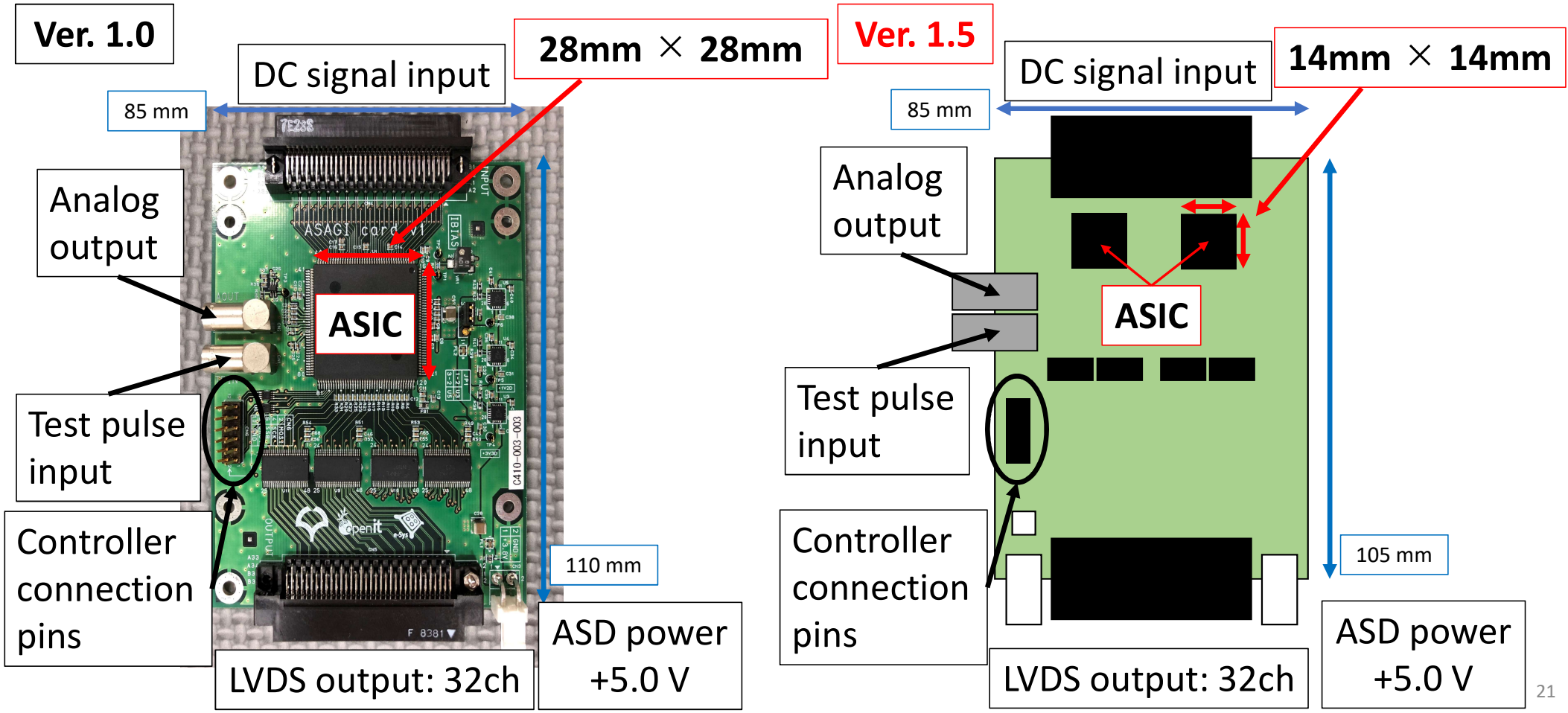
ASAGI-card update

Ver. 1.0 → Ver. 1.5

Improvement points for Version 1.5

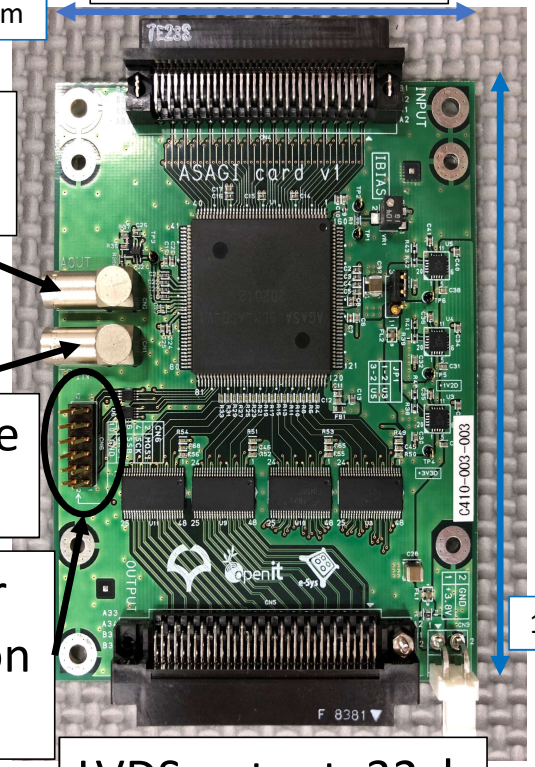
1. **Change ASIC package** and **16ch used by one ASIC**
   - Ver. 1.0: ASIC digital output and ground line coupling problem
   - Ver. 1.5: **Compact package** and **two ASICs** used for suppressing coupling
2. **Use optical communication** for register setting
   - Noise reduction in case of using metal lines
   - Introduction of **Tx chips** for optical communication
   - Fabrication of **HUL mezzanine extension board** for **Tx chips** configuration
3. **GND pin position** of LVDS-output **can be changed** depending on TDC module
   - 1,2 pin : KEK type
   - 33,34 pin : LeCroy type
4. **Other**
   - Register setting pins of ver. 1.0 are also available.
   - Anagoge output of each ASIC can be selected by changing jumper pins.

1. ASIC change

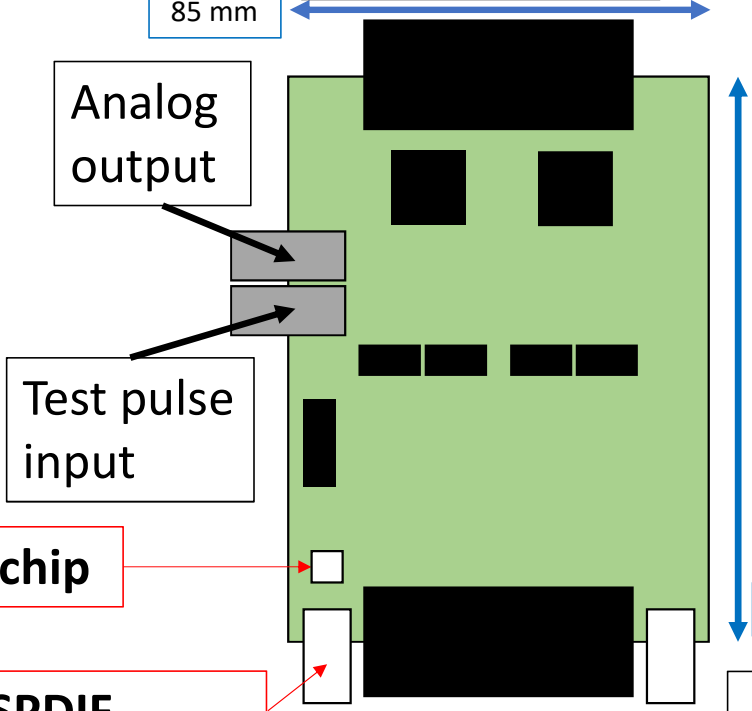


2. Optical communication: Tx chip

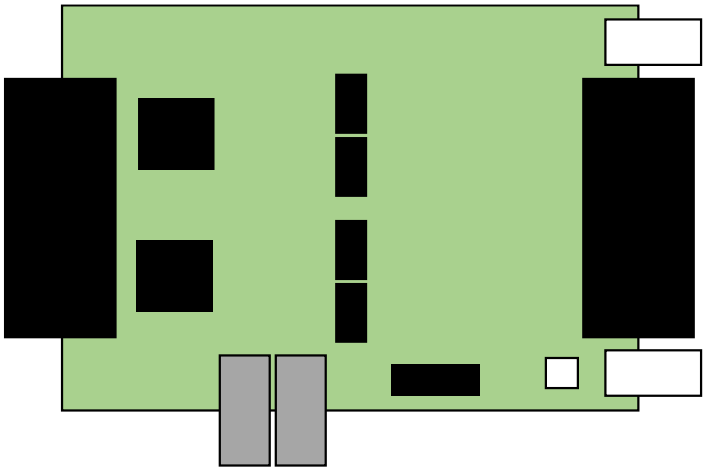
Ver. 1.0



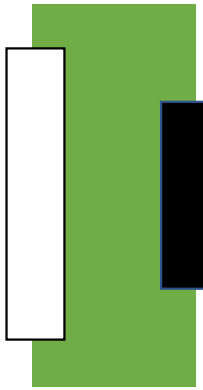
Ver. 1.5



2. Optical communication: HUL extension board



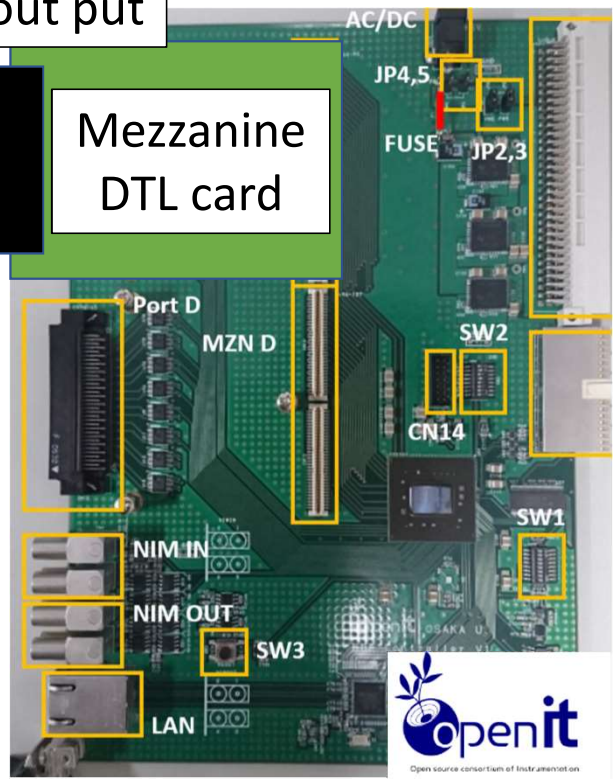
Optical connect 16ch



Flat cable

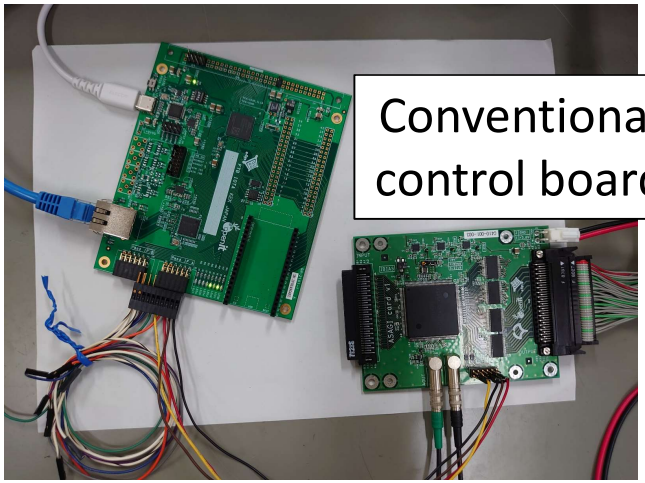
32ch out put

Mezzanine DTL card



HUL

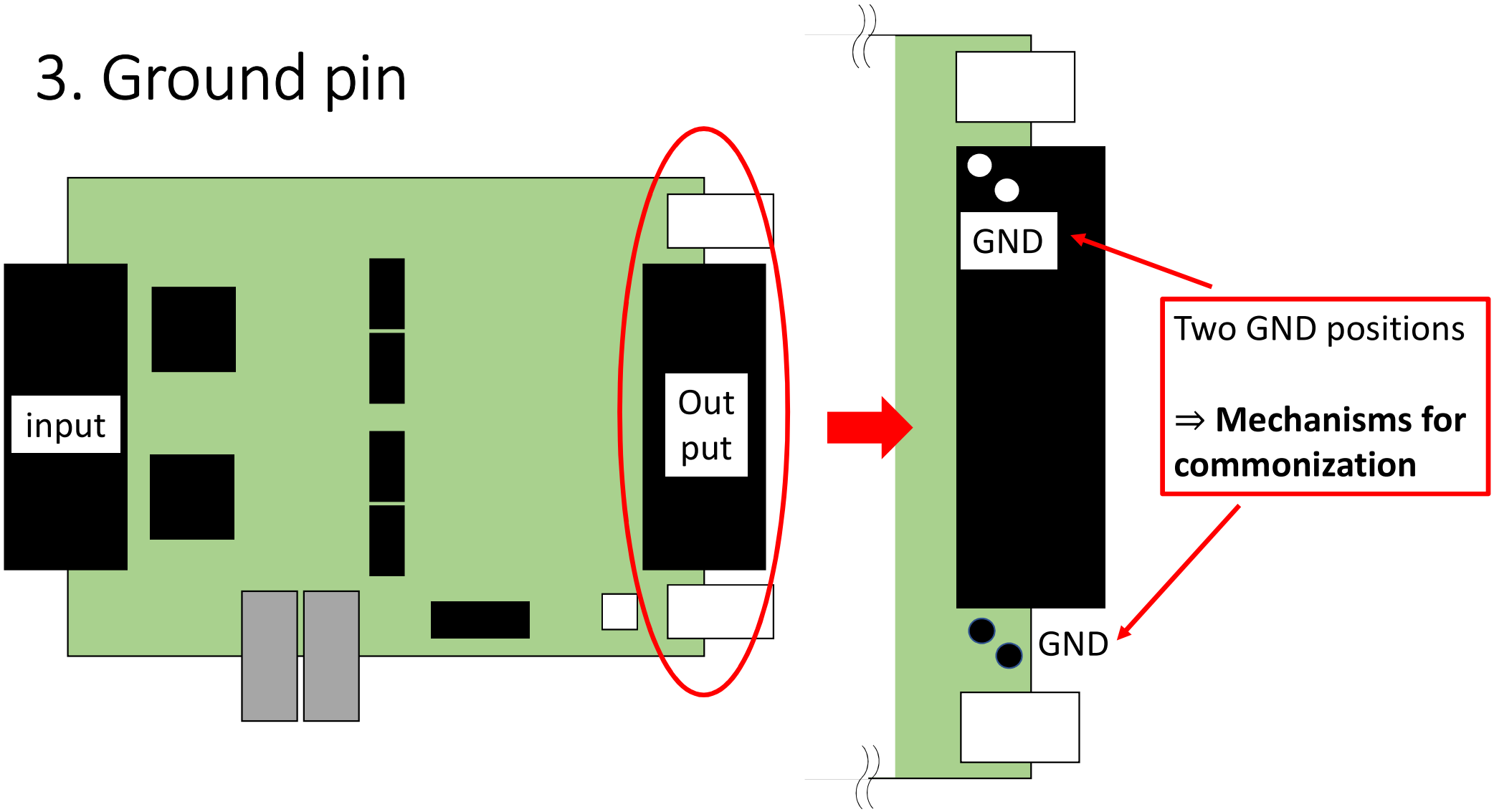
Mezzanine extension board
16ch ×2



Conventional control board

Mezzanine DTL card × 2
&
Mezzanine extension board × 4
⇒ 64 channels / HUL

3. Ground pin


input
Out
put
GND
GND
Two GND positions
⇒ **Mechanisms for commonization**

Summary

- Development of **an ASD card with a new ASIC chip** for the E50 experiment **: ASAGI-card**
- **ASAGI card with AGASA ASIC** (**AGASA**: **A**sic for **G**as detector **A**mp **Sha**per discriminator)
  - **Charge amplification factor, pole-zero cancellation effect, shaping time** and **the threshold of the discriminator can be adjusted**

⇒ **Common readout ADC card** for various gas detectors

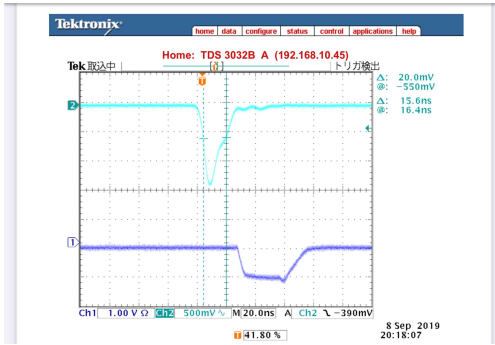
- **Performance evaluation of ASAGI with a drift chamber @SPring-8 LEPS2**
  - **Threshold : Charge Vth/MIP =** 1 / 5.6
  - **Efficiency plateau curve** is consistent with the old ASD card
  - **Width** = 100～300 ns (wider than old ASD card ⇒ Smaller shaping time constant will be tested)

- **ASAGI card update**
  - **Change the package** and **read 16ch per ASIC**
  - **Use optical communication** for register setting for noise reduction
  - **GND pin position** of LVDS output **can be changed** according to TDC module

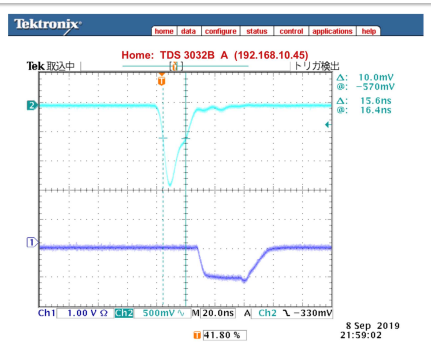
Back up

比較　Rの比（Cの比）が同じものR_{PZC}：R_{CSA}＝1：2,　（C_{PZC}：C_{CSA}＝2：1）

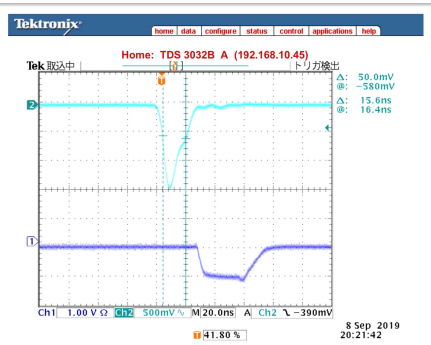
ほぼ同じ形、大きさの波形が得られた



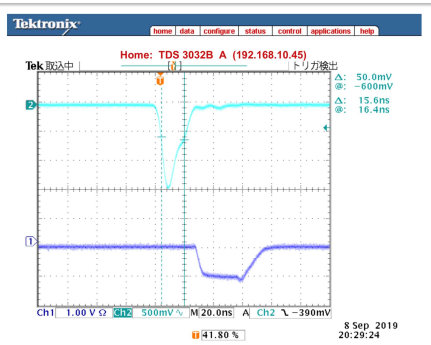
pzcR1C2_csaR2C1



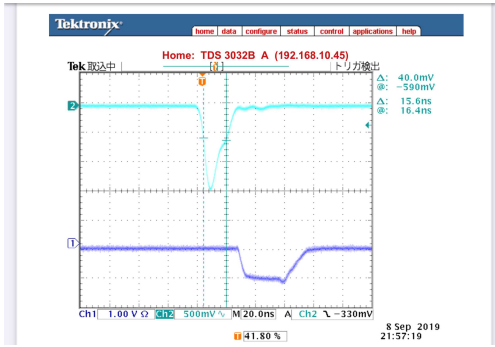
pzcR2C2_csaR4C1



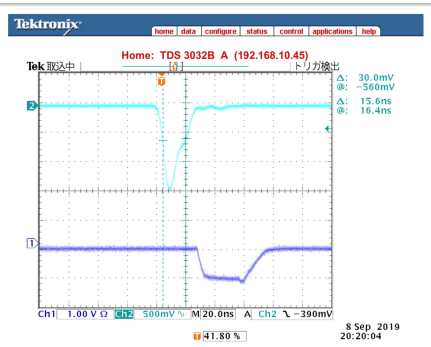
pzcR1C8_csaR2C4



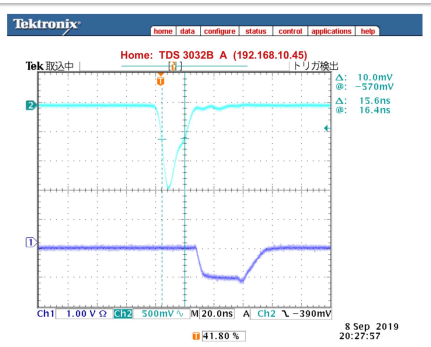
pzcR2C6_csaR4C3



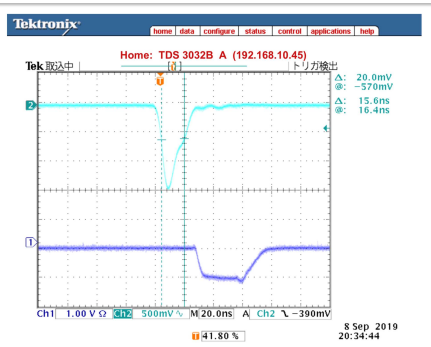
pzcR1C4_csaR2C2



pzcR1C6_csaR2C3



pzcR2C4_csaR4C2



pzcR2C8_csaR4C4

パラメータと波高の倍率

PZC:R1*C1,CSA:R1*C1

SHP	mV	倍率	SHP	mV	倍率	SHP	mV	倍率	SHP	mV	倍率
11	480	1	21	720	1.5	31	820	1.708333	41	900	1.875
12	360	0.75	22	440	0.916667	32	500	1.041667	42	520	1.083333
13	280	0.583333	23	320	0.666667	33	360	0.75	43	360	0.75
14	240	0.5	24	260	0.541667	34	280	0.583333	44	280	0.583333
15	200	0.416667	25	240	0.5	35	240	0.5	45	240	0.5
16	180	0.375	26	200	0.416667	36	200	0.416667	46	200	0.416667
17	160	0.333333	27	160	0.333333	37	180	0.375	47	180	0.375
18	140	0.291667	28	160	0.333333	38	160	0.333333	48	160	0.333333

SHP:R3*C1

pzcR:csaR	mV	倍率	pzcR:csaR	mV	倍率
1:1	820	1			
3:4	1100	1.341463	4:3	700	0.853659
2:3	1200	1.463415	3:2	600	0.731707
1:2	1400	1.707317	2:1	450	0.54878
1:3	1750	2.134146	3:1	350	0.426829
1:4	2050	2.5	4:1	200	0.243902

0.1pF*1.2V　0.12pC

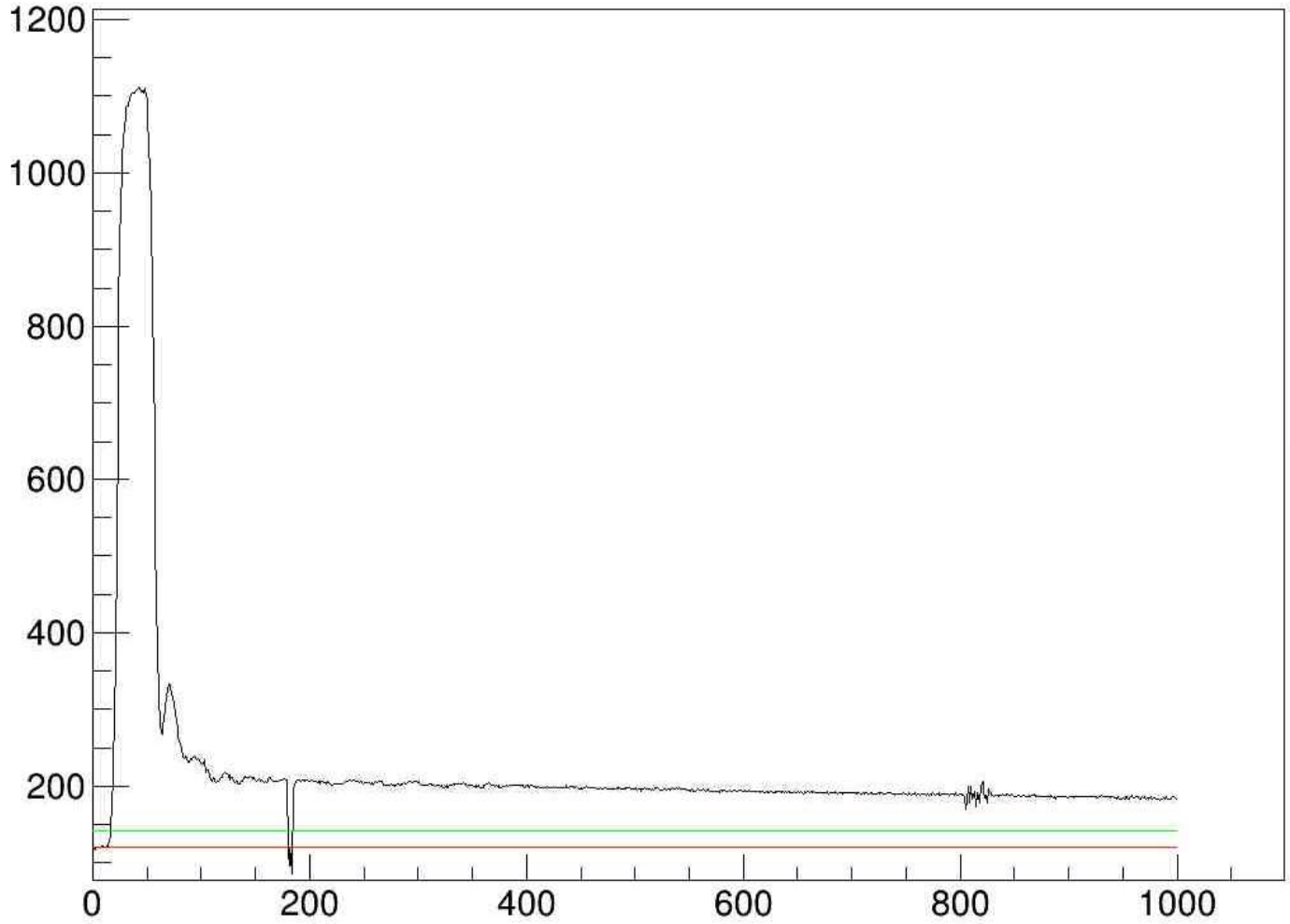
最小のゲインが得られる組み合わせ

例）114114
SHP：R1*C1
PZC：R4*C1
CSA：R1*C4

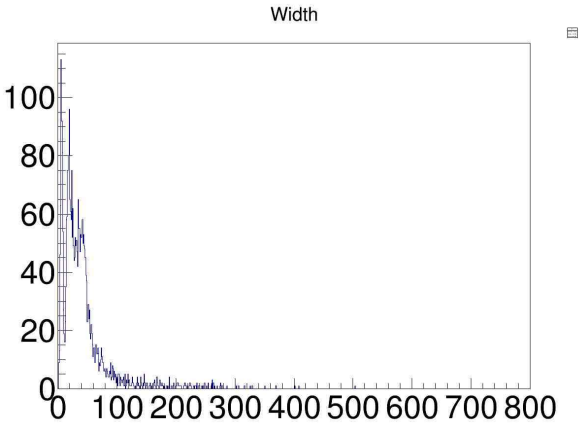
param	mV	倍率	param	mV	倍率	param	mV	倍率	param	mV	倍率
114114	205	0.426829	214114	307	0.640244	314114	350	0.729167	414114	384	0.800305
124114	154	0.320122	224114	188	0.39126	324114	213	0.444614	424114	222	0.462398
134114	120	0.248984	234114	137	0.284553	334114	154	0.320122	434114	154	0.320122
144114	102	0.213415	244114	111	0.231199	344114	120	0.248984	444114	120	0.248984
154114	85	0.177846	254114	102	0.213415	354114	102	0.213415	454114	102	0.213415
164114	77	0.160061	264114	85	0.177846	364114	85	0.177846	464114	85	0.177846
174114	68	0.142276	274114	68	0.142276	374114	77	0.160061	474114	77	0.160061
184114	60	0.124492	284114	68	0.142276	384114	68	0.142276	484114	68	0.142276

最大のゲインが得られる組み合わせ

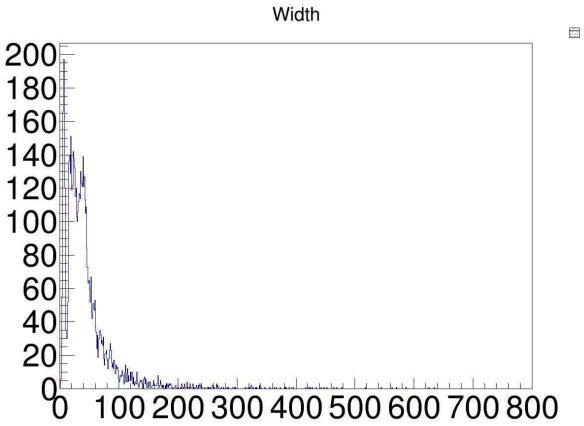
param	mV	倍率	param	mV	倍率	param	mV	倍率	param	mV	倍率
111441	1200	2.5	211441	1800	3.75	311441	2050	4.270833	411441	2250	4.687500
121441	900	1.875	221441	1100	2.291667	321441	1250	2.604167	421441	1300	2.708333
131441	700	1.458333	231441	800	1.666667	331441	900	1.875	431441	900	1.875
141441	600	1.25	241441	650	1.354167	341441	700	1.458333	441441	700	1.458333
151441	500	1.041667	251441	600	1.25	351441	600	1.25	451441	600	1.25
161441	450	0.9375	261441	500	1.041667	361441	500	1.041667	461441	500	1.041667
171441	400	0.833333	271441	400	0.833333	371441	450	0.9375	471441	450	0.9375
181441	350	0.729167	281441	400	0.833333	381441	400	0.833333	481441	400	0.833333


Graph
1200
1000
800
600
400
200
0
200
400
600
800
1000

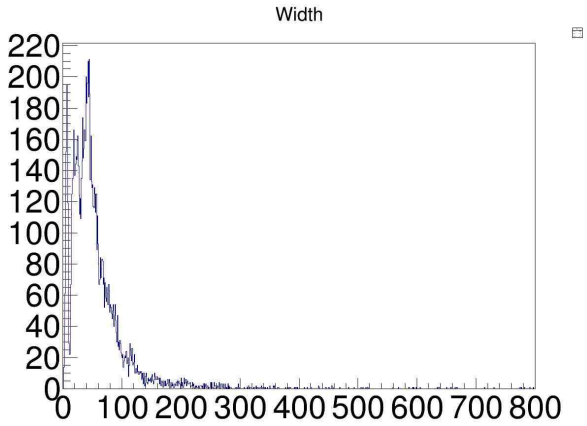
TDC Width



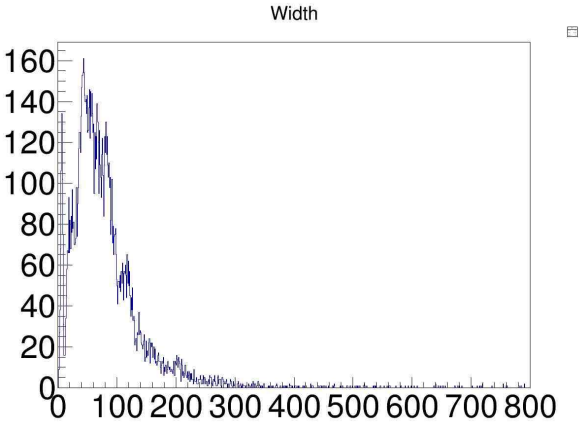
Potential wire 1.90 kV



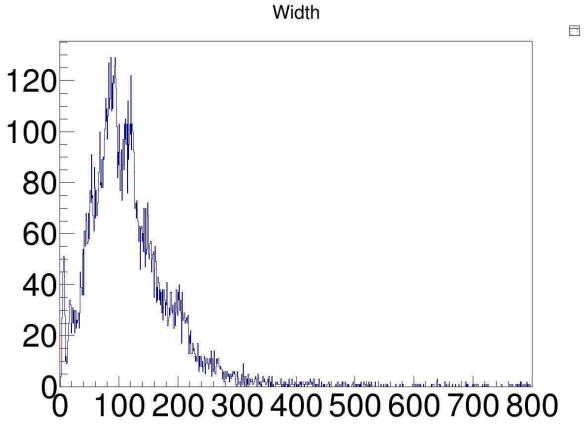
Potential wire 1.95 kV



Potential wire 2.00 kV



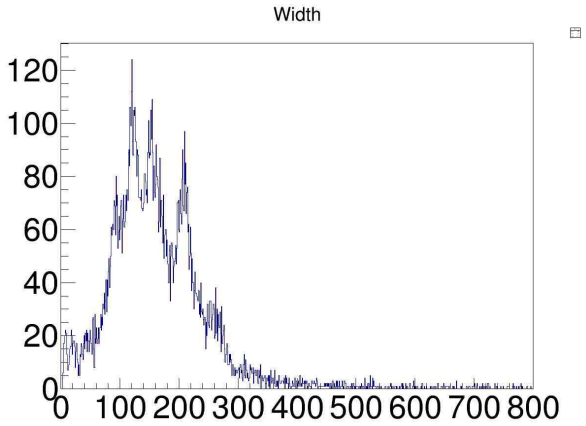
Potential wire 2.05 kV



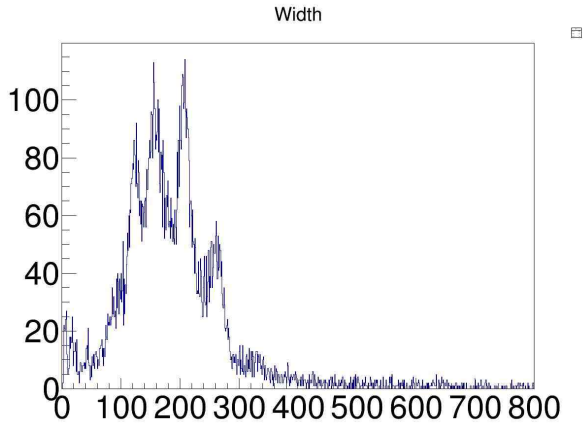
Potential wire 2.10 kV

ASAGI-param
SHP：R3*C1
PZC：R4*C3
CSA：R3*C4
Vth：33.0 mV

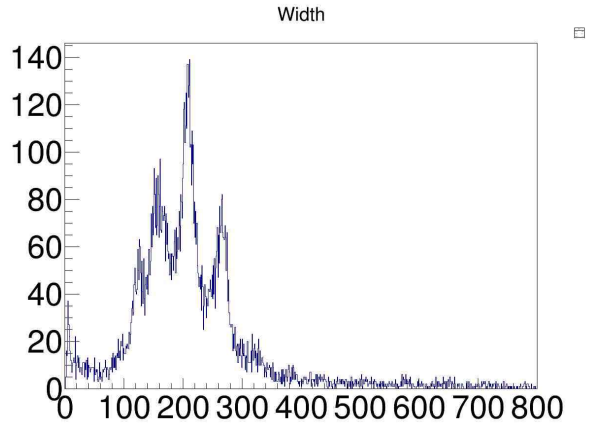
TDC Width



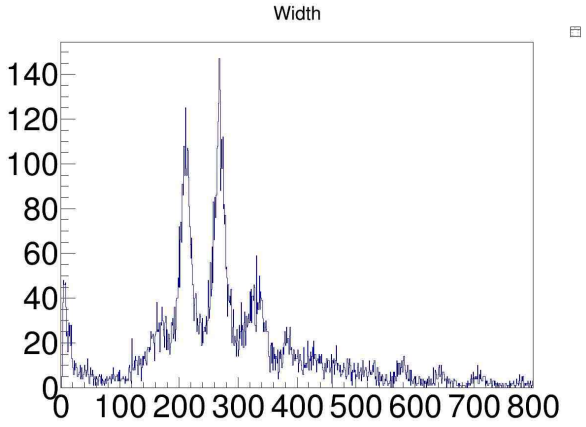
Potential wire 2.15 kV



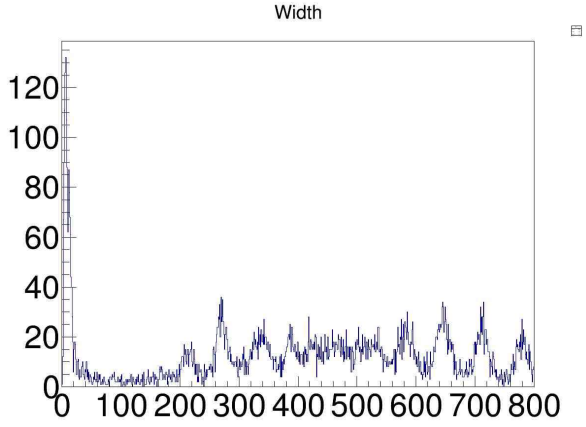
Potential wire 2.175 kV



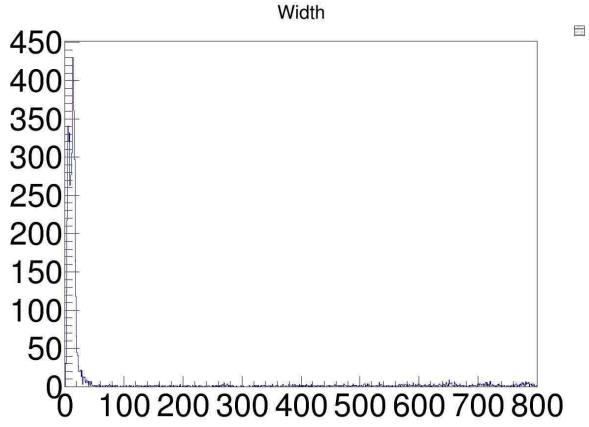
Potential wire 2.20 kV



Potential wire 2.25 kV

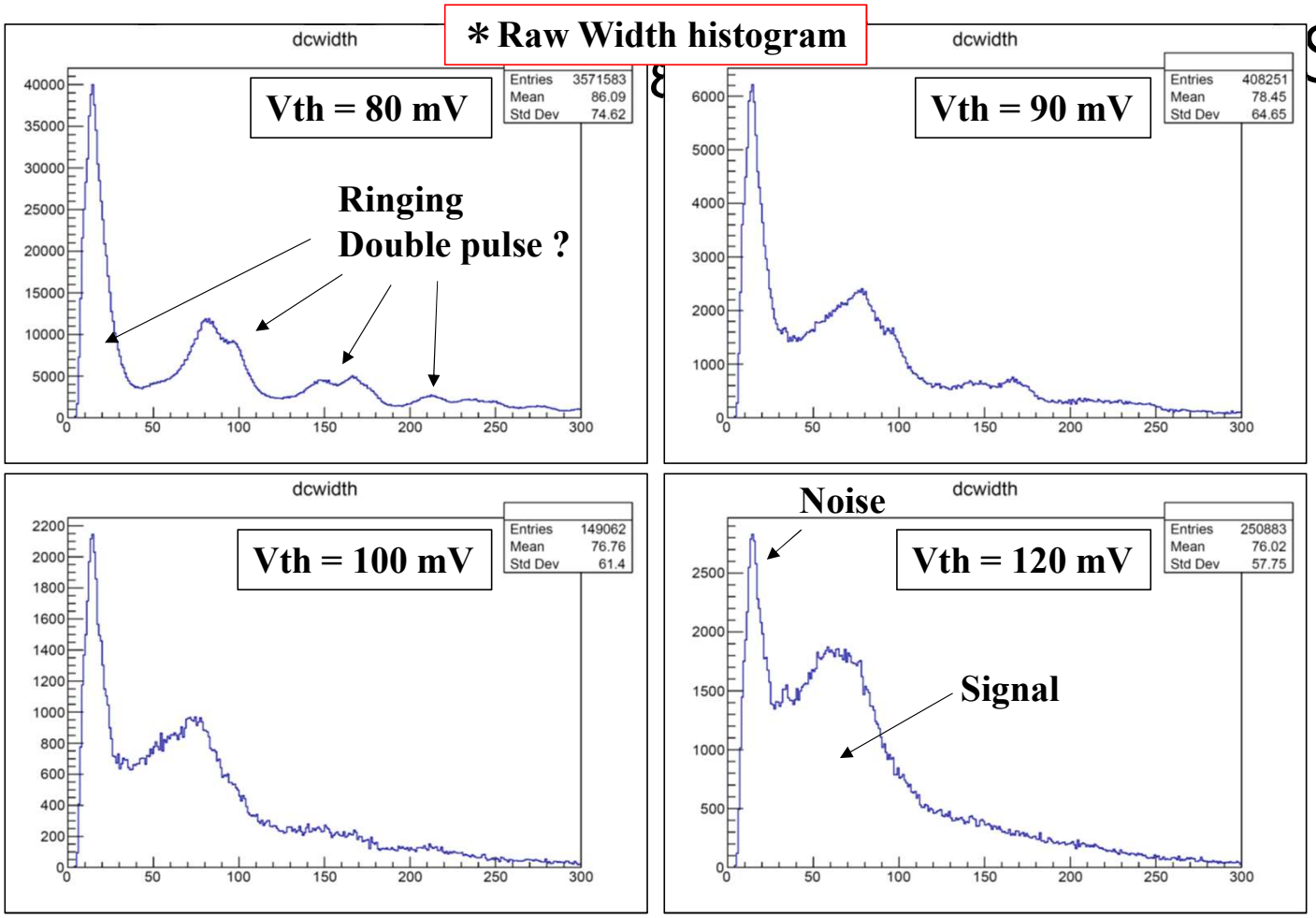


Potential wire 2.30 kV



Potential wire 2.35 kV

SDA (GNA@200)



- All layer @ Low rate
  - V = 2.15 kV
  - **$Ar:CO_2 = 90:10$**
  - Efficiency: > 99% in each Vth
  - Cross talk signal

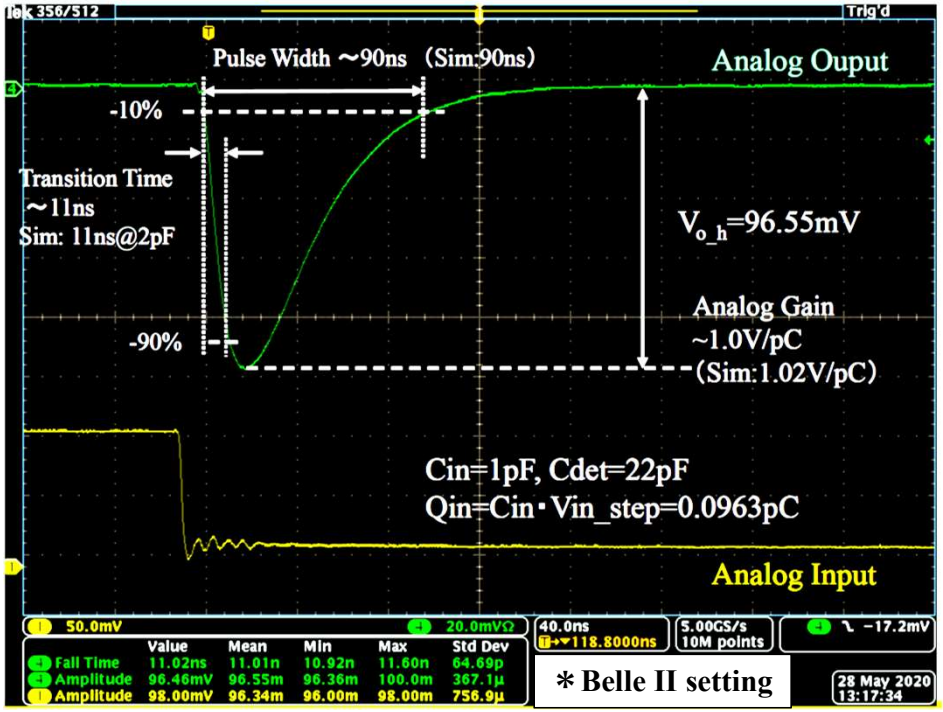
⇒ Issue for new DC ASD

- It is expected to be suppressed by using ASAGI card.
  - Better for TOT filter

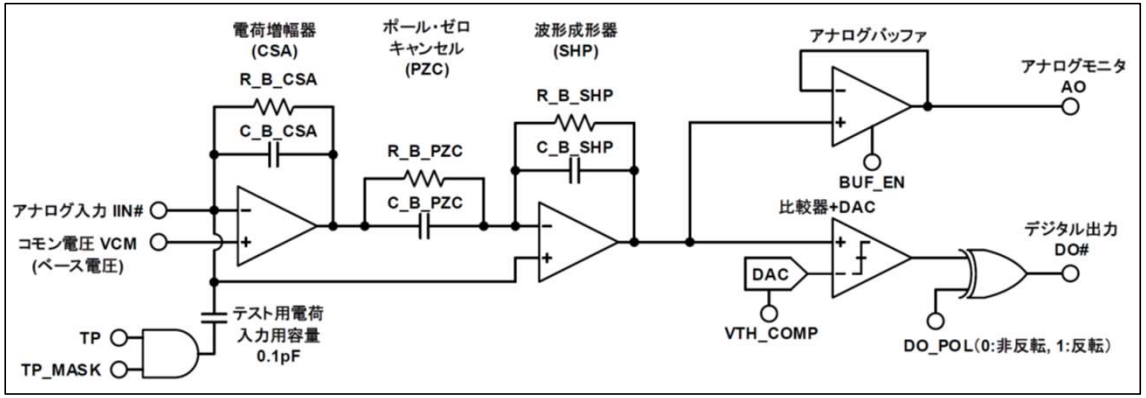
AGASA ASIC information

- Asic for Gas detector Amp Shaper discriminator
  - Conversion gain: 63mV/pC – 32V/pC
  - Peaking time: ~10 ns
  - Dynamic range: 0 – 2.0 pC
  - Pulse width: a few 10 nsec – a few μsec
  - Noise: 2200 electrons
  - Power consumption: ~12 mW/ch

Typical pulse shape

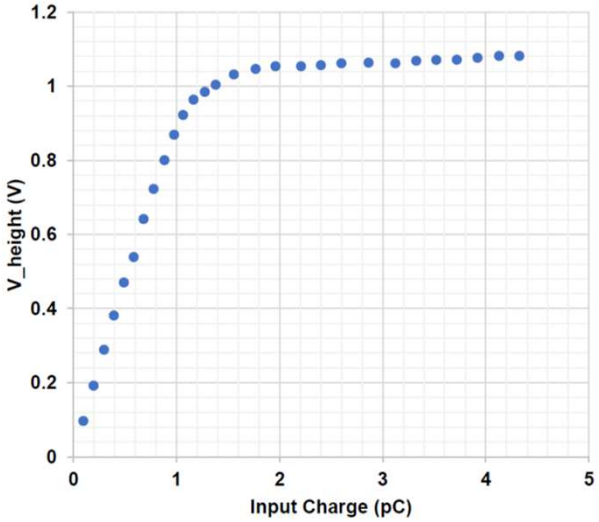


Electric circuit of 1 ASD channel

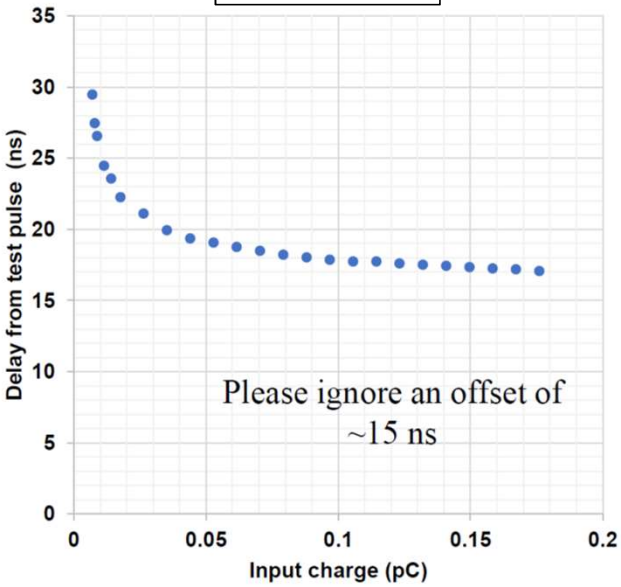


ASIC performance

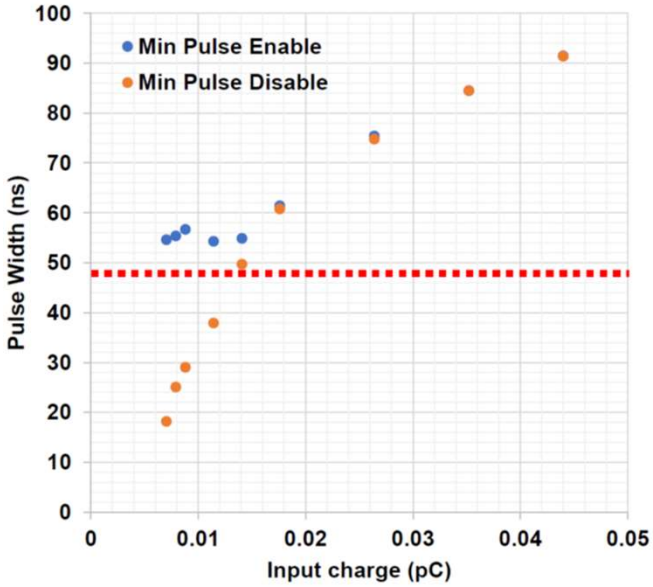
Linearity
(ASD parameters were tuned for Belle II CDC)



Time-Walk



Pulse width



＊Please ignore Min Pulse Enable case. This is only implemented in an ASIC for Belle II CDC. (Minimum pulse width of 48 ns is guaranteed by the pulse width generator.)

ASAGI Ver. 1.5 common part