ATLAS ITkモジュール量産における性能評価システムの開発

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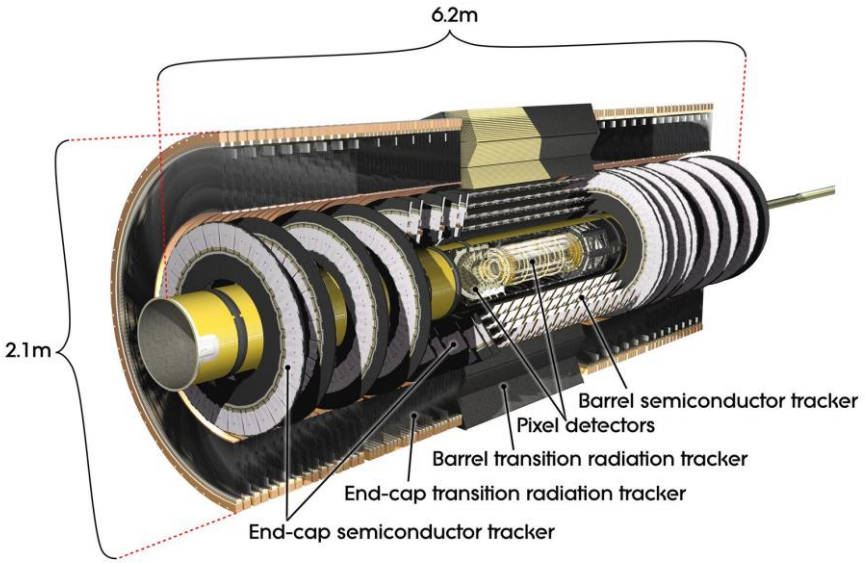
On behalf of the ATLAS ITk Pixel group

HL-LHC ATLAS Experiment

ATLAS実験：新粒子探索、標準理論の精密測定

ハドロン衝突型加速器の大型改造計画(High Luminosity LHC: HL-LHC)に合わせて
ATLAS検出器の入れ替え (ID → ITk)

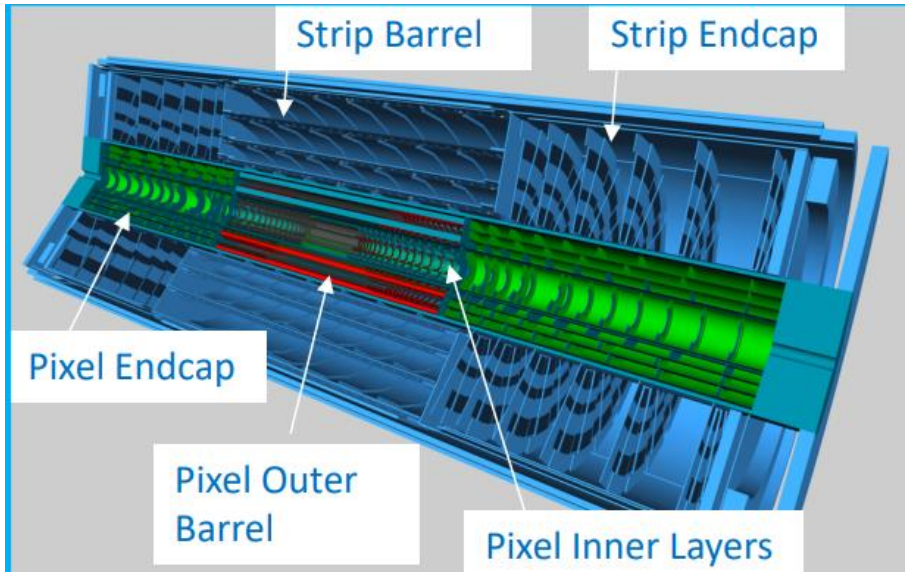
現存の Inner Detector (ID)



積分ルミノシティ~300 fm^{-1}

~2029

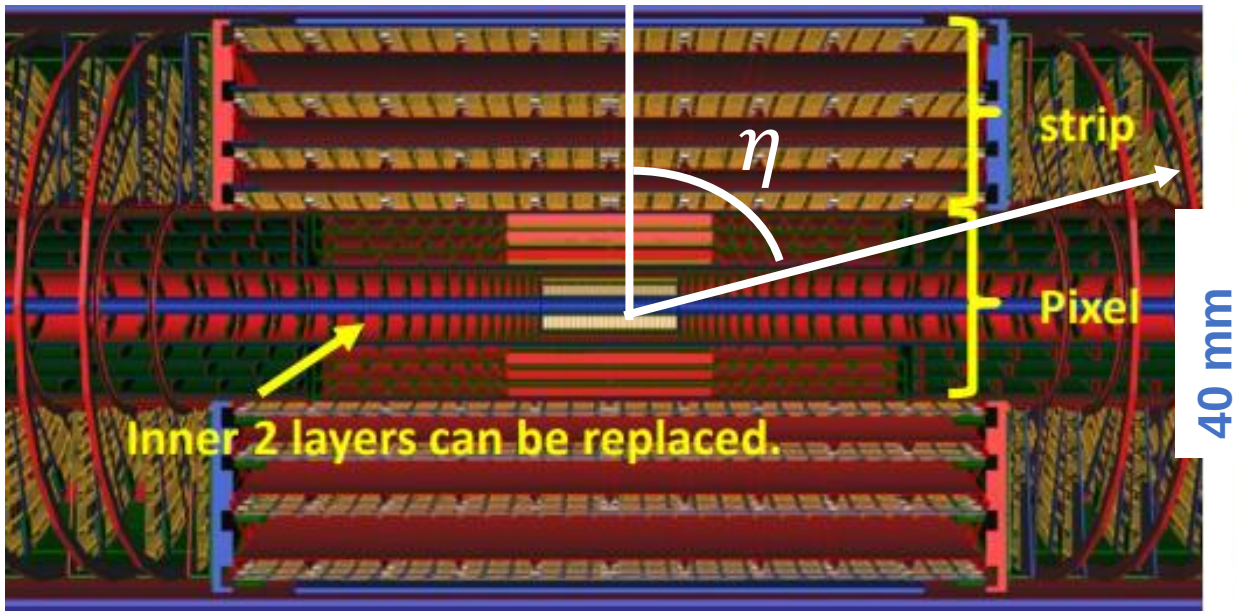
現在製造中のInner Tracker (ITk)



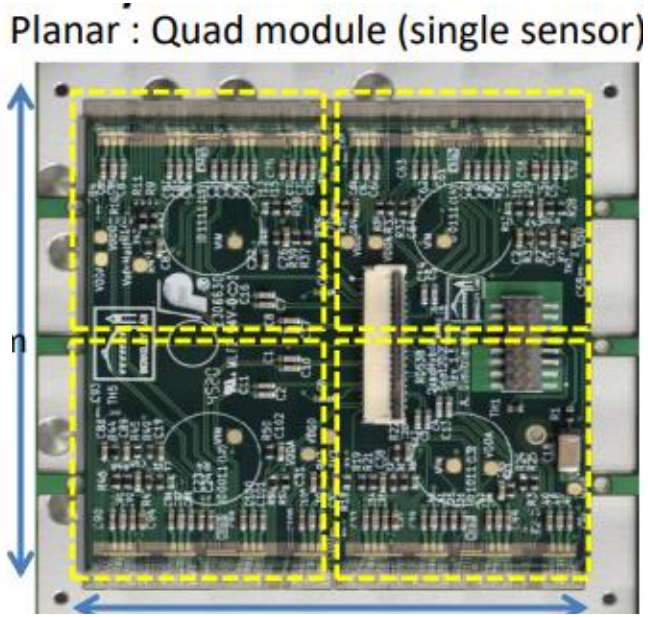
積分ルミノシティ~4000 fm^{-1}

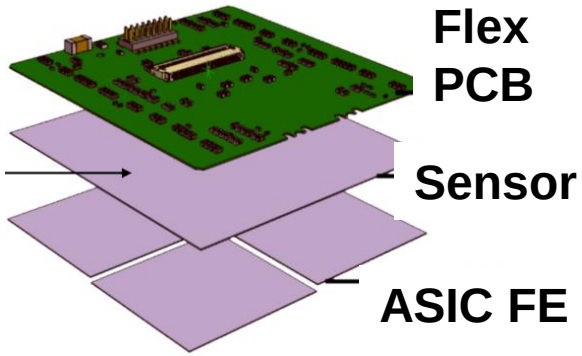
ITk detector and ITk module

ITk detector design



ITk module design

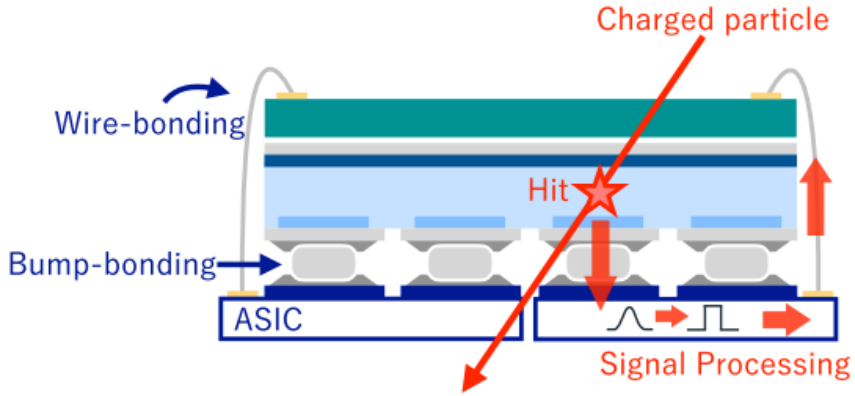




Larger coverage area :

- Pixel : ID =2.7 m^2 ➔ ITk=8.2 m^2
- Strip : ID=34 m^2 ➔ ITk=165 m^2

Higher Forward coverage : η=2.4 → 4.0



Production Plan for ITk detector

現在

2023	2024	2025	2026	2027	2028	2029	2030

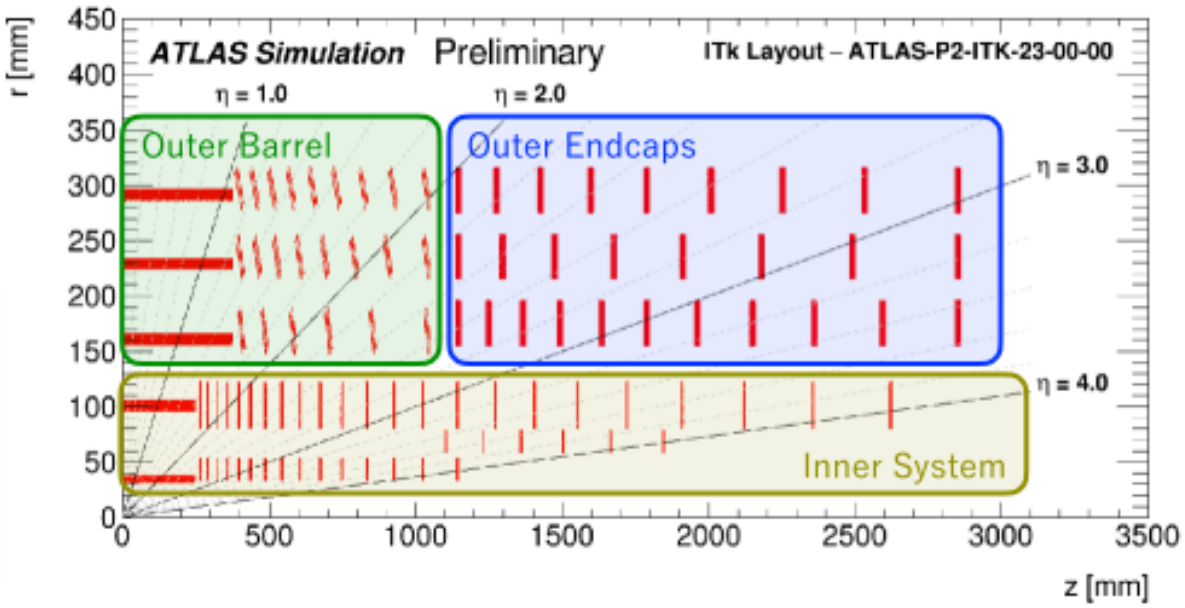
Pre-Production → Mass Production → HL- LHC Run

2024/4 mass production開始

ITk pixel ~10000 modules

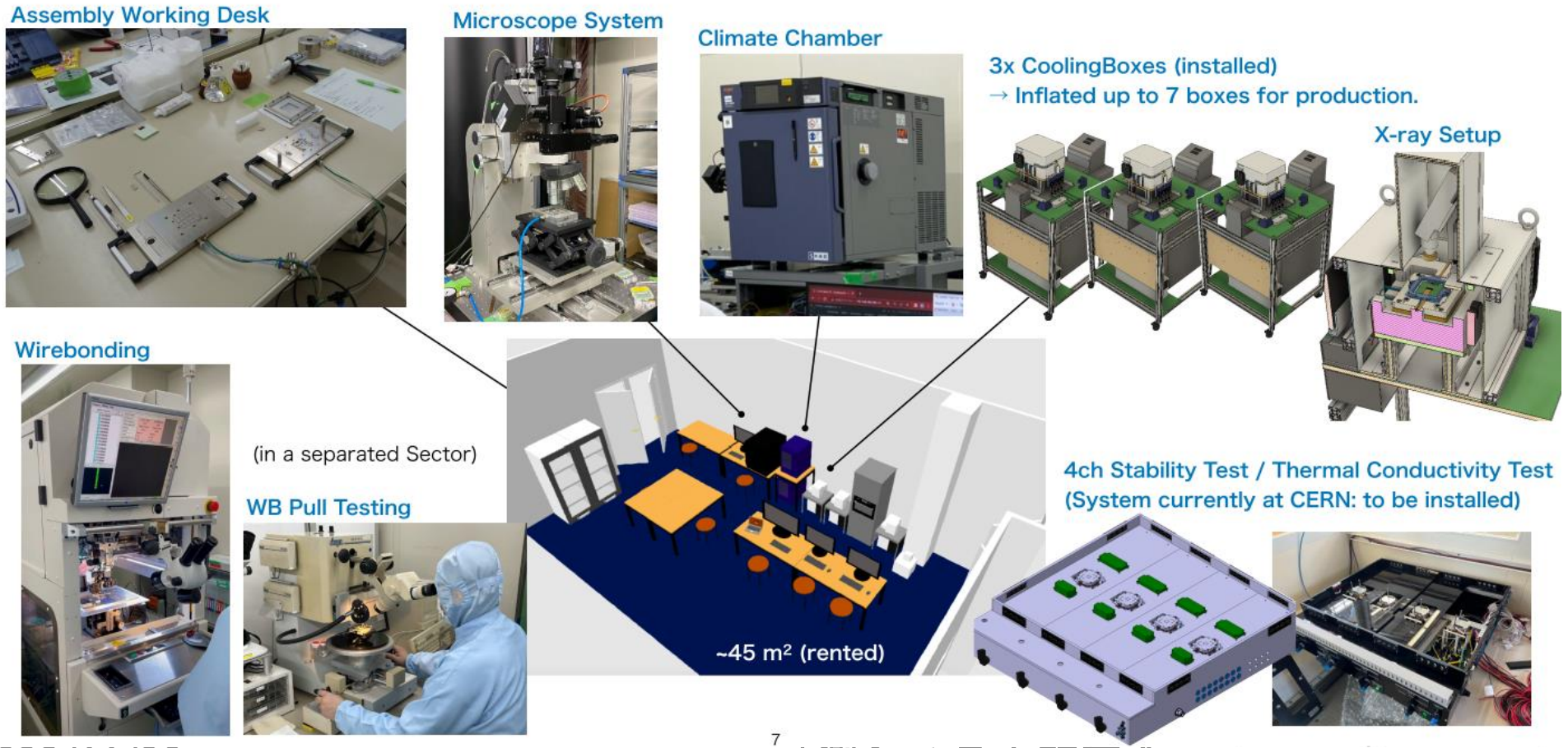
日本：2200 modules (+600)

- **Outer Barrel (OB) : 1350 modules (+600)**
- **Outer Endcaps (OE) : 850modules**



ITk production site at JAPAN

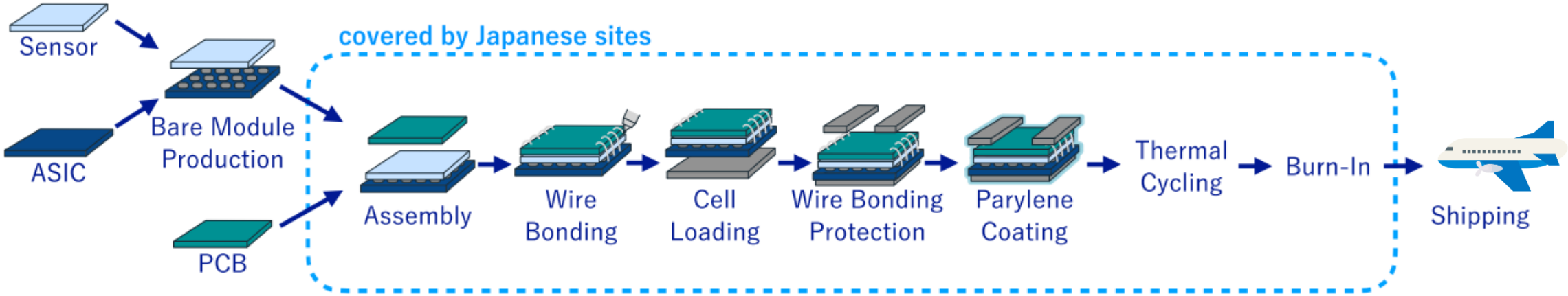
林REPIC(千葉県館山市)でITk 生産サイトを立ち上げ
モジュールの組み立てから性能評価までほとんど対応

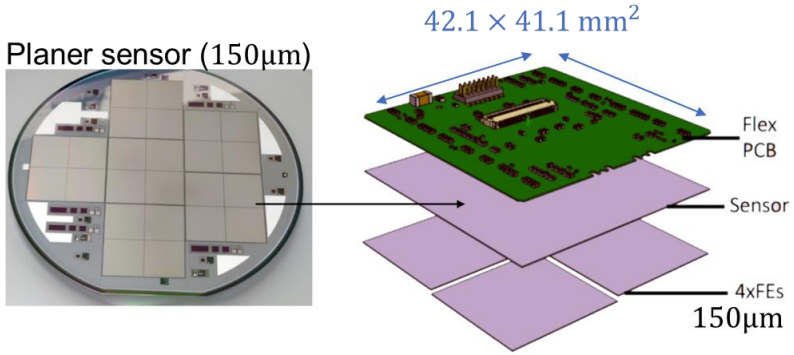


Preproduction
現在1 module/日でモジュール生産中
→ 3 modules/日に拡張予定

Mass production
7 modules/日

Module production Process

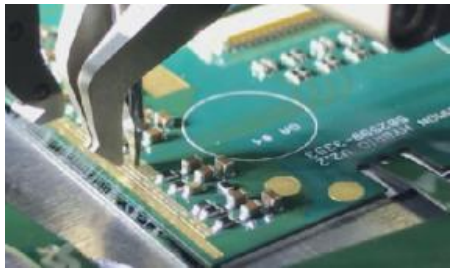


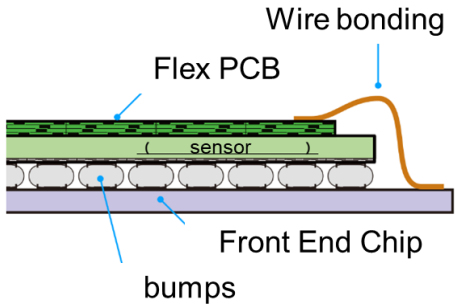


Pixel matrix 400 × 384
152800 pixels per chip

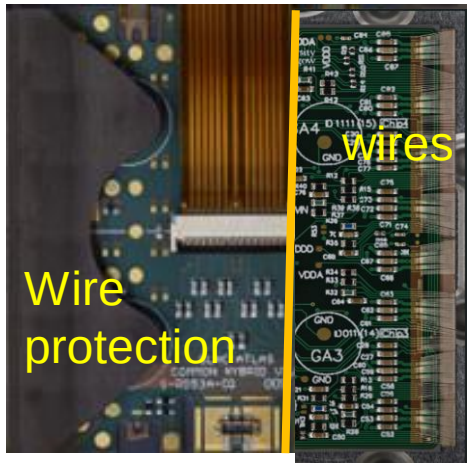
Assembly

Wire bonding



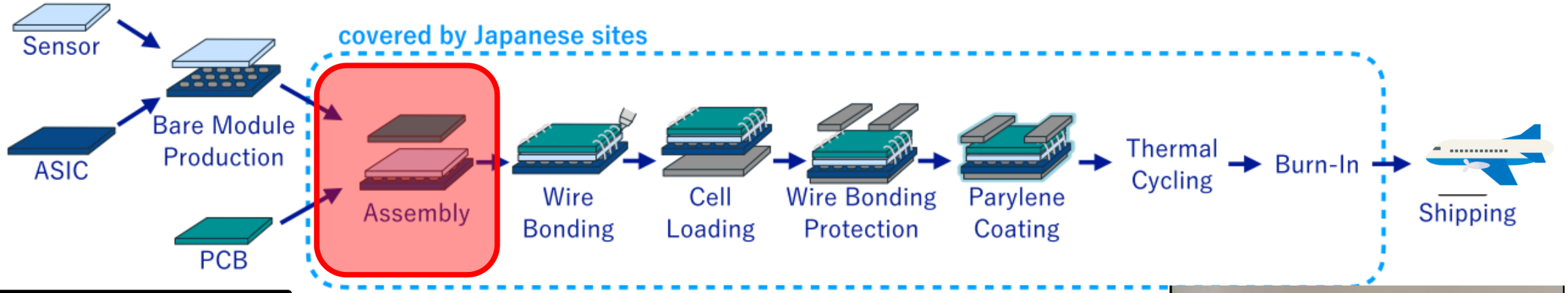


Wire bonding protection

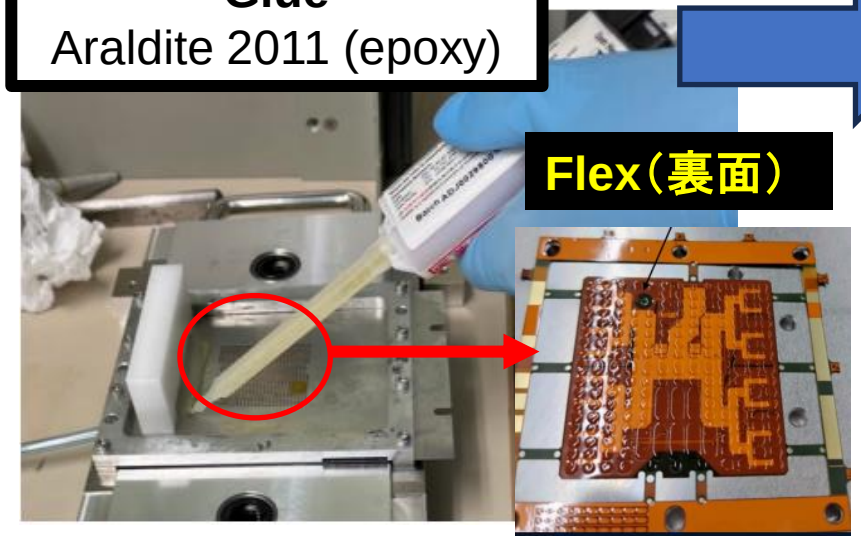


Parylene coating

Module production Process

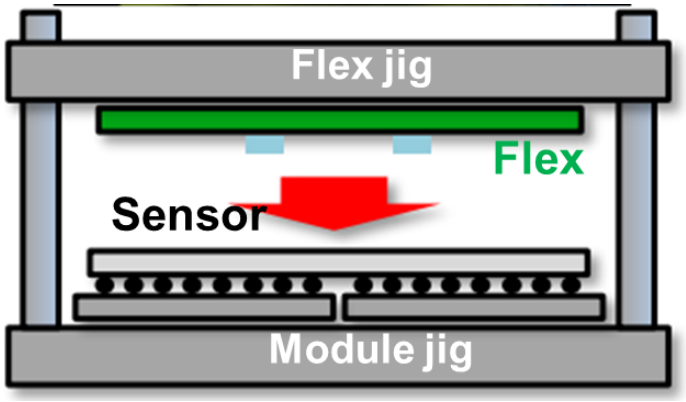


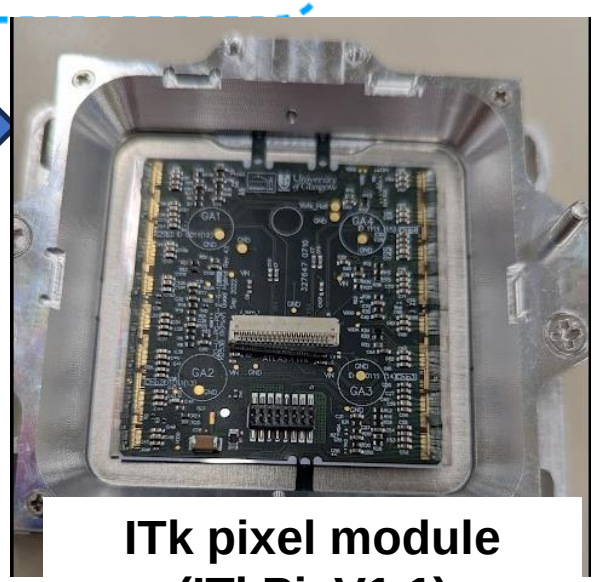
Glue
Araldite 2011 (epoxy)



Flexの裏面にGlueを貼り付け

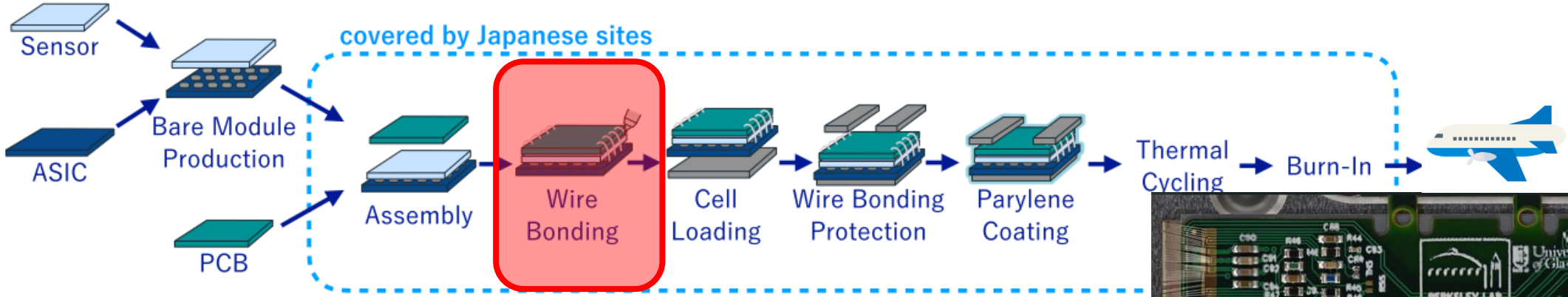
接着



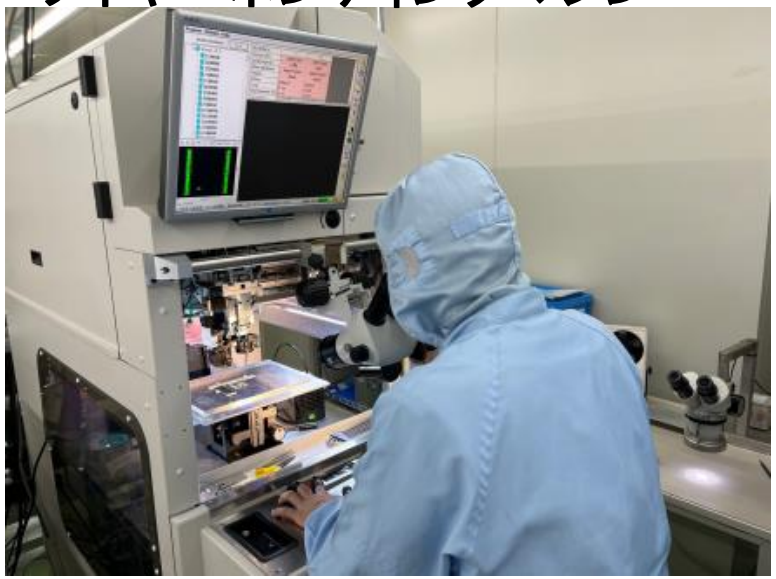


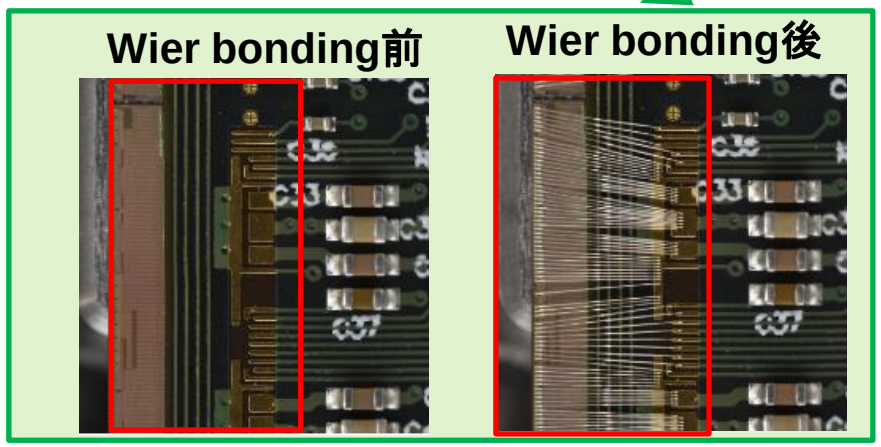
ITk pixel module (ITkPixV1.1)

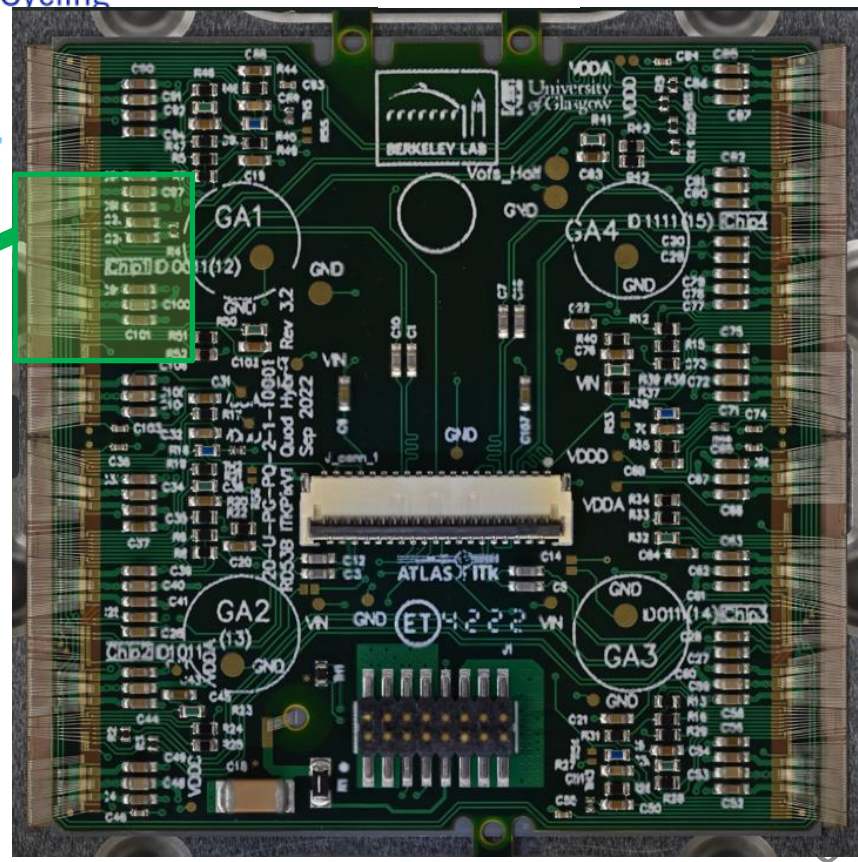
Module production Process



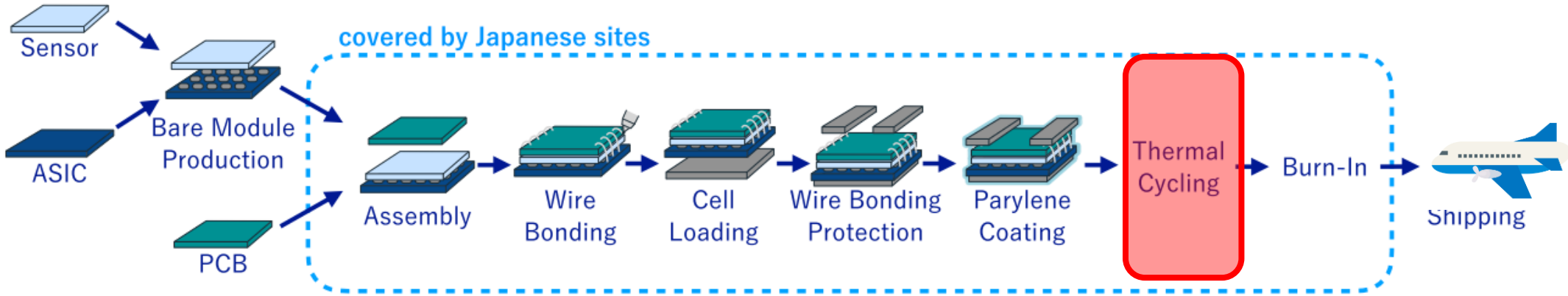
ワイヤーボンディングマシン



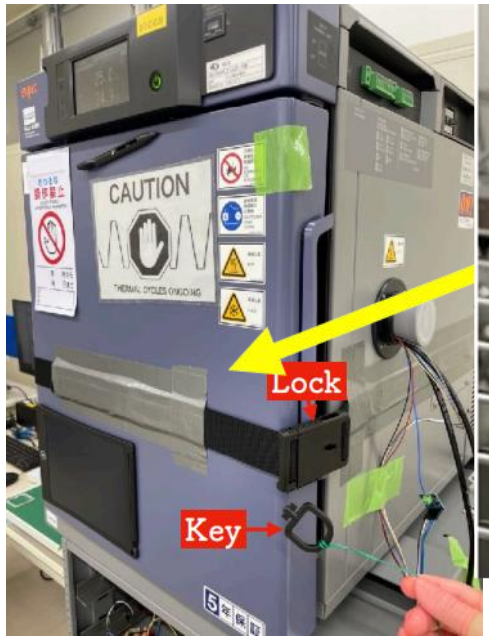


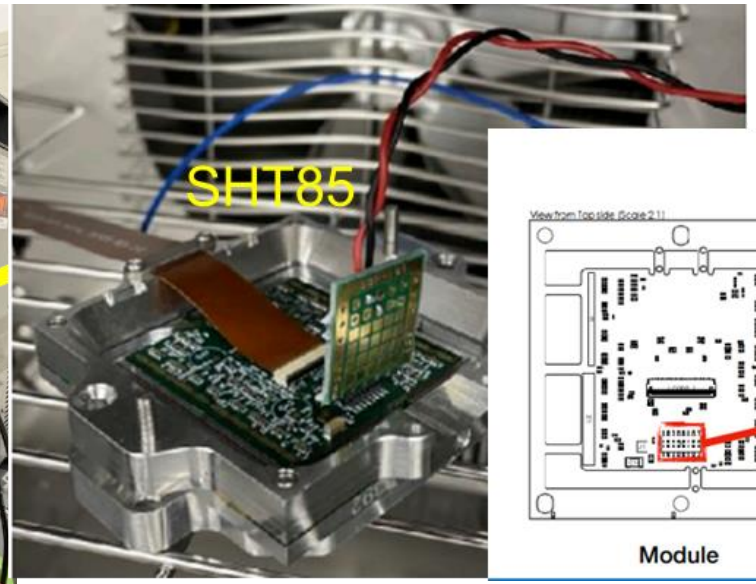


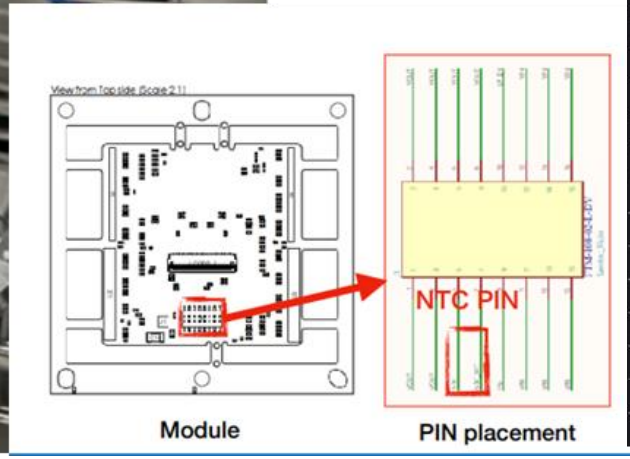
Module production Process



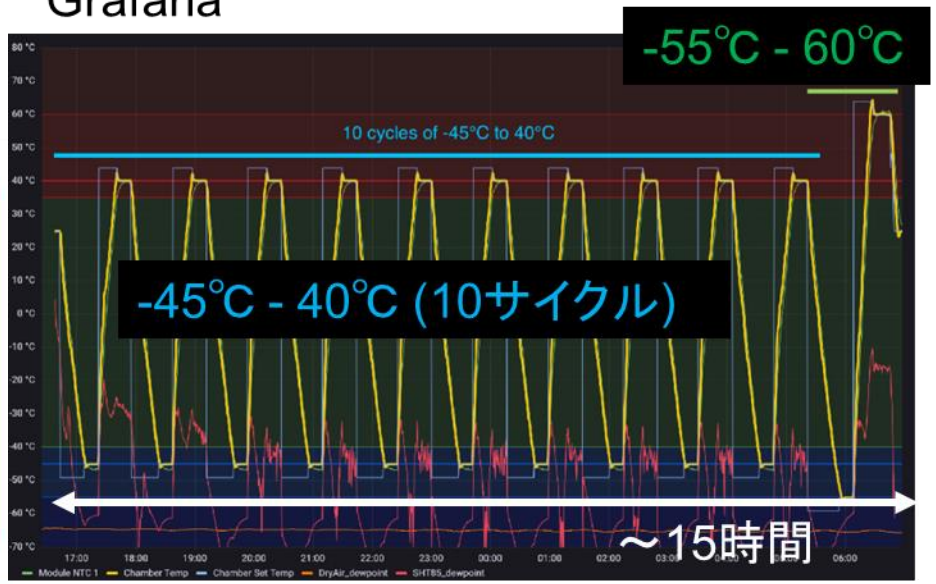
温度サイクルチェンバー



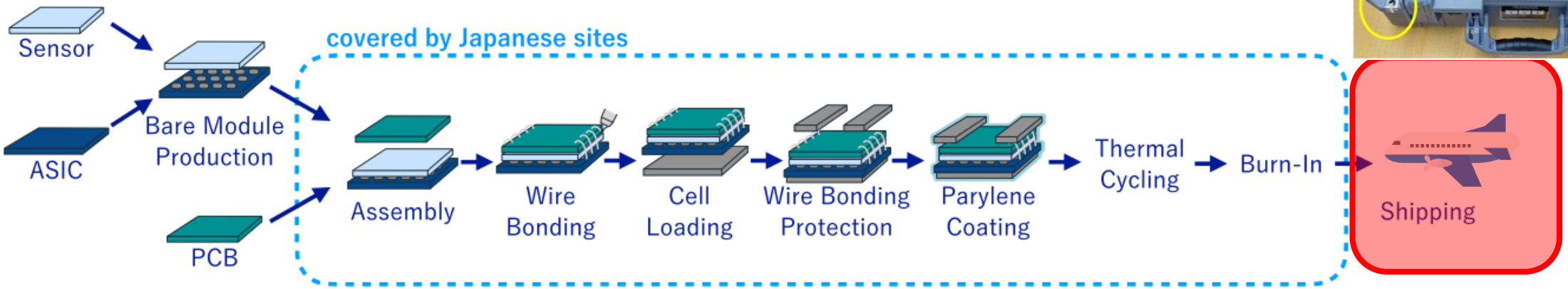




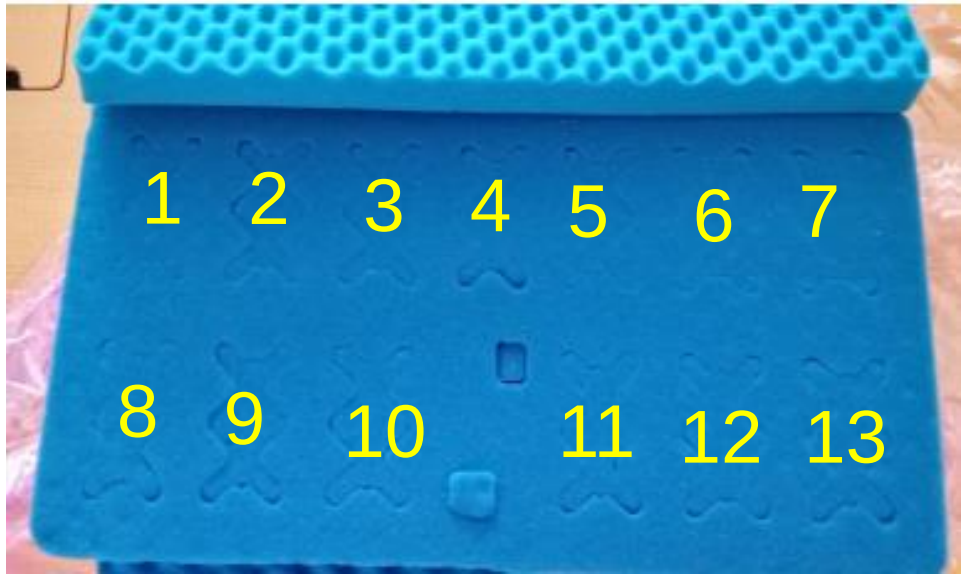
Grafana



Module Shipping



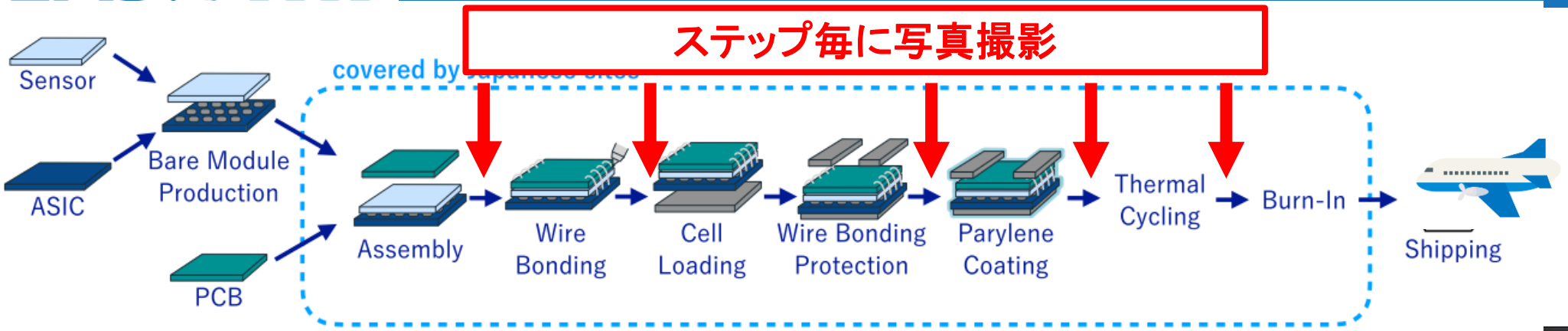
13 moduleの収納可能

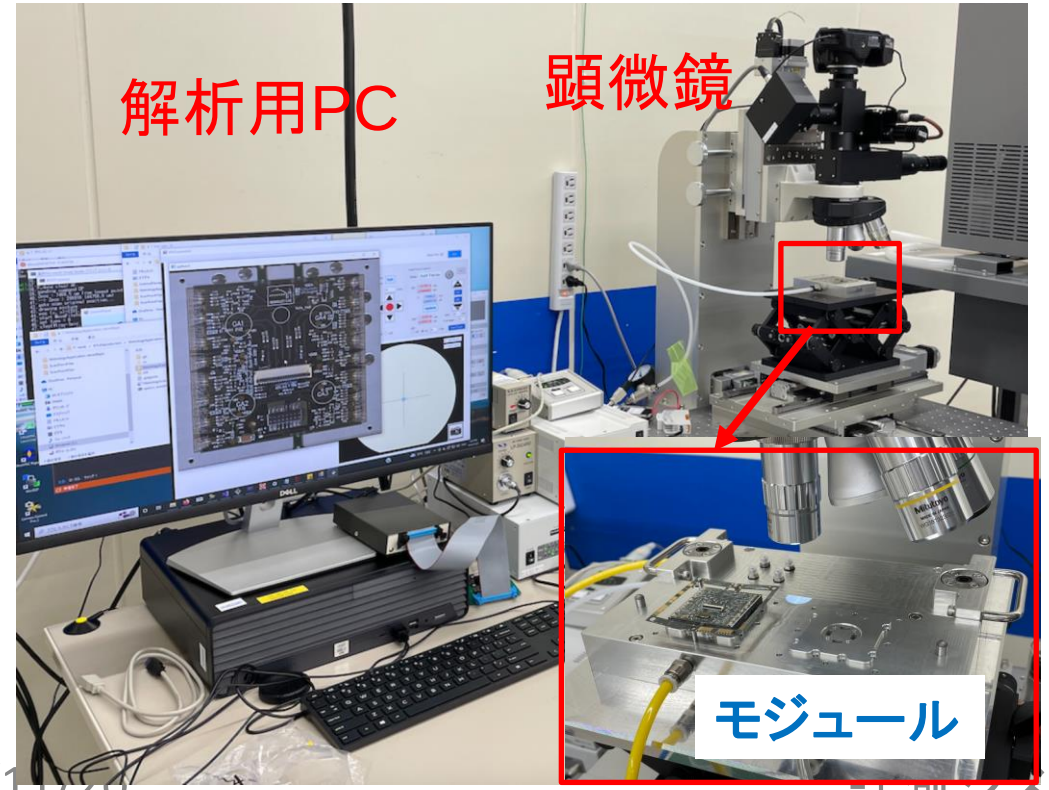


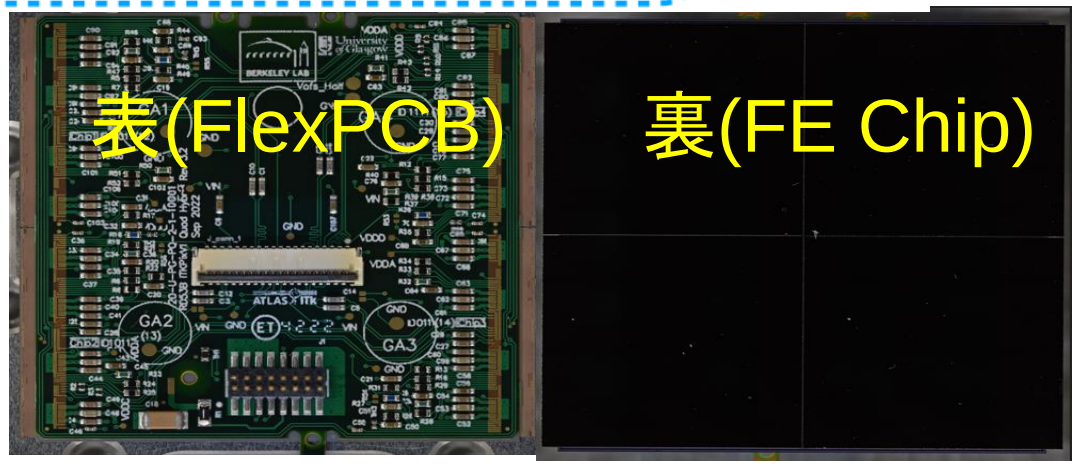
REPICからCERNに着くまでの期間：約1か月
→ (輸送期間)1週間 ＋(手続き期間) 前後1週間
輸送頻度：月１回

- 140 modules/month (7 modules/day)
- 10-11 cases (13 modules /輸送ケース)

Visual Inspection

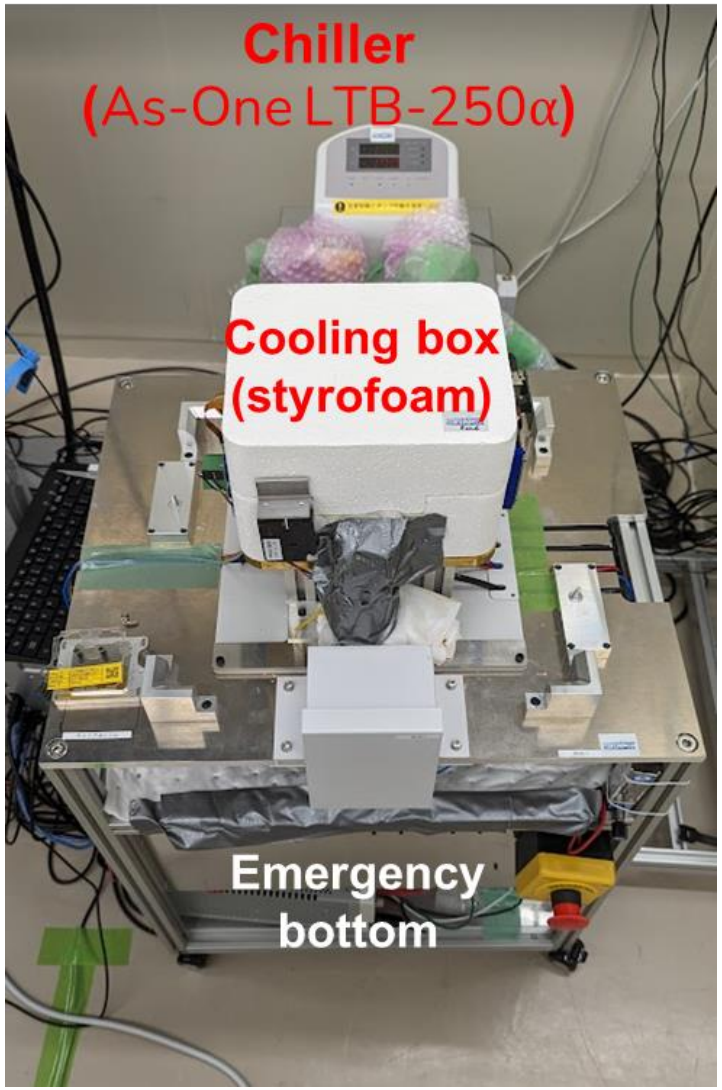


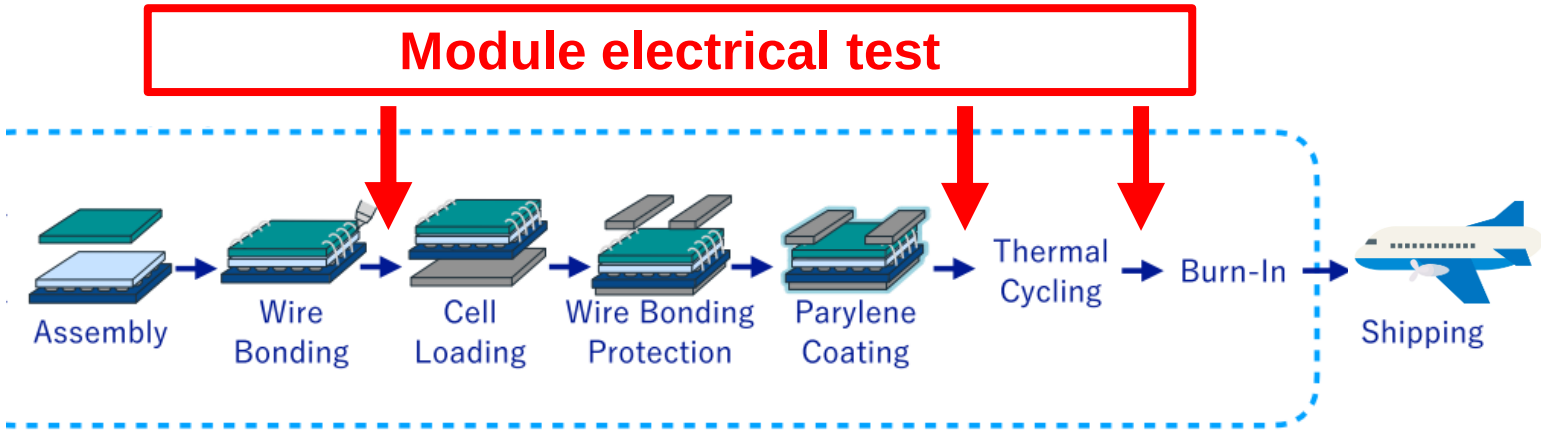




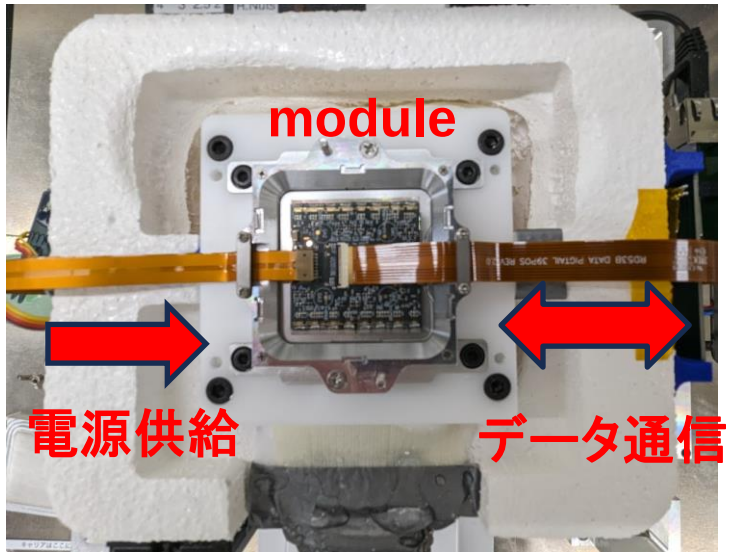
- ✓ モジュールの形状測定(厚さ、幅)
- ✓ モジュールの外部損傷測定
- ✓ Wire bondingの確認

Electrical module test system





Cooling Box中

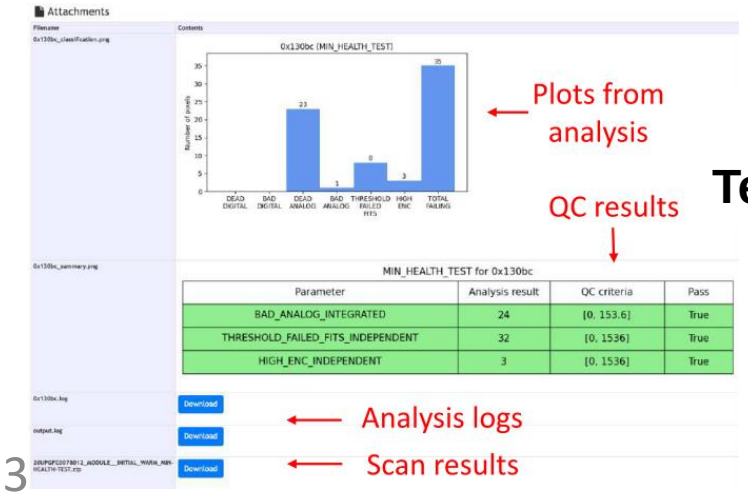


YARR

Module readout system

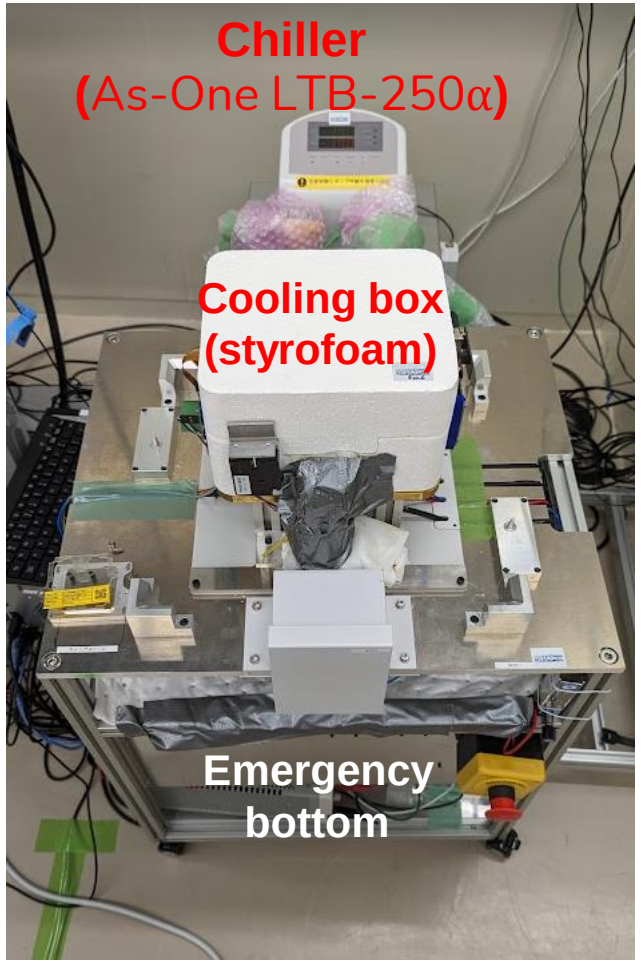
LocalDB

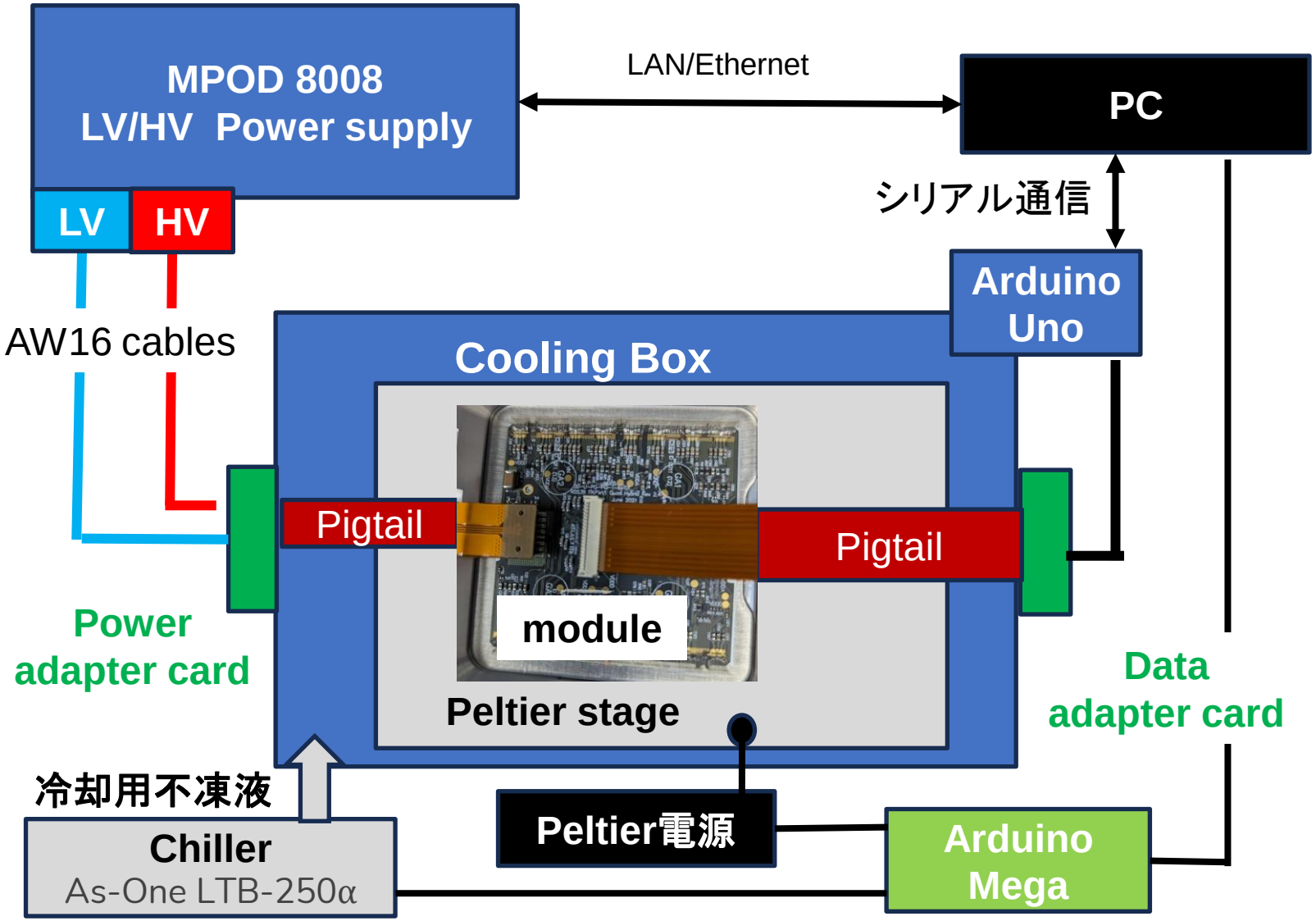
Database



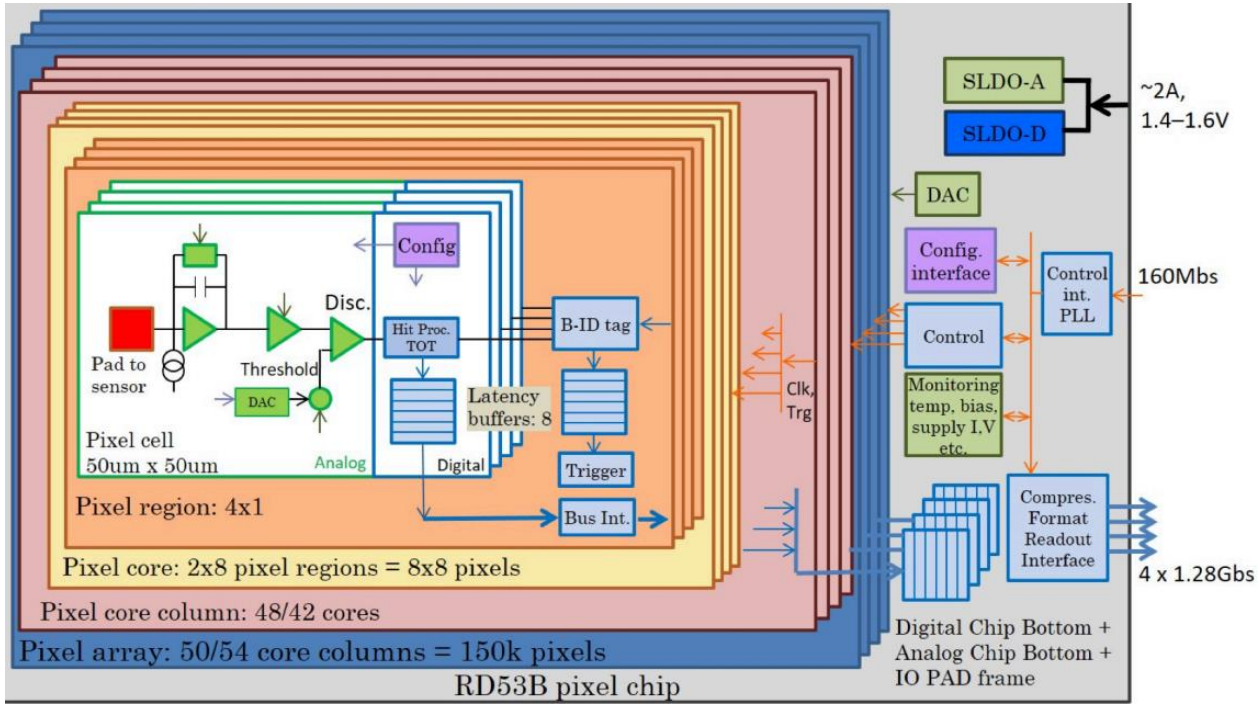
LocalDB
Test results

Electrical module test system





Readout Chip and test environment



ATLAS FE chip

- Chip size : $20 \times 20\ \mathrm{mm}^2$
- Pixel size : $50 \times 50\ \mu\mathrm{m}^2$
- Pixel matrix 400×384
- 152800 pixels per chip
- Data bandwidth 4×1.28 Gbit/s
- Data encoding 64b66b

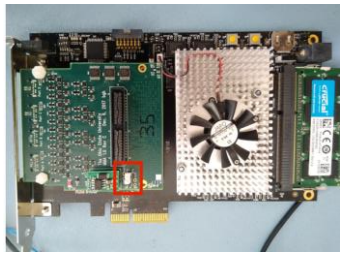
モジュールテスト環境:
電源供給条件(MPOD電源)
LV : I = 5.88 A (定電流), V ~ 2.3 V
HV : V = -80 V (定電圧), I ~ 数10 nA

YARR
Module readout system

Xilinx KC705

FPGA bord

Ohio Multi Module Adapter

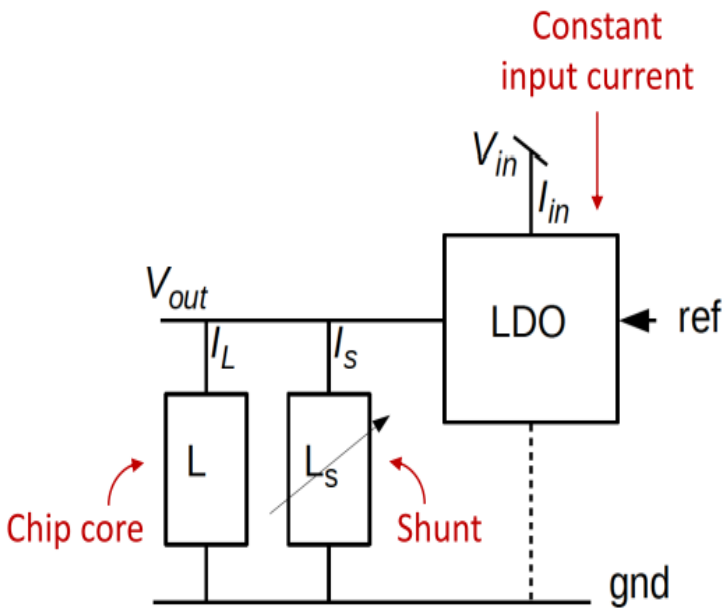


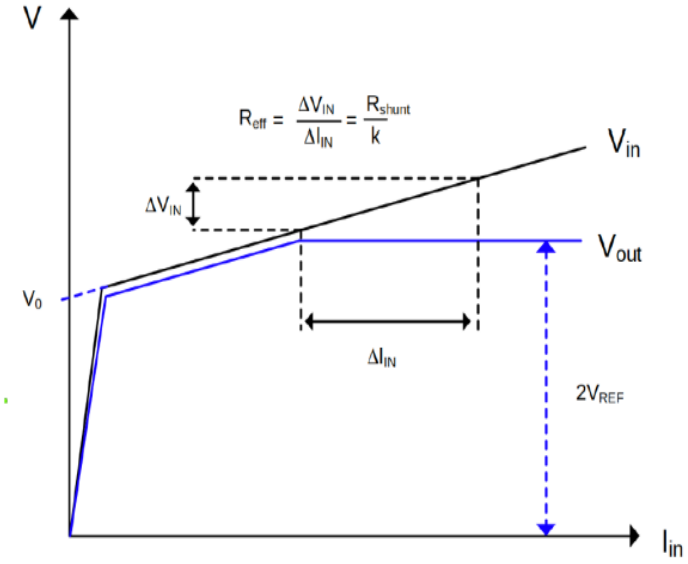
Adapter Cards

Shunt Low DropOut (SLDO) regulator

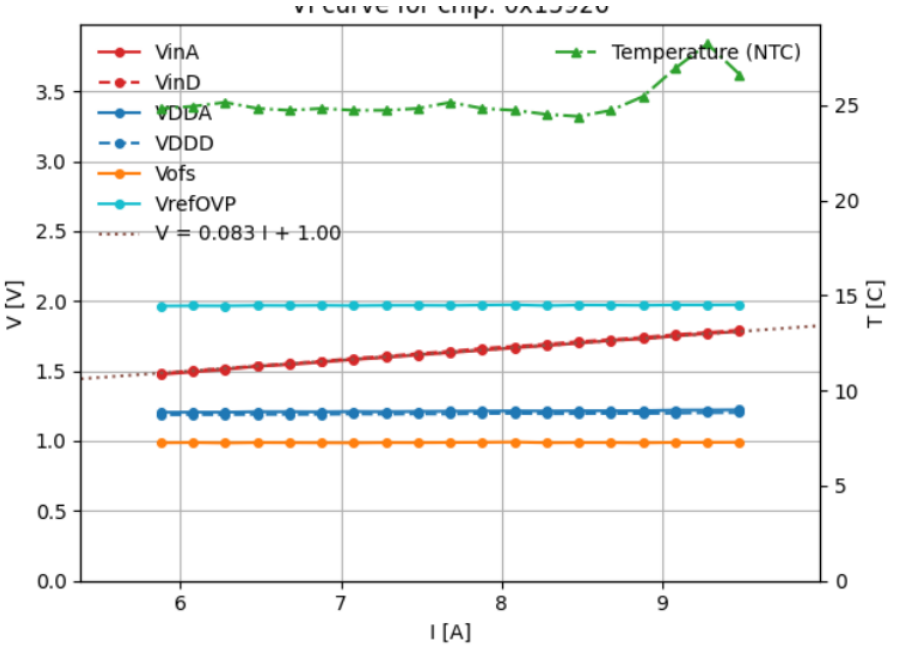
ITk module：Shunt LDOレギュレータ(SLDO)を並列に接続した定電流動作

→ 入力電流を設計値以上に増やせないことで放熱量を抑制



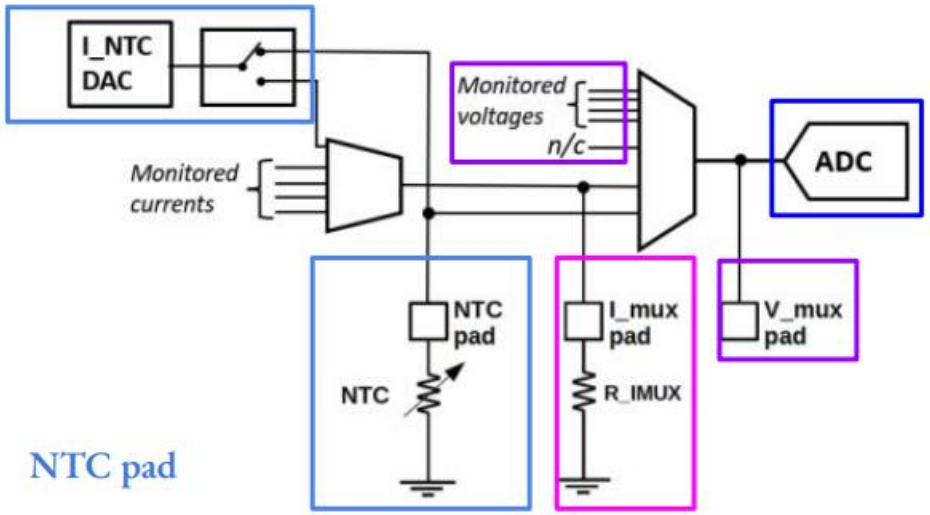


$$I_{in} = I_L + I_s = \frac{V_{in} - V_0}{R_{\text{eff}}} \quad [V_{in} > V_0]$$



Chip sensing and monitoring

電流と電圧のマルチプレクサ(IMUX/VMUX)は ADC の入力に供給
VMUX：25電圧チャンネル (VDDA,VDDD, ….)
VMUX,IMUX, NTC(温度モニター)の出力を確認(Analog readback test)



NTC pad

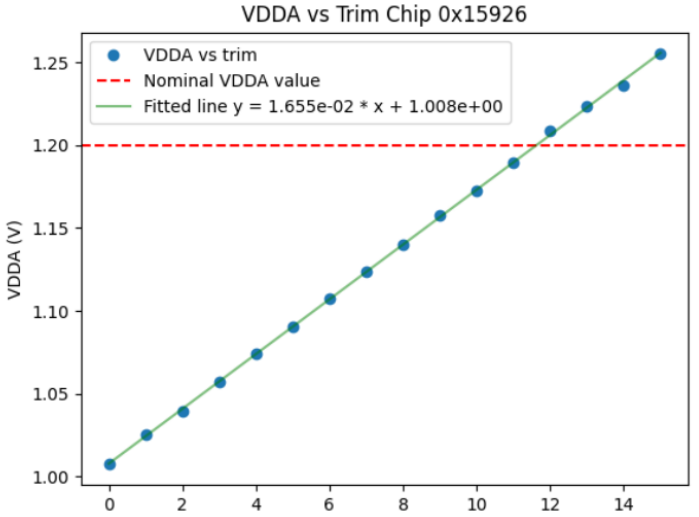
Analog to Digital Converter

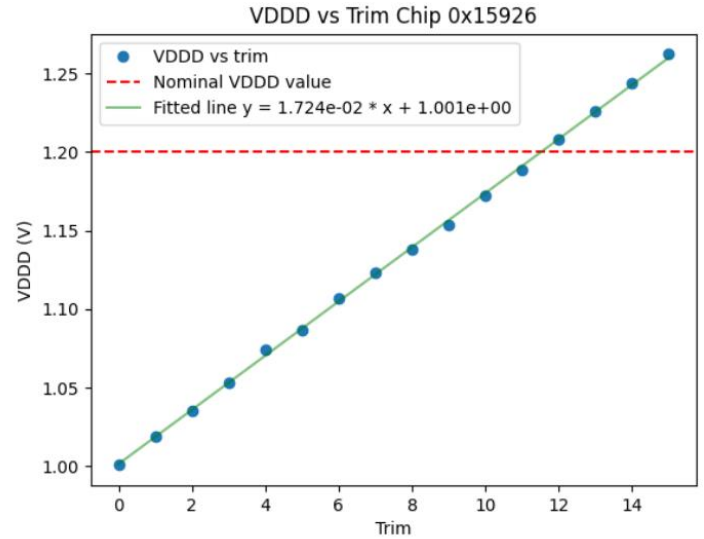
VMUX and VMUX pad

Analog voltage multiplexer

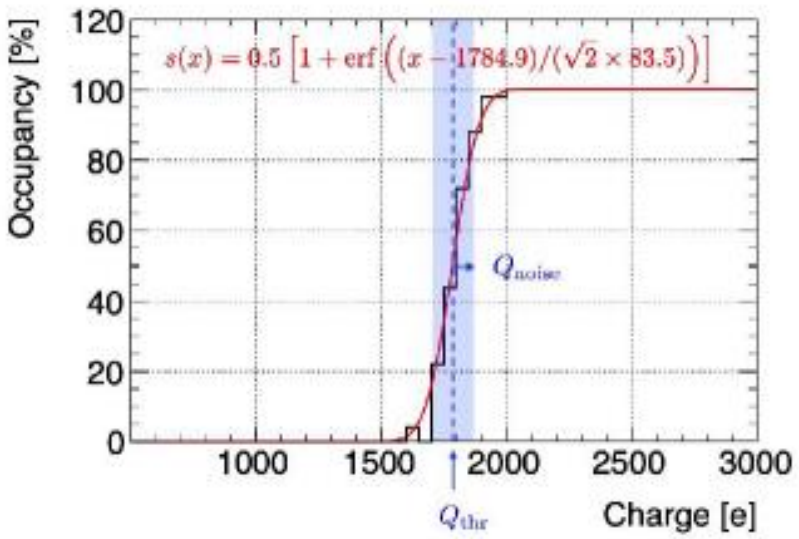
IMUX and IMUX pad

Analog current multiplexer

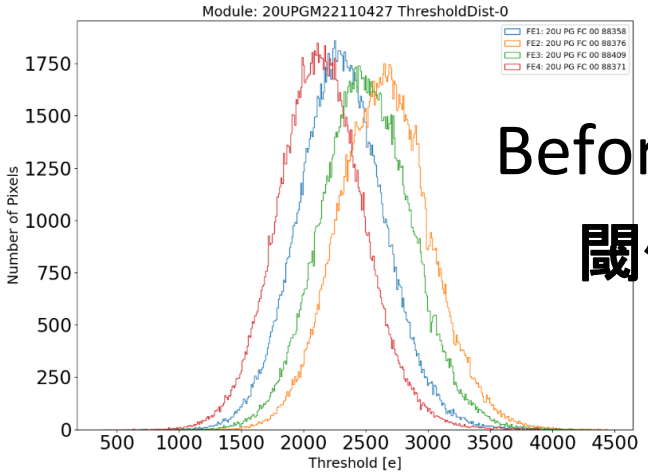




Threshold Tuning and Noise Scan

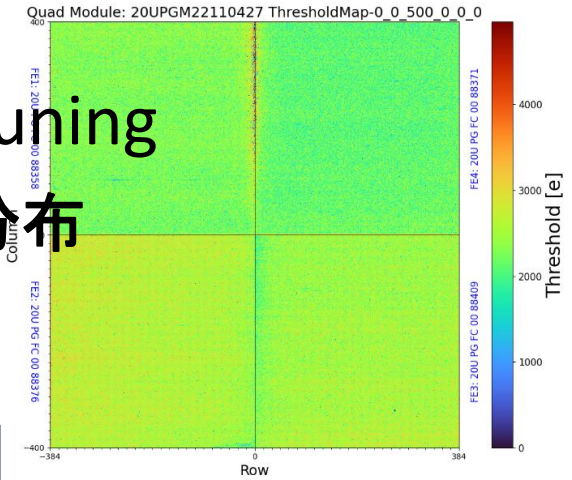


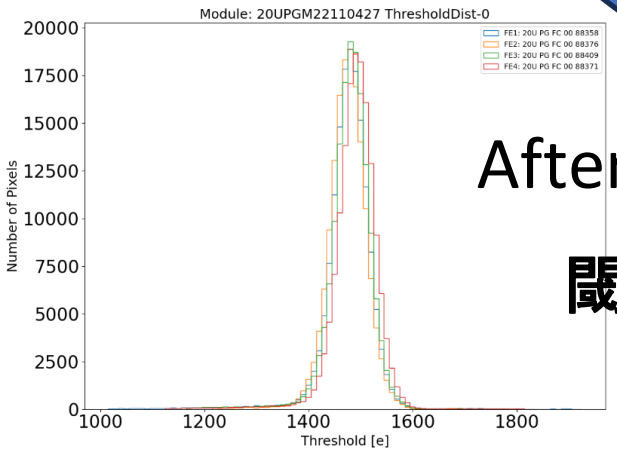
Injection Charge (Q)と応答率の相関分布を(s-curve)フィッテング
→ 中央値から閾値を導出



Before tuning

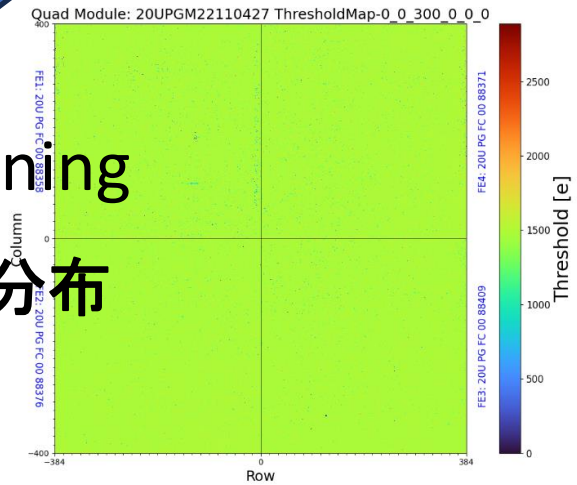
閾値分布





After tuning

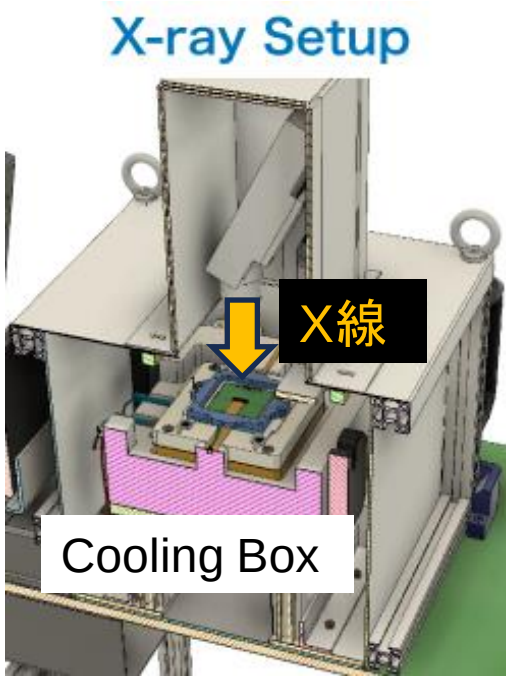
閾値分布



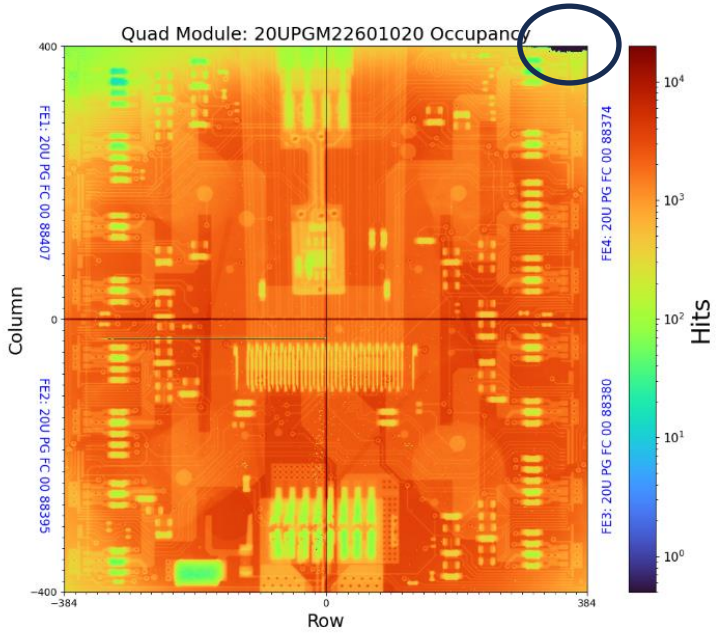
Disconnected/bumped failed Scan

Source scan

X線照射により生じた電荷を測定

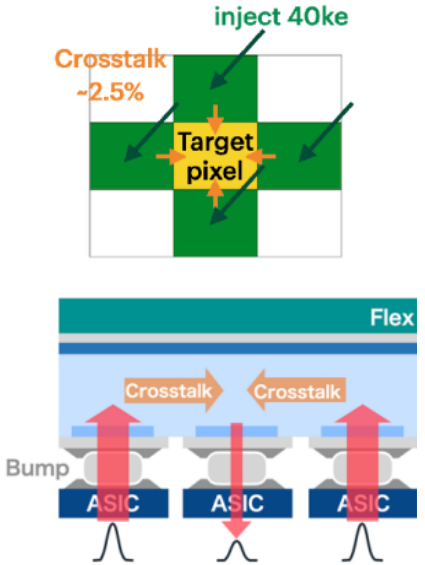


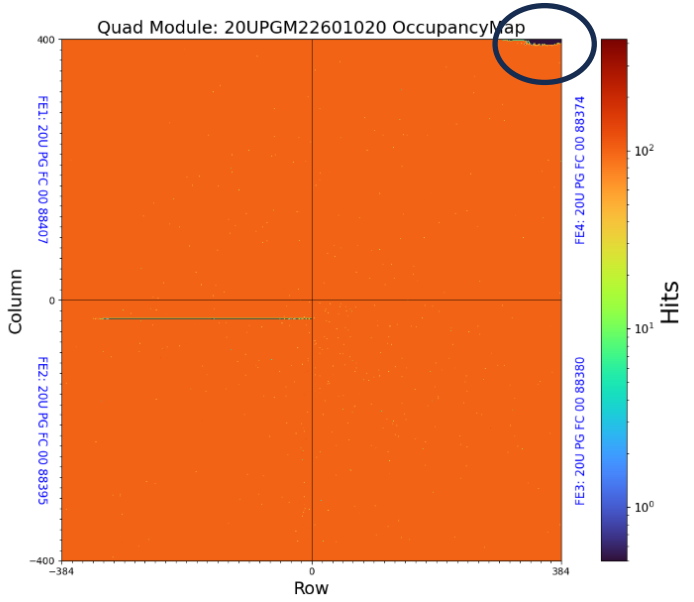
剥がれ



Disconnected bump scan

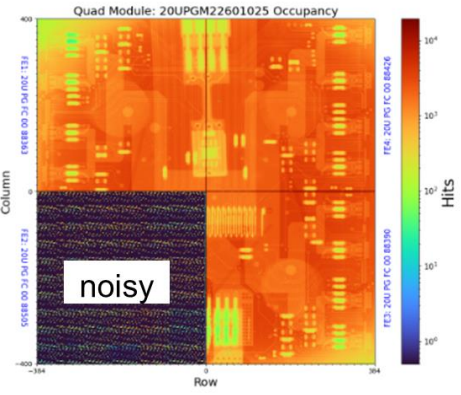
クロストークの性質を利用してバンプ剥がれを評価

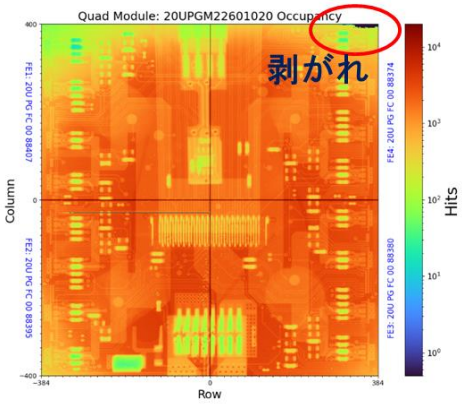


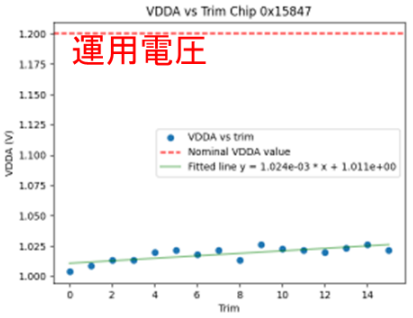


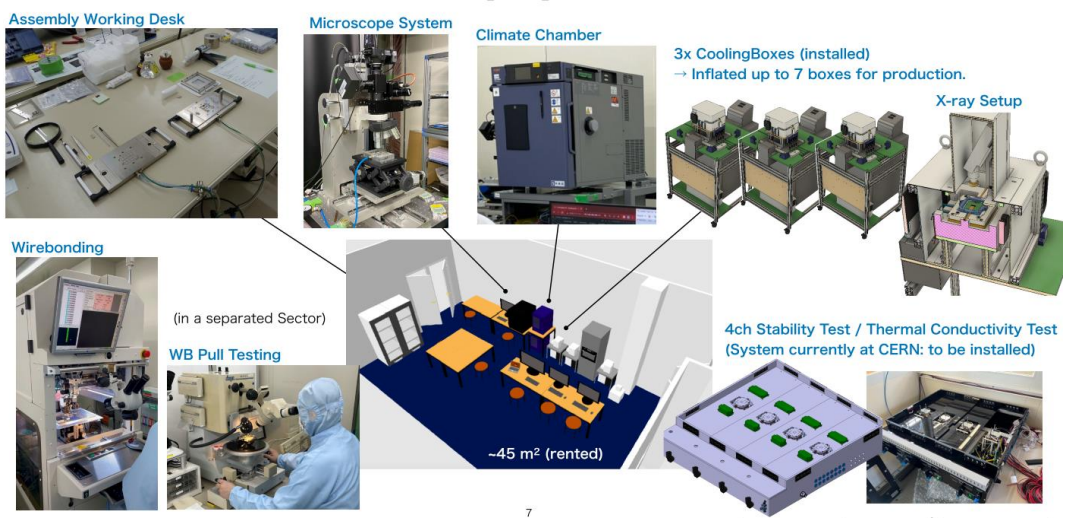
Issue for ITk mass production

- 生産レート(7 modules/days)
  - 時間的制約 (9時～17時 : 計8時間)
    - Electrical test = 1 module ~3時間 × 2 (25℃/−15℃) ×3回 > 8 時間
    - Wirebonding+ pull test = 2~3時間/module × 7 module/days > 8時間
    - Visual inspection(写真撮影＋解析) :ステップが多く7module/daysは厳しい
  - 作業スペースの制約($45\mathrm{m}^2$)
    - CoolingBox (electrical test system) : 3 → 7
- Module Failed (~10/80 modules)







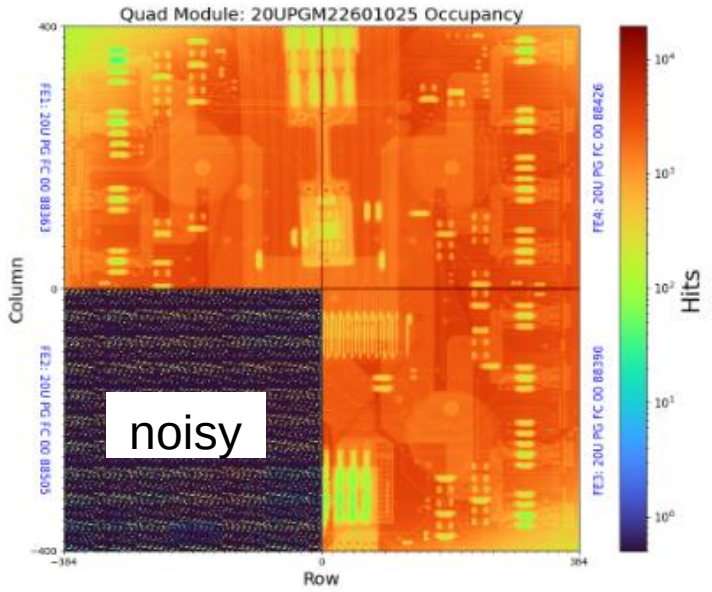


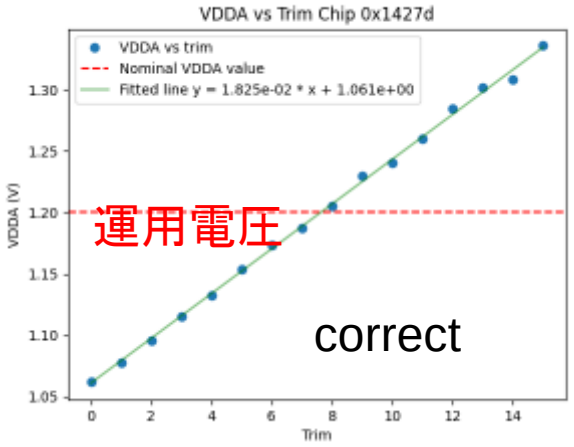
Conclusion

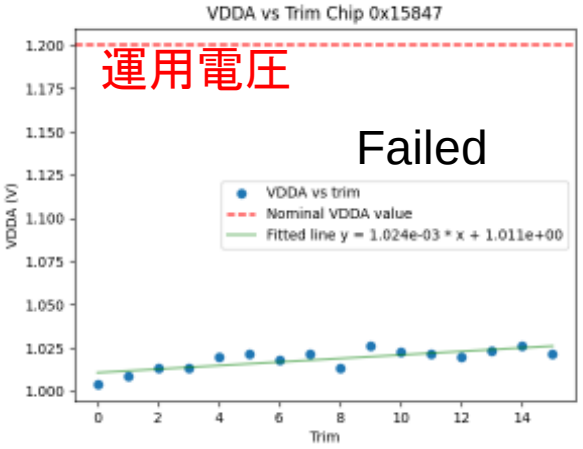
- 加速器の大型改造(HL-LHC)に向けて内部検出器をアップグレード(ITk検出器) →日本グループは2200モジュールを製造予定。
- ITk productionに向けて林REPICで生産ラインを確立→Pre-Productionでのモジュール生産の着手開始
- AssembleからElectricalテスト,thermal cycleのテスト環境は整っている
- 生産レートを向上に向けてCoolingBoxの増設、およびプロダクションサイトの増設(KEK,九州大、阪大 etc.)

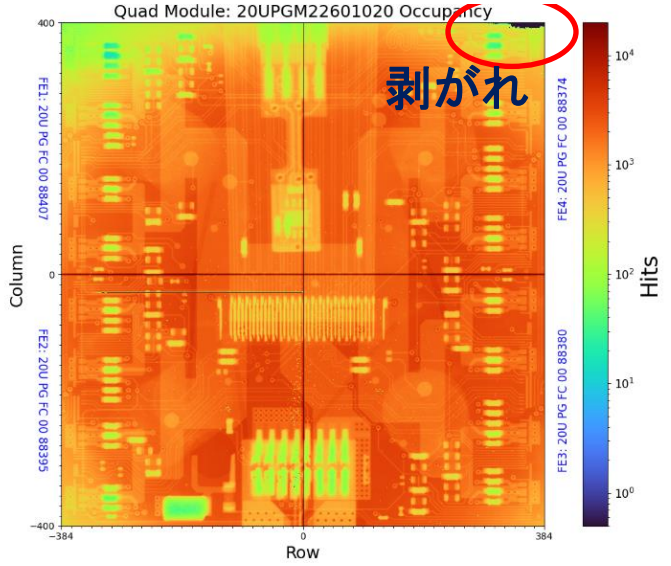
backup

Failed modules









1割ぐらいのモジュールがelectrical testで失敗

- DAQシステムがまだ不完全
- Module起因か読み出しの問題か？

Hayashi REPIC bottlenecs

- Quantity of the assembly jig determines the production rate.
  - At present only 1 kit present → 1 modules / day w/o cooling block
  - Arrival of jigs for cooling block assebmly + WB protection expected in Oct → 3 modules / day.
- **Wirebonding** may become a bottleneck for producing 7 modules / day.
  - Takes ~3 hours for sum of (WB + pull test) per module.
    → May speed-up by 20% with experience.
  - Mitigation: dropping the pull test will help.
  - For pre-production (3 modules / day), this is not a bottleneck.
- The Microscope system (visual insp., metrology) will **likely** become a bottleneck for supporting 7 modules / day.
  - Mitigation: Demanded lighter photo-taking system (by a camera: in development) for unloading some fraction of tasks.
- The climate chamber is likely **not** a bottleneck, assuming hosting 8 modules at once.
  - We have a spare: possible to use 2nd climate chamber if this is needed.

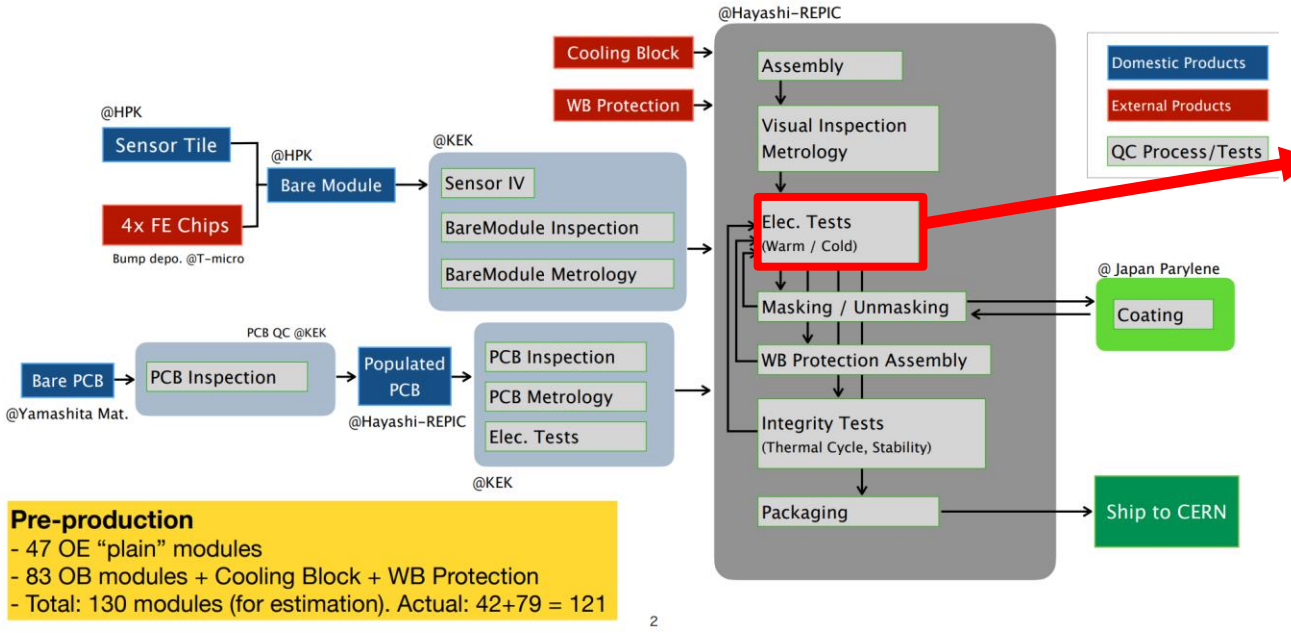
Hayashi REPIC bottlenecs2

- The electrical testing system (CoolingBox) **is a bottleneck for Pre-production**.
  - Already installed 3 boxes, fully asynchronous operation (debug time loss minimized).
  - Turned out that allocating **1 box / module / day is insufficient** for the entire pre-production menu.
  - Even with the best case scenario (100% duty factor), most likely needing to commission additional boxes (ultimately 7 boxes in total).
    - Parts were already prepared, but **power/data boards are short**.
- **Separate stability testing system** is needed to avoid bottleneck.
  - System is currently at CERN. Its assembly recently completed, but commissioning and qualification needs to come after its arrival at Japan in October. Realistic starting of opearation not before December.
  - Is the additional 20h stability test (on top of ~30h of nominal testing) really **gaining anything**?
- How many CoolingBoxes are needed for supporting 7 modules / day production operation in order to avoid bottleneck **strongly** depends on the **final menu** of electrical testing.
  - We are very close to getting to the resource limit (room areas).
  - Should carefully build-up the testing time against its merit.
- The allocated (rented) clean room area (~45m^2) can become a bottleneck.

Electrical QC Test

3~4 hour testing × 2 cycle (warm/cold)

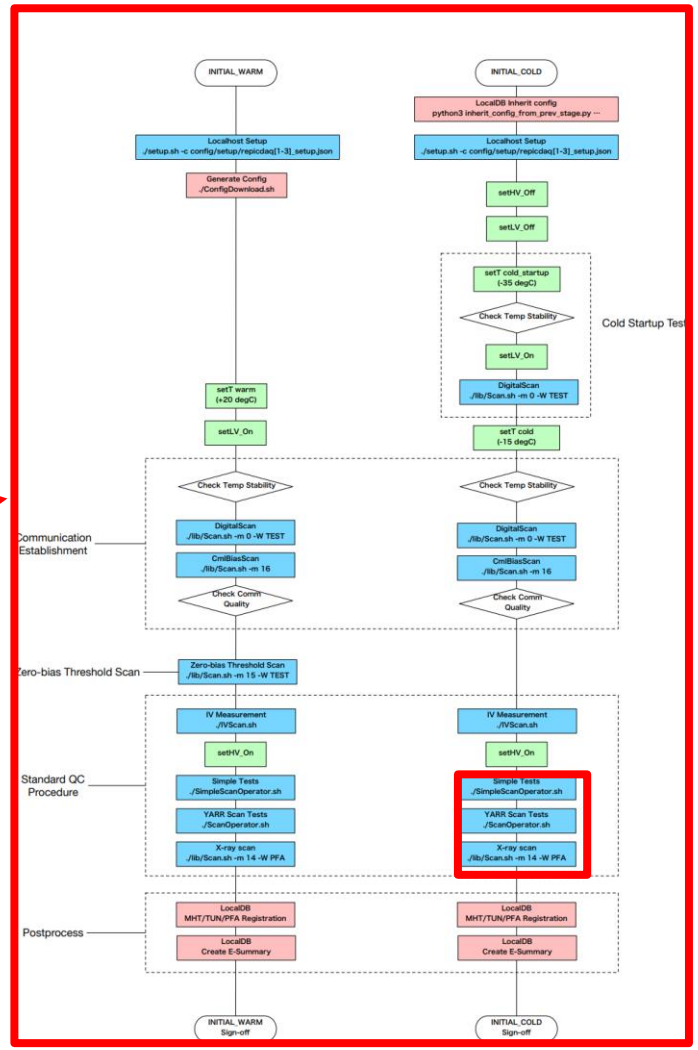
Pre-production Flow / Organization in Japan



Pre-production
- 47 OE "plain" modules
- 83 OB modules + Cooling Block + WB Protection
- Total: 130 modules (for estimation). Actual: 42+79 = 121

2

Electrical QC Process

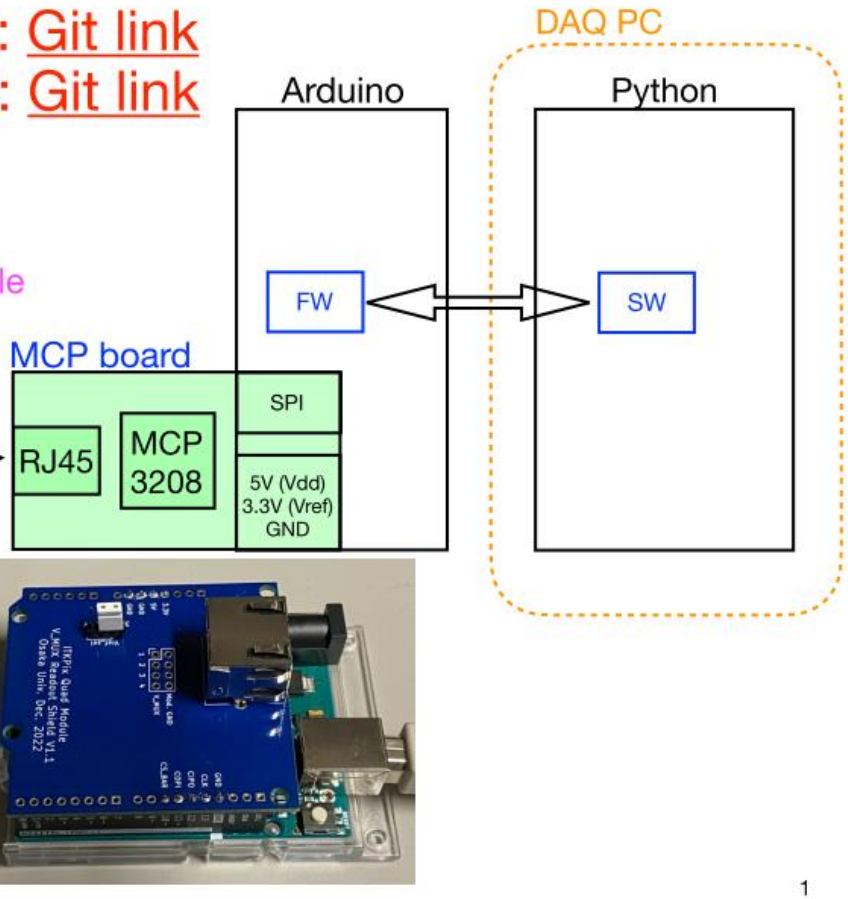


Backup

MUX Readout system

MUX Readout @ REPIC

FW&SW: Git link
Board: Git link



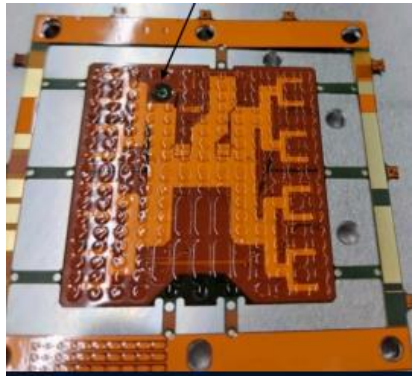
1

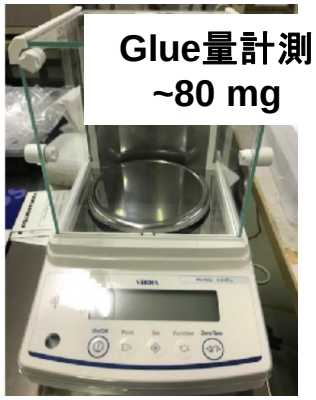
Module Production (assemble)

1. Glueの貼り付け

Glue
Araldite 2011 (epoxy)

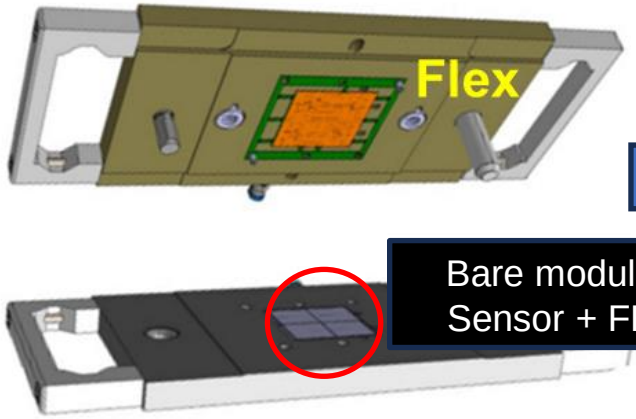
Flexの裏面にGlueを貼り付け

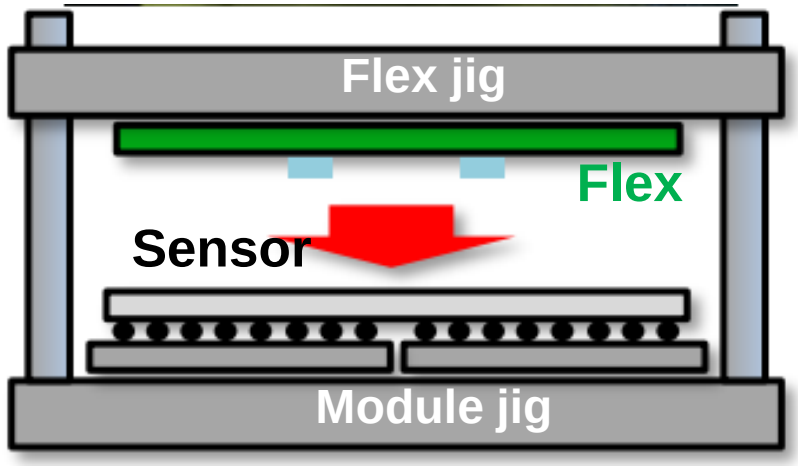




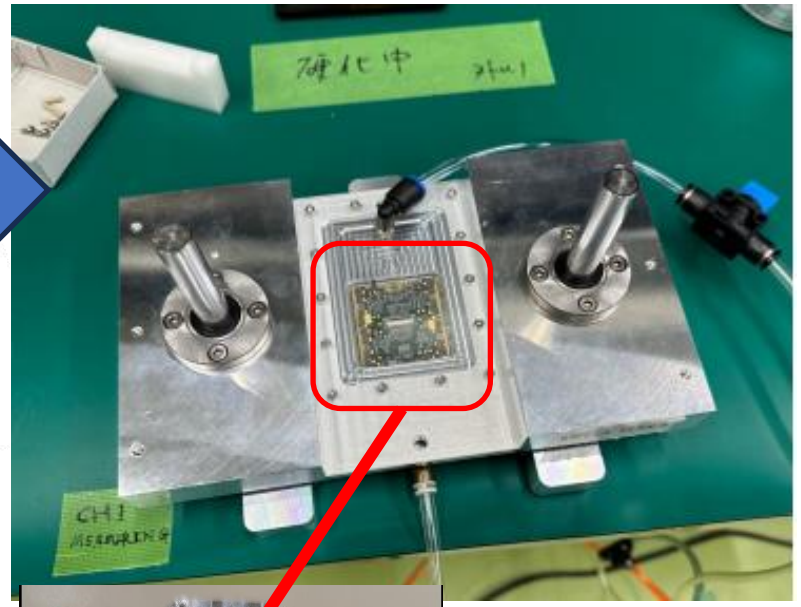
Glue量計測
~80 mg

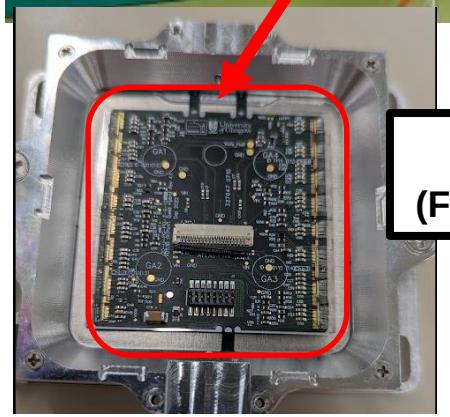
2. 接着





3.硬化





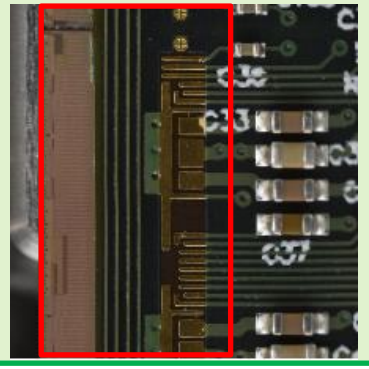
Module
(Flex + BareModule)

Wire bonding Process

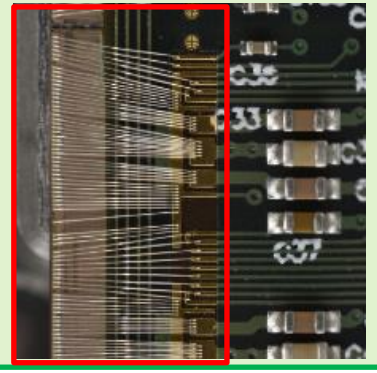
Wirebonding

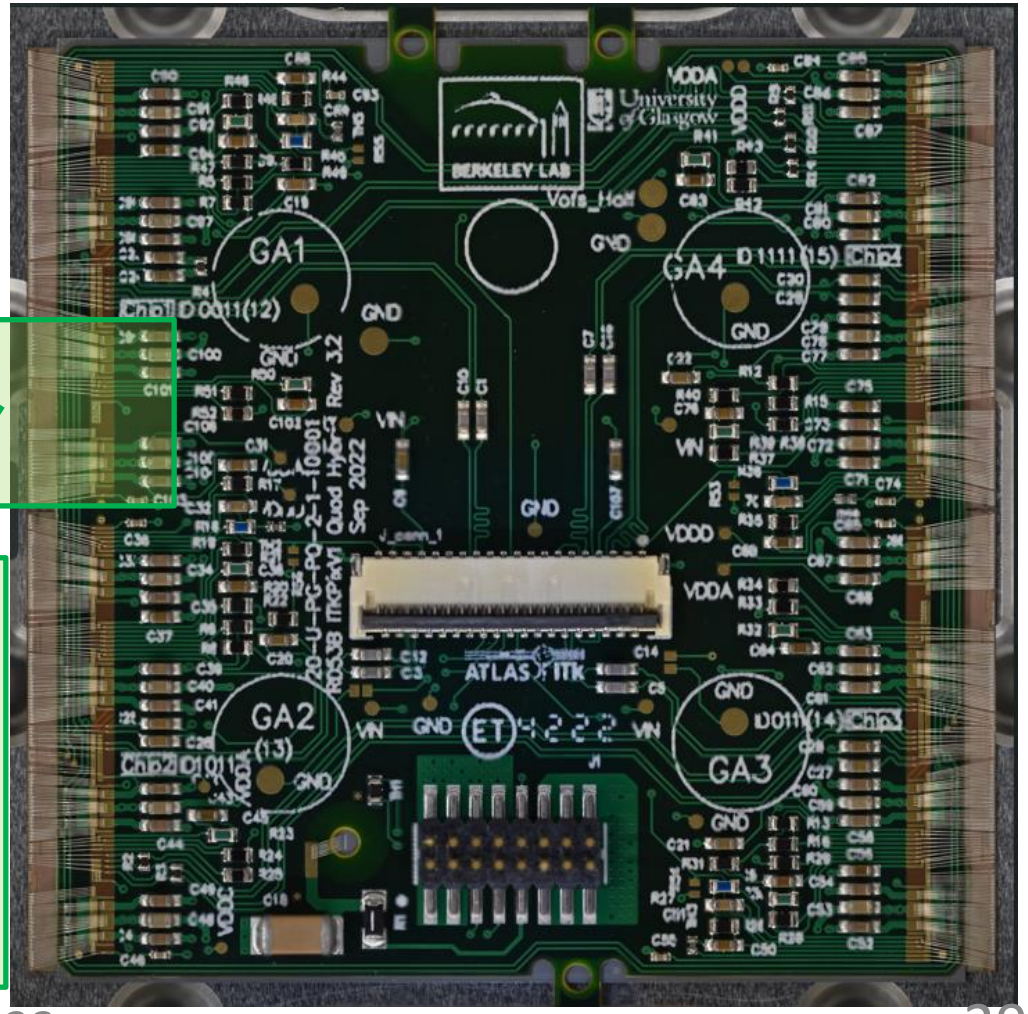
WB Pull Testing

Wier bonding前



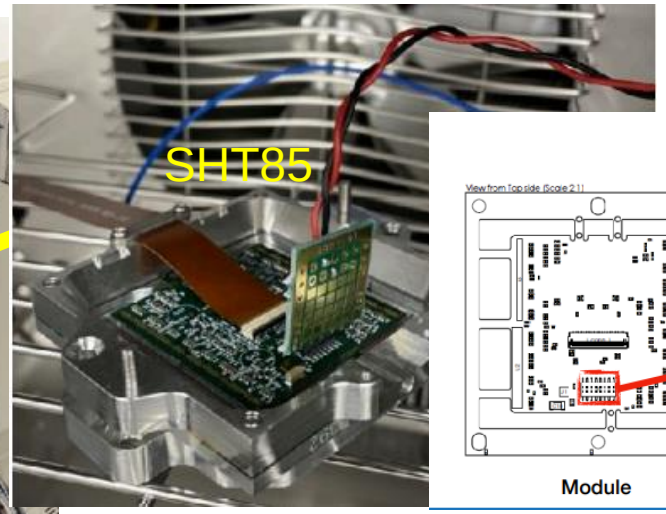
Wier bonding後

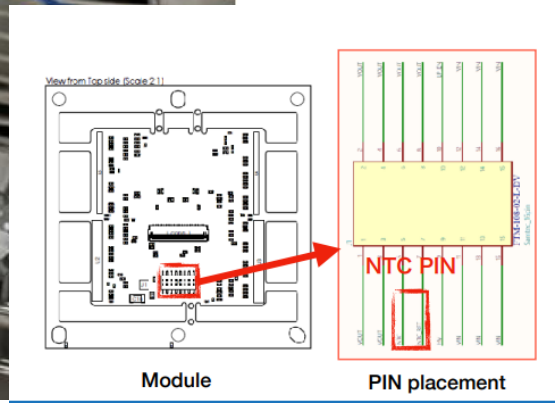




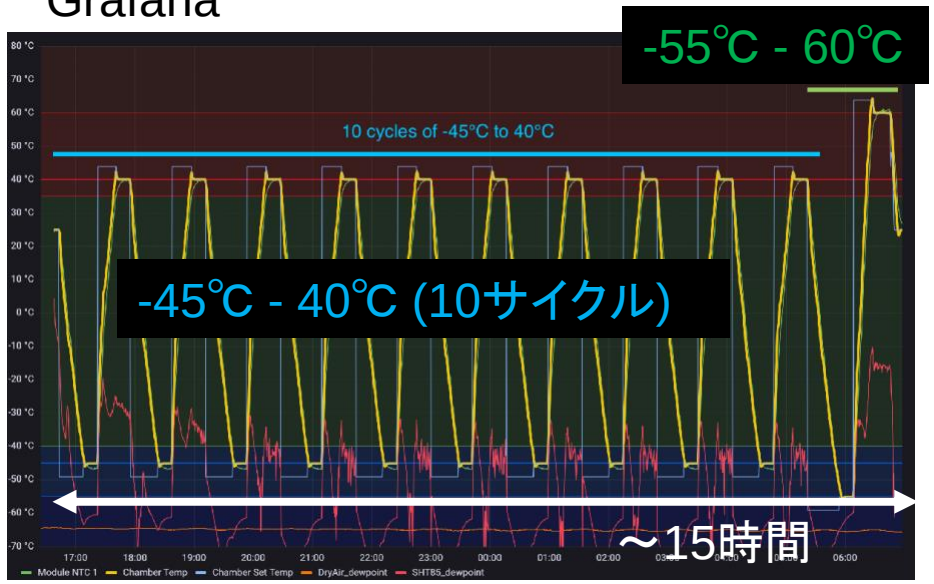
Thermal cycle

温度サイクルチェンバー





Grafana

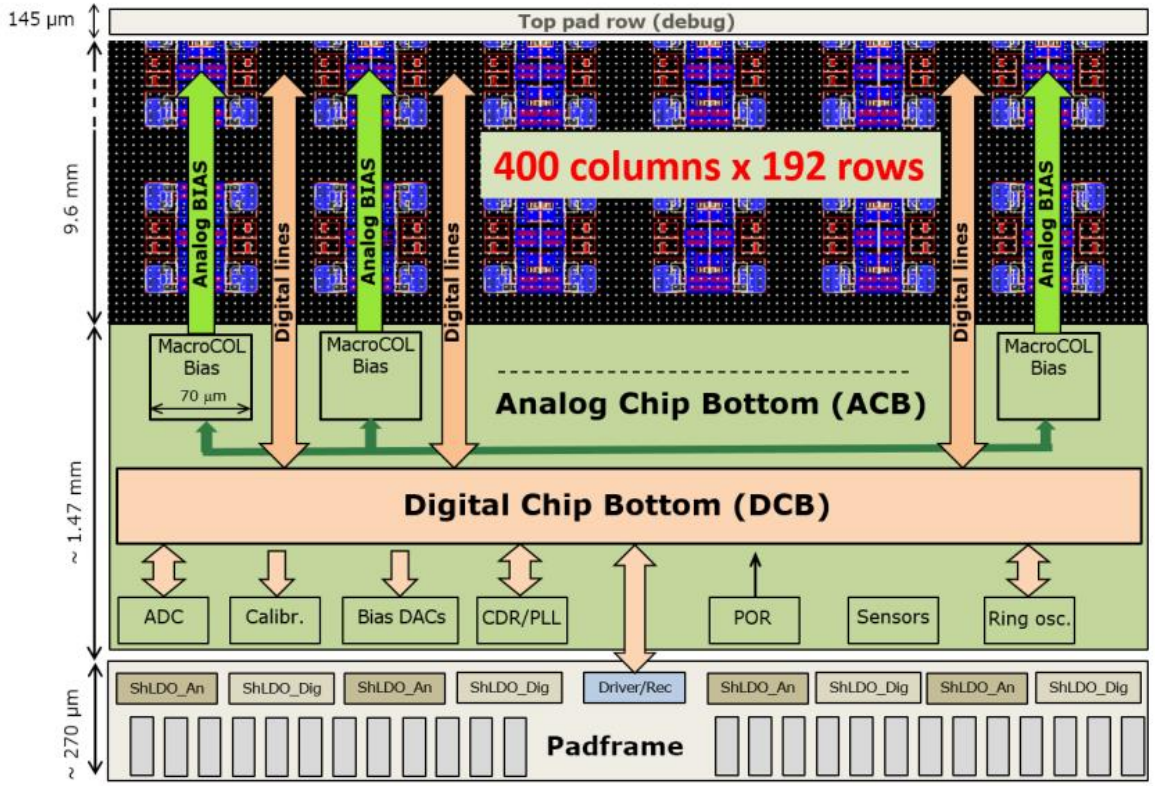


現pixel検出器は~ – 35℃で運用(漏れ電流抑制)、

NTC電圧(V_{NTC})を測定

Steinhart-Hart式により温度値に変換

Electrical QC test



ATLAS FE chip

Chip size : $20 \times 20\ \mathrm{mm}^2$

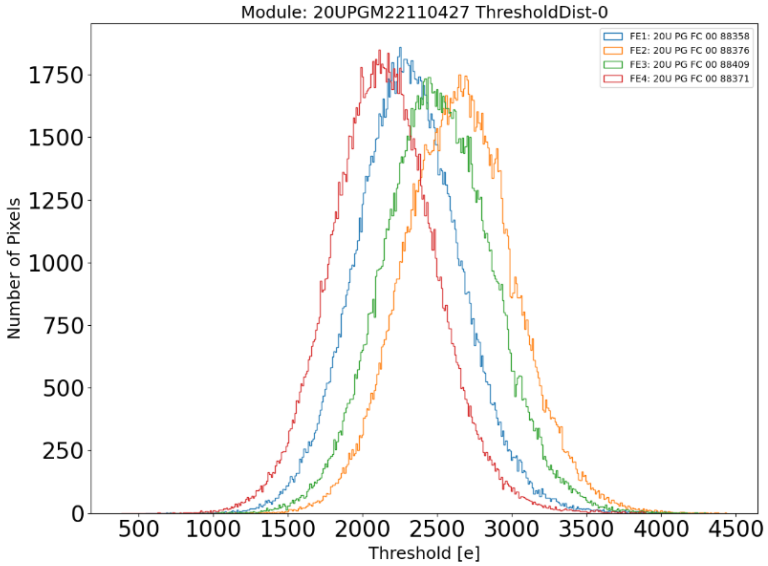
Pixel size : $50 \times 50\ \mu\mathrm{m}^2$

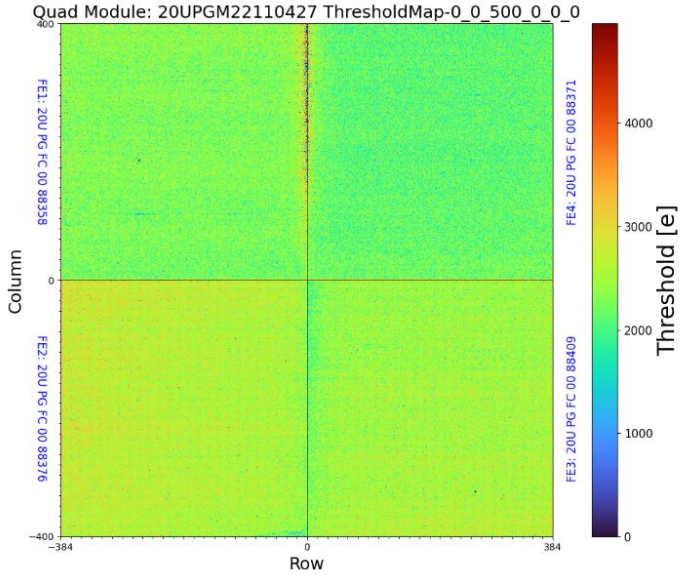
Pixel matrix 400×384

Data bandwidth $4 \times 1.28\ \mathrm{Gbit/s}$

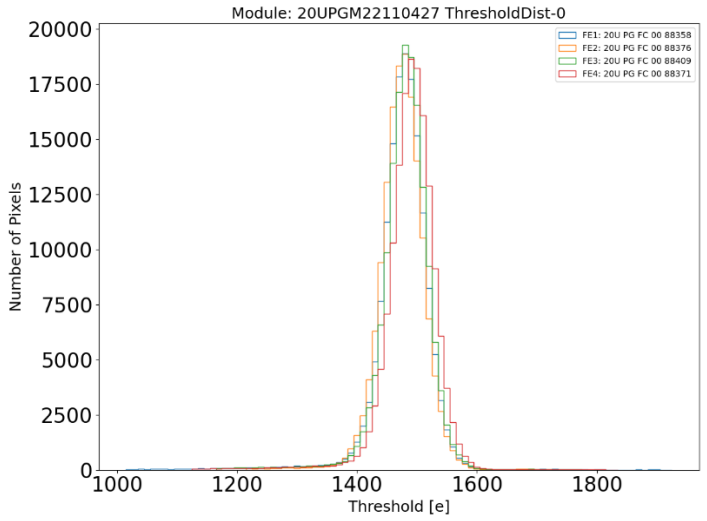
Data encoding 64b66b

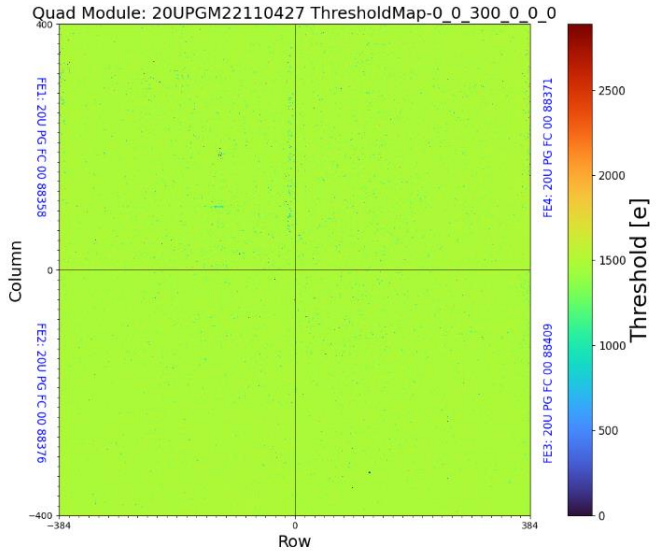
Threshold Tuning and Noise Scan





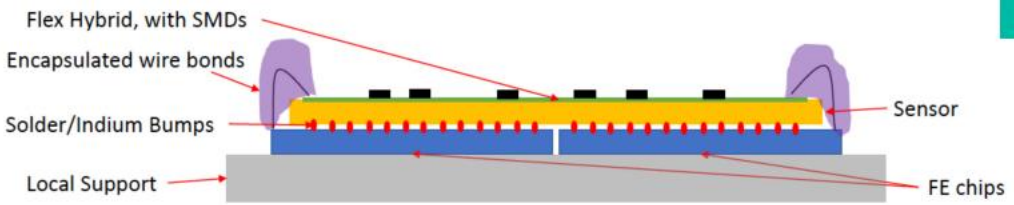
Before tuning

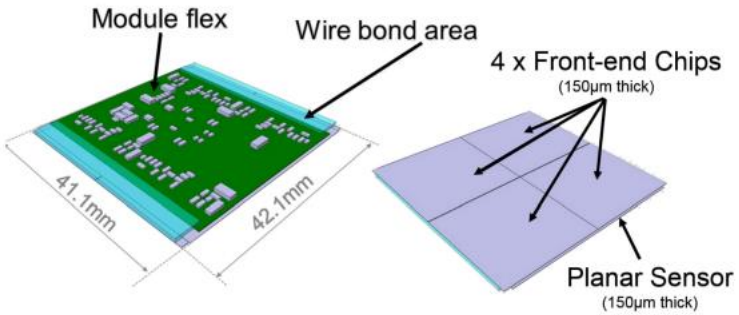


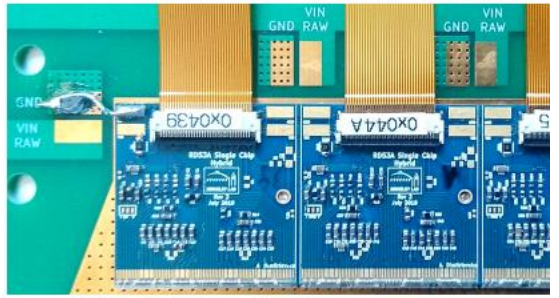


ITk module

- ~ 10000 modules needed for ITk
- L0: triplets for barrel (linear) and ring (round)
- L1-4: common quad modules everywhere
- Module flex PCB designs being finalised
  - Quad PCB: 3 copper layers at ~250 μm thickness







Linear RD53A triplet module

First ITkPixV1 digital quad module on proto

ITk module

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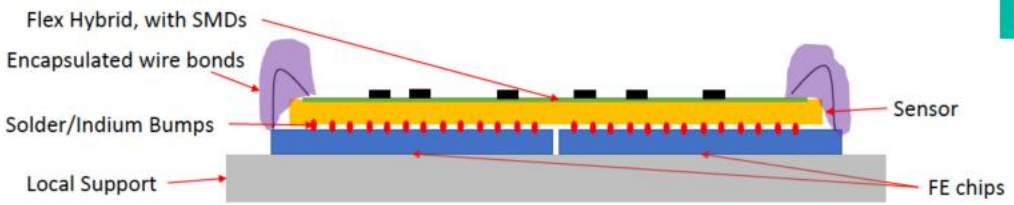

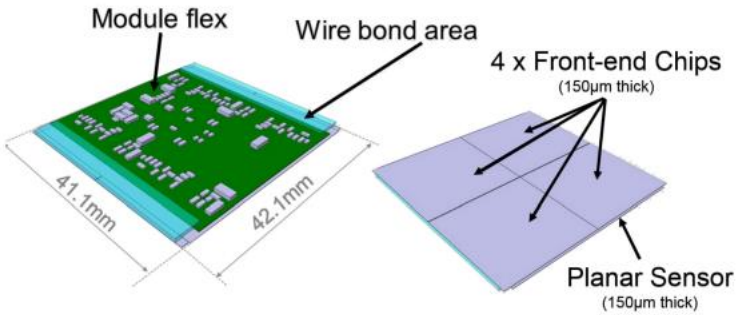

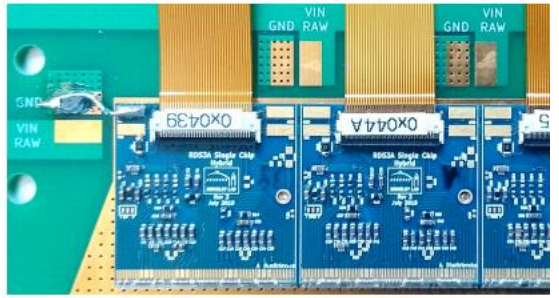

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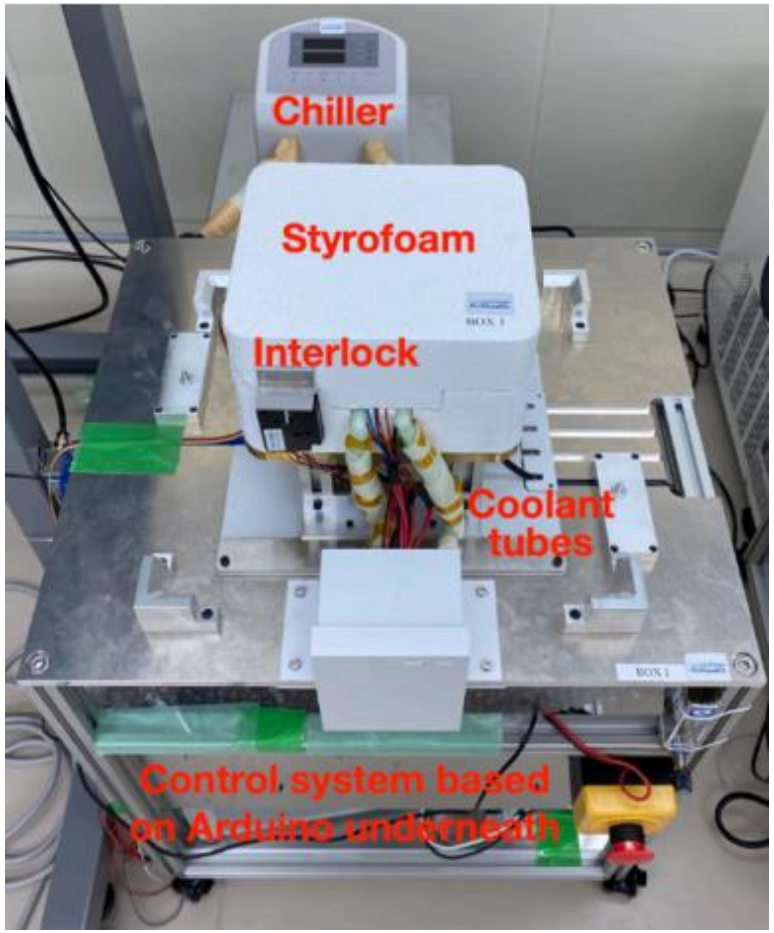
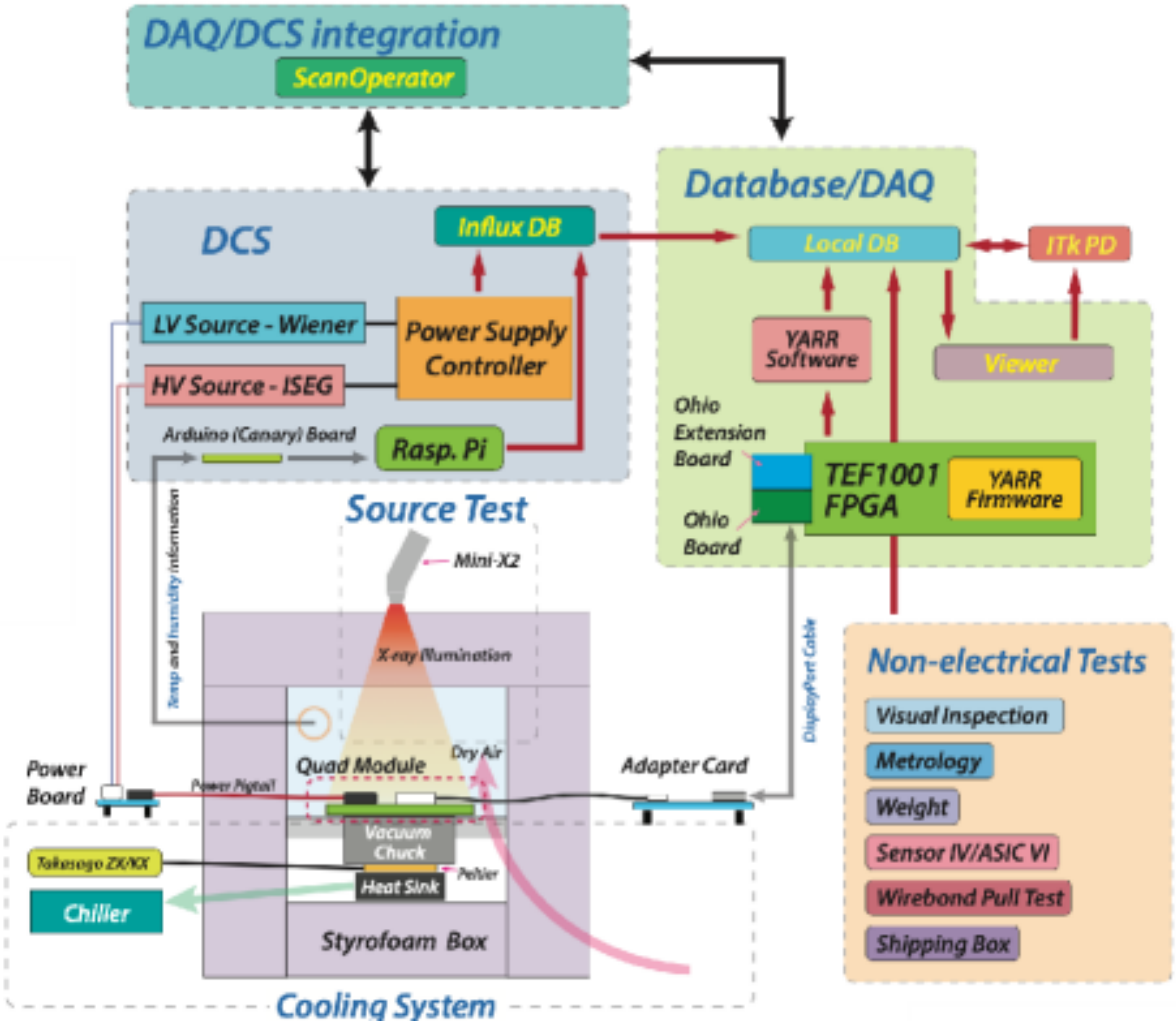
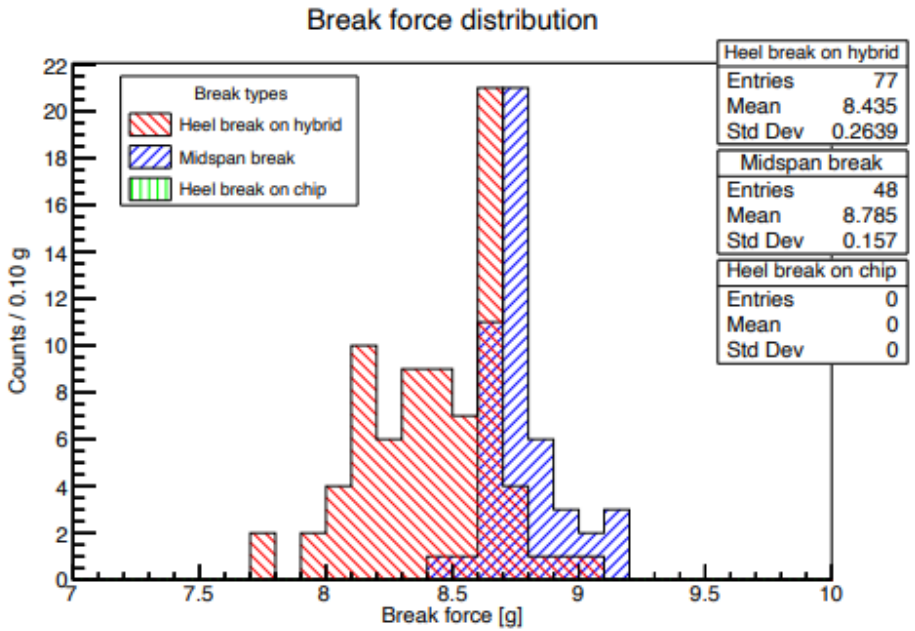
Electrical QC test





Pull test

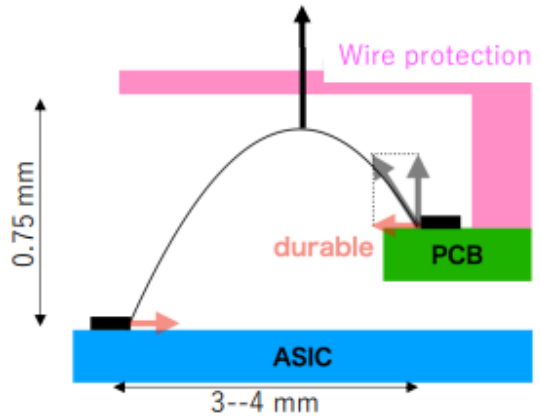
Pull tests



- Each break force > 5 g at least
- Mean break force > 8 g
- StdDev < 15%

→ All satisfied

(Note)
Almost half of break type was wire break …
However it's reasonable considering the low wire height of < 600 um with the pad distance of 3—4 mm.
(discussed in Flex Attach meeting on 23/May)



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