連続読み出しHigh-Resolution TDCの現状とその先

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Toward trigger-less data-streaming DAQ system

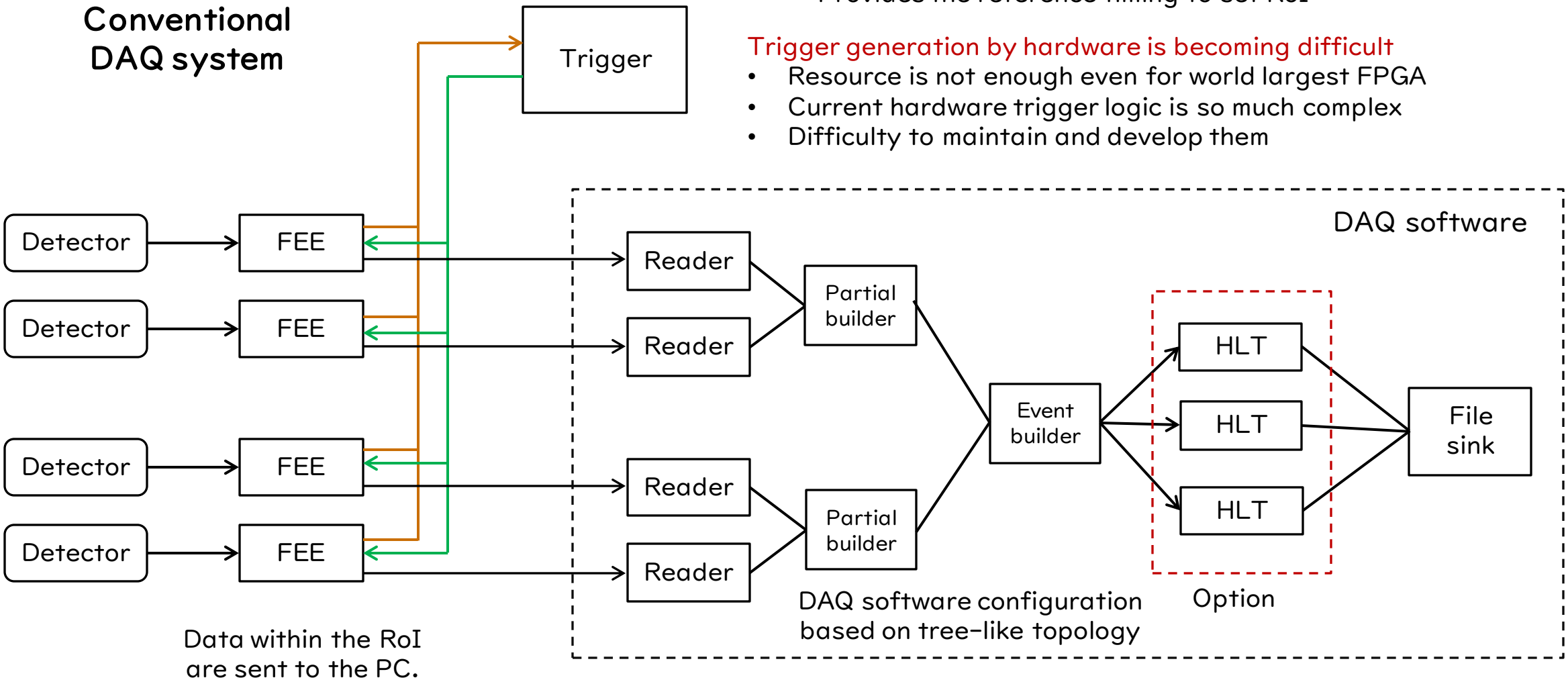
Conventional DAQ system

Event selection by hardware based trigger

- Define a data block, “Event”
- Provides the reference timing to set RoI

Trigger generation by hardware is becoming difficult

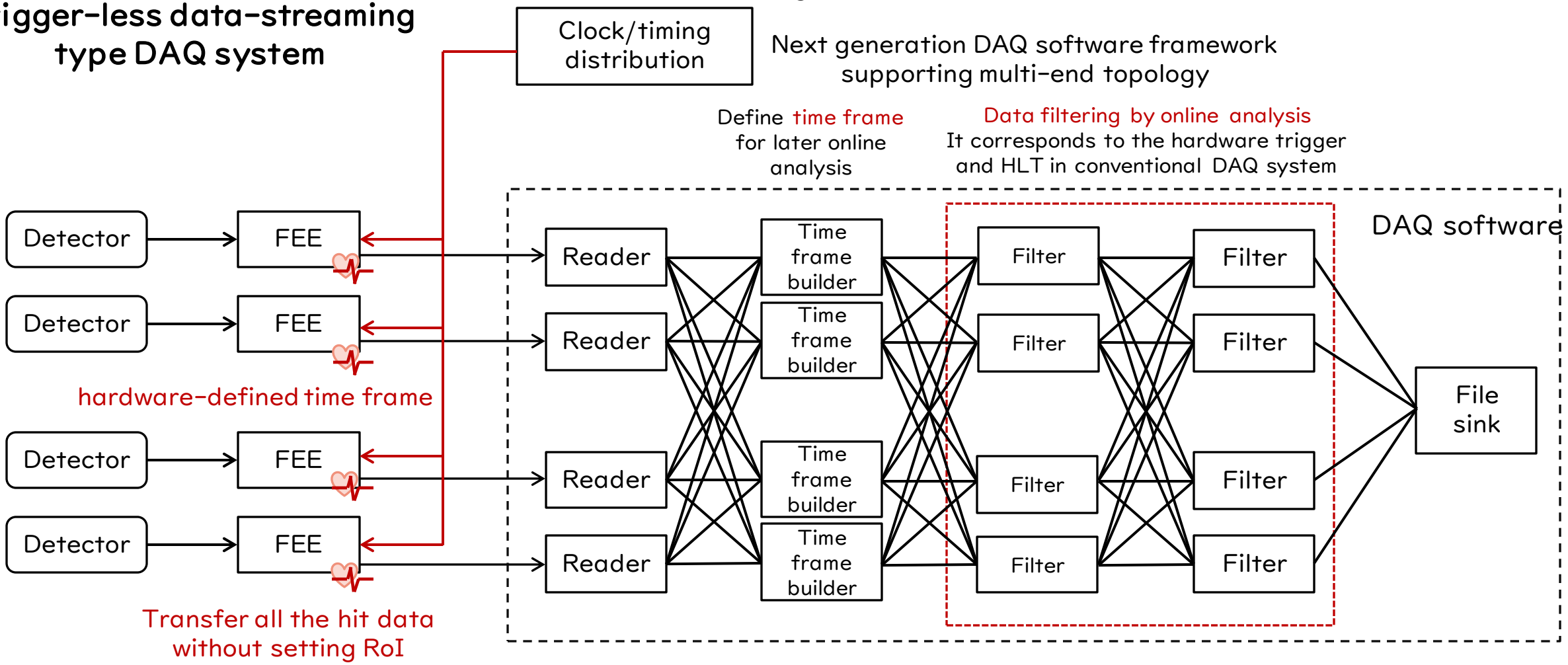
- Resource is not enough even for world largest FPGA
- Current hardware trigger logic is so much complex
- Difficulty to maintain and develop them



Toward trigger-less data-streaming DAQ system

Trigger-less data-streaming type DAQ system

Clock/timing distribution
to reconstruct the time among FEEs



Is the streaming DAQ system for the big experiment?
We think NO. There is merit even for small experiments!

Development policy

The development of front-end electronics (FEE) should be assembling work of key technologies.

Key technologies

- ADC technique
- TDC technique
- Digital filter technique
- Clock synchronization
- Data communication
- etc...

Should has not only generality but also room for extension

Electronics System Group

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This is not new idea, but the FEE is usually dedicated for the target experiment.

Standardization

- We would like to promote standardization of developed items under SPADI-alliance
- An FEE is for many experiments

SPADI Alliance

Key technologies for high-resolution streaming TDC

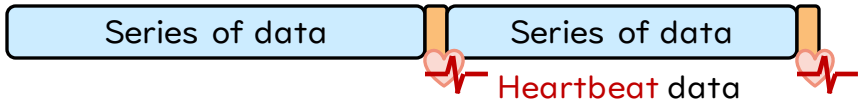
Define the time frame

From taking a picture to recording a video

Trigger

Trigger-less

Time stamp is a unique way to reconstruct event

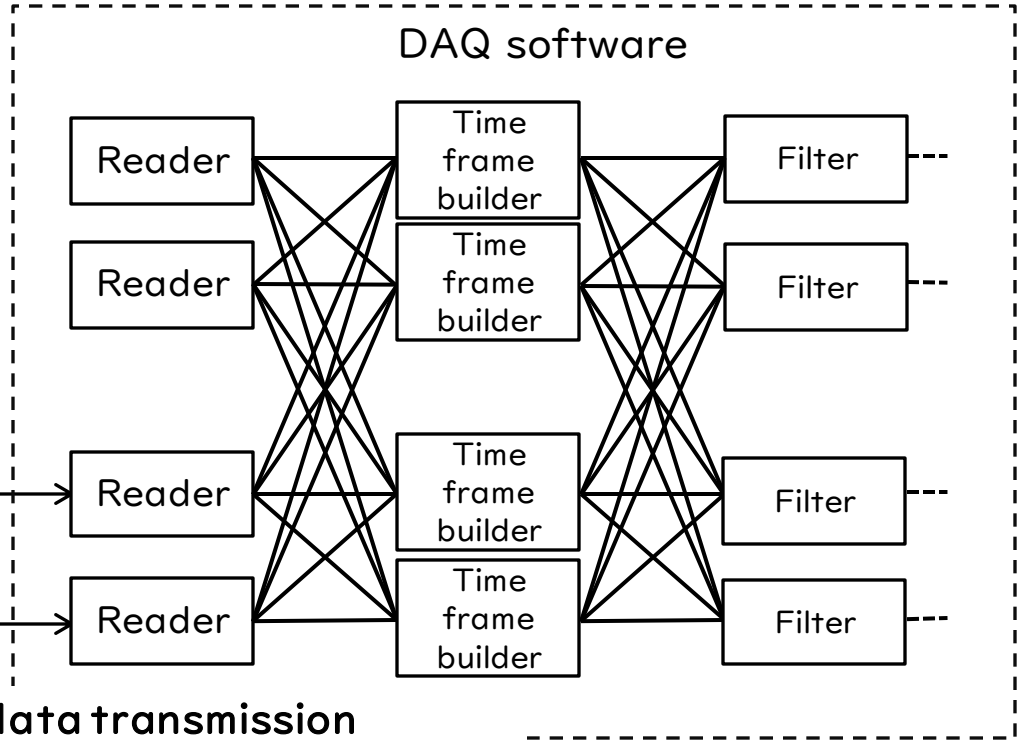


Heartbeat data

Boundary of time frame

Nest generation DAQ software (NestDAQ)

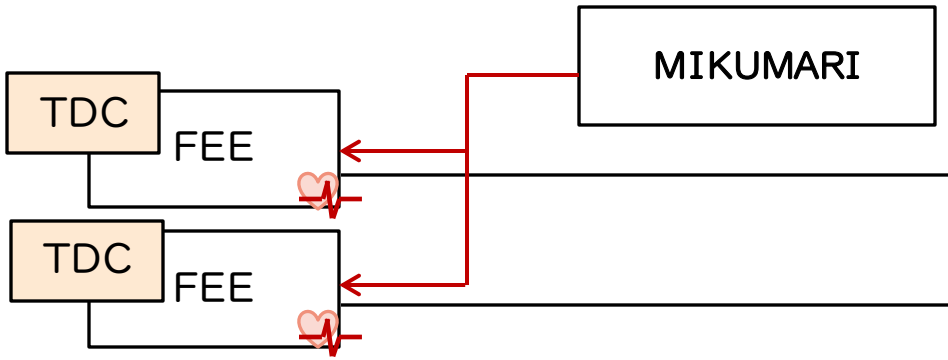
Support multi-end topology for load balancing



Synchronization

Simple & light-weight clock-data-recovery

(MIKUMARI: 水分, R. Honda, IEEE TNS, 70 (6), 1102 (2023).



Tapped-delay-line based TDC

- Implement using CARRY4 in AMD FPGA
- 15 ps (σ) in my design
- See slide on 計測システム研究会2017

Fast data transmission

- PCB design skill
- FPGA technology (10GbE SiTCP)
- Knowledge for computing

Data collection relying only on timestamps

Structure of TDC data

Fine count (n-bit) + **Coarse count (m-bit)**

Provided by timing interpolation techniques
- Sampling by multi-phases clock signals
- Tapped-delay-line

Independent from data acquisition function

Generated by the DAQ function driven by system (base) clock signal.

In conventional TDC
- The bit-length depends on the record length since it is the relative timing measurement respect to the trigger.
  - E.g., ring-buffer length ⇔ coarse count bit-length

In streaming TDC
- No local timing reference. It will be free running, but what length is necessary?

FEE data format

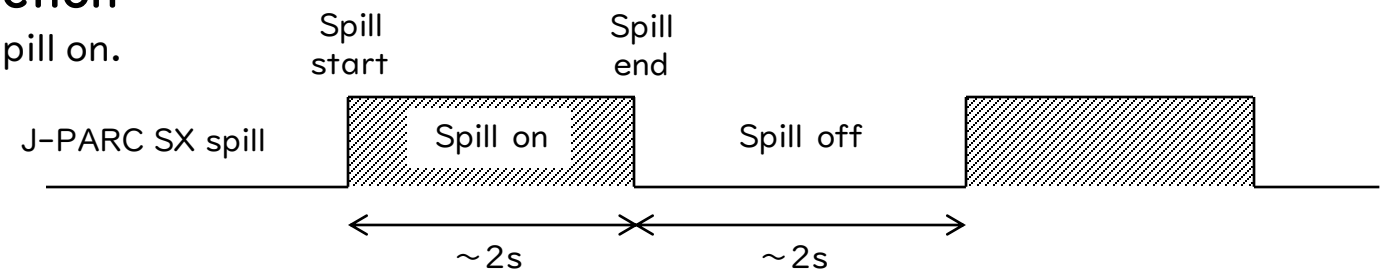
In conventional TDC
- Data header (trailer) exists as the boundary of the data block.
  - It may contains data size, event number, flags, etc...

In streaming TDC
- No local data block, an event, exists. Another data format must be introduced.

Data collection relying only on timestamps

Consider the case for J-PARC slow extraction

- DC beam are delivered to the beamline during spill on.

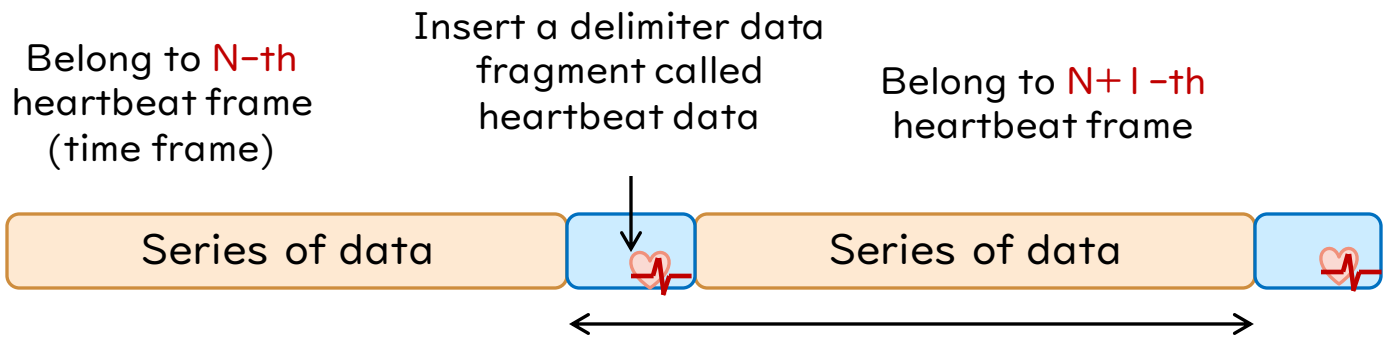


We need the continuous timing measurement over 2 s (spill duration of J-PARC slow extraction)

- Required dynamic range: $\sim 10^{10}$ (1 ns TDC case)

Introduce **heartbeat method**: a technique to reconstruct the time without a long-length time stamp.

- Insert a special data word periodically
- 16-bit heartbeat counter generates this period ⇔ 16-bit coarse count

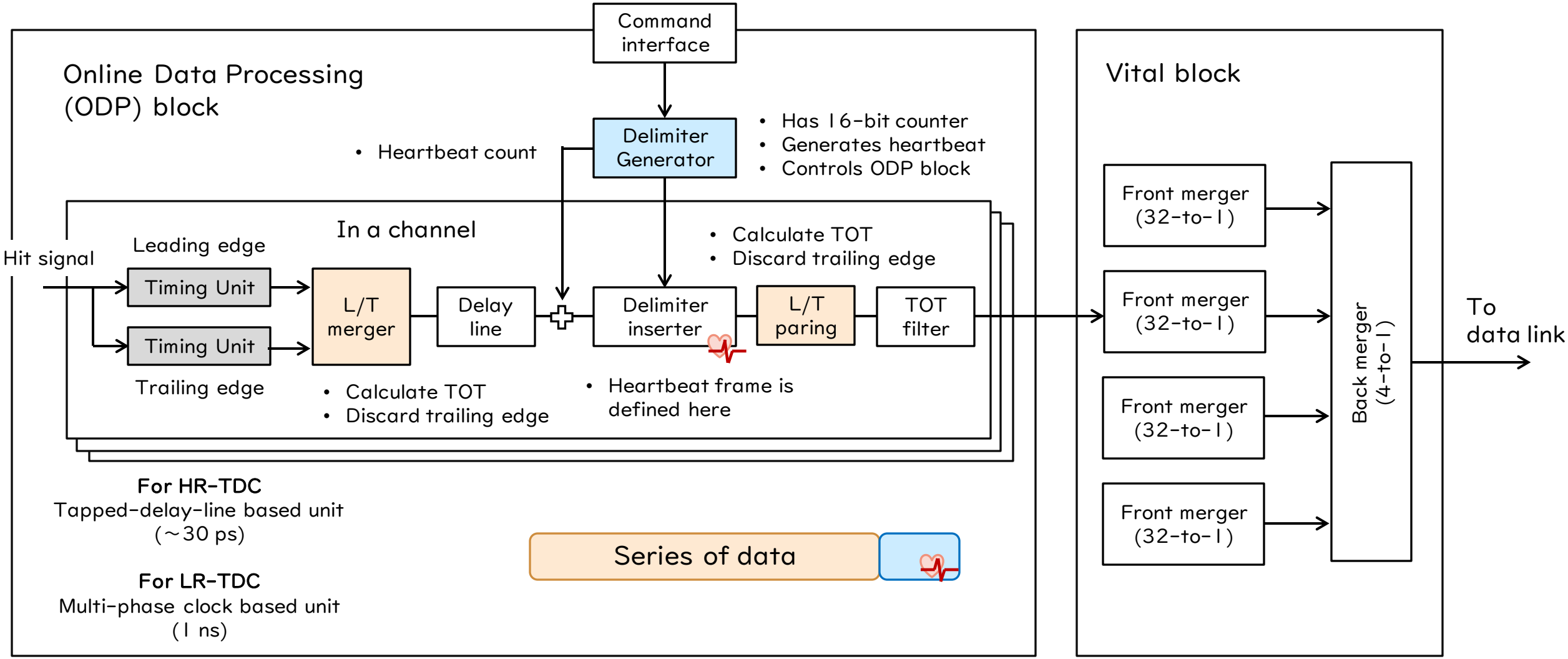


R. Honda et al., PTEP, ptab128, https://doi.org/10.1093/ptep/ptab128

Heartbeat frame length

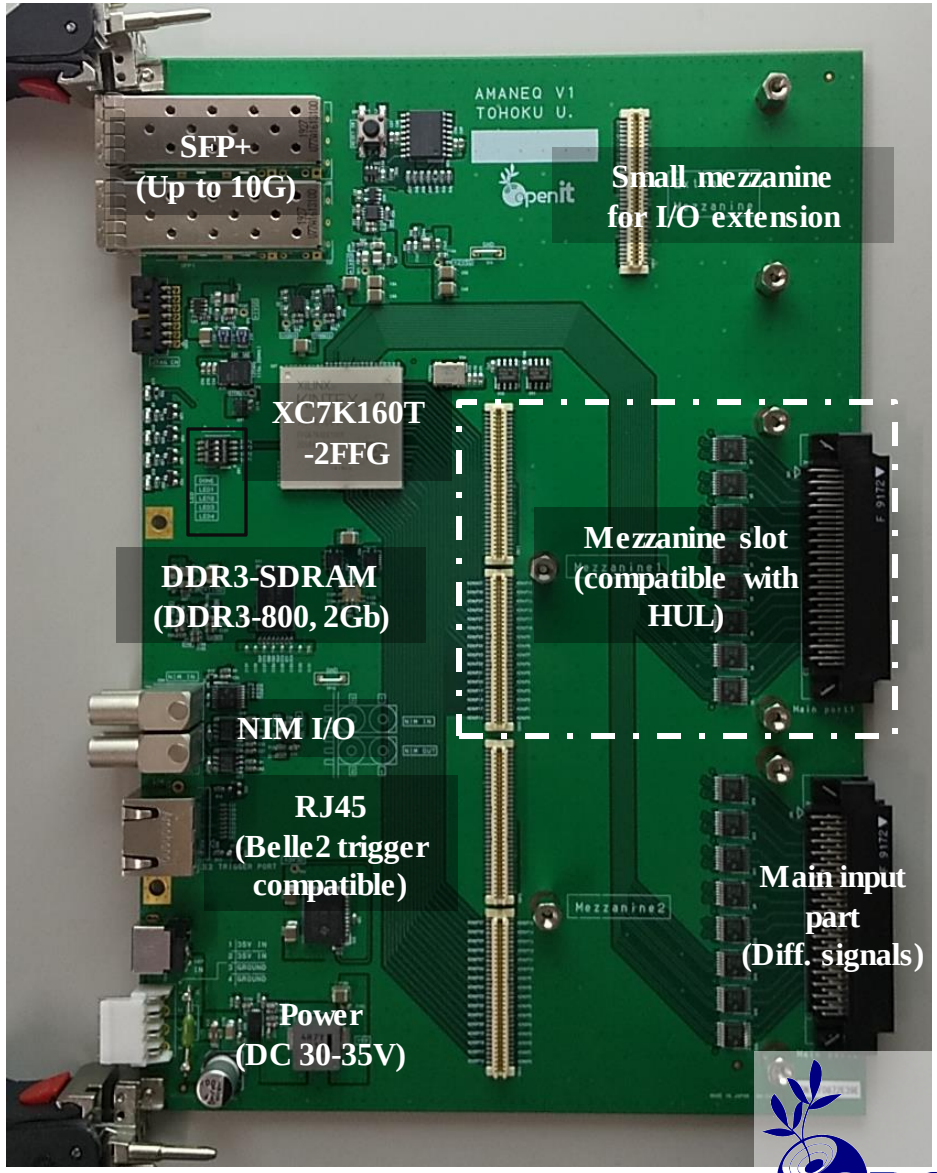
- 1/(125 MHz) x 0xffff = 524 us

Block diagram of Str-TDC



Implementation

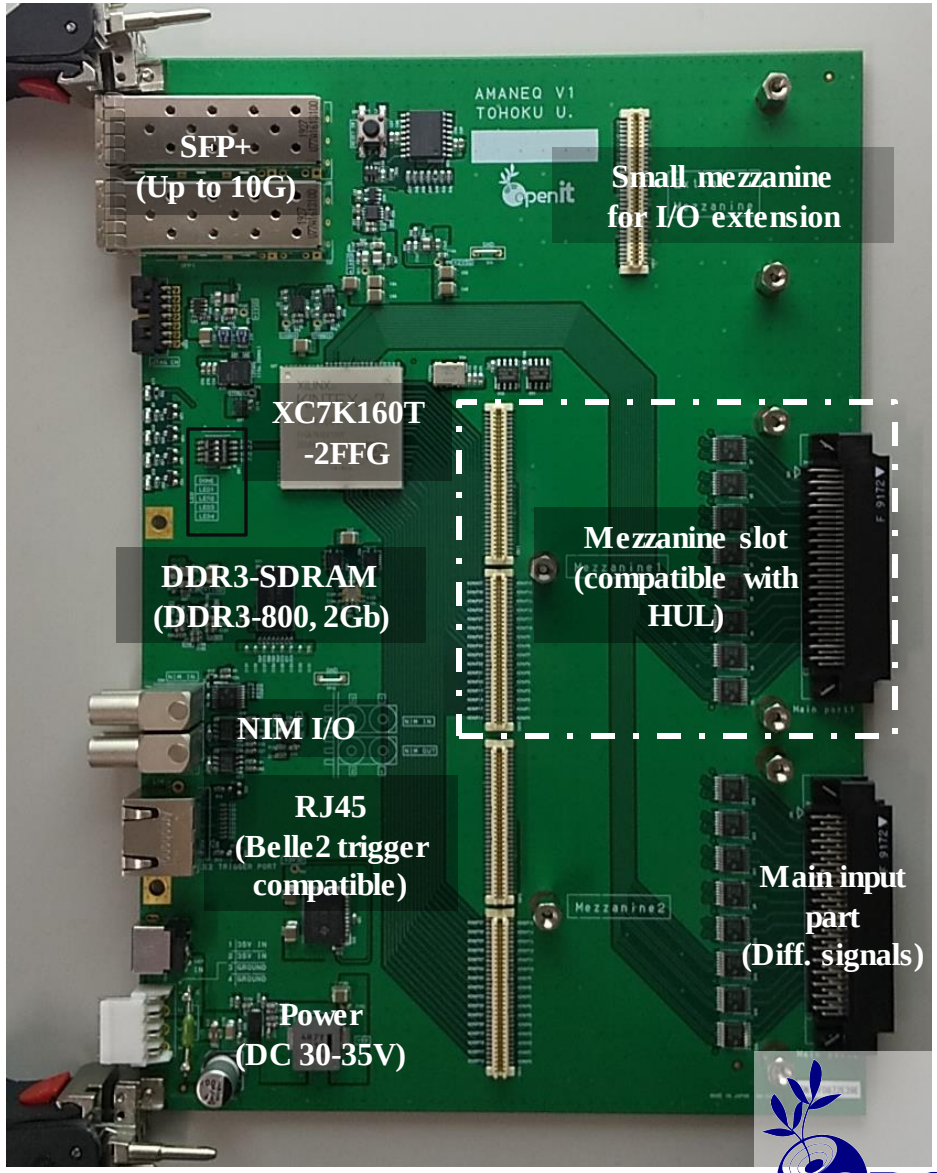
Hardware



A main electronics for network oriented trigger-less data acquisition system (AMANEQ)

- VME 6U size but it doesn't have VME bus
  - VME crate without the power is used as a housing box
- Kintex7 with speed grade -2
  - Transceiver bandwidth up to 10Gbps
  - Can implement SiTCP-XG
- Main input ports compatible with HUL
- Has two mezzanine slot
  - Compatible with HUL
  - Mount HUL mezzanine HR-TDC
  - Mount DCR mezzanine for DC readout
- Belle2 trigger port (master clock)
- Has a jitter cleaner (CDCE62002)
- DDR3-SDRAM as a de-randomizer
  - DDR3-1333 with 16-bit bus width.
  - 2 Gb
  - It allows us to use spill off time for data transfer
- Powered by the external power supply with DC 30-35V

Hardware



Attach

HUL/AMANEQ mezzanine HR-TDC

32 ch tapped-delay-line (TDL) based HR-TDC

- Input IO std.: LVDS (ECL is not supported)
- TDL consists of a CARRY4 primitive chain.
- Both leading/trailing edges
- Intrinsic resolution: 15 ps (σ)

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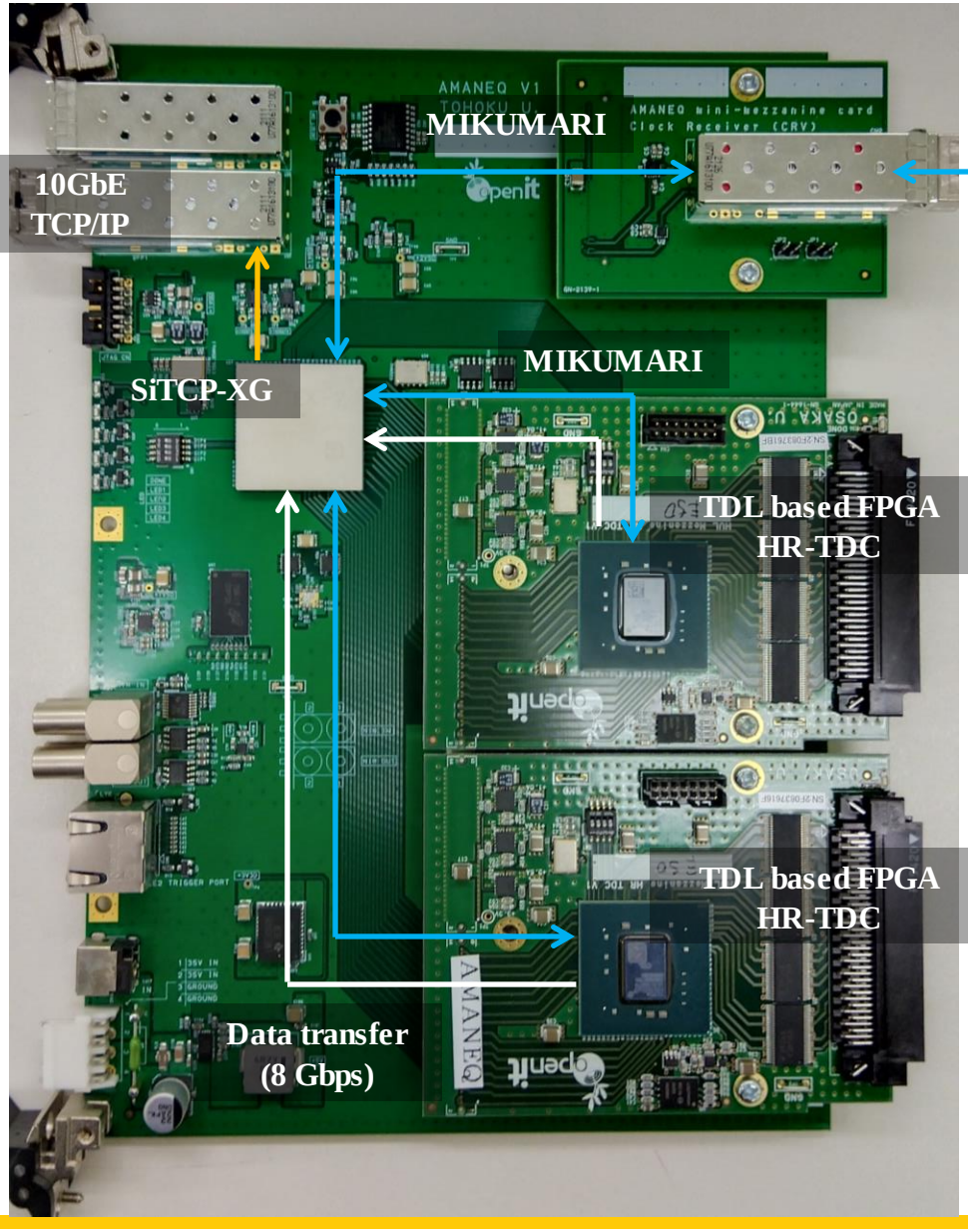
Streaming HR-TDC on AMANEQ



Modulated clock
from upstream (distributer) module

AMANEQ Str-HRTDC

- Input : 64 ch (32+32)
- Timing resolution: ~25 ps (σ)
  - Synchronization precision of MIKUMARI is included
- Data link: 10GbE
  - TCP/IP provided by SiTCP-XG
- Operation mode
  - Stand alone mode
  - Sync with MIKUMARI system

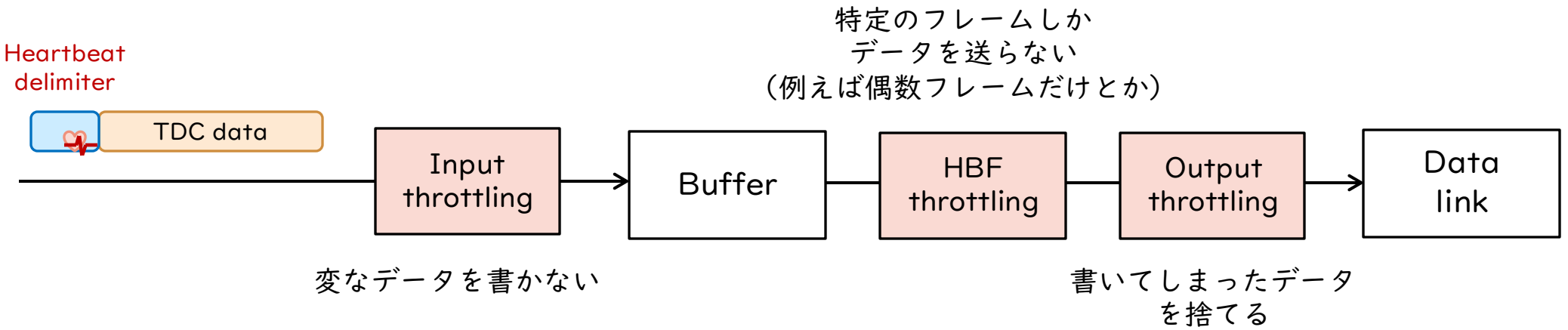
Tested in the beam experiments at RCNP Grand RAIDEN and J-PARC hadron facility

その先
（連続読み出しにたいする雑感）

データスロットリングの必要性

バッファがあるれそうになると…
- TDCデータの書き込みを遮断しハートビート文字だけを書くモードに入る
  - ハートビート文字が転送できないとソフトが時刻を見失うため

溺れつつある状況ですぐにバッファは本当にいっぱいになる
- Programmable full thresholdの設定にもよるが数msもたない



ただ問題点も…
- ノイジーな検出器がいるとinput throttlingが頻繁に働く
- DAQ efficiencyの見積もりが煩雑になる（というか未だに完全な計算が出来るのかやや疑っている）
  - TriggerとBusyによるハンドリングは偉大

FEEがDAQ RUN中にいなくなる事の標準化

モジュールからデータが返ってこなくなる例

- FEEバッファが一杯になってデータ構造がクラッシュする（先ほどの例）
- 放射線損傷により一時的にFEEが離脱する
- 誰かがファイバーを引っこ抜く

こういう時DAQを止めるか止めないかのチョイスがあり最近の大きな実験は止めない方針を取っている

ソフトウェアによるリカバリープロセス

- モジュールの離脱と自動復帰をDAQの標準的な考えに組み込みたい
- 不安定なまま走れてしまう事による弊害も考えられる
    - 全FEEが揃っているデータが殆どなくてイベント再構成が出来ないのにデータを取り続けてしまう

いずれにせよDAQ efficiencyの計算とモニターが重要な課題になってくる

真の時刻同期へ

Trigger-less DAQでは時刻だけが事象再構成のよりどころ

時刻同期 (Clock synchronization)
- 自身の時計を基準時刻に合わせること

素核実験ではFEEのクロック信号同期はするが
時計の針合わせまではやらない事が多い（解析でやる）

世の中の時刻同期プロトコル
- クロック信号の周波数同期をしないとせいぜいus精度
- 周波数同期をするとns精度

更にその先：CERNのWhite Rabbit
- 2地点のクロック信号の相対位相補償を自動で行いsub-ns精度を得る

White Rabbitの限界
- Synchronous Ethernetに基づいているため任意の周波数を伝送できない

結果としてWhite Rabbitは素核のFEE上で走るには至っていない
MIKUMARIでここを埋めに行けないか？

PTPのような手法と位相差補償機能をFPGAだけで実現し
sub-nsの確度と50 ps精度を得ることを目標に

Summary

- So far, we have developed several key technologies for the general purpose DAQ system
  - Tapped-delay-line based FPGA high-resolution TDC
  - Heartbeat method to overcome a problem of long-length counter
  - Simple and light-weight synchronization technology: MIKUMARI

Today, we are considering not only the development of key technologies but also the standardization of the developed items.

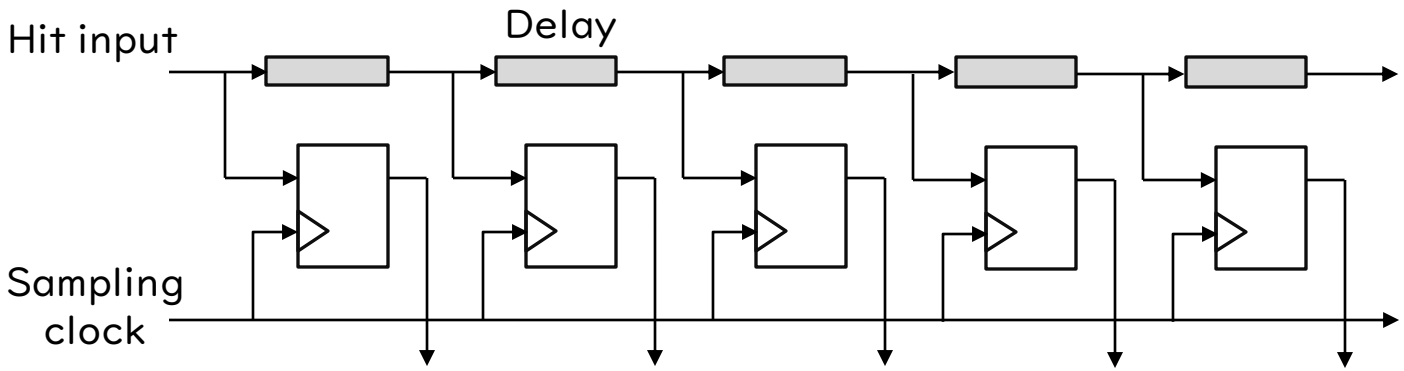
- **Implementation of Streaming HR-TDC into the AMANEQ board**
  - TDL based HR-TDC is outsourced to the mezzanine card
    - 64 (32+32) ch input per AMANEQ using two HR-TDC mezzanine cards
  - ～25 ps timing resolution including the synchronization precision.
  - Data communication by 10GbE

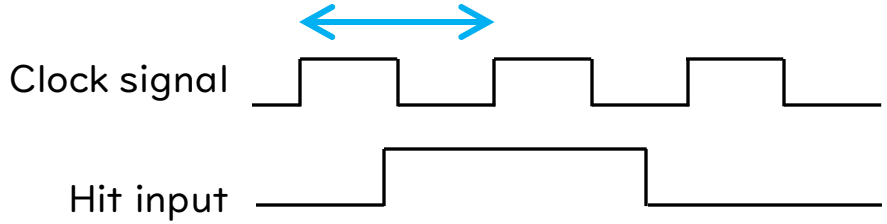
- Clock/timing distribution system, MIKUARI system was developed.

- The developed Str-HRTDC was tested in the RCNP Grand RAIDEN and J-PARC hadron facility.

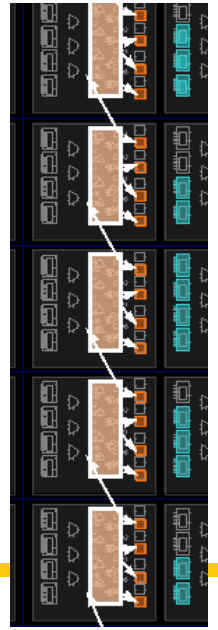
Tapped-delay-line based FPGA TDC

Timing interpolation technique using tapped-delay-line (TDL)





Take a snap shot of a pulse running on TDL



TDC implemented in AMD Kintex-7 FPGA

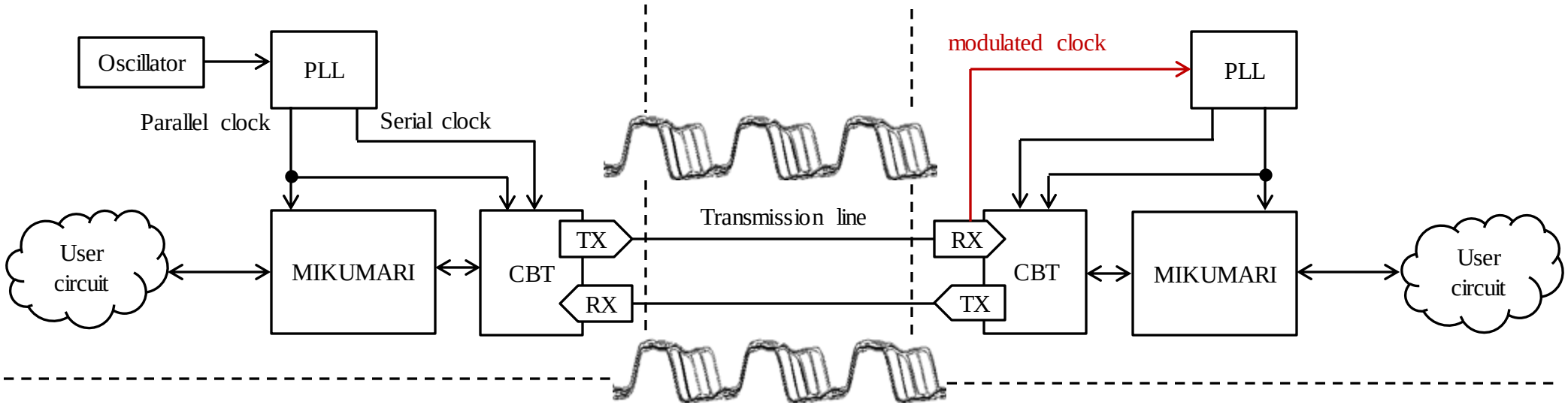
- Use CARRY4 element
- 192 taps corresponding to the vertical size of a clock region.

Timing resolution: 15 ps (σ)

詳しくは17年の計測システム研究会のスライドを参照

MIKUMARI link

Clock/data distribution system based on the modulated clock signal (CDCM) using a single transmission line



Functions

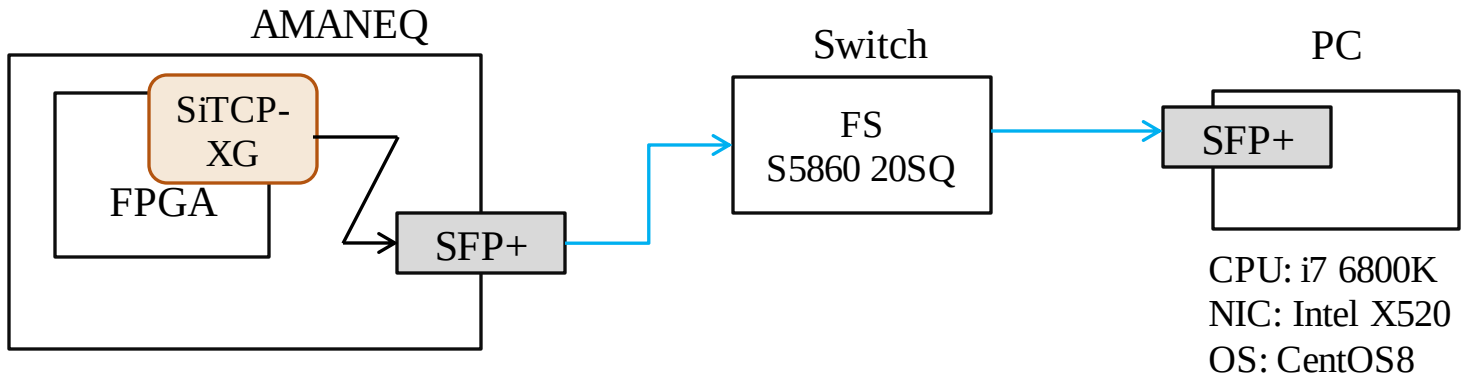
- Frequency synchronization by transmitting a modulated clock signal
- Data communication based on a data frame
- Pulse transmission with the fixed latency (synchronized with parallel clock signal)

Features

- Can be implemented in a regular bank. It's independent from high-speed serial transceivers such as MGT in AMD FPGAs.
- Any PLL is workable as the clock recovery circuit.

Data transfer speed via SiTCP-XG

Test setup

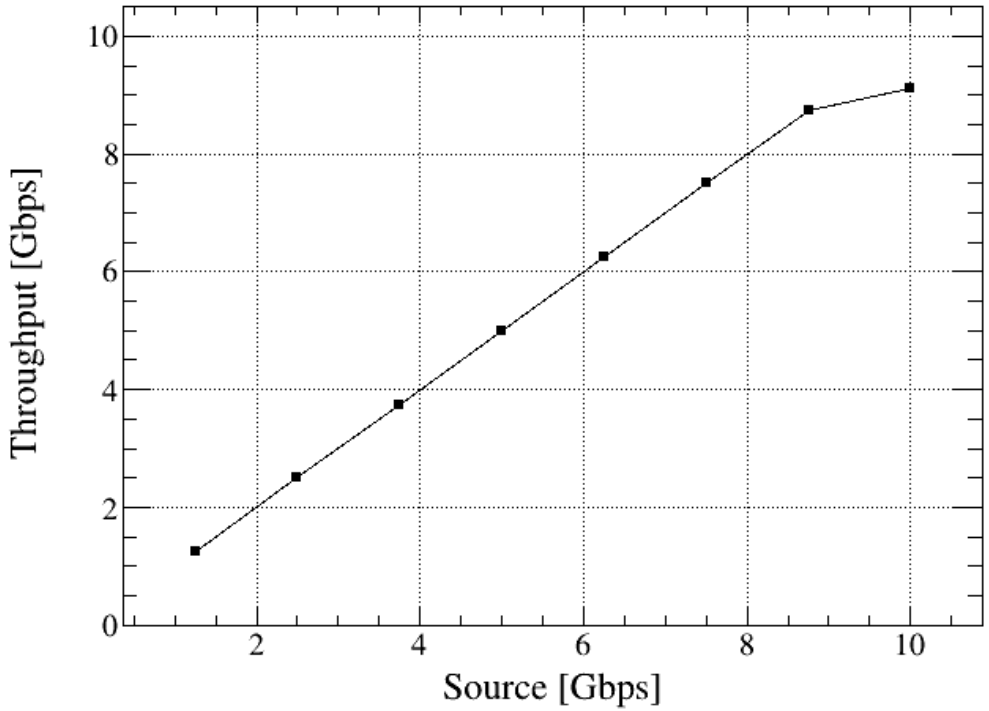


Read data using C++ software.

CPU: i7 6800K
NIC: Intel X520
OS: CentOS8

Tested by H. Sendai (KEK E-sys)

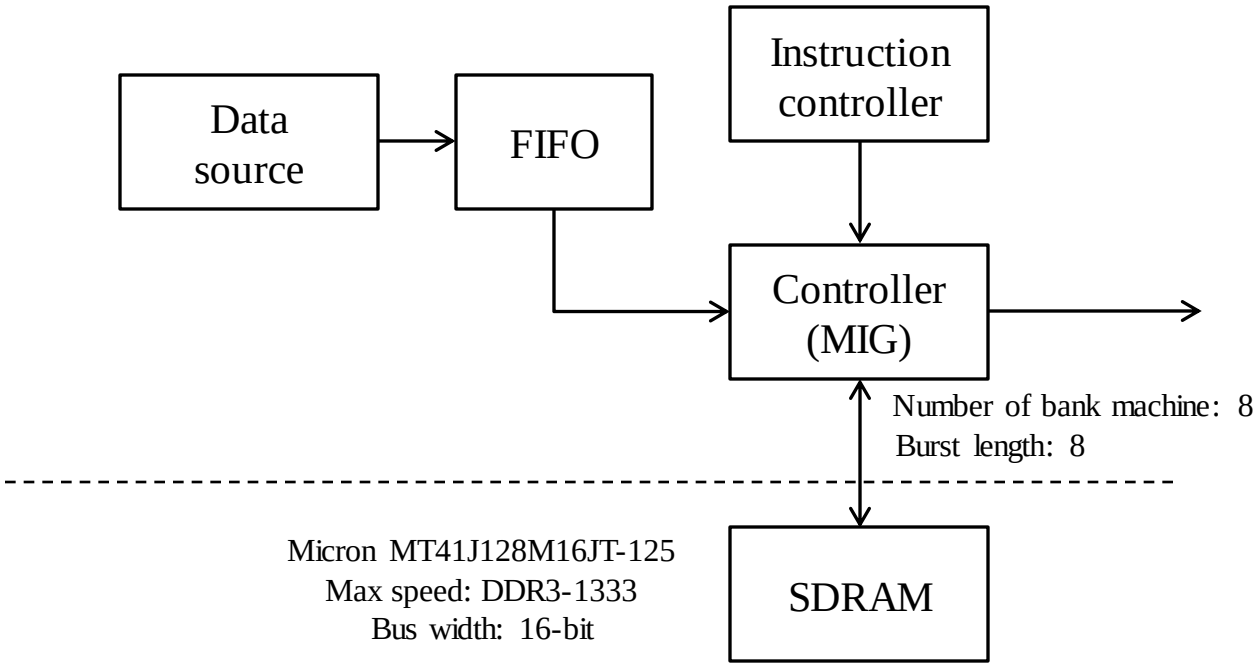
Measured throughput

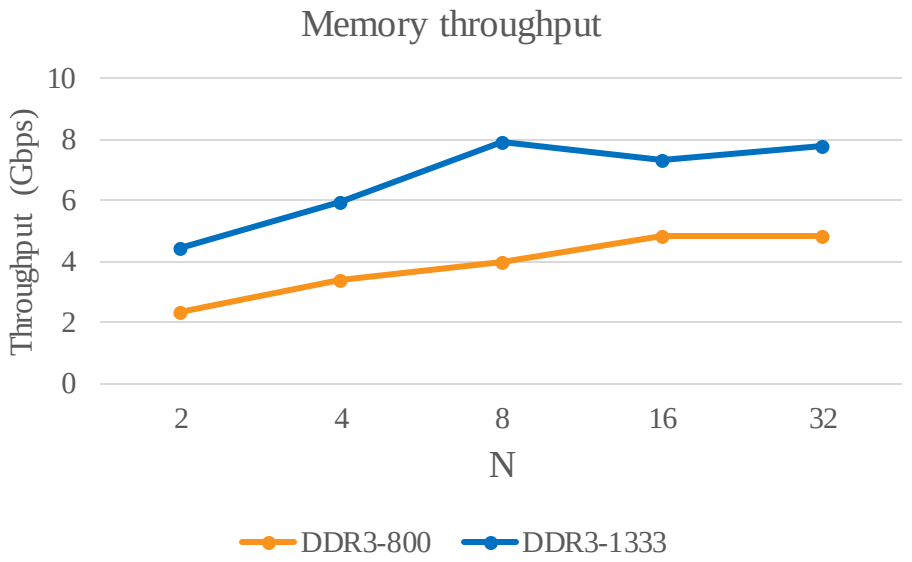


Obtained throughput: 9.12 Gbps
~96% of TCP payload limit (MTU 1500)

Throughput of DDR3-SDRAM

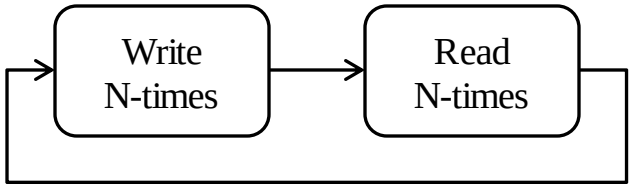
Firmware configuration





Data bus of SDRAM is bi-directional.
Memory operation is determined by command.

Tested write/read pattern.



Obtained throughput (reference value)

DDR3-800

- ~4.8 Gbps (6.4 Gbps)

DDR3-1333

- ~7.9 Gbps (10.66 Gbps)

***Access to the same memory bank.
Larger over head when changing the bank address.