大阪大学
THE UNIVERSITY OF OSAKA

RCNP

K Program

MEASUREMENT SYSTEMS WORKSHOP, 17TH-18TH OF NOVEMBER, 2025

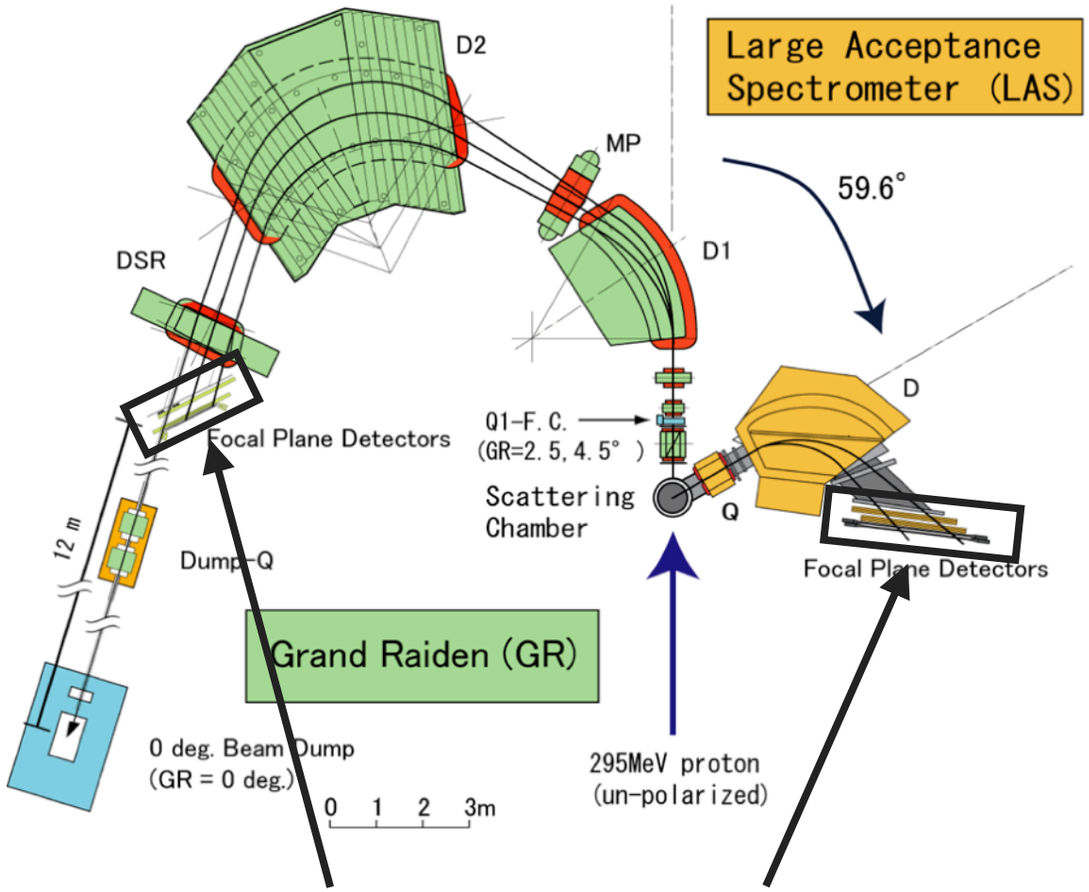
An all-in-one board for the readout of gaseous detectors

LAKMIN WICKREMASINGHE

RCNP-DAID, THE UNIV. OF OSAKA

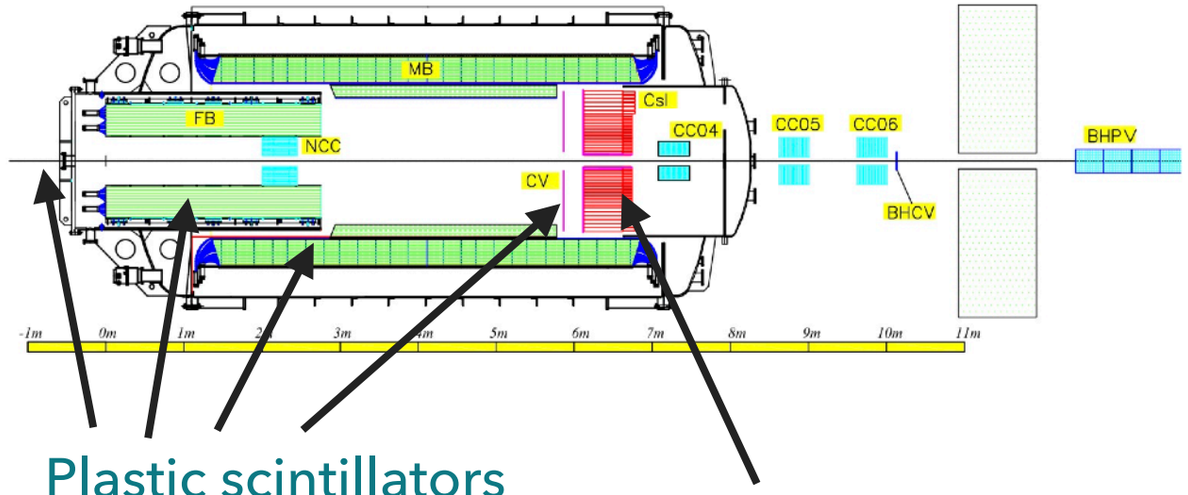
Particle detectors in experimental physics

Nuclear physics: Grand Raiden and Large Acceptance Spectrometers, RCNP, UOsaka



VDC's (vertical drift chambers) & plastic scintillators as focal plane detectors

Particle physics: : KOTO Experiment, JPARC



Plastic scintillators as veto detectors

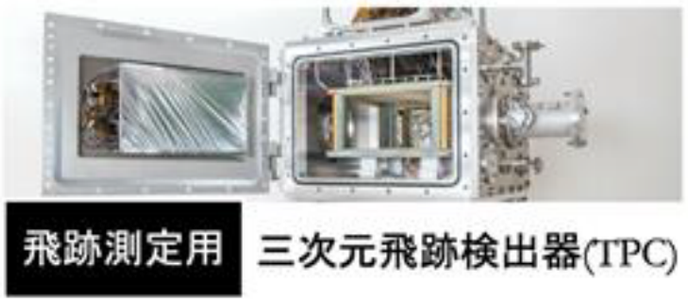
CsI scintillators for the calorimeter

- While particle detector technology has advanced in recent years, so has the DAQ,
  - From NIM & CAMAC modules based
  - To FE-ASIC and FPGA based

Introduction from the K-program side

- In the JST K-program project 「仮想測位基準点を構築する即時分散データ処理技術・研究者代表：大田 晋輔、研究分担者：本多 良太郎、馬場 秀忠」, we are developing DAQ technology for air shower detectors. One task is the development of all-in-one cards.

Time Projection Chamber



Cherenkov Detector

Drift Chamber

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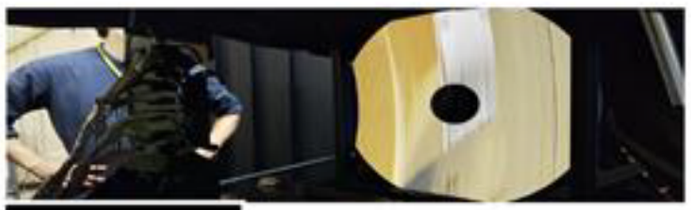
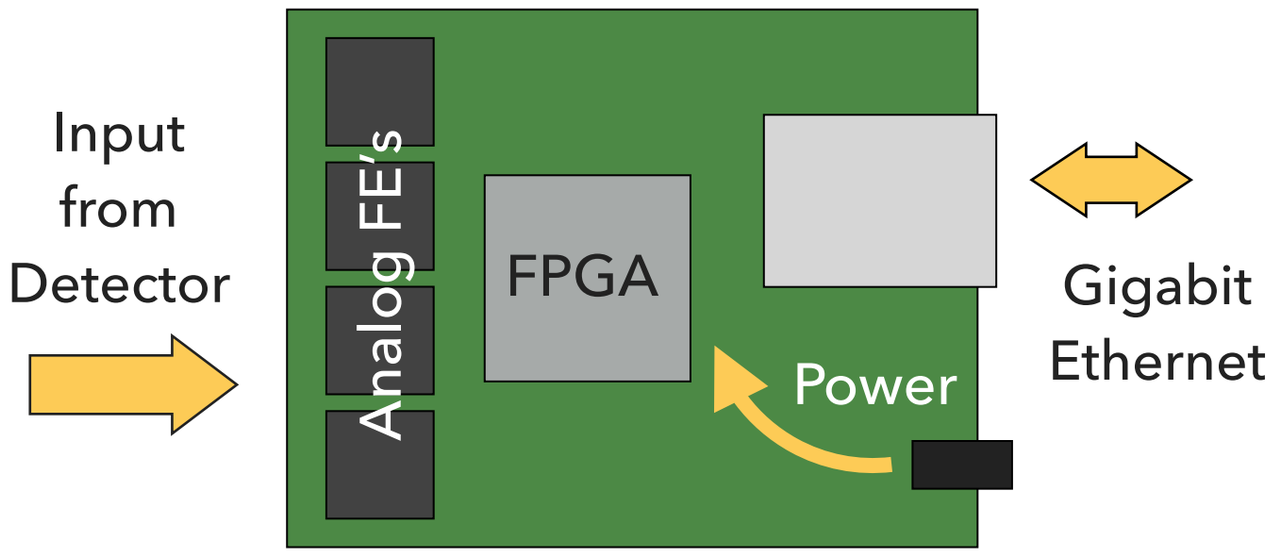
Cherenkov Detector



Drift Chamber

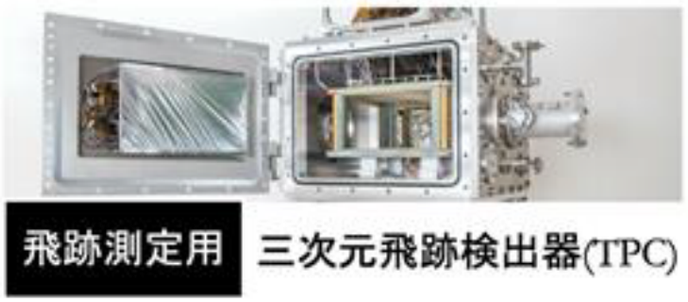
- ***All in one*** - Analog front end & FPGA in one board, eliminating need for cables.
- ***Compact*** - Ability to fit into compact geometries and spaces like vacuums.
- ***Generic*** - Satisfies requirements of different detectors/experiments.

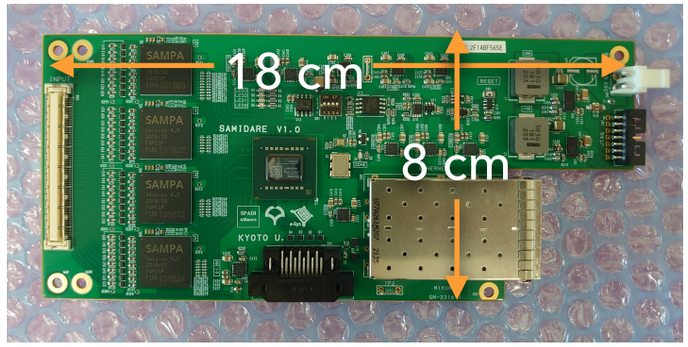


Introduction from the K-program side

- The development is ongoing also with the collaboration of SPADI (***S***ignal ***P***rocessing ***A***nd ***D***AQ ***I***nfrastructure) Alliance.

Time Projection Chamber

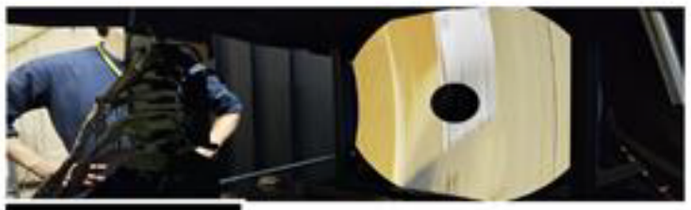


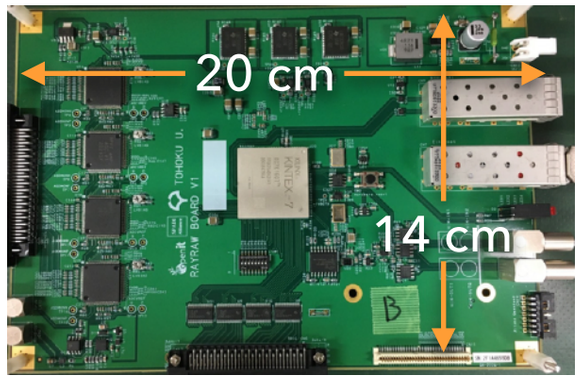


SAMIDARE by S.Nagafusa (Kyoto Univ.) et al.

Further R&D at RIKEN

Cherenkov Detector

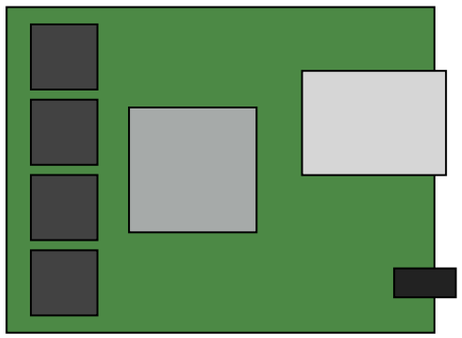




RAYRAW by R.Honda (IPNS) et al.

Further R&D at Tohoku Univ.

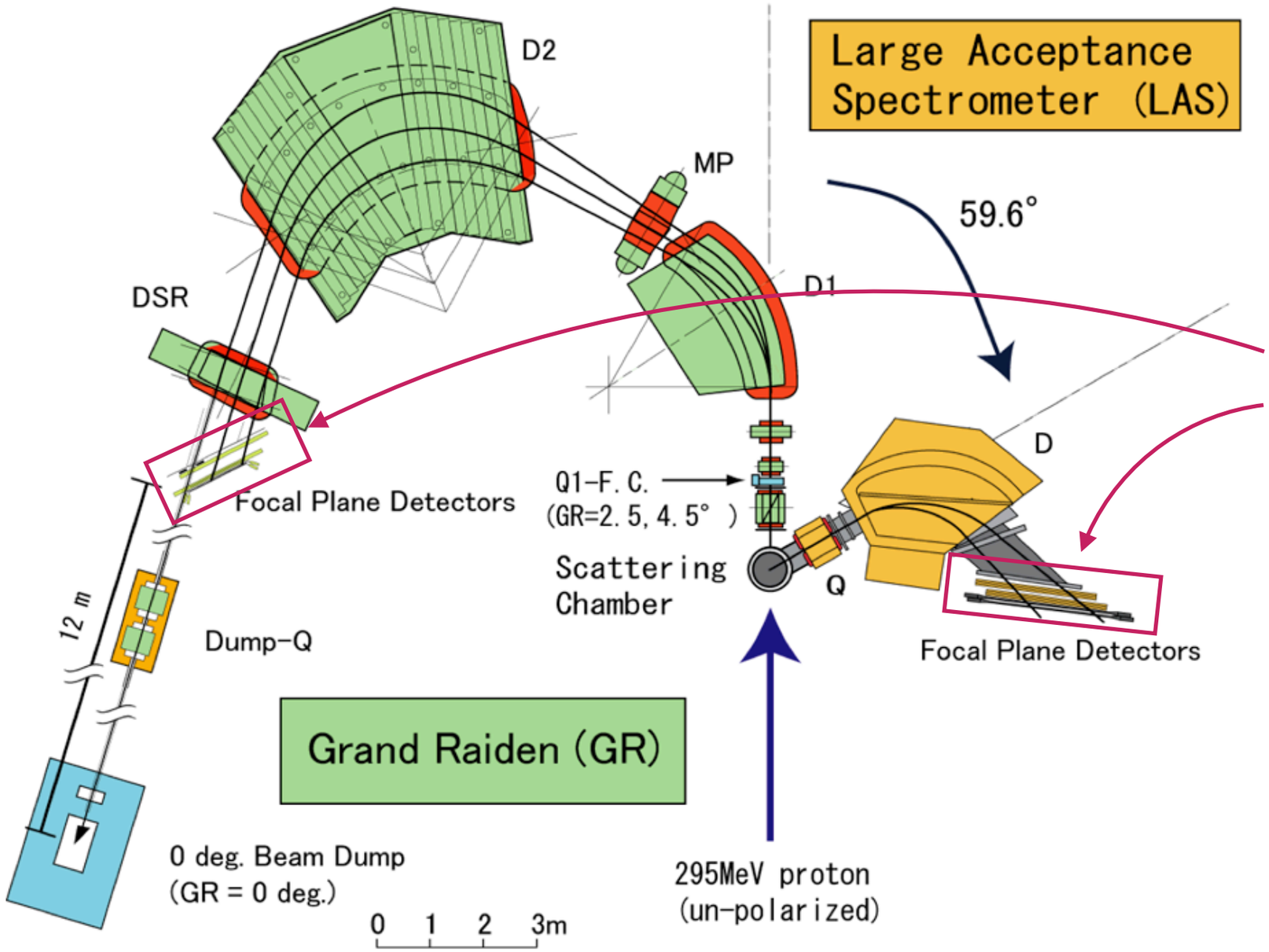
Drift Chamber



Under development

This Talk!

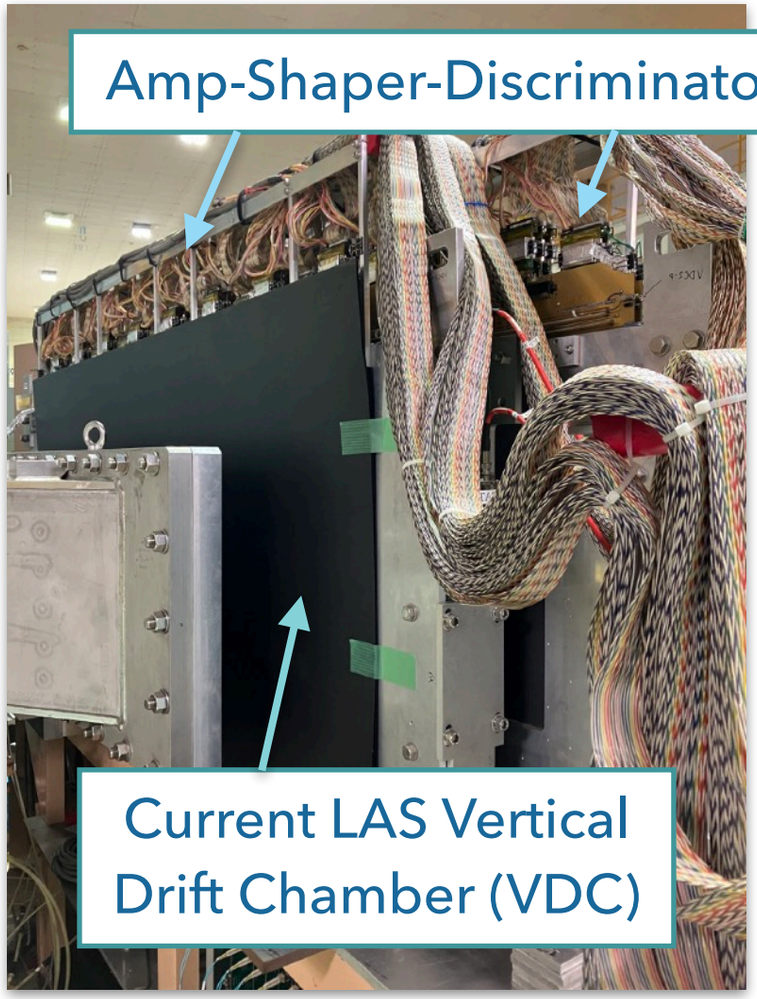
Introduction from the LAS upgrade side



The focal plane (FP) detectors consist of VDC's and plastic scintillators.

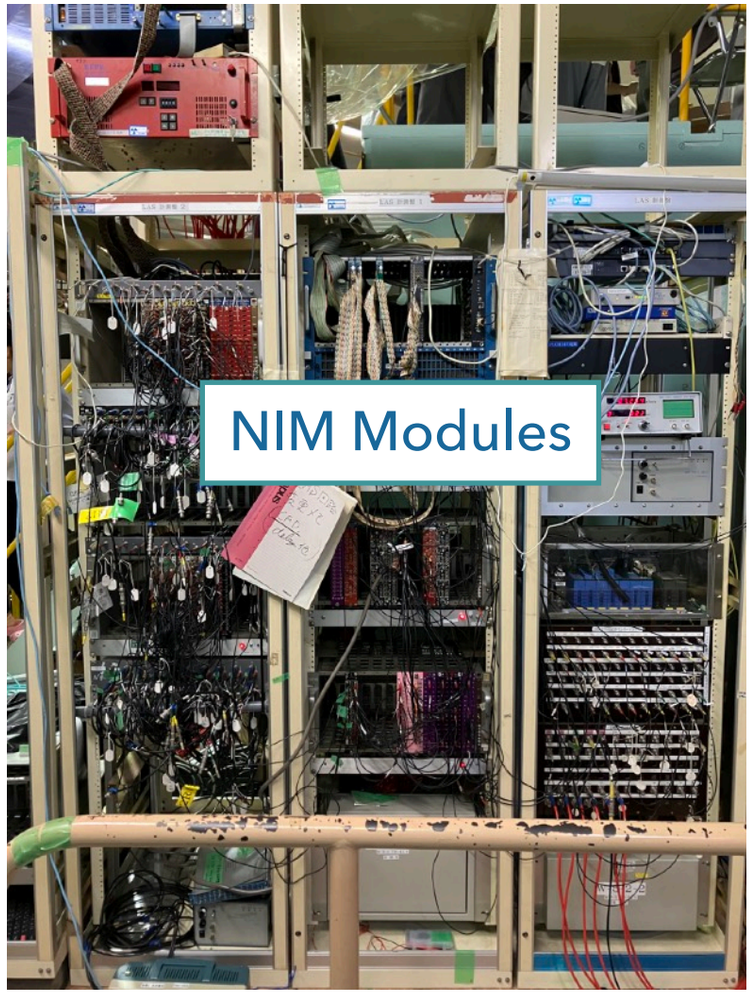
- Due to future experiment requirements, we will upgrade the LAS FP detectors.
- After the upgrade, we expect data rates in the order of ~6 Mcps for LAS.

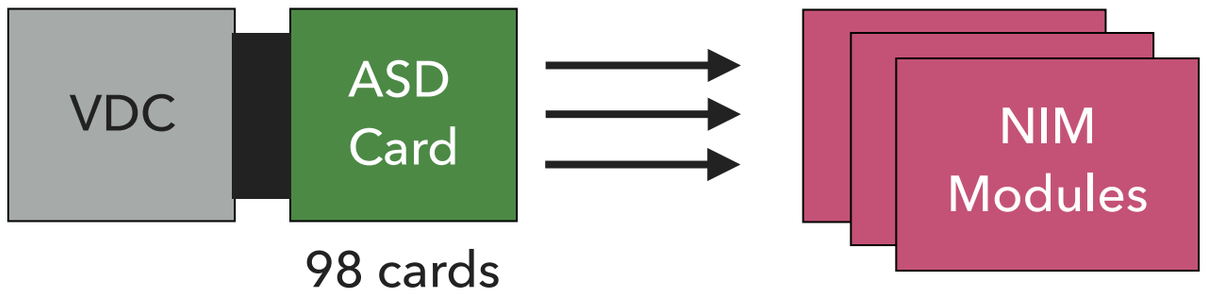
Introduction from the LAS upgrade side



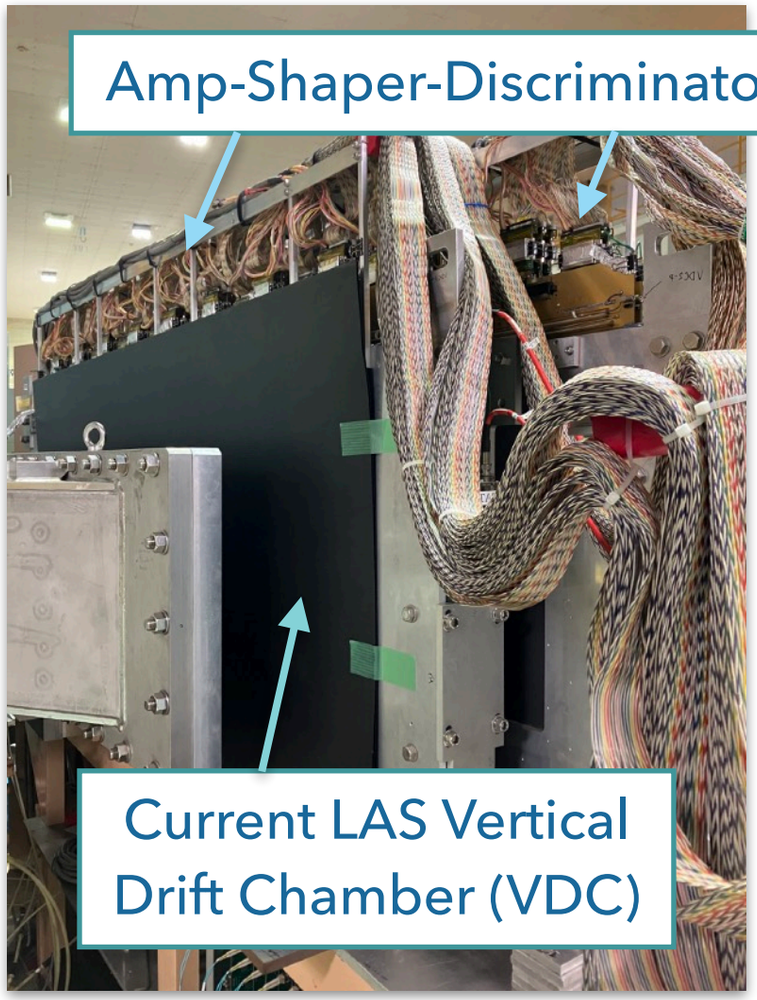
Time over Threshold (ToT)

Could only handle DAQ rates of up to (O)10~(O)100 kcps



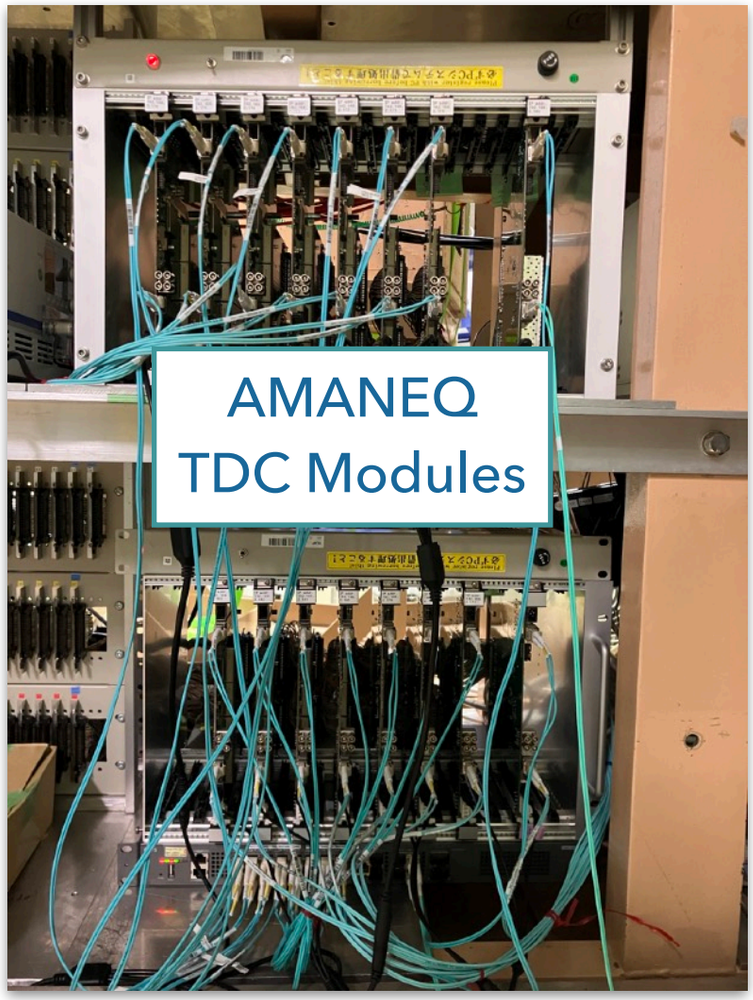


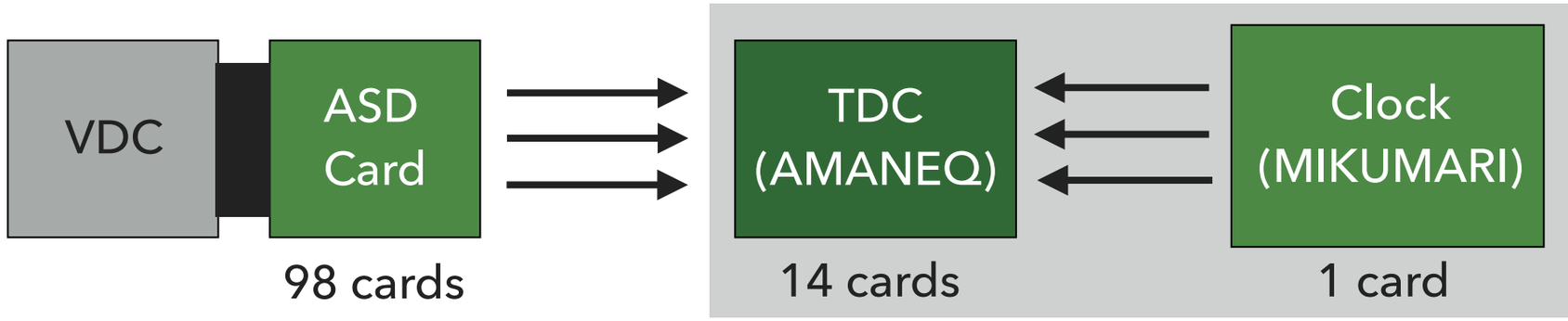
Introduction from the LAS upgrade side



Time over Threshold (ToT)

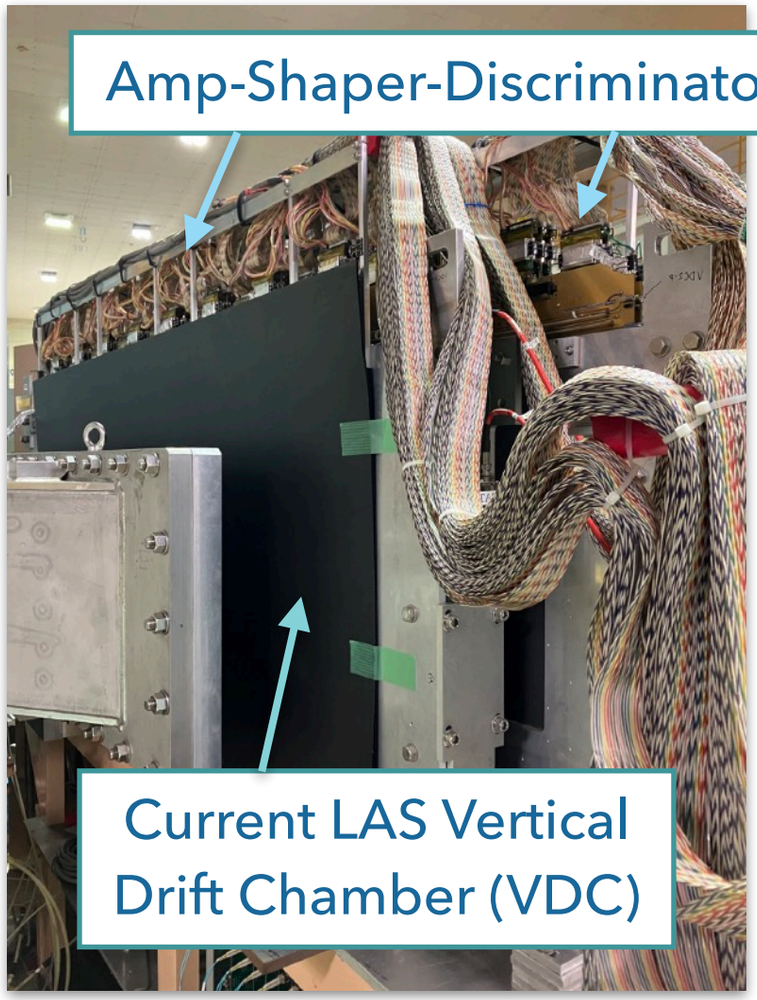
Changing to a trigger-less streaming DAQ system ➡ Can handle DAQ rates of ~(O)Mcps

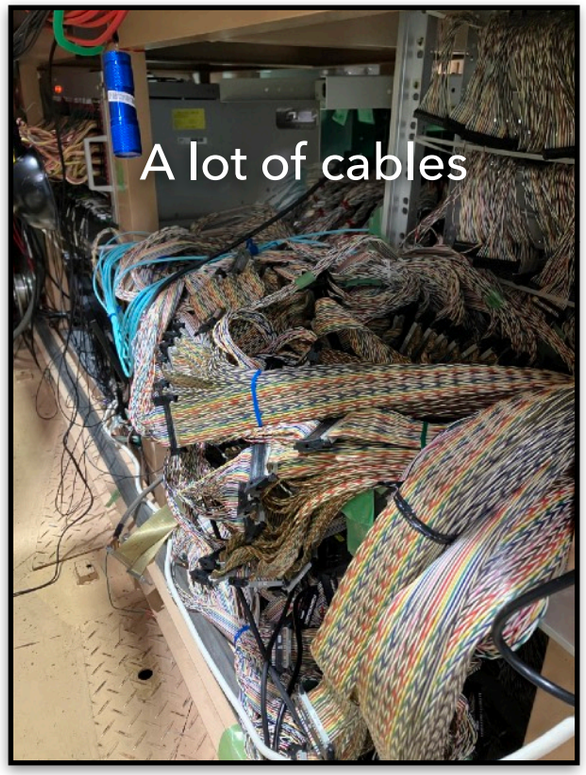


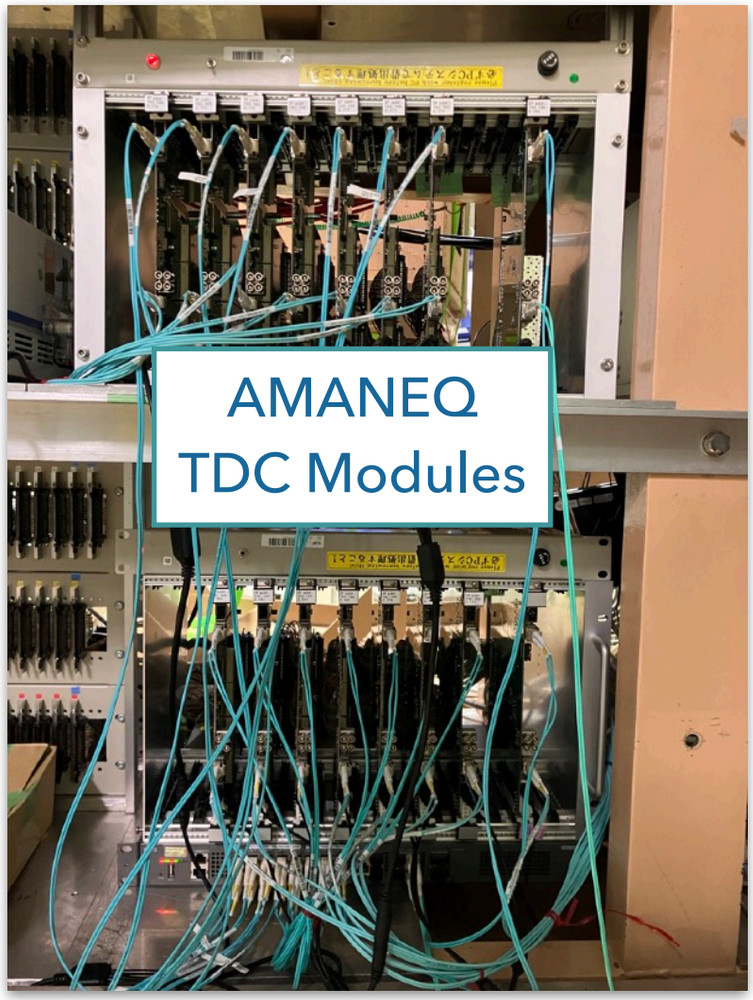


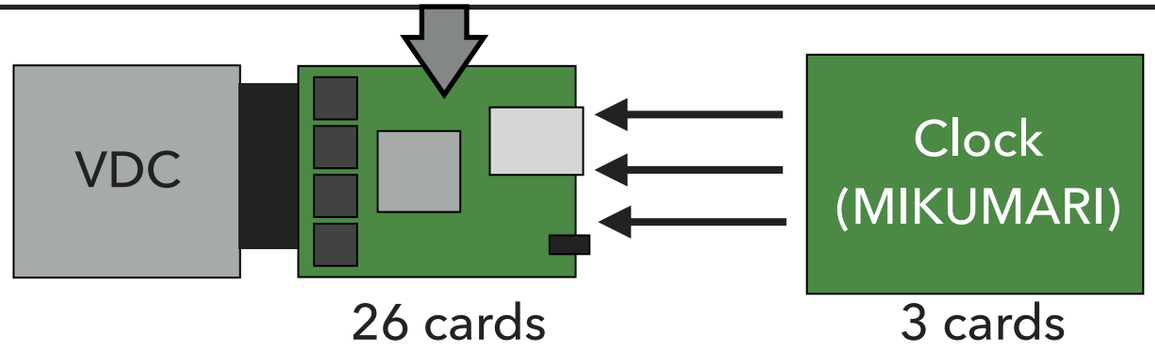
Developed by R.Honda et al.

Introduction from the LAS upgrade side







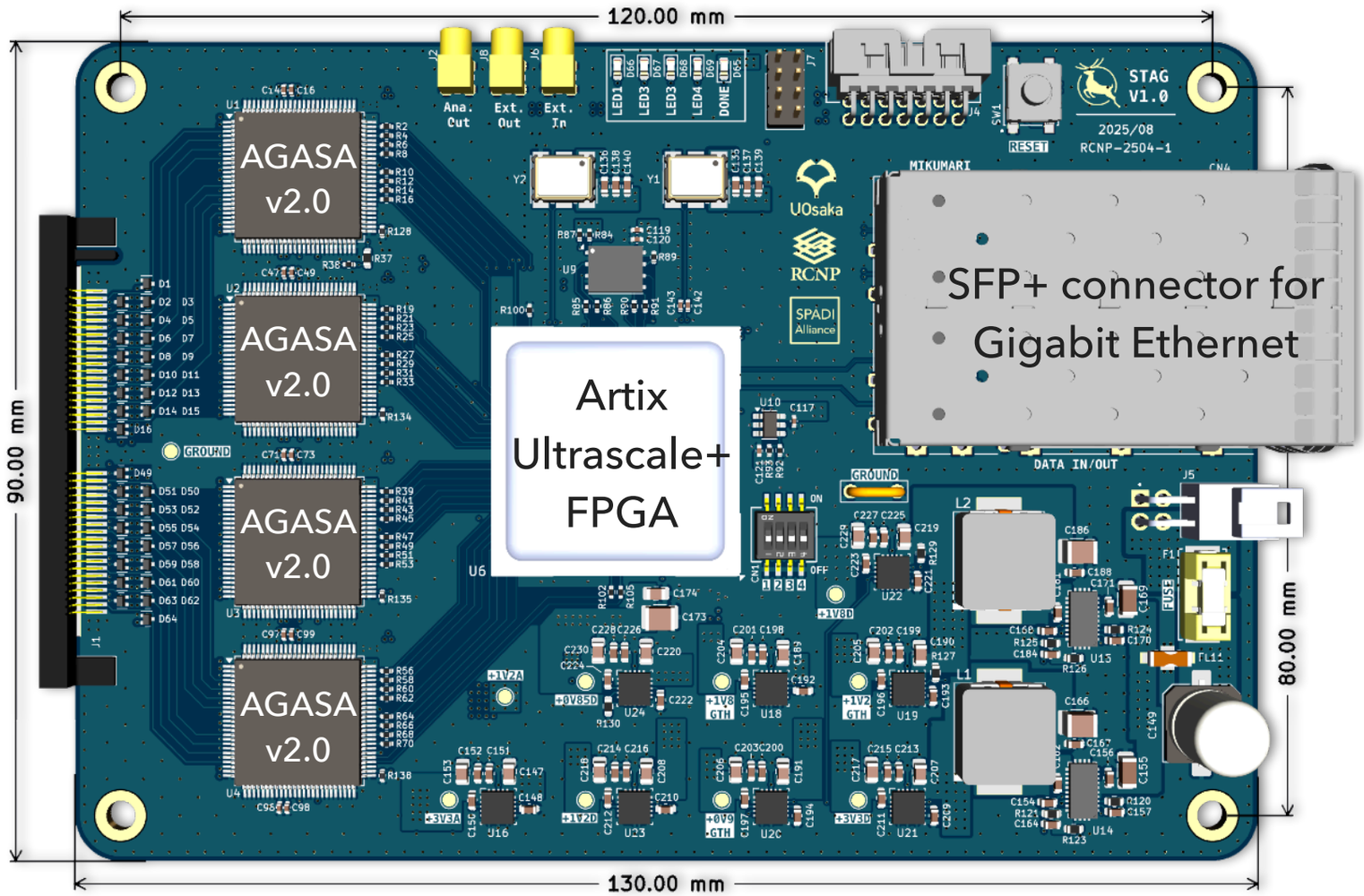


After the upgrade of the LAS VDC ➡ More compact system

The all-in-one STAG Board

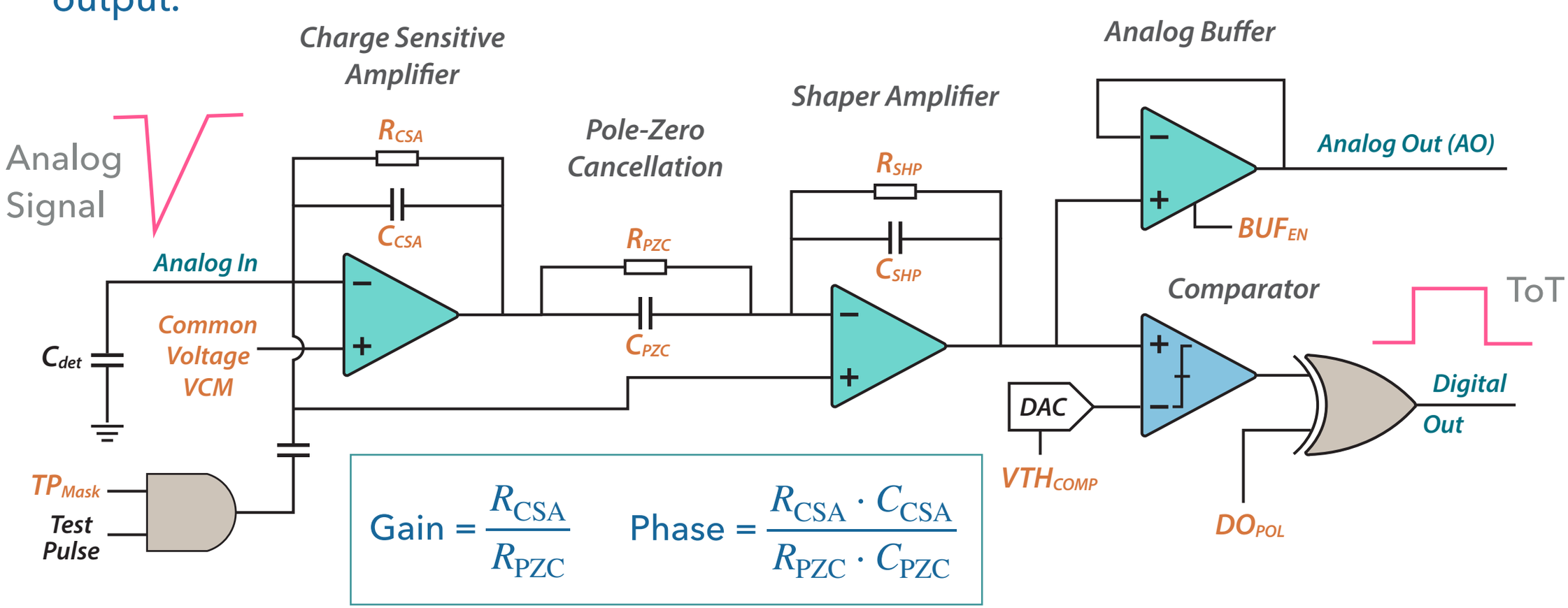
- The STAG (***ST***reaming readout with ***A***GASA for ***G***aseous detectors) board is designed by Lakmin.W and M.Ikeno (RCNP-DAID).
  - ***Analog FE***: AGASA analog ASIC developed by M.Miyahara (KEK), R.Honda (KEK), et al.
  - ***FPGA***: Artix Ultrascale+
  - ***Size***: 9 cm x 13 cm
  - ***Aim for low cost***:
    ~200,000 yen per board,
    or ~3200 yen/channel.

Input from 64 VDC channels



AGASA ASIC

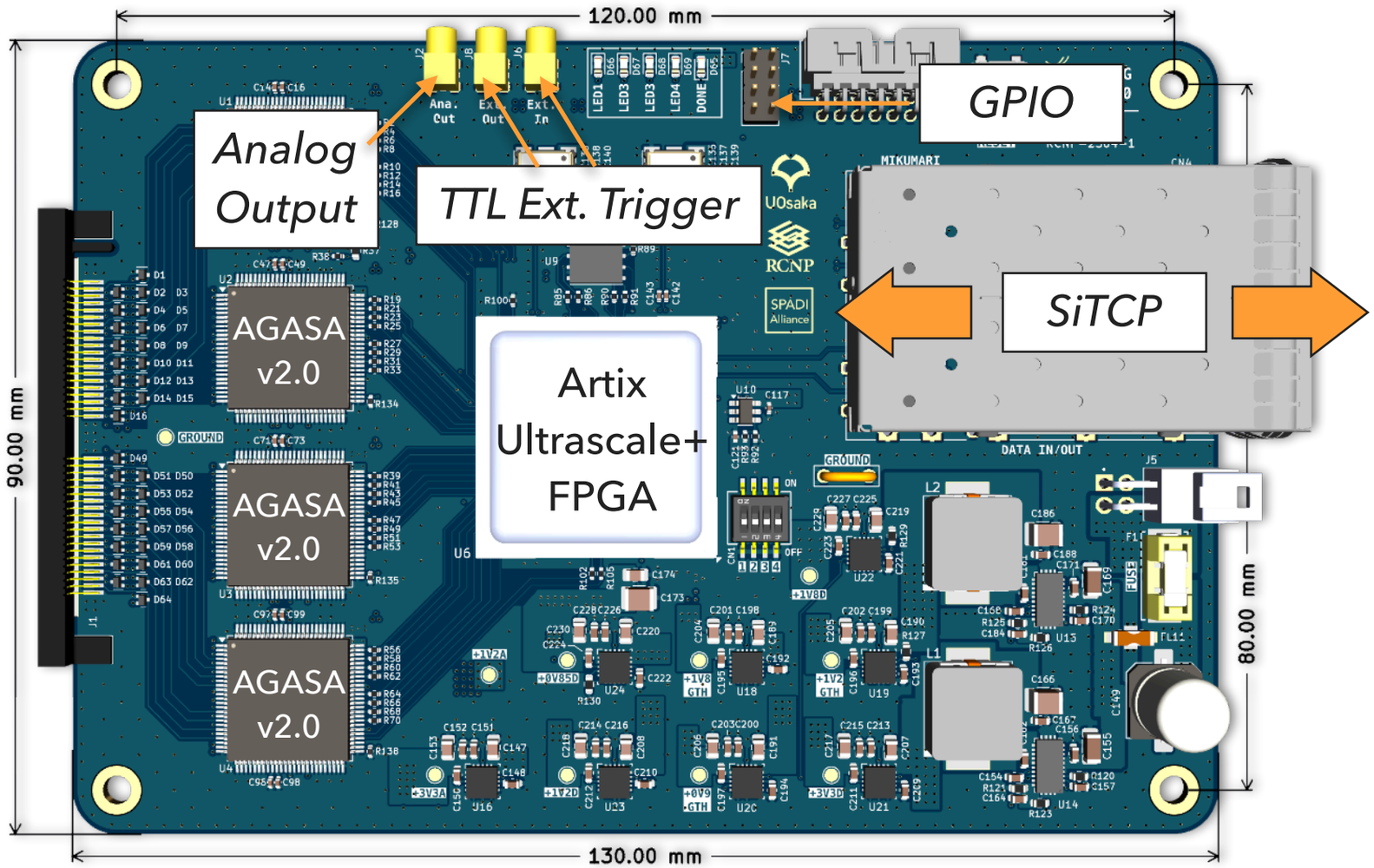
- AGASA comprises of a Charge Sensitive Amp, Pole-Zero cancellation, Shaper Amp, and Comparator (i.e Discriminator).
- Meant to be a generic ASIC, to be used in different gas detectors.
  - Hence, the parameters shown in ***Orange*** are configurable. In other words, you can change the gain, phase, comparator thresholds, etc. Also you can monitor the analog output.



The all-in-one STAG Board

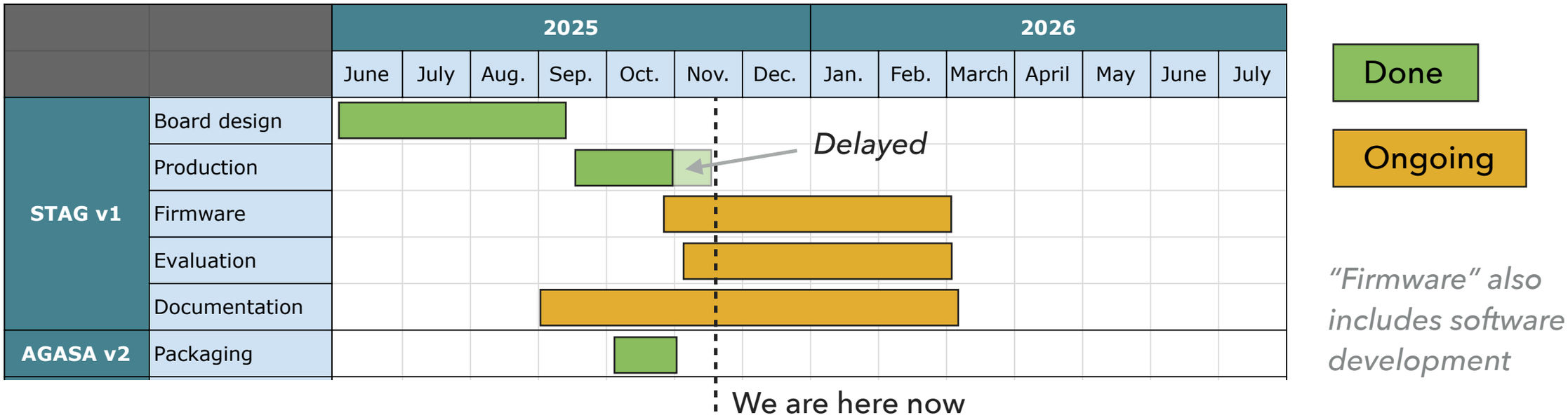
- Other specifications decided by a questionnaire to the SPADI-A community.
  - ***DAQ rates*** ➡ 1 Gbps (~16 Mcps/board)
  - ***Output*** ➡ Mostly ToT, with pulse monitoring.
  - ***Triggering*** ➡ Through MIKUMARI & External TTL signals.
  - ***TDC Resolution*** ➡ 100~300 ps
  - ***Communication*** ➡ SiTCP

Input from 64 VDC channels



STAG board development timeline

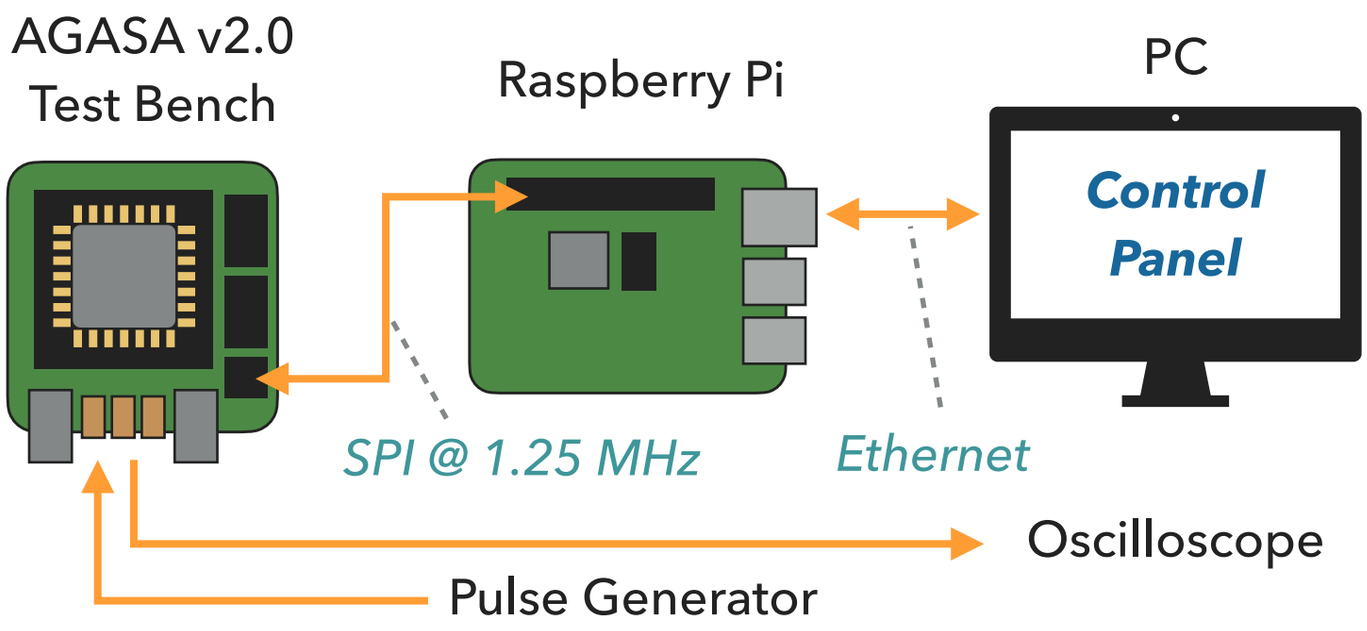
- Several development steps are outlined in the timeline below.
  - STAG v1 board design & production is done, and just arrived in Osaka.
  - We are putting effort in the documentation as well ➡ Creating a knowledge base in all-in-one card designing.

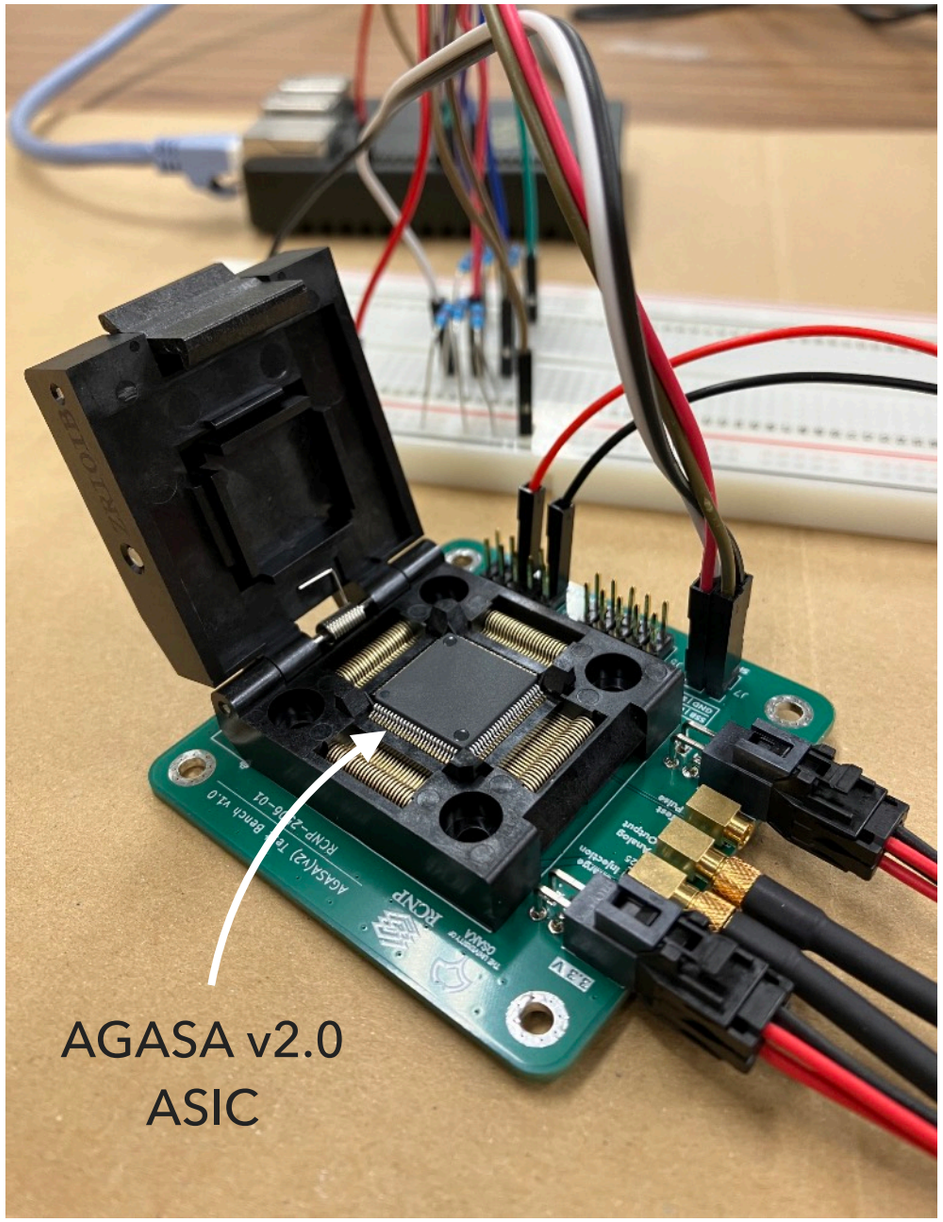


- Since we didn't get the STAG board in time to evaluate, we built a test bench to evaluate the AGASA ASIC.

Evaluation of the AGASA v2.0 ASIC

- Designed a test bench to test the AGASA v2.0 ASIC. This test bench has several purposes,
  - To develop the STAG board control software.
  - To test the ASIC's that before placing on the STAG board.
  - Eventually expand as a QA/QC test bench.





AGASA v2.0 Test Bench

The development towards STAG control panel

- Developing as a prototype for the AGASA v2 test bench, and then expand to the STAG control panel based on user feedback.

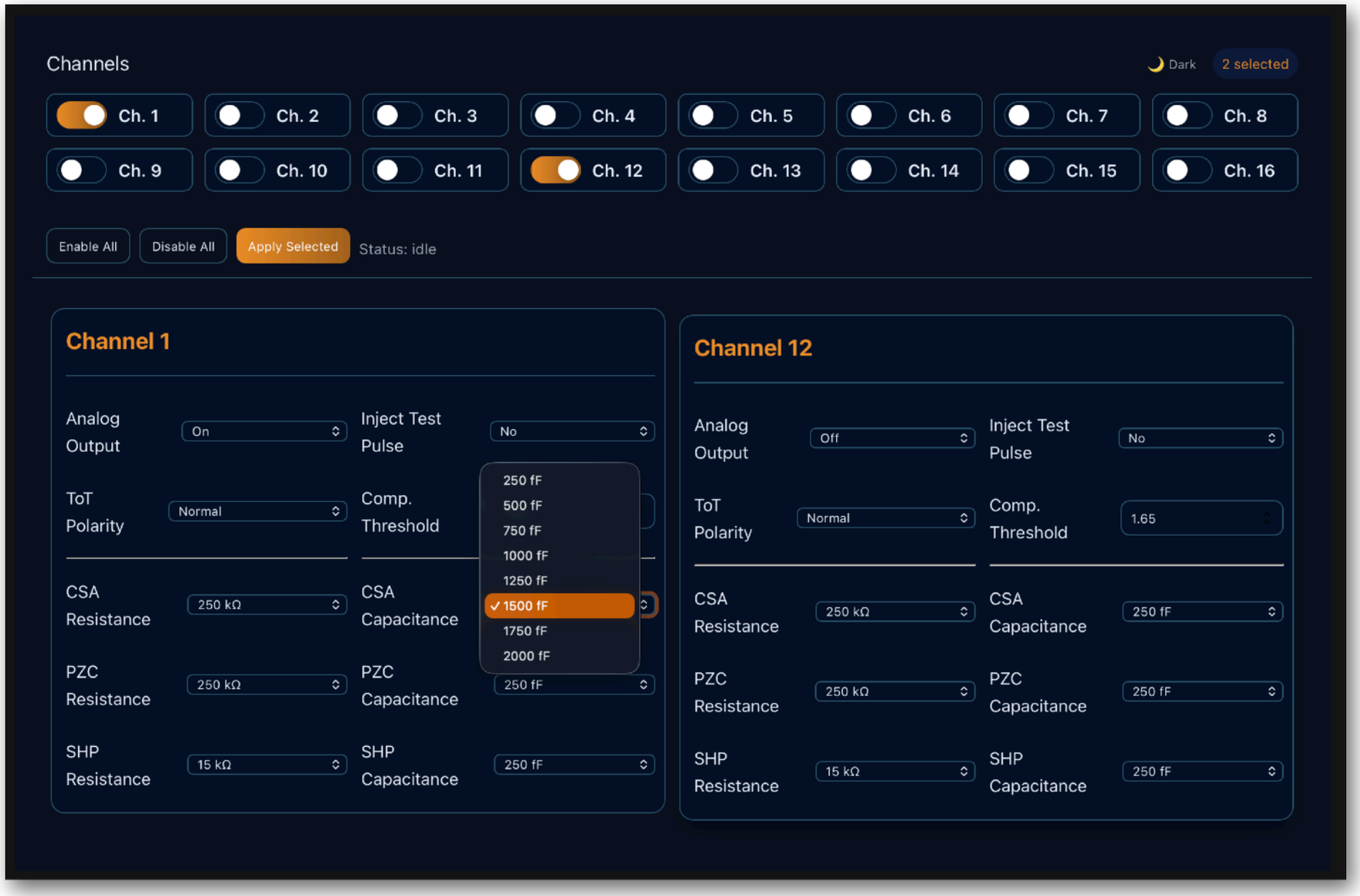
Developed using

Vue.js

(Front-end UI)

FastAPI

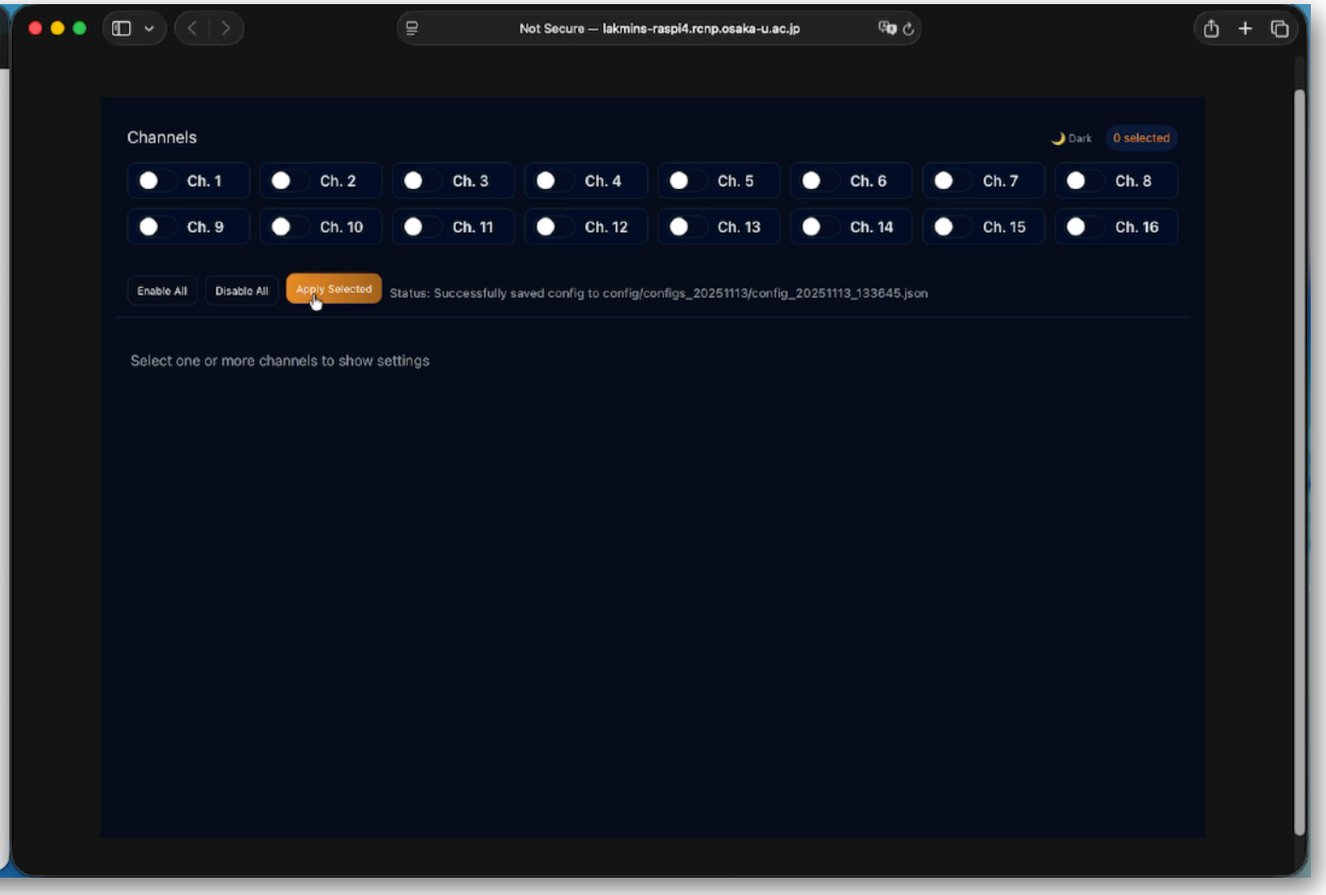
(To handle back-end responses)



The demonstration of the control panel

Oscilloscope

Control Panel (for AGASA test bench)



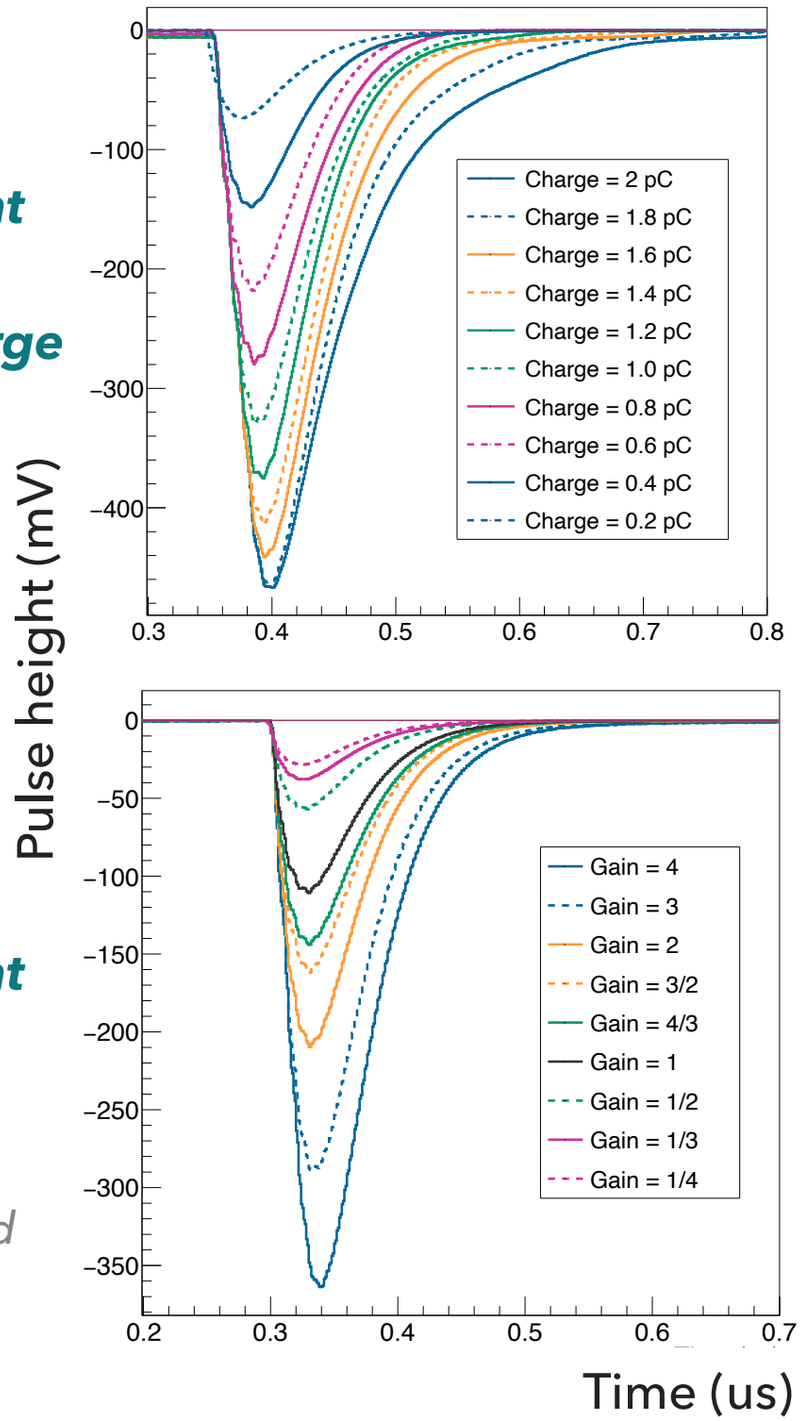
- Still very much under development ➡ Any feedback towards improvement of the tool is welcome!

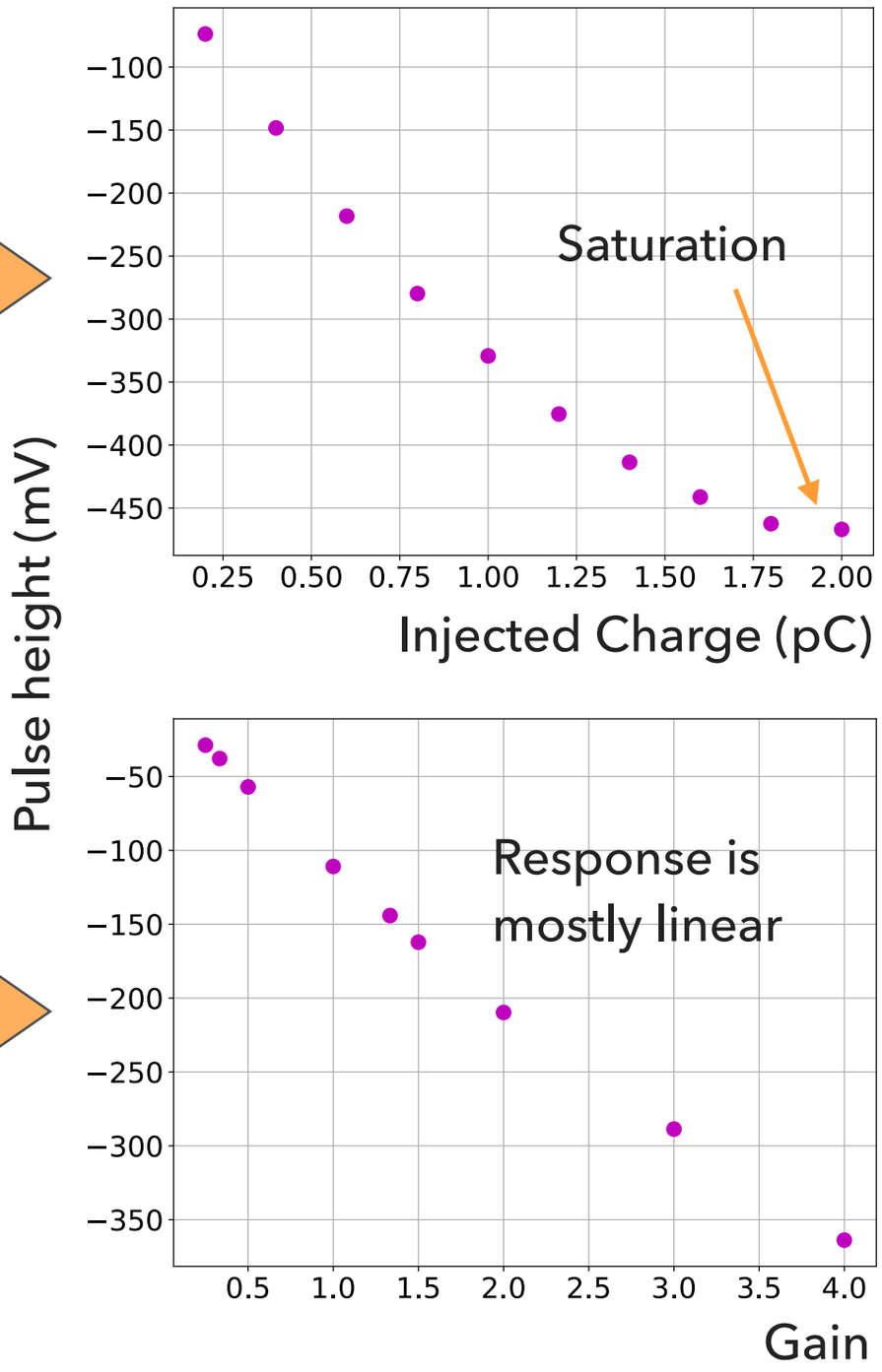
Evaluation of the AGASA v2.0 ASIC

Pulse Height

vs

Injected Charge





Pulse Height

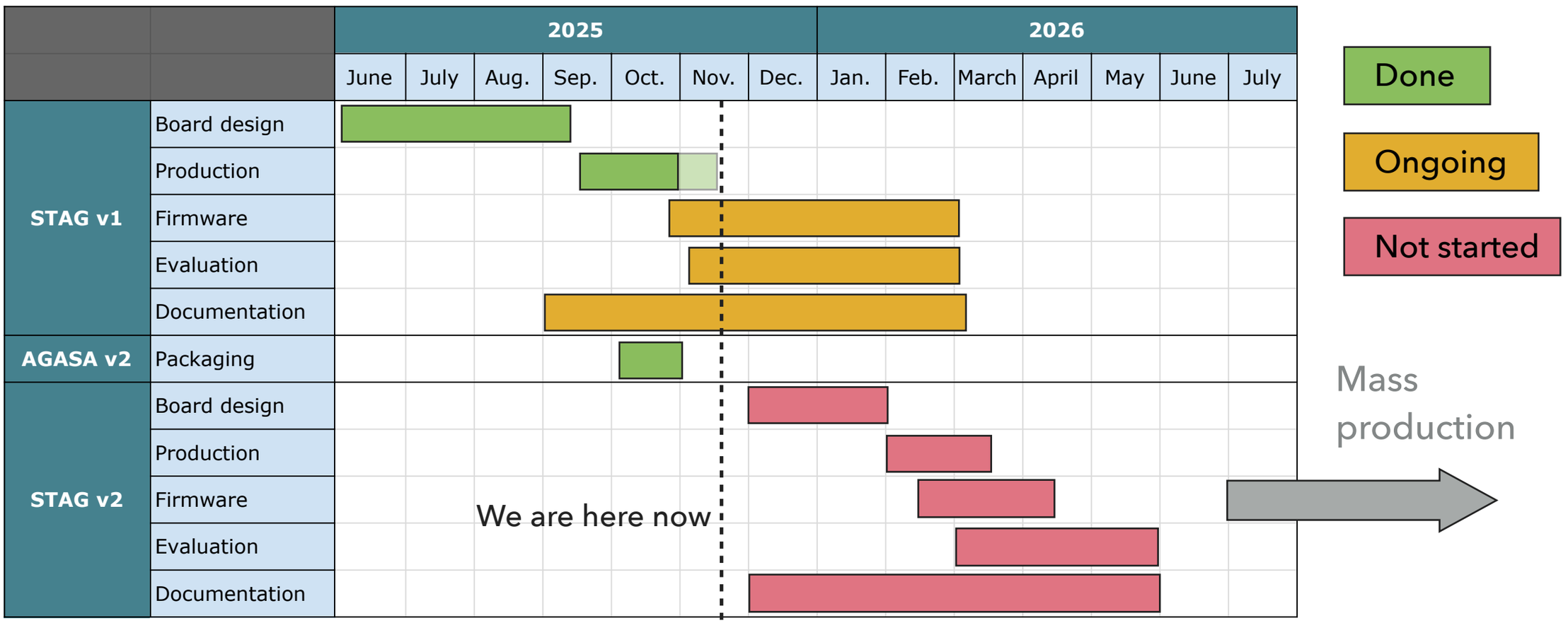
vs

GAIN

For an injected 0.3 pC pulse

STAG board development timeline

- STAG v2 development is planned to start soon.
  - STAG v1 is developed as a prototype, so STAG v2 will be the production version.
  - After the STAG v2 evaluation, we aim determine the final version to be mass produced.



"Firmware" also includes software development

Summary & remarks

- As a part of the JST K-program, we are developing an all-in-one readout boards for different air shower detectors.
- In RCNP, we are developing an all-in-one readout board for gaseous detectors.
  - Combine the ASD and TDC in one board, while being compact and generic.
  - Ability to handle 1 Gbps data rates, 100~300 ps TDC resolution, etc.

- Development ongoing as a part of the SPADI alliance WG1 task force,
  - People who are interested are welcome to join!

K Program
経済安全保障重要技術育成プログラム

本研究は、JST経済安全保障重要技術育成プログラム【JPMJKP24J2】の支援を受けたものです