# Belle II実験データ収集システム

山田悟 (KEK素核研)

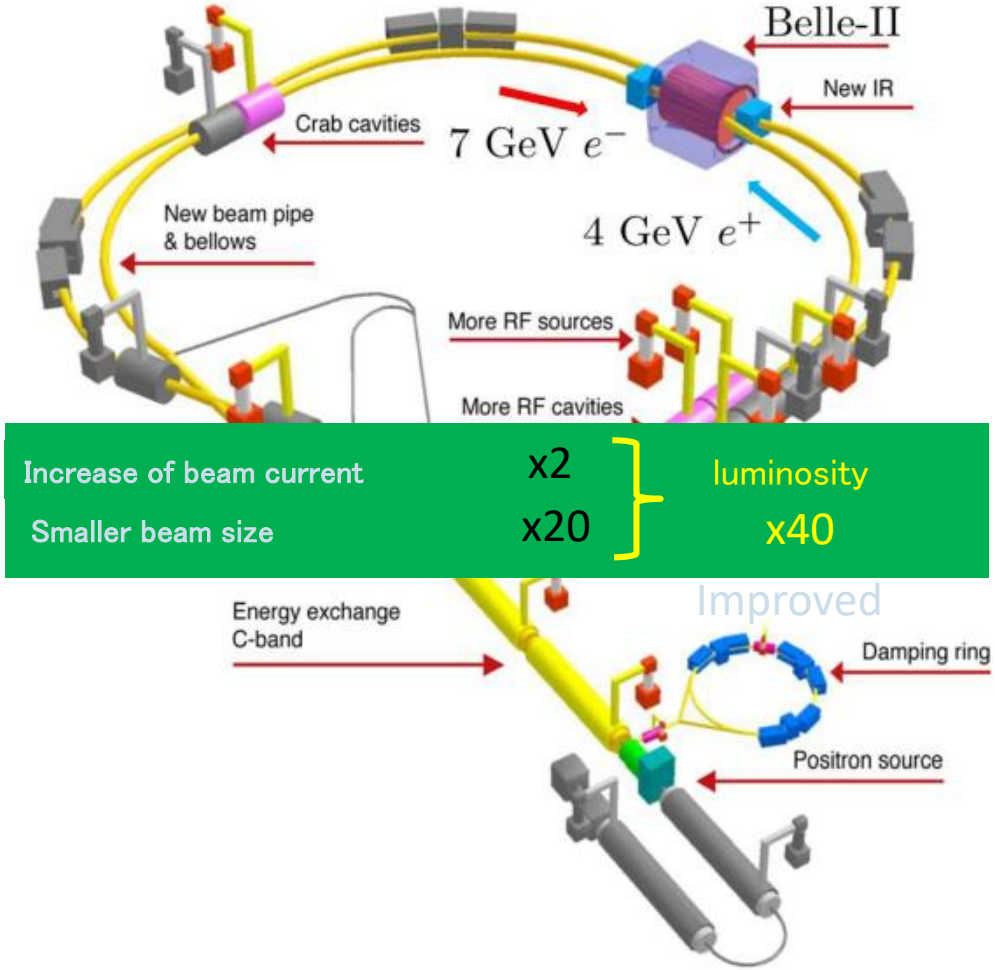
1. イントロダクション
2. Belle II データ読み出しシステム
3. DAQシステムのパフォーマンス
4. 外層検出器の宇宙線試験
5. Belle II 読み出し系のアップグレード計画

# Belle II実験

➢ Search for new physics beyond the Standard Model(SM) via high precision measurement with high statistics samples of B/D/tau decays.

➢ **SuperKEKB accelerator**
- ➢ Designed luminosity: 40times as large as KEKB
- ➢ 50 $ab^{-1}$ in 10 years
  (cf. 1$ab^{-1}$ @ Belle experiment)

Belle II collaboration :
～750 collaborators from 24 countries



# SuperKEKB のルミノシティ(予測)

**Phase I : (2016 Feb.-Jun.)**

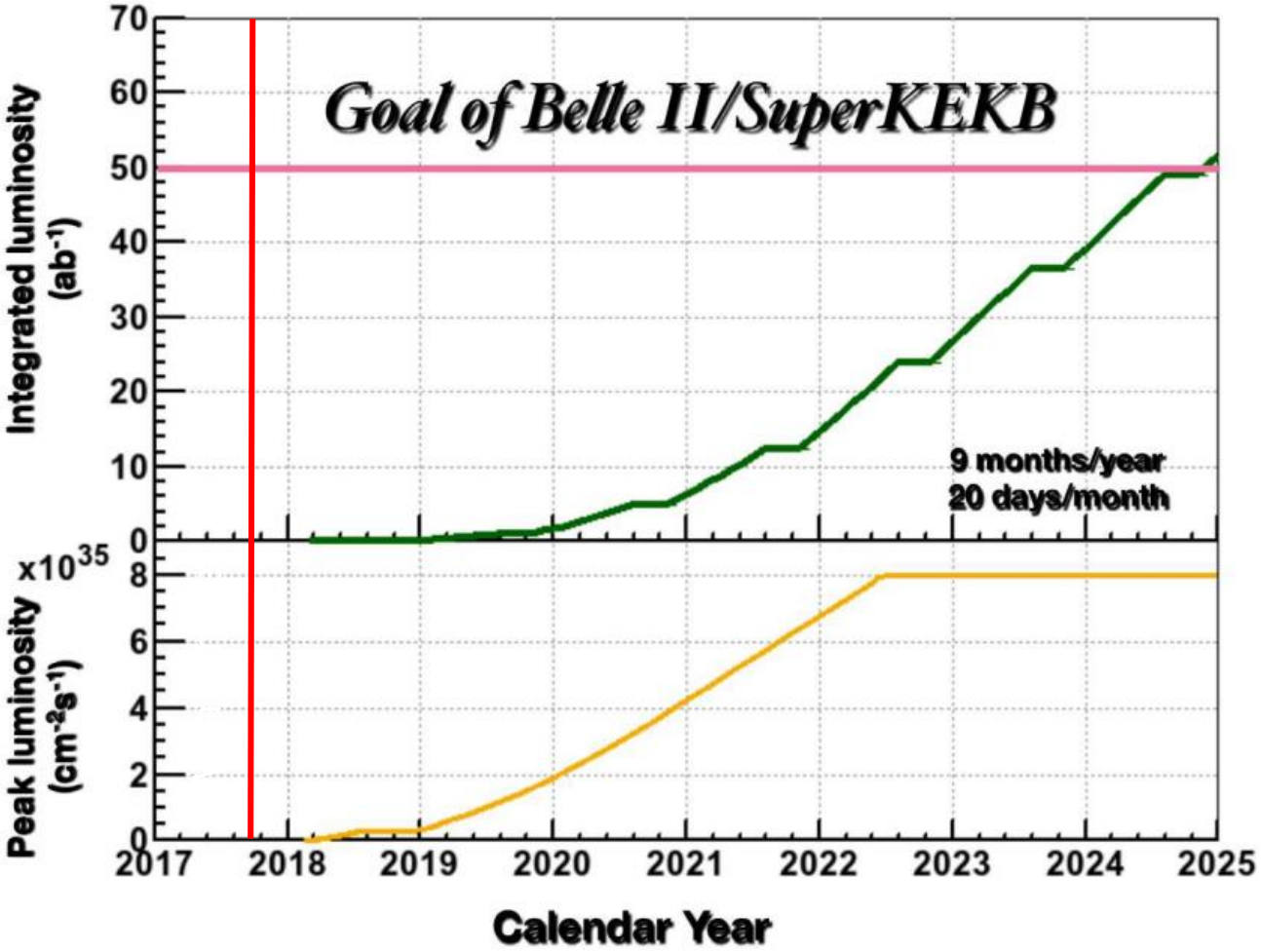
- Accelerator commissioning w/o final focusing magnets
- w/o the Belle II detector
- First turns of SuperKEKB
- Vacuum scrubbing

**Phase II : (2018Feb.-Jul)**

- Accelerator commissioning and physics run
- with the Belle II detector except for vertex sub-detectors

**Phase III : (around the end of 2018-)**

- Physics run with the full Belle II detector



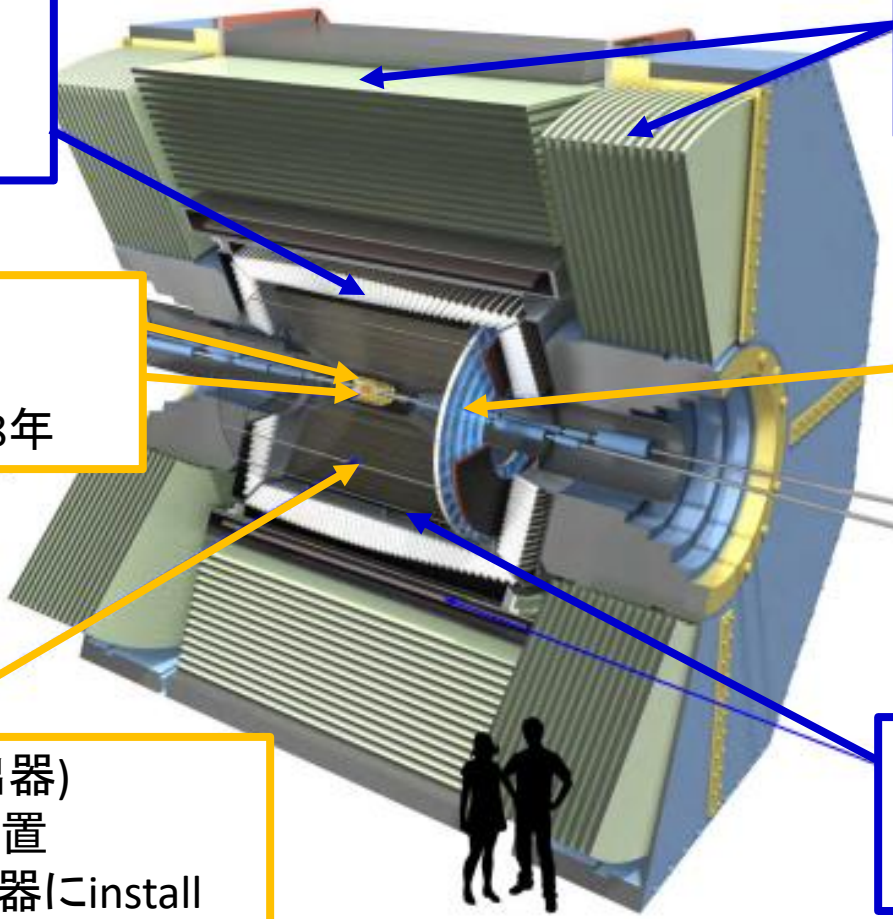
# 各detectorのインストール状況

ECL(電磁カロリメータ)
-> install済み

KLM(Klong muon検出器)
-> install済み

崩壊点検出器
(PXD,SVD)
完全なinstallは2018年

ARICH(エアロジェルリングイメージングチェレンコフカウンタ)
実験ホールで組立作業
2017年にinstall



CDC(中央飛跡検出器)
実験ホールに仮設置
10月にBelle II検出器にinstall

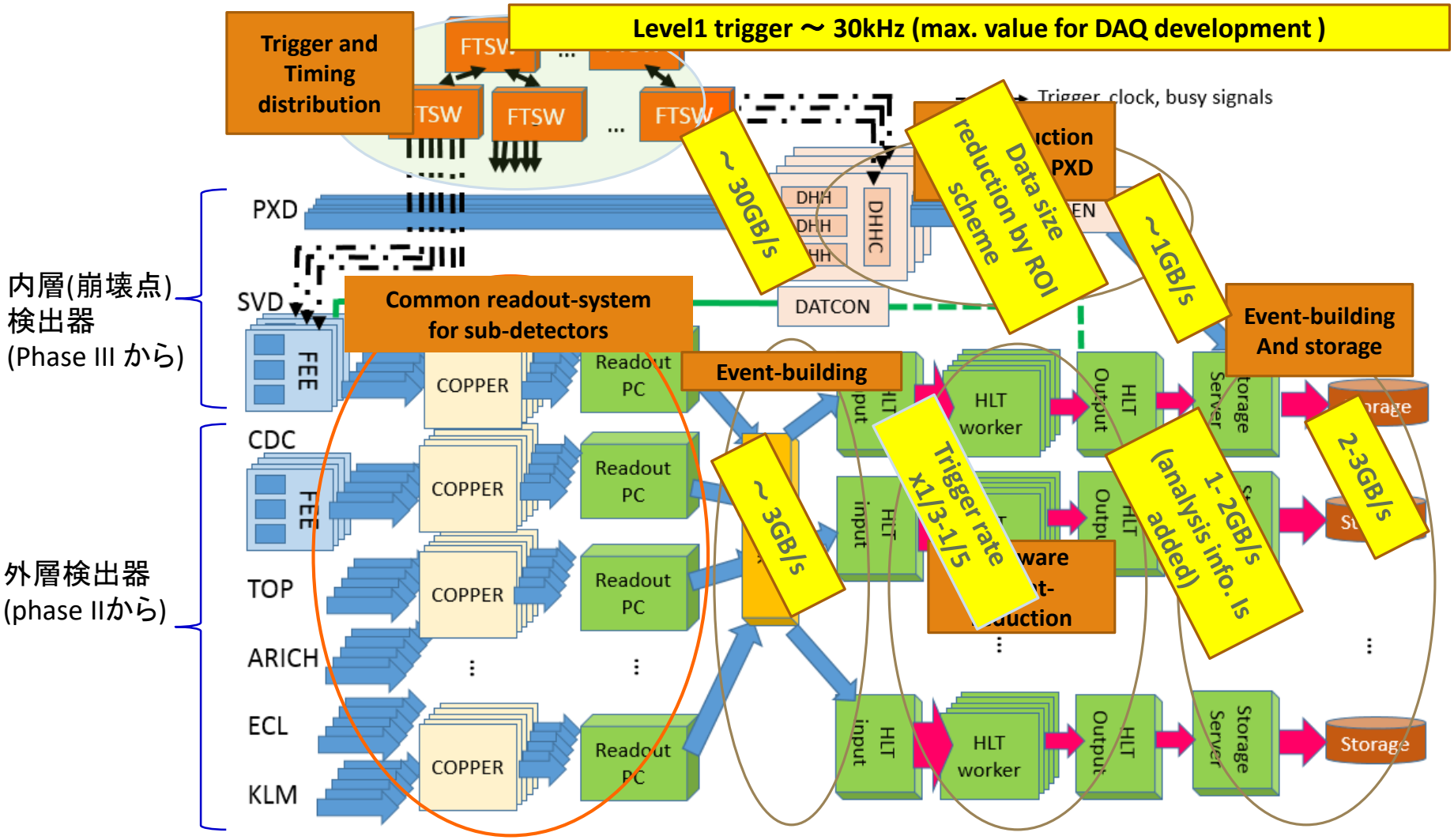
TOP(Time of Propagation)カウンタ
-> install済み

# 測定器設置、コミッショニング等のスケジュール

1. イントロダクション
2. Belle II データ読み出しシステム
3. DAQシステムのパフォーマンス
4. 外層検出器の宇宙線試験
5. Belle II 読み出し系のアップグレード計画

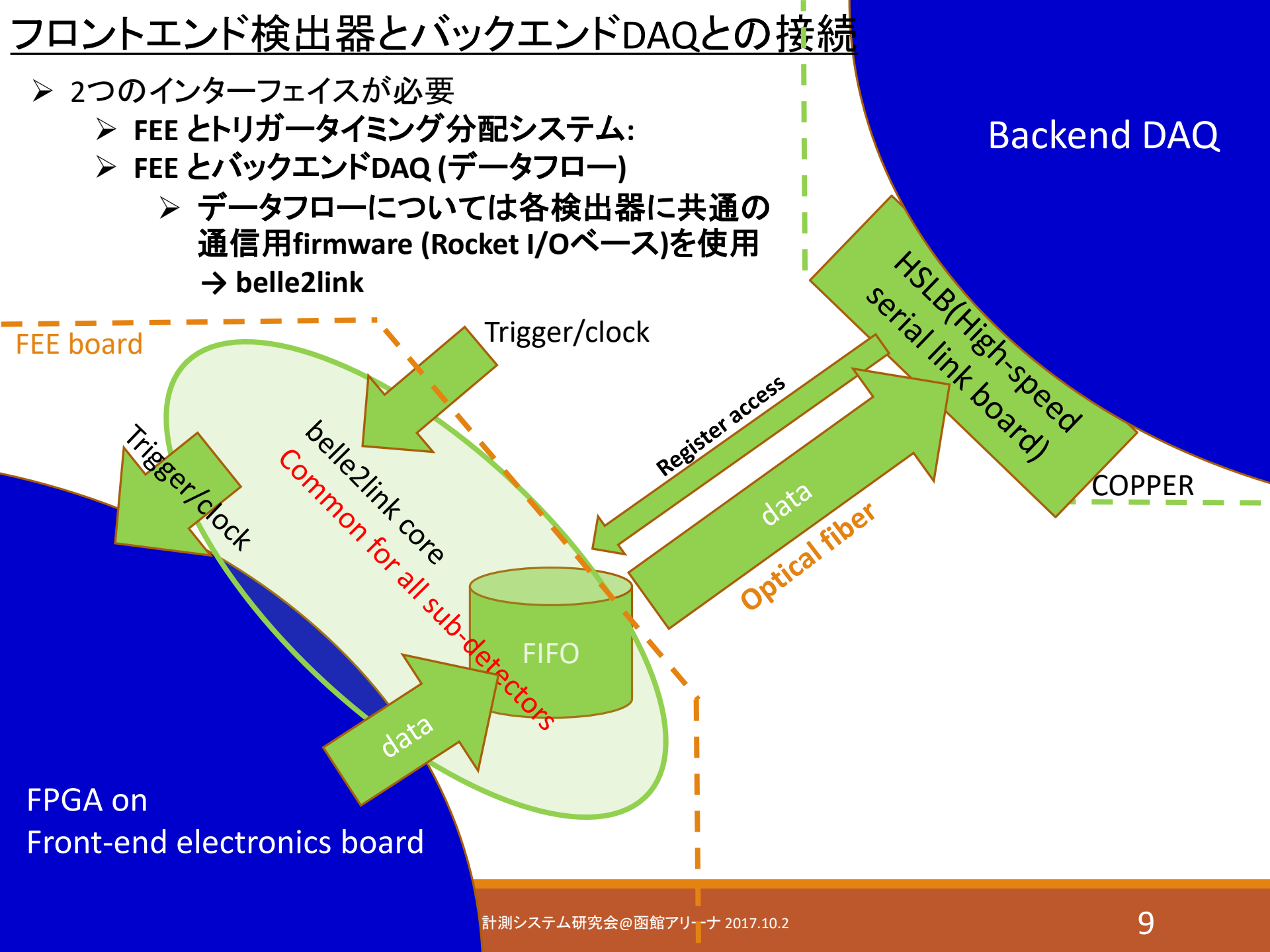
# Belle IIデータ収集システム (今回は読み出しシステムの話を主に)

- FEEとのinterfaceは各検出器共通(PXD以外)
- HLTによるrate reduction + Region of InterestによるPXDのevent size reduction



# フロントエンド検出器とバックエンドDAQとの接続

- 2つのインターフェイスが必要
  - **FEE とトリガータイミング分配システム:**
  - **FEE とバックエンドDAQ (データフロー)**
    - **データフローについては各検出器に共通の通信用firmware (Rocket I/Oベース)を使用**
      **→ belle2link**



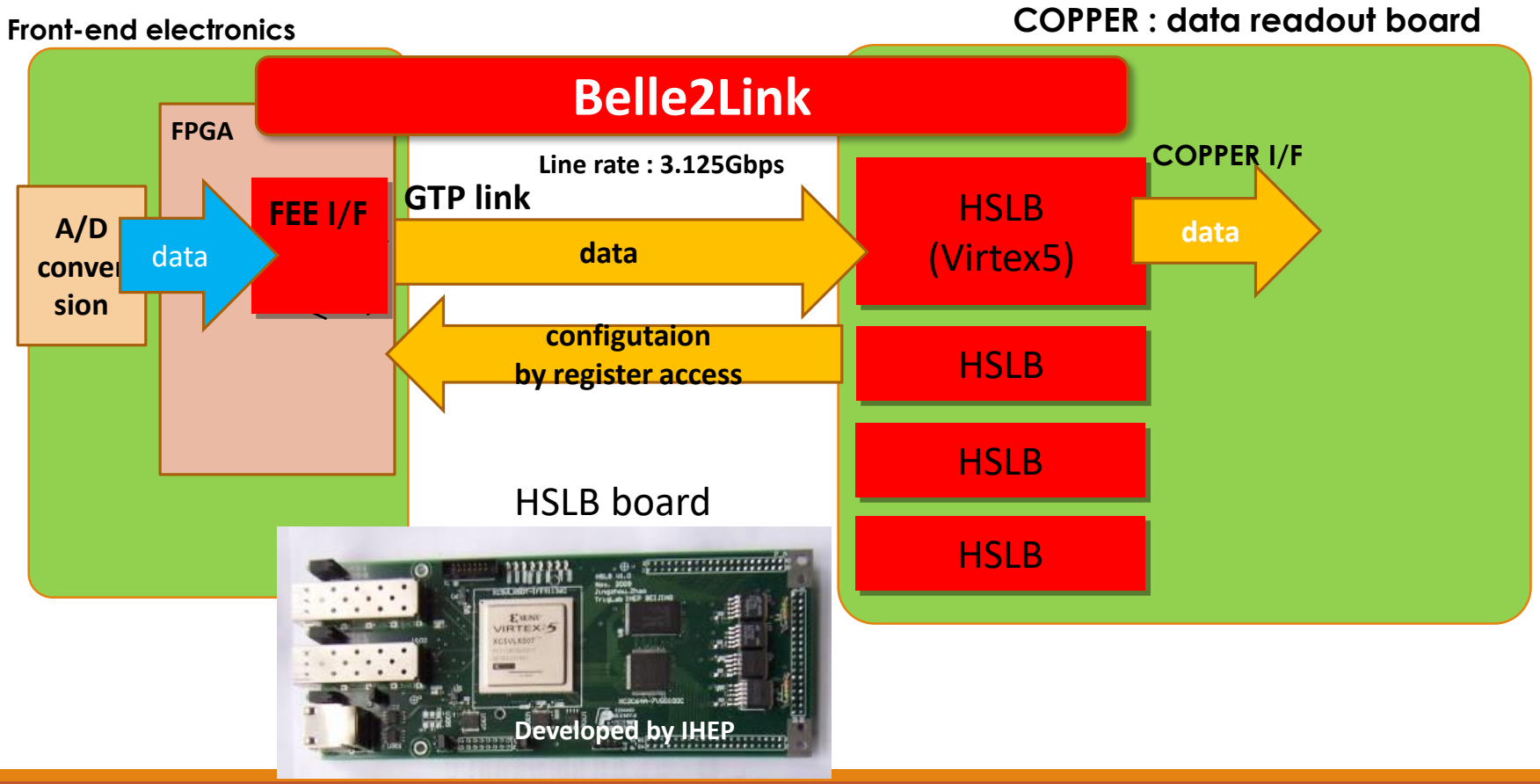
# フロントエンド電子回路からのデータ読み出し

## Belle2Link : (D. Sun et. all, hysics Procedia Volume 37, 2012, pp. 1933-1939 )

Unified high speed link which connects Front-End Electronics (FEE) and DAQ system for signal with data transmission based on Rocket I/O

FEE side : Functions for I/F with FEE and Trigger Timing Distribution on FPGA

DAQ side : High Speed Link Board(HSLB) as a data receiver

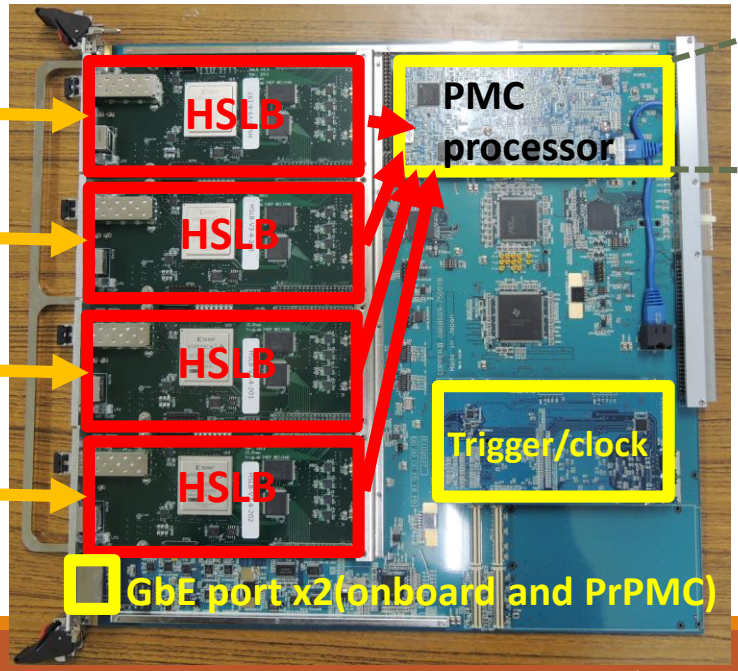


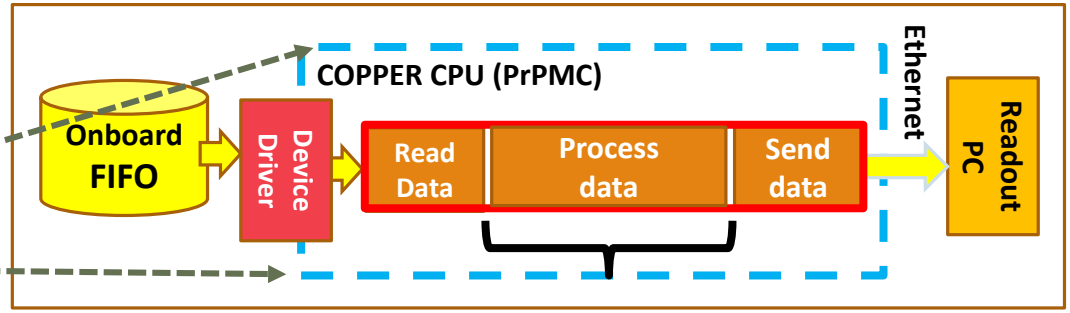
# 読み出しボードでのデータ処理

- Readout board : COPPER ( COmmon Pipelined. Platform for Electronics Readout )
  - Versatile DAQ board developed at KEK
    -> basically same functionality in the previous Belle experiment
  - can be equipped with various I/O cards and CPU card
    -> new daughter-boards for Belle II are used


- CPU: Intel Atom 1.6GHz Z530P
- DDR2 SDRAM 512MB
- PXE boot from ROPC
- Gigabit Ethernet x1

**COPPER board**

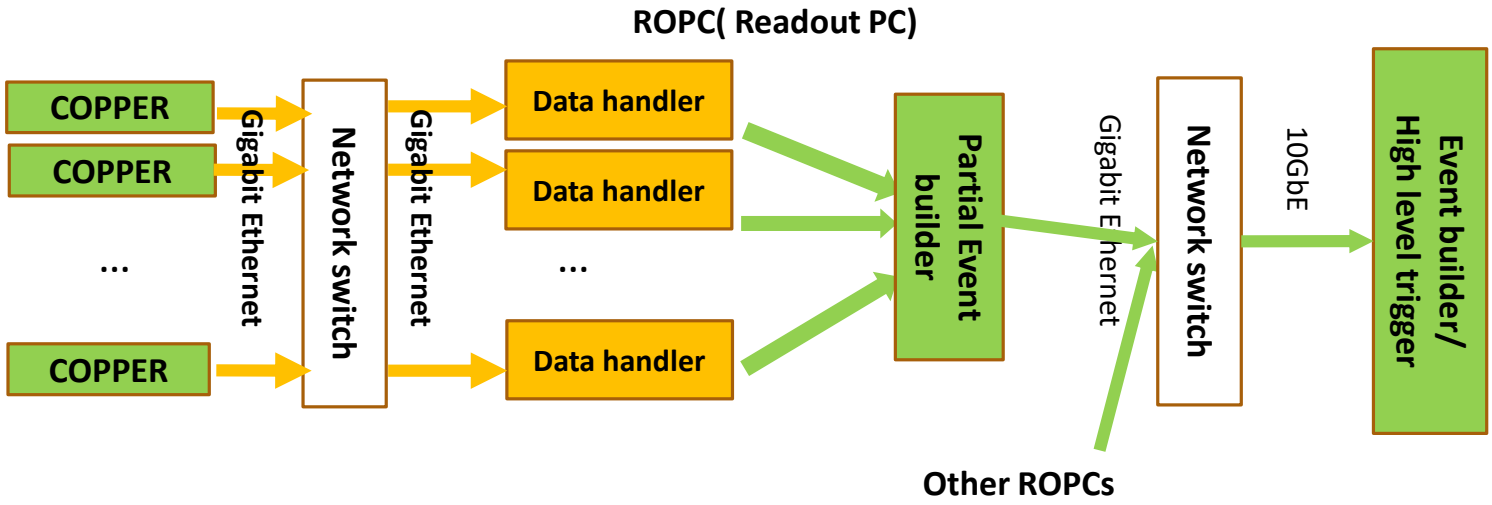



- **Data processing on COPPER CPU**
  - Data formatting (Add header and trailer to raw data)
  - Plain data check
    - Event incrementation, check magic word etc.
  - Add XOR checksum
  - Report data-flow status to slow control

# 読み出しPC上でのデータ処理

I. data check by data-handler process
   I. Calculate CRC16 and compare CRC value attached by FEE
   II. XOR checksum calculated by software on COPPER
II. Data size reduction
   merging redundant header/trailer attached by b2link and COPPER )
   Reduction by 15MB/s/ROPC at 30kHz trigger rate( <- 5COPPERs/ROPC, 4HSLB/COPPER )
III. Collect data from several COPPERs and do partial event-building and send data to High level trigger unit.



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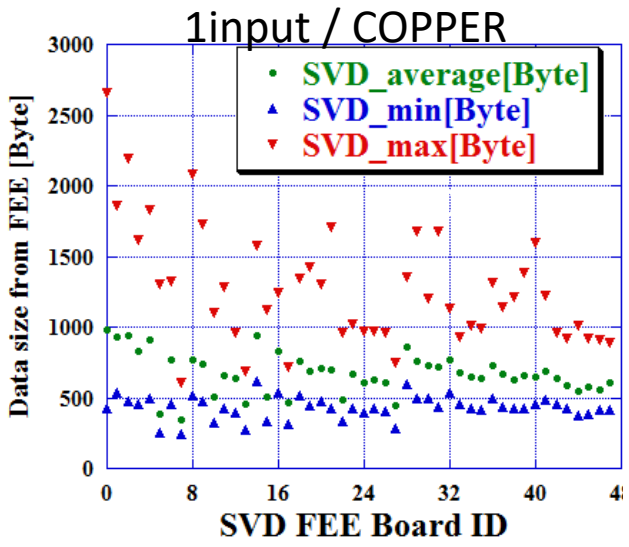
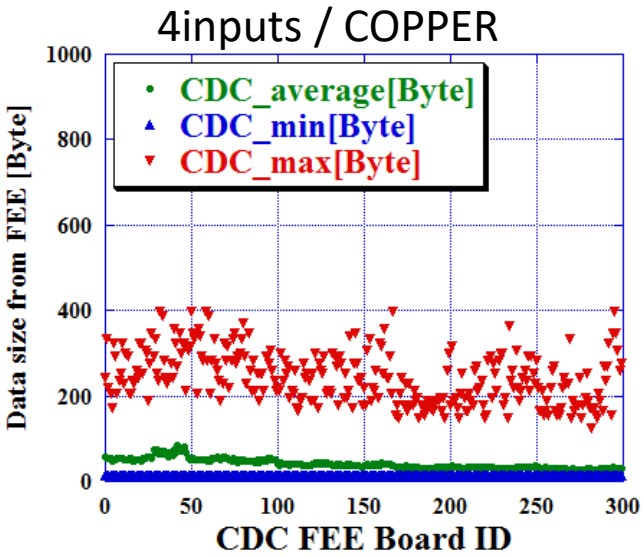
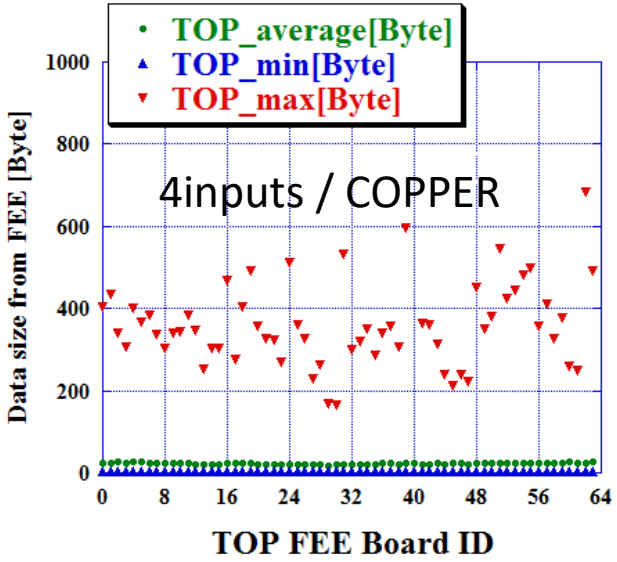
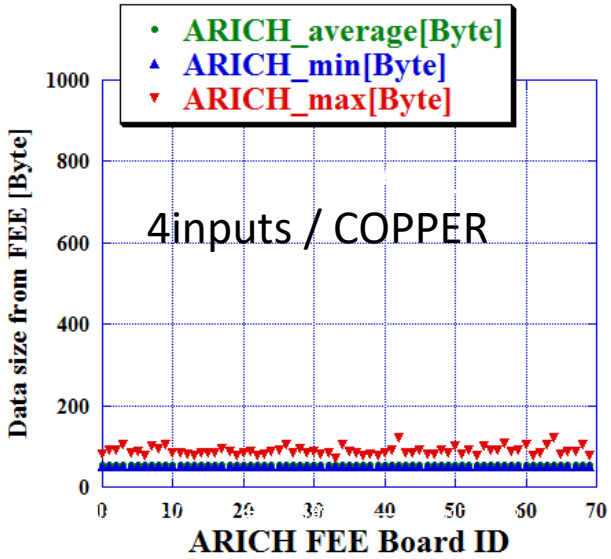
# 各検出器でのBelle II のイベントサイズ見積もり

More detailed data size estimation for some sub-detectors with MC data to consider assignment of readout boards.

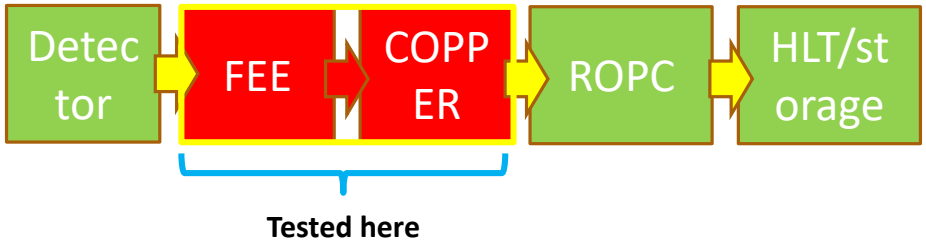



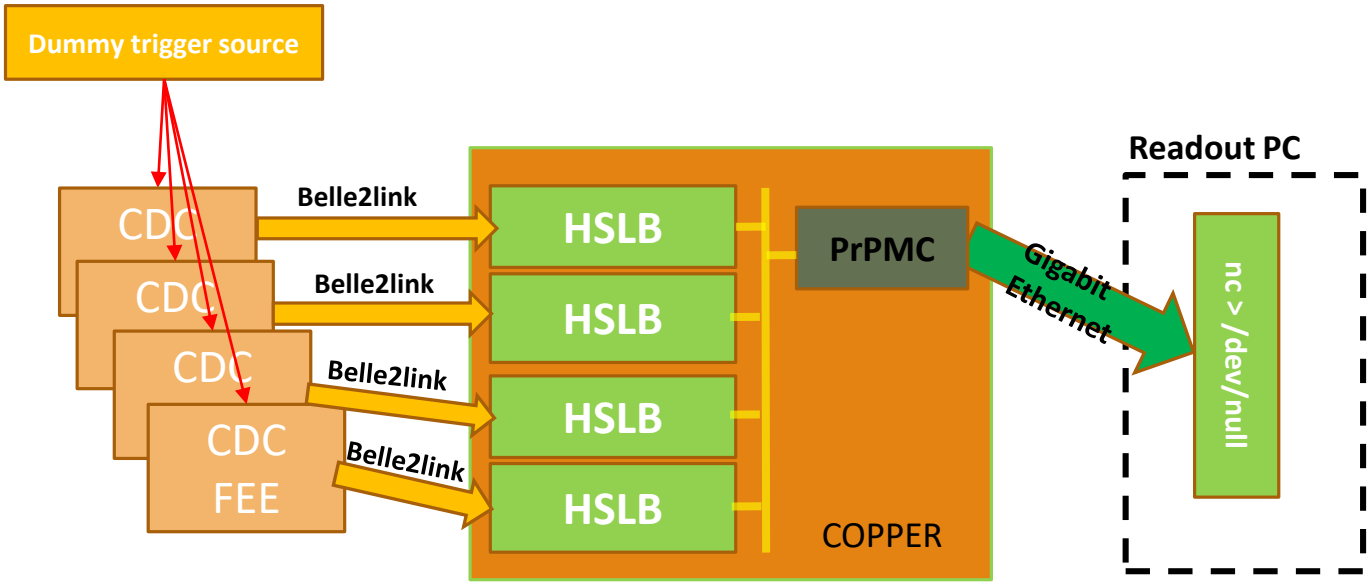




- Difference of event size is handled by the number of receiver cards on COPPER
- SVD : 1HSLBs/COPPER
- ECL : 2HSLBs/COPPER
- CDC/TOP/ARICH/KLM : 4HSLBs/COPPER

# パフォーマンス測定(1)：FEEとCOPPER CPU



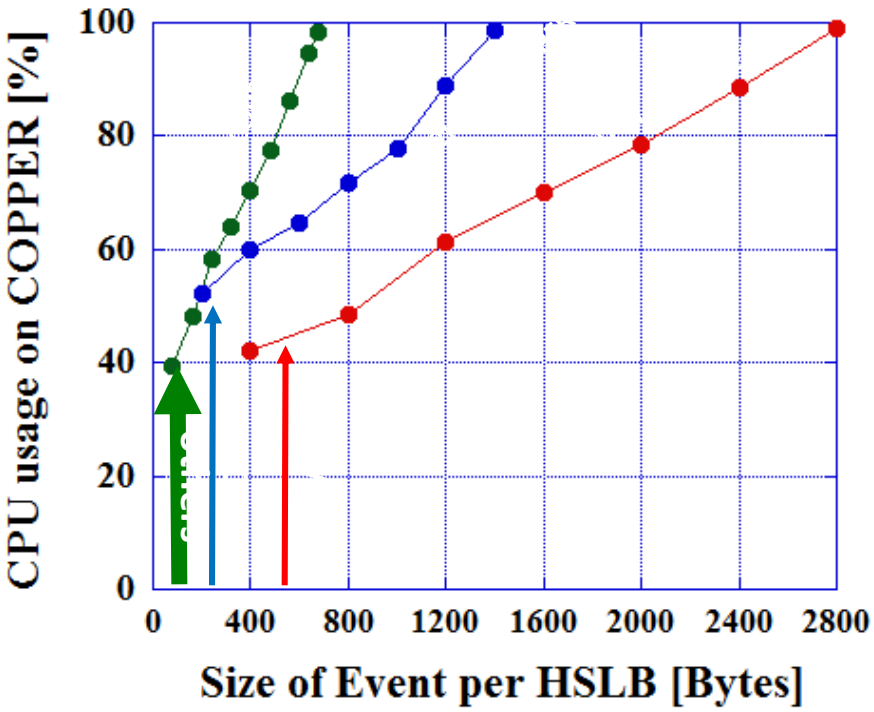

- Test setup



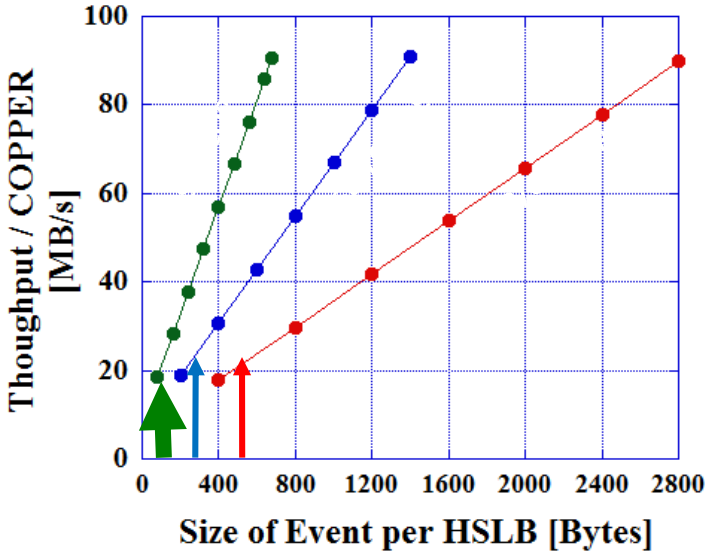

We can test
- data-transfer performance of belle 2link
- CPU usage on COPPER PrPMC

# 結果:

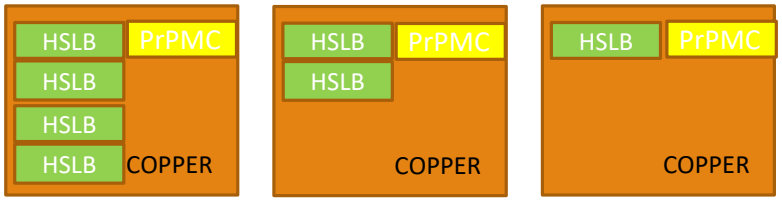
CPU usage on COPPER PrPMC




Throughput from COPPER




- 30kHz operation was achieved.
- CPU usage will be the bottleneck when the event size becomes larger than expected.
- Throughput in Belle2link and Gigabit Ethernet to a readout PC has still enough remaining room.



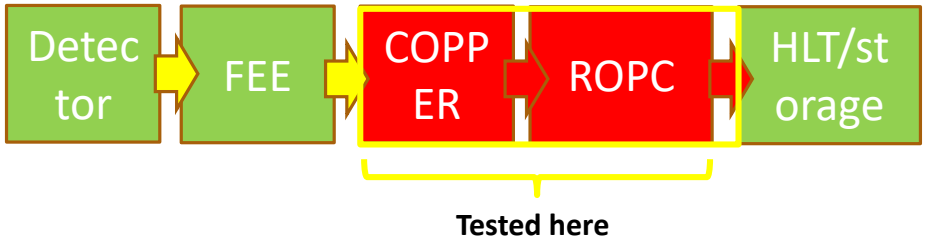

CDC
TOP
ARICH
KLM

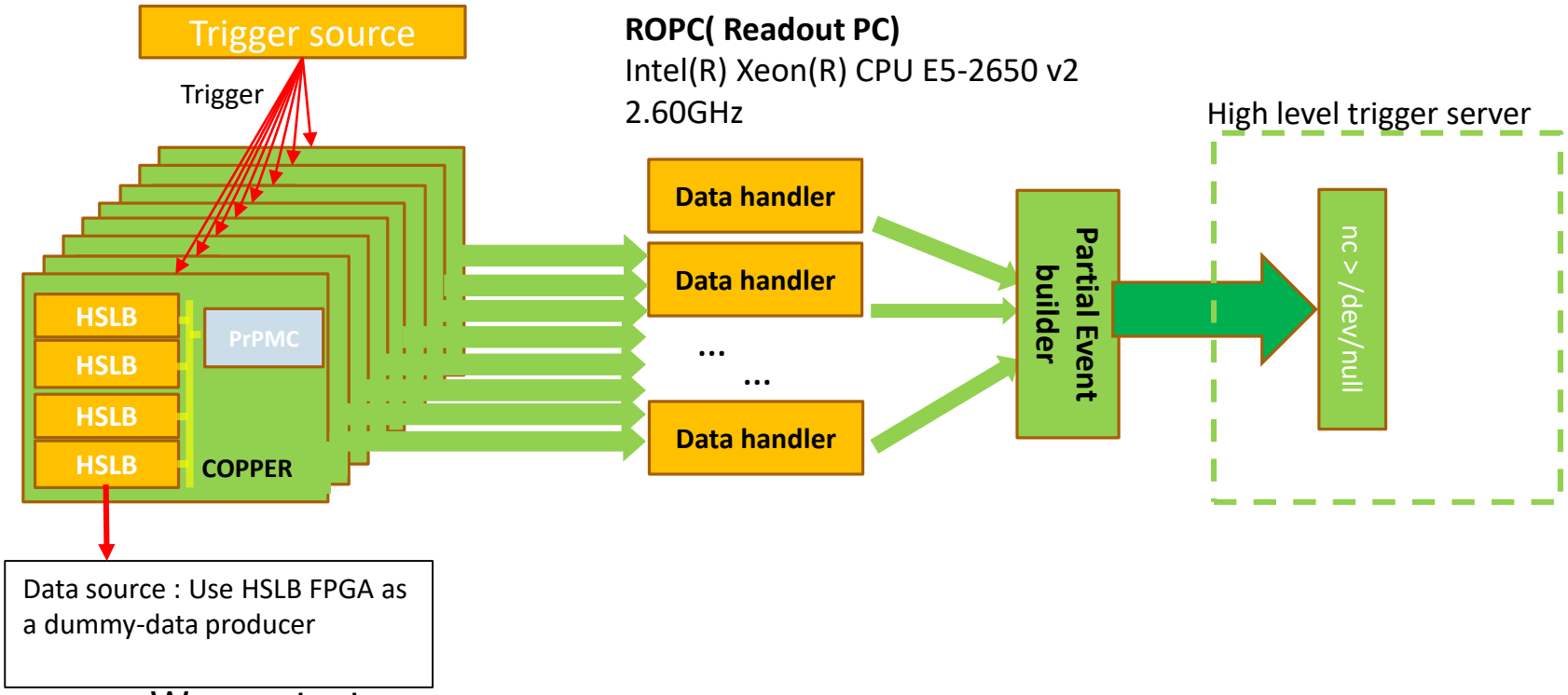
ECL

SVD

# パフォーマンス測定(2)： COPPER -> readout PC

- 1ROPC and several COPPERs.
- # of COPPERs differs over sub-detectors due to the difference of event size
- Provide trigger to COPPER board to produce dummy data by HSLB.



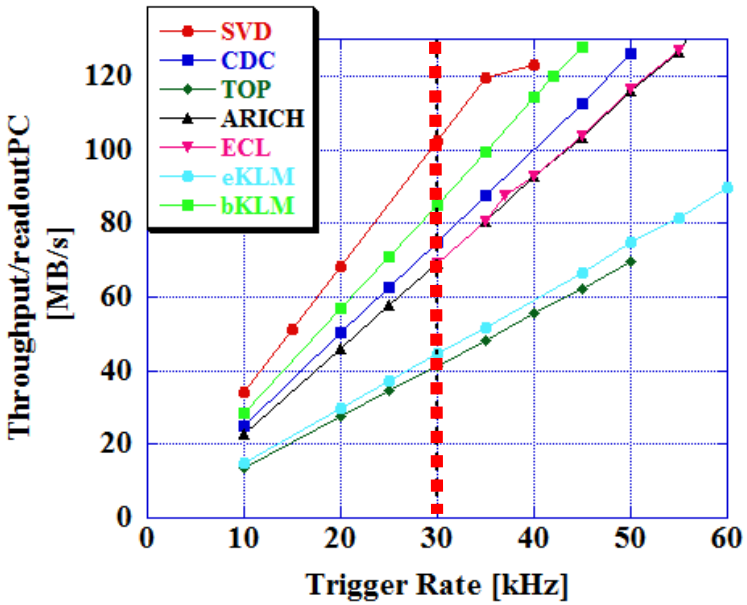




We can test

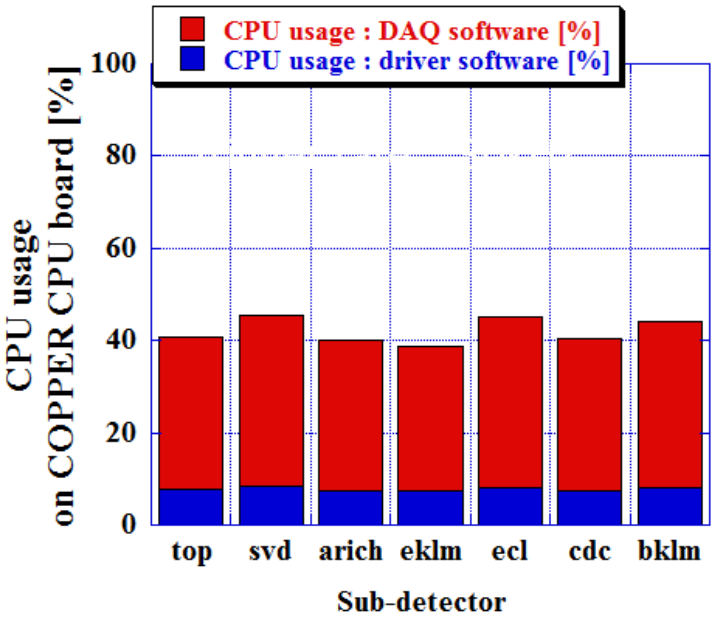
- Processing power of COPPER and ROPC
- data-transfer performance between COPPER and ROPC, ROPC and HLTin.

# COPPER -> readout PC　結果：

Throughput on ROPC




CPU usage on COPPER

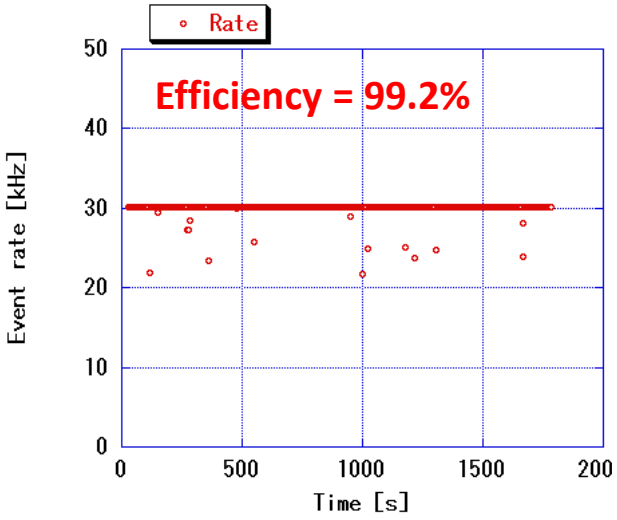



- 35kHz for SVD is the max. event rate.
- Bottleneck : Output data flow to HLT is near the limit of GbE.
  - CPU usage on COPPER CPU is still room to increase the rate
- Increase # of Readout PCs or increase throguhtoput between ROPC and HLT will increase the limit.

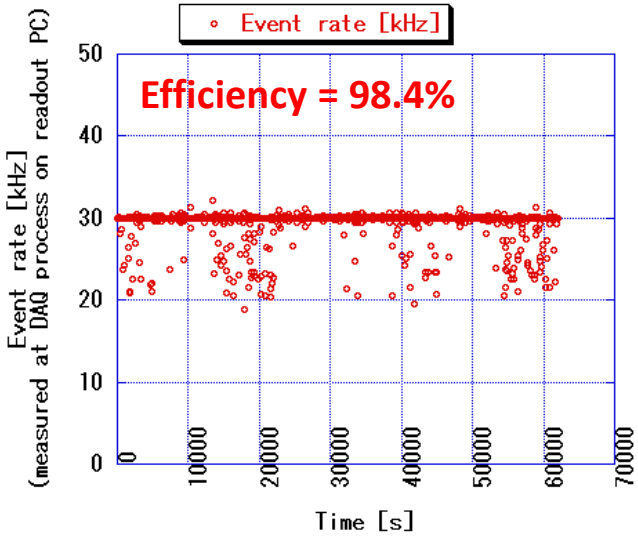
# ECL検出器での high rate testの結果

- Setup : 36FEE -> 18 COPPERs -> 7 readout PC
- Throughput : about 33MB/s/COPPER ( the expected event size from MC )
  - Event size was adjusted by HIT threshold of ECL FEE
  - Total throughput for Barrel ECL : 600 MB/s
- Constant 30kHz trigger -> efficiency = 99.2%
- Pseudo-Poisson 30kH trigger -> efficiency = 98.2 %
  - The deadtime comes from trigger limitation (5trigger in 26us due to SVD FEE ).

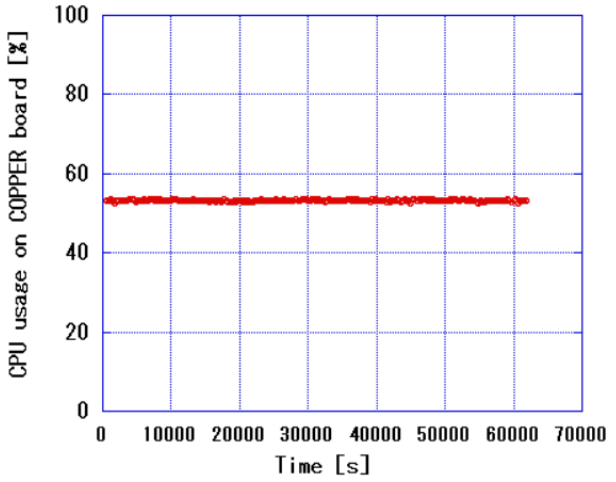
Constant 30kHz trigger rate




Pseudo-Poisson 30kHz trigger rate

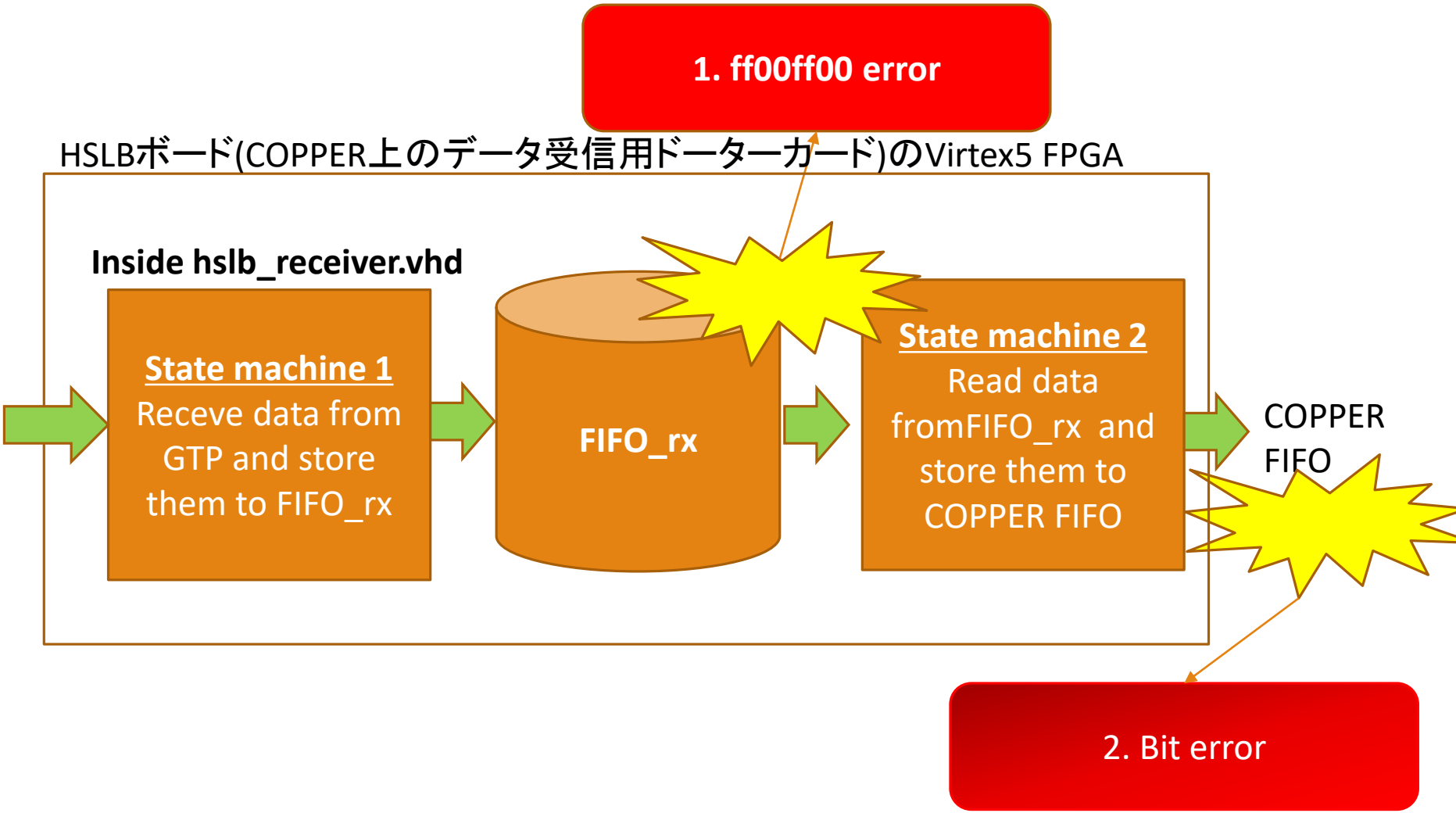



CPU usage on a COPPER board

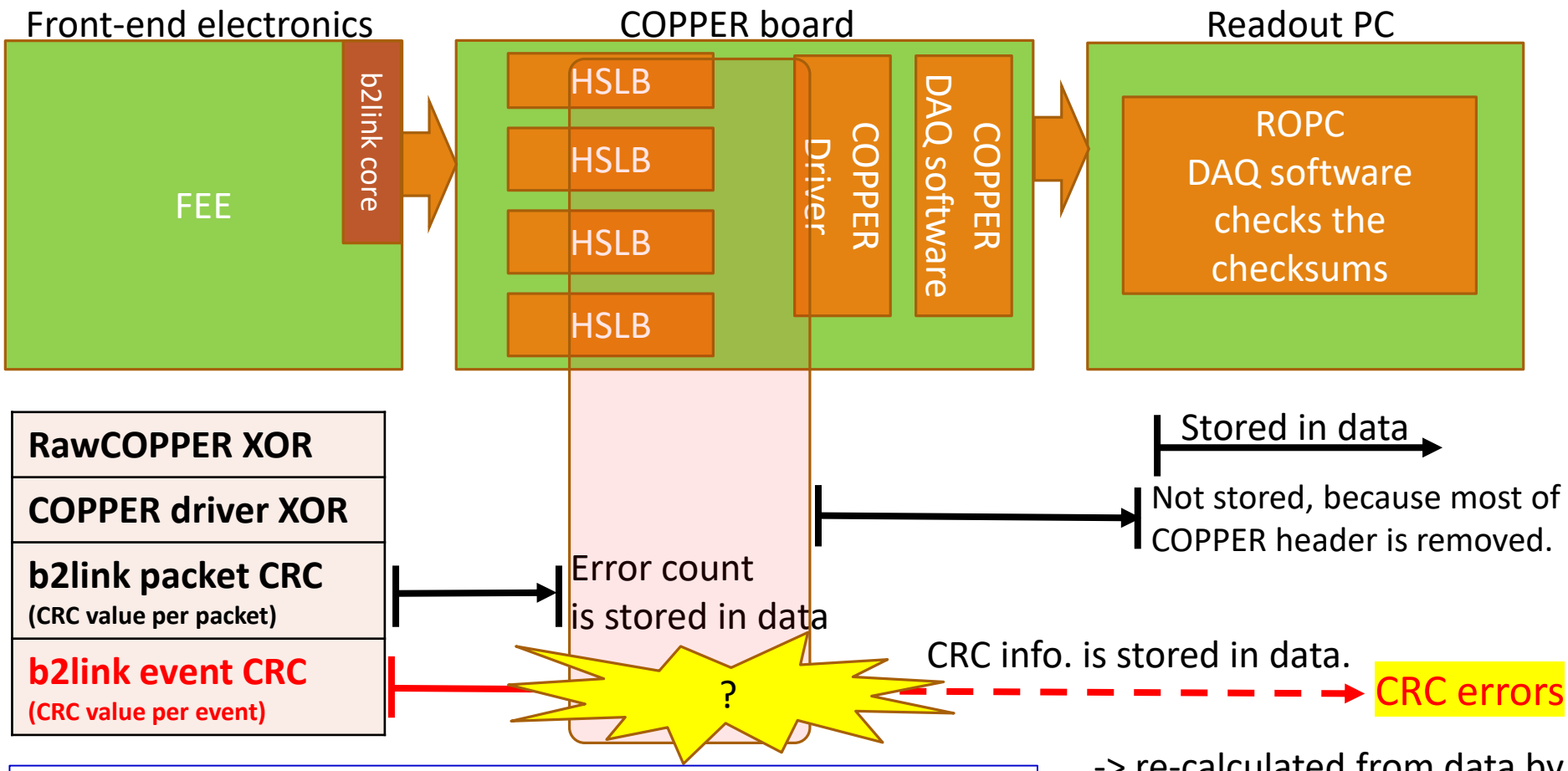



-> High efficiency(nearly 100%) was achieved !

# COPPERボード上でのデータ化け問題



# How CRC error is detected




"b2link packet CRC" has not been observed.
-> b2link transmission is O.K.
But "b2link event CRC" error was detected.
-> Data should be corrupted after receiving data from a FEE.

# 1. FPGA内でのデータ化け

- A large amount of ‘ff00ff00’ appeared after an FEE footer
- “b2link packetCRC” error is not detected. -> data corruption after HSLB received data.

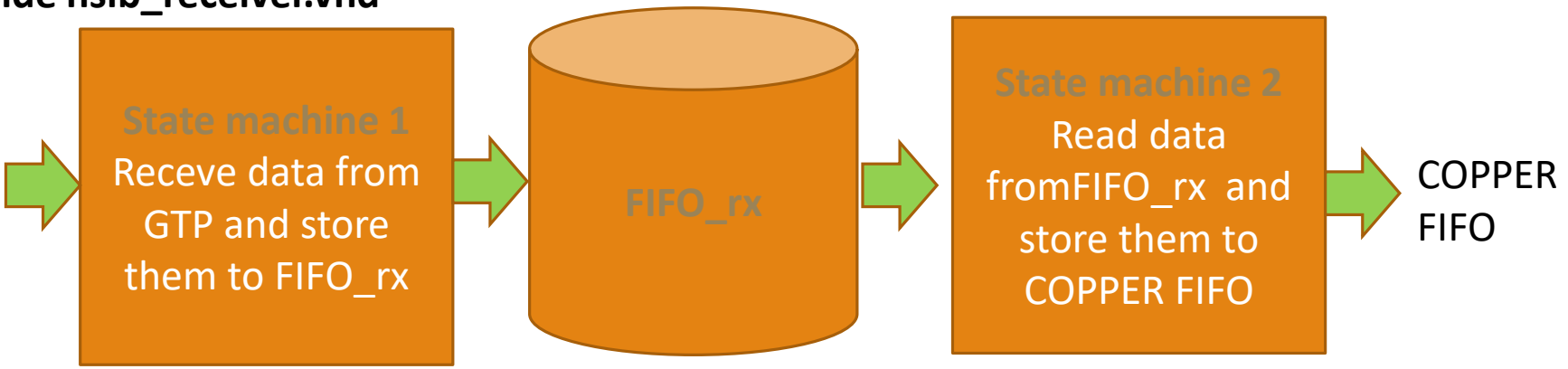
: header/footer attached by HSLB
: header/footer attached by FEE
: data contents of FEE
: strange data

Belle II : 1ワード = 32ビット (4バイト)

**Data of slotD HSLB (corrupted data)**

ffaa41b5 ff000b4d b8c70002 41b55881 f7af0004 d4000b4d c8c02000 00f24693 00000002 41b50b4d b8c741b5 7b36fe00
ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00
...
ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff00ff00 ff550000

**Inside hslb_receiver.vhd**




Data check

**CRC32 check -> O.K.**

**CRC16 check -> N.G.**

-> Data should be corrupted around FIFO in HSLB FPGA

# Why data are filled with “ff00ff00”

Data of slotD HSLB (corrupted data)

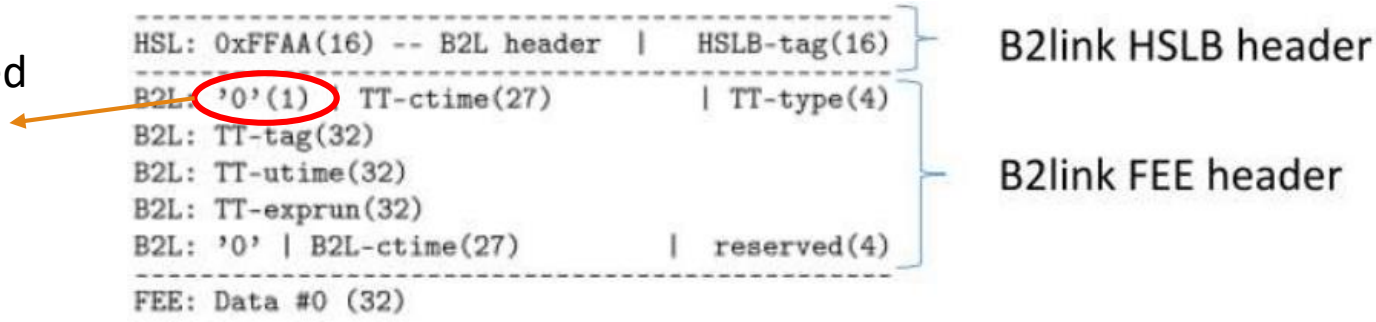
ffaa41b5
ff000b4d
B8c70002
41b55881
…
b8c741b5
7b36fe00
Ff00ff00
ff00ff00

- When FIFO is empty, the output is “ff00”.
- For some reason, “ff00” is inserted at the beginning of the event.
  - Data are shifted by 2bytes.
- “fe00” is the delimiter to indicate the end of the event. But due to the 2byte shift, this delimiter is ignored and empty FIFO is read repeatedly, which returns “ff00”.

# Workaround to avoid the first “ff00”

- Just ignore if the 1st byte of an event from FIFO_rx is ‘ff’ .

The 1st byte is supposed to never be “ff”.



# 2. COPPERボード上のbitエラー

## Data corruption in “ffffffff 0000000” pattern

### Effect of SSO (simultaneous switching outputs )?

### A. どのように化けるか

[DEBUG] 00000000 ffffffff 00000000 ffffffff 00000000 ffffffff 00000000 ffffffff 00000000 02ffffff
[DEBUG] 00000000 ffffffff 00000000 ffffffff 00000000 ffffffff 00000000 ffffffff 00000000 ffffffff
[DEBUG] 00000000 ffffffff 00000000 ffffffff 00000000 ffffffff 00000000 ffffffff 00000000 ffffffff
[DEBUG] 00000000 ffffffff 00000000 ffffffff 00000000 ffffffff 00000000 8effffff 00000000 ffffffff

### B. Reduction of the current drive of HSLB data output works :

- in hslb_***.ucf. (default 12mA to 2mA)
- Errors after the modification at the B2/B3 test bench
- B3 setup
  - 12xCOPPER (4HSLB/COPPER)
  - Input trigger 30kHz Poisson : output trigger 1.1kHz
  - Data pattern : ffffffff 00000000
  - No data corruption in 118.5hours for 323.3Mevents

しかしこれでもまだTOP検出器のCRCエラーは解決せず(次ページ)

# Data corruption in “feffffff 0100000” pattern

## A. TOP 検出器データの化け方

- Using the output log of an error event, I put the same data pattern to dumhslb firmware.
- Data corruption occurred in the B3 test bench and the data pattern seemed to be similar in error events.

The red bits became ‘0’ in the corrupted events.

feff0400 fefffdff feff0000 01000000 02000500 03000200 0300ffff fcfff9ff f5fff7ff f5fffbff

…

feff0400 fefffdff feff0000 01000000 02000500 03000200 0300ffff fcfff9ff f5fff7ff f5fffbff

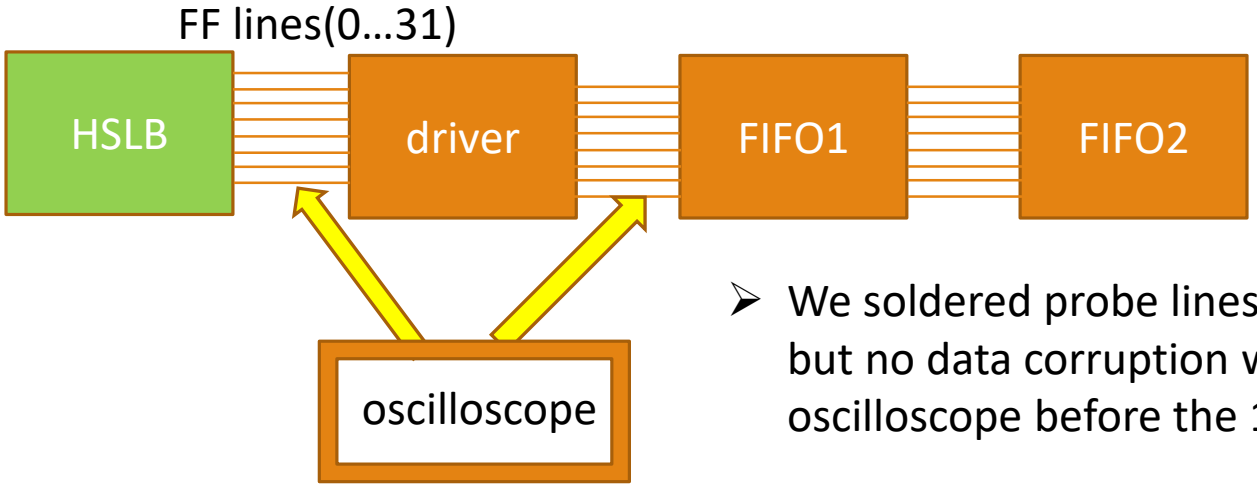
…

fefffbff f6fff6ff 01000300 0900ffff 01000200 07000000 f9fffdff fafffeff 00000000 f7fff6ff

## B. テストパターン “feffffff 01000000”

- We tried “feffffff 0000000” pattern and it caused data corruption.
  - [DEBUG] 01000000 feffffff 01000000 feffffff 00000000 feffffff 01000000 feffffff 01000000 feffffff
    [DEBUG] 01000000 feffffff 01000000 feffffff 01000000 feffffff 01000000 feffffff 00000000 feffffff
- “fbffffff 04000000” also caused data corruption
  - 04000000 fbffffff 00000000 fbffffff 04000000 fbffffff 04000000 fbffffff 04000000 fbffffff
- On the other hand, no errors in 2hours with “fffeffff 00010000 ”

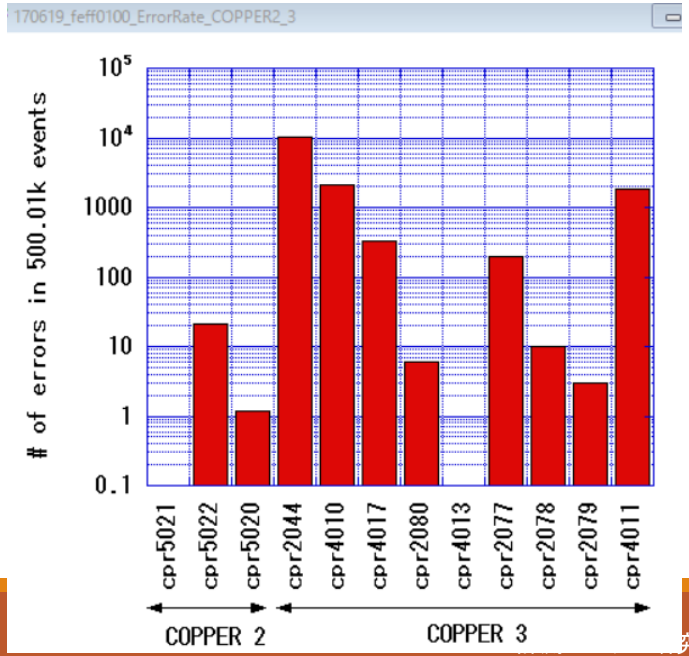
## C. オシロで “feffffff 00000000” を探す




- We soldered probe lines on a COPPER board but no data corruption was detected by an oscilloscope before the 1st FIFO.

## D. COPPERボードの個体差もあるようである

# of CRC errors in feffffff 01000000 test pattern




- So far, no prospect of fixing this problem.
- Since the error rate differs in COPPER(HSLB) boards, we are considering replacing some TOP COPPERs to reduce the error rate.

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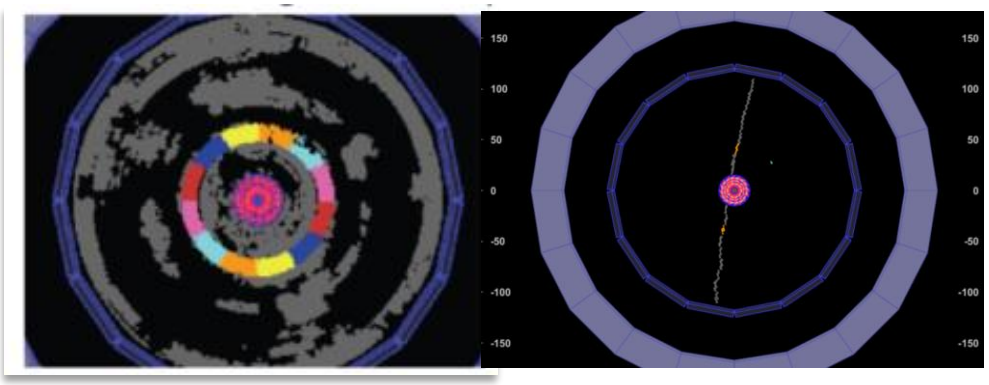
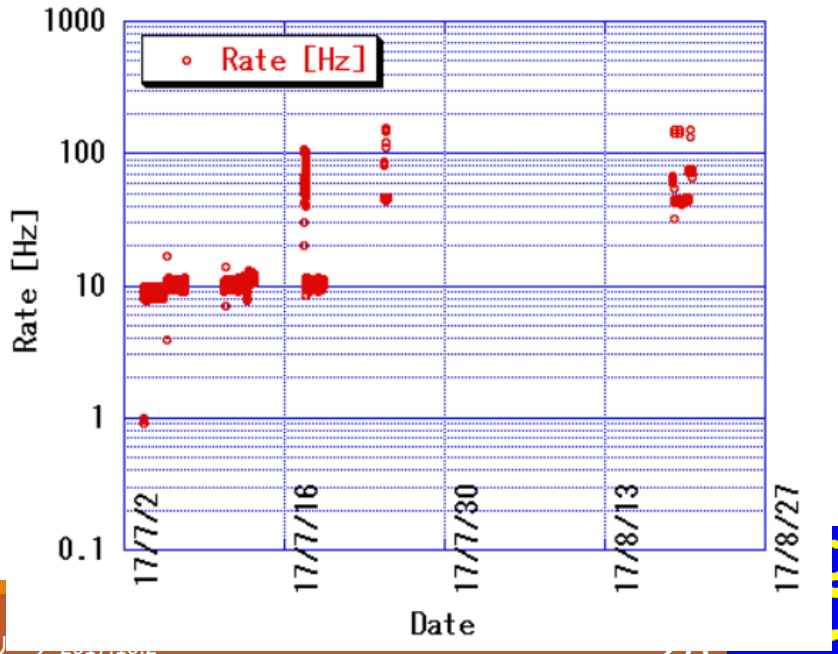
# 統合宇宙線テスト

- 2017年7月,8月 : QCS(収束磁石), Belle II ソレノイド(1.5T)を定格運転した状態で宇宙線測定
- 測定器 : CDC、TOP、ECL、KLM
  - PXD, SVD, ARICHについては現在開発および試験段階なので参加せず
- トリガー : CDC track segment finder + ECL timing
  - 1 super-layerのtrack segment finderロジックを使用
  - Trigger rate
    - Back-to back (同色の2つのsegmentを通ることを要求) TSF && ECL(timing) : ～10Hz
    - Single TSF && ECL(timing) : ～100Hz



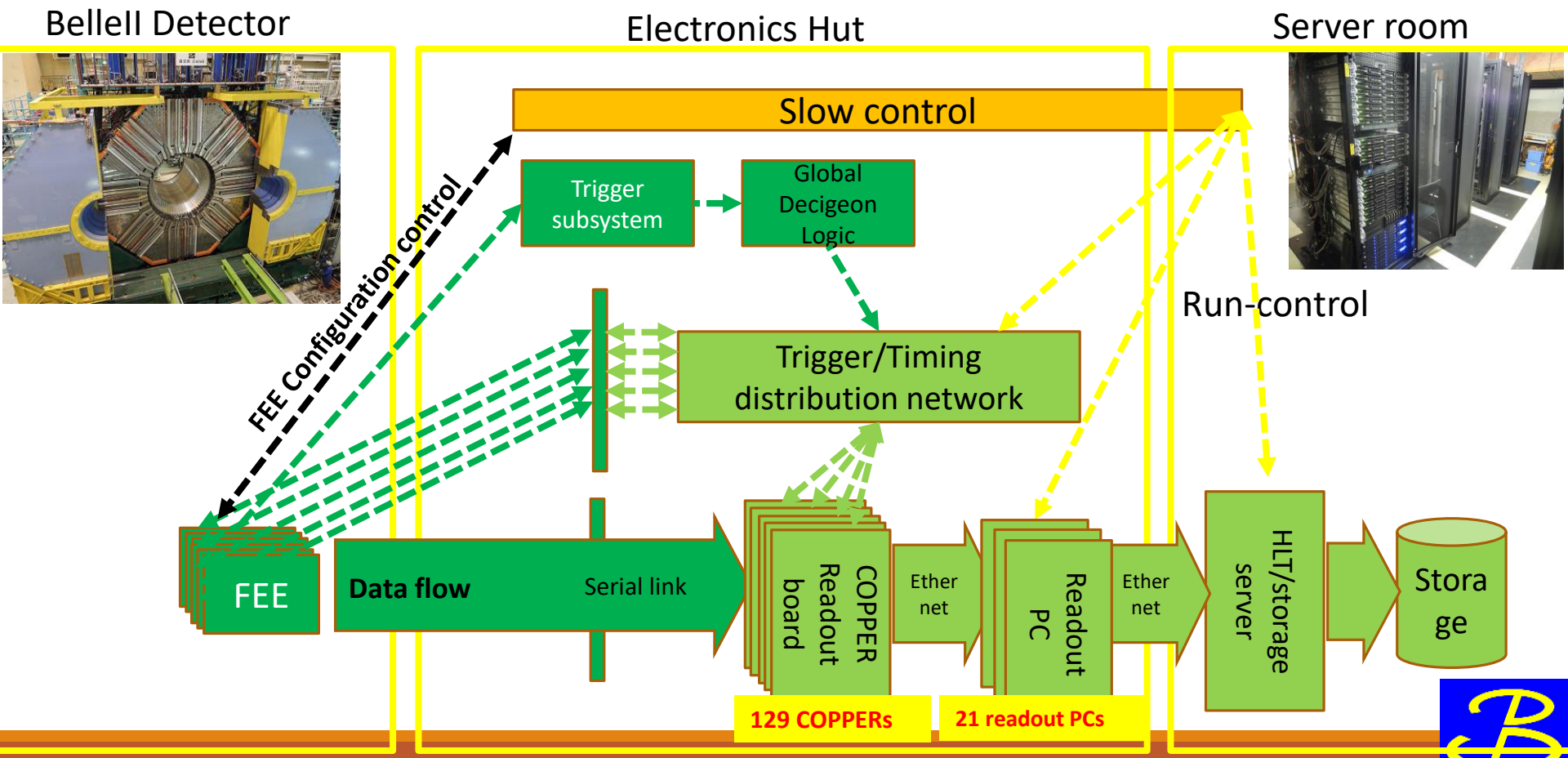
CDCをビーム方向から見た図
色がついているのが今回使用した
triggerのsegment

宇宙線テストでのevent rate



# 宇宙線試験でのデータ収集システム

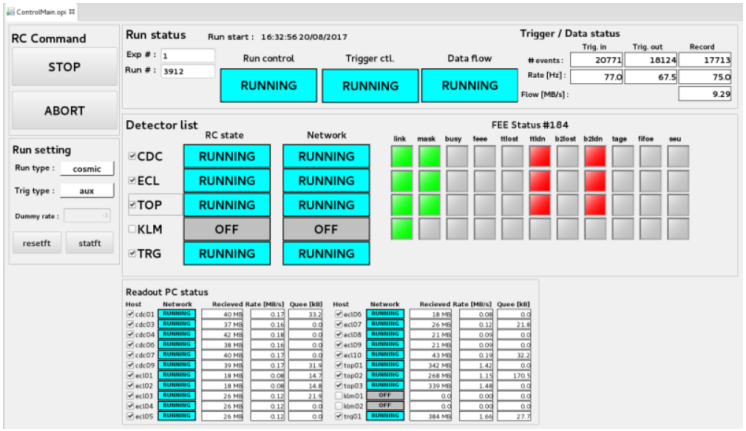
- 実際のビームランで使うDAQシステムを使用
- Front-End Electronics boards はそれぞれの測定器で異なる
- FEE -> COPPER読み出しボードのprotocolは統一されており、backend　DAQは各測定器共通。



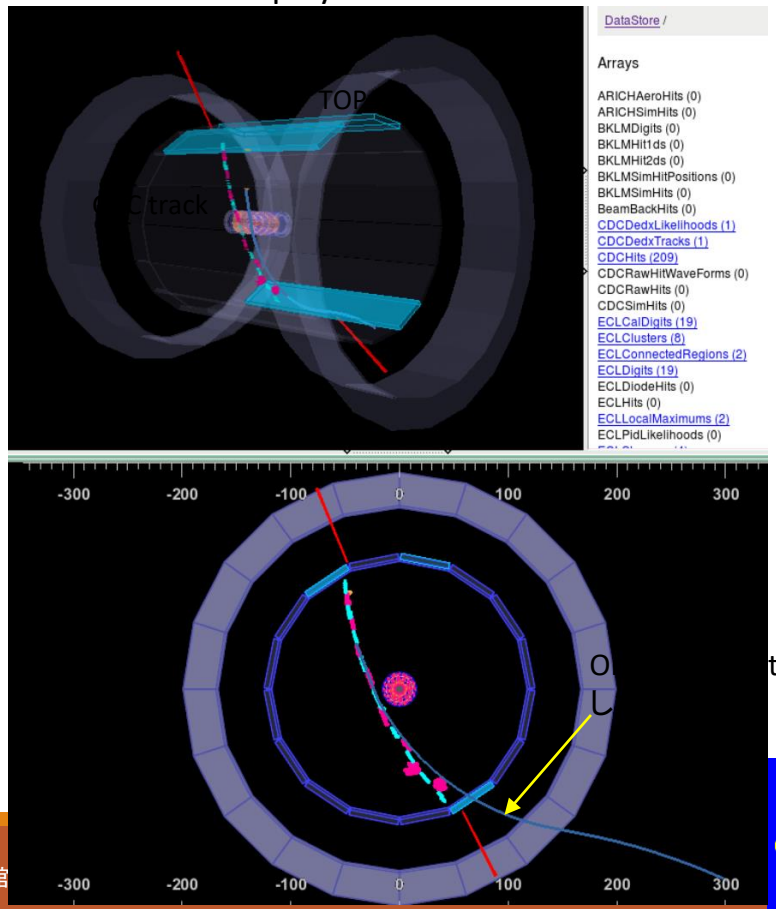
# 宇宙線テストのオペレーション

- 実際のbeam runと同様に、non-expertのexperiment shifterがデータ収集を担当し、夜間もデータ取得
  - Chat tool (rocket chat)でexpert-shifterのcommunication
- High Level Triggerにてオンラインで CDCのtracking
- 各検出器のdata qualityのonline monitor


Run-control GUI




Online Event display




Data quality monitor


truction

1. イントロダクション
2. Belle II データ読み出しシステム
3. DAQシステムのパフォーマンス
4. 外層検出器の宇宙線試験
5. Belle II 読み出し系のアップグレード計画

# Issues to be considered for the Belle II DAQ system

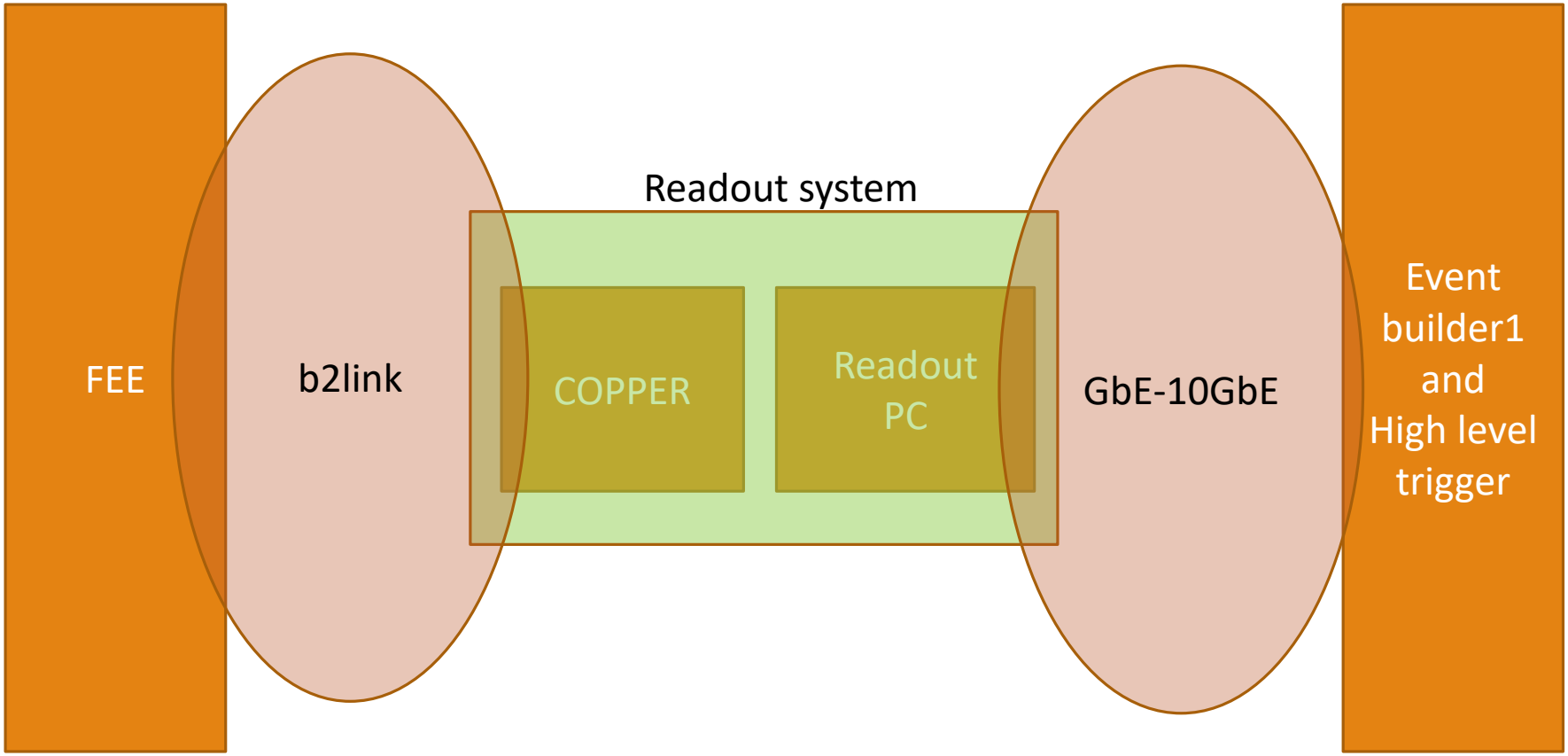
## Difficulty in maintenance during the entire Belle-II experiment period

- The number of discontinued parts is increasing.
  - e.g. chipset on a PrPMC card, FIFO and LAN controller on COPPER III
  - For older COPPER II, it is basically difficult to replace parts according to manufacturer.
- Four different types of boards( COPPER, TTRX, PrPMC, HSLB ) should be taken care of.

## Limitation in the improvement of performance of DAQ

- A. Bottlenecks of the current COPPER readout system
  - CPU usage
    - About 60% COPPER-CPU is used at “30kHz L1 trigger rate with 1kB event size/COPPER”(=Belle II DAQ target value )
  - Data transfer speed
    - 1GbE/COPPER
- B. Bottleneck due to network output of ROPC
- We need to upgrade the readout system when
  * luminosity of SuperKEKB exceeds expectations.
  * Lower threshold of L1 trigger is used or trigger-less DAQ is realized.
  - Depending on throughput, network and HLT farms also need to be upgraded.

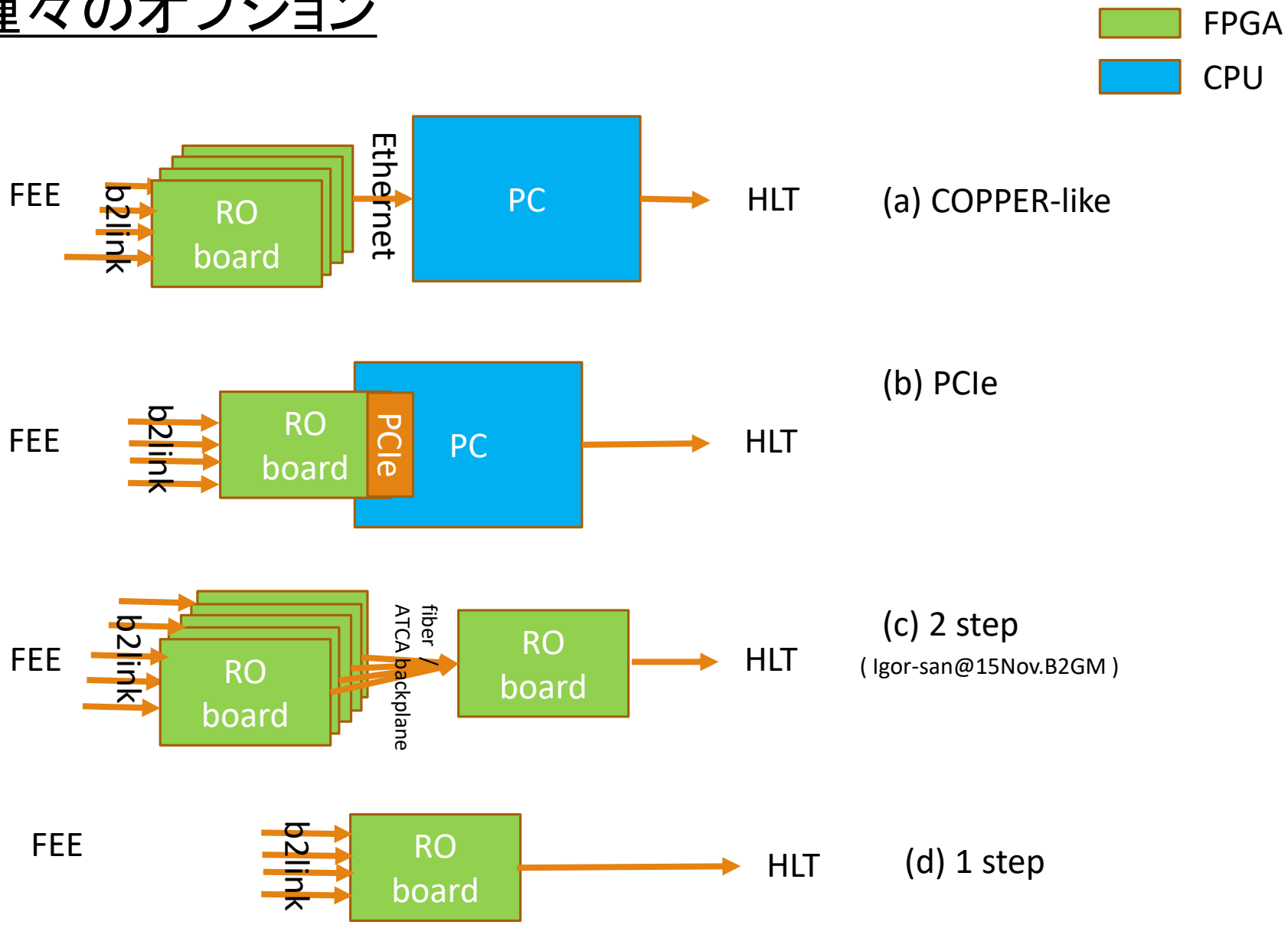
# アップグレードの際の境界条件




Basic framework of belle2link (Rocket-IO based serial link) should be the same. Otherwise FEE's FW/HW update might be needed.

Upgrade like GbE -> 10GbE will be possible, if we upgrade switches.

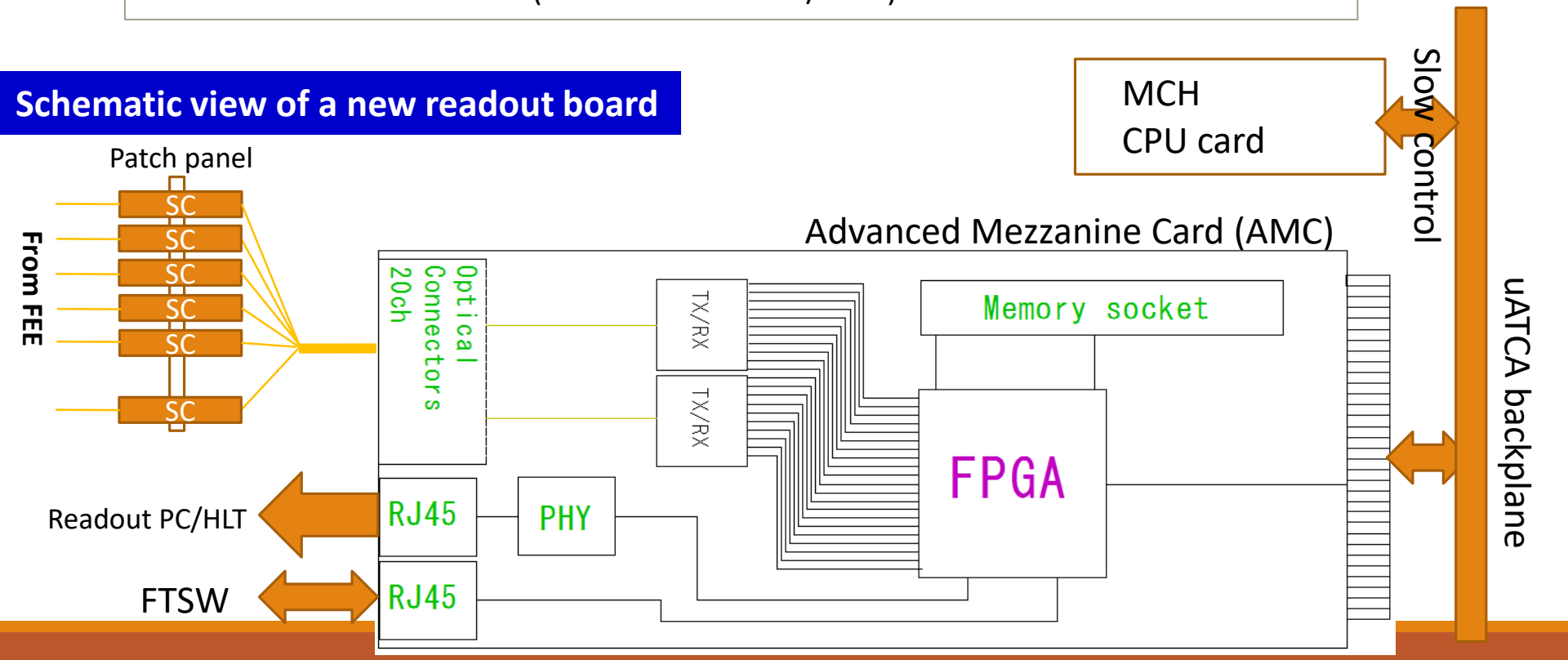
# 種々のオプション


FPGA
CPU
FEE
b2link
RO board
Ethernet
PC
HLT
(a) COPPER-like
FEE
b2link
RO board
PCIe
PC
HLT
(b) PCIe
FEE
b2link
RO board
fiber / ATCA backplane
RO board
HLT
(c) 2 step
( Igor-san@15Nov.B2GM )
FEE
b2link
RO board
HLT
(d) 1 step

# **New readout system =** High-density FGPA-based system using uTCA

- Data processing speed
  - Fast FPGA-based data processing
- Data transfer speed
  - 10GbE ( directory connected to a HLT unit ) or  1GbE ( keep readout PCs )
- Compact and high-density system
  - high density connector and higher throughput
- Easier maintenance
  - Currently : 5 COPPERs, 5 TTRXs, 5PrPMCs, 20HSLBs
    -> one AMC board (in the case of 20ch/AMC)

## Schematic view of a new readout board



# まとめ

- Belle II実験

  2018年 2月からの phase II run (崩壊点検出器以外インストール、first collision, beam b.g. 測定)に向けて準備が進んでいる。
- Belle II実験読み出しシステム
  - 7つのサブ検出器のうちPXDは特殊な読み出し系。その他は共通の読み出しシステムを使用。
  - 読み出しボード(COPPER)に新たに開発した高速データ受信ボード、AtomCPUボードを搭載してFEEとの通信とデータ処理を行う。
- 読み出しシステムのパフォーマンス試験
  - FEE <->COPPER
  - COPPER <-> readout PC

-> Belle II 実験のトリガーレート(30kHz)で動作することを確認

- 読み出しボードのupgradeを検討中
  - 高密度、高スループット化